

General Description

The WSD4098DN56 is the highest performance trench Dual N-Ch MOSFET with extreme high cell density, which provide excellent R_{DS(on)} and gate charge for most of the synchronous buck converter applications.

The WSD4098DN56 meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

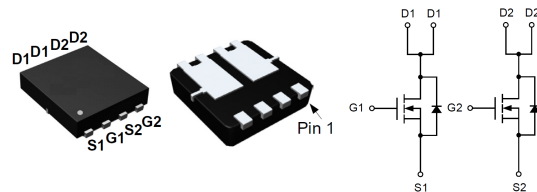
Product Summary

BVDSS	R _{DS(on)}	ID
40V	7.8mΩ	22A

Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

DFN5X6C-8-EP2 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit	
Common Ratings				
V _{DSS}	Drain-Source Voltage	40	V	
V _{GSS}	Gate-Source Voltage	±20	V	
T _J	Maximum Junction Temperature	150	°C	
T _{STG}	Storage Temperature Range	-55 to 150	°C	
I _S	Diode Continuous Forward Current	T _A =25°C	11.4	A
I _D	Continuous Drain Current	T _A =25°C	22	A
		T _A =70°C	22	
I _{DM} ^b	Pulse Drain Current Tested	T _A =25°C	88	A
P _D	Maximum Power Dissipation	T _A =25°C	25	W
		T _C =70°C	10	
R _{θJL}	Thermal Resistance-Junction to Lead	Steady State	5	°C/W
R _{θJA}	Thermal Resistance-Junction to Ambient	t ≤ 10s	45	°C/W
		Steady State ^b	90	
I _{AS} ^d	Avalanche Current, Single pulse	L=0.5mH	28	A
E _{AS} ^d	Avalanche Energy, Single pulse	L=0.5mH	39.2	mJ

Note a : Max. continuous current is limited by bonding wire.

Note b : Pulse width limited by max. junction temperature.

Note c : Surface mounted on 1in² pad area, steady state t = 999s.

Note d : UIS tested and pulse width limited by maximum junction temperature 150°C (initial temperature T_J=25°C).

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

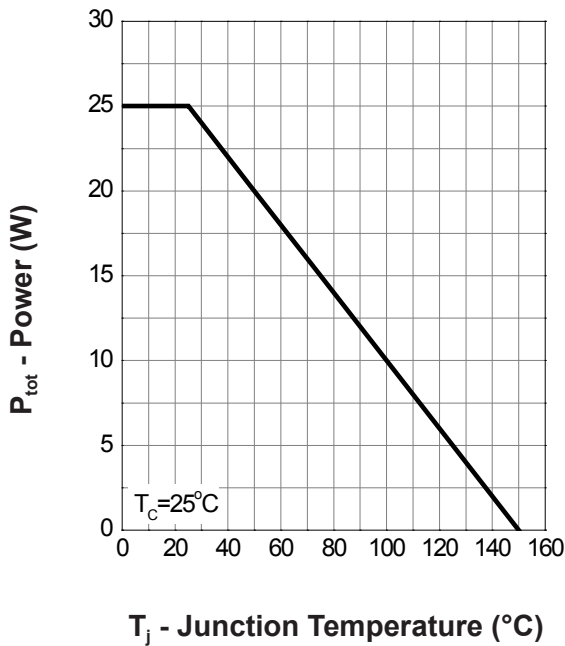
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250μA	40	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =32V, V _{GS} =0V	-	-	1	μA
		T _J =85°C	-	-	30	
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250μA	1.2	1.8	2.5	V
I _{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
R _{DS(ON)} ^e	Drain-Source On-state Resistance	V _{GS} =10V, I _{DS} =14A	-	6.8	7.8	mΩ
		V _{GS} =4.5V, I _{DS} =12A	-	9.0	11	
Diode Characteristics						
V _{SD} ^e	Diode Forward Voltage	I _{SD} =1A, V _{GS} =0V	-	0.75	1.1	V
t _{rr}	Reverse Recovery Time	I _{SD} =20A, dI _{SD} /dt=100A/μs	-	23	-	ns
Q _{rr}	Reverse Recovery Charge		-	13	-	nC
Dynamic Characteristics^f						
R _G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, F=1MHz	-	2.5	-	Ω
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =20V, Frequency=1.0MHz	-	1370	1781	pF
C _{oss}	Output Capacitance		-	317	-	
C _{riss}	Reverse Transfer Capacitance		-	96	-	
t _{d(ON)}	Turn-on Delay Time		-	13.8	-	
t _r	Turn-on Rise Time	V _{DD} =20V, R _L =20Ω, I _{DS} =1A,	-	8	-	
t _{d(OFF)}	Turn-off Delay Time	V _{GEN} =10V, R _G =6Ω	-	30	-	
t _f	Turn-off Fall Time		-	21	-	
Gate Charge Characteristics^f						
Q _g	Total Gate Charge	V _{DS} =20V, V _{GS} =10V, I _{DS} =6A	-	23	28	nC
Q _g	Total Gate Charge	V _{DS} =20V, V _{GS} =4.5V, I _{DS} =6A	-	22	-	
Q _{gth}	Threshold Gate Charge		-	2.6	-	
Q _{gs}	Gate-Source Charge		-	4.7	-	
Q _{gd}	Gate-Drain Charge		-	3	-	

Note e : Pulse test ; pulse width≤300μs, duty cycle≤2%.

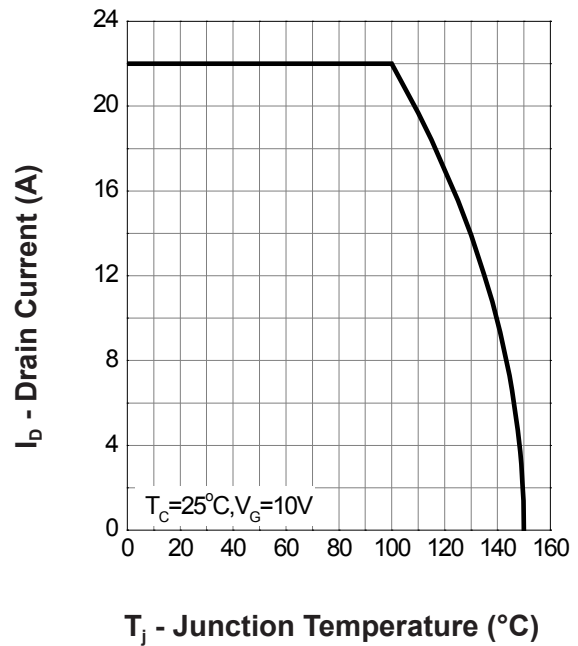
Note f : Guaranteed by design, not subject to production testing.

Typical Operating Characteristics

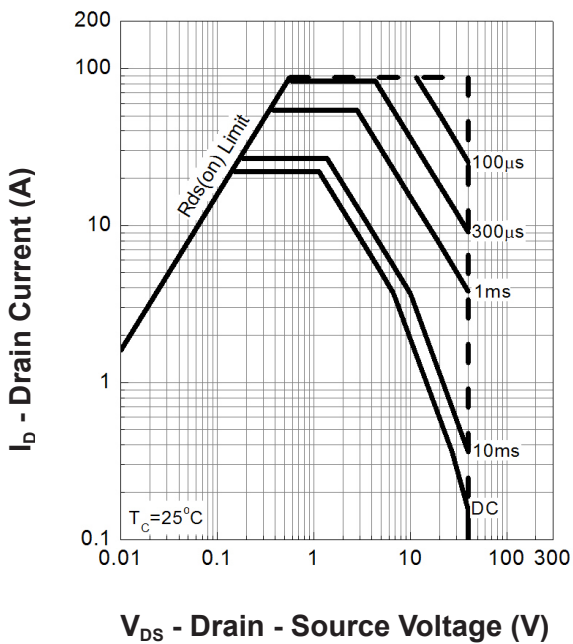
Power Dissipation



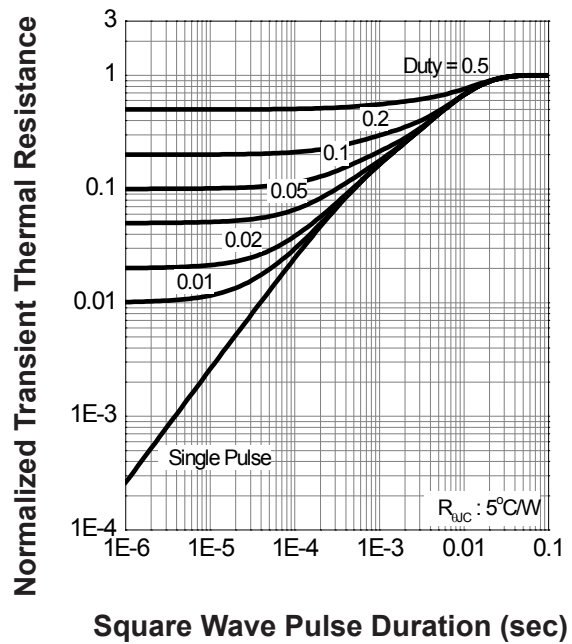
Drain Current



Safe Operation Area

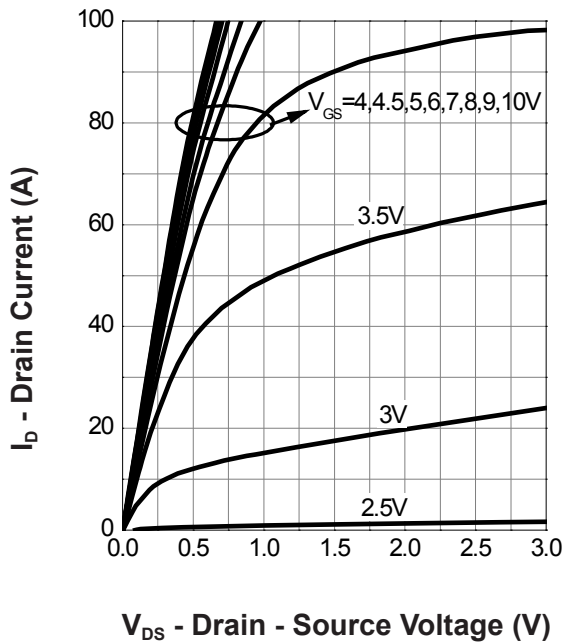


Thermal Transient Impedance

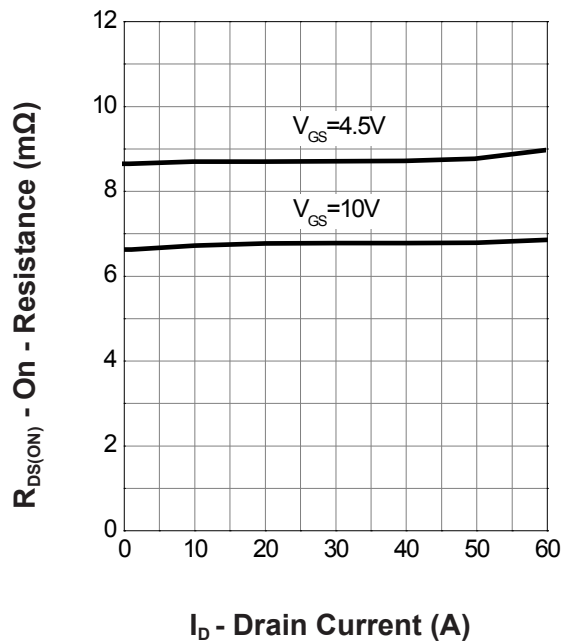


Typical Operating Characteristics(Cont.)

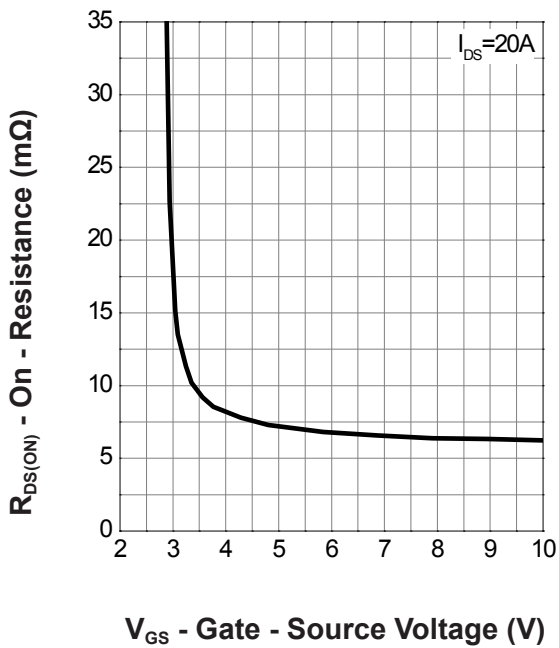
Output Characteristics



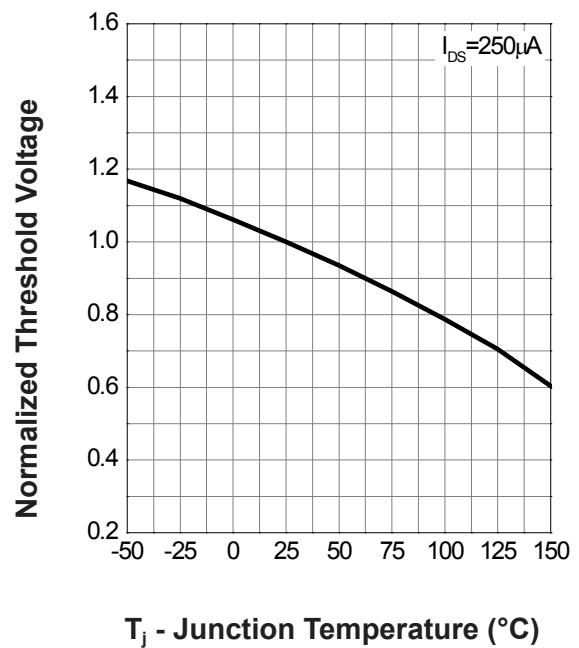
Drain-Source On Resistance



Gate-Source On Resistance

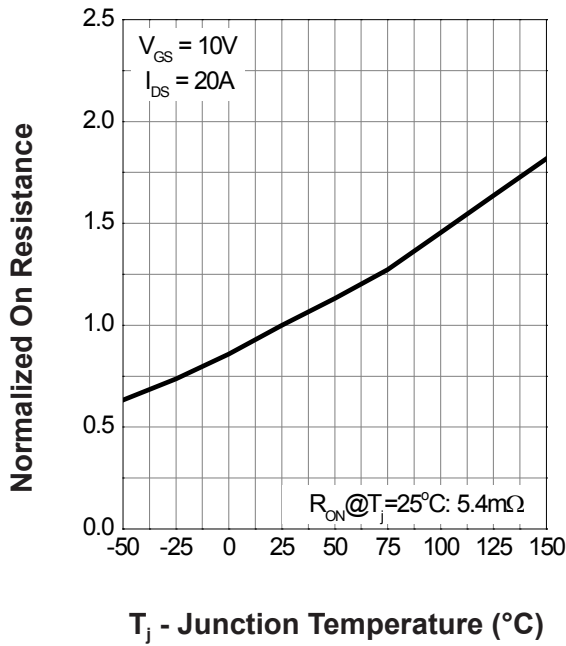


Gate Threshold Voltage

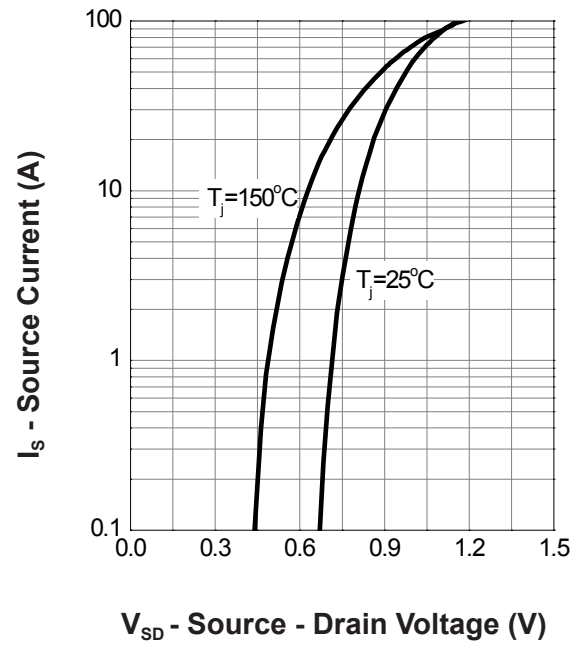


Typical Operating Characteristics(Cont.)

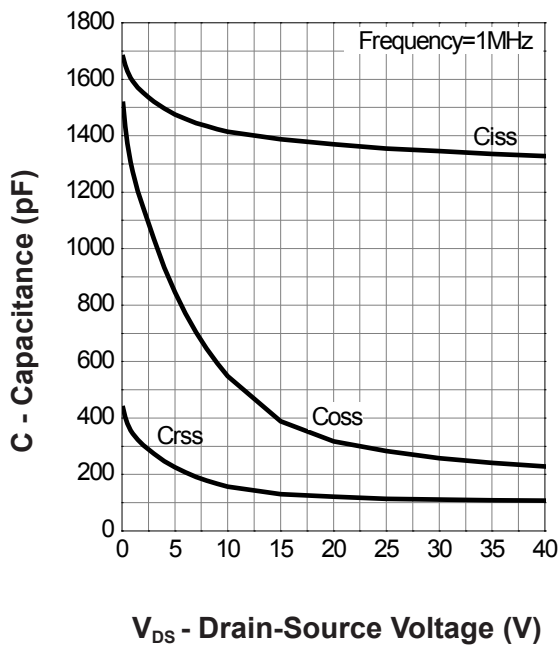
Drain-Source On Resistance



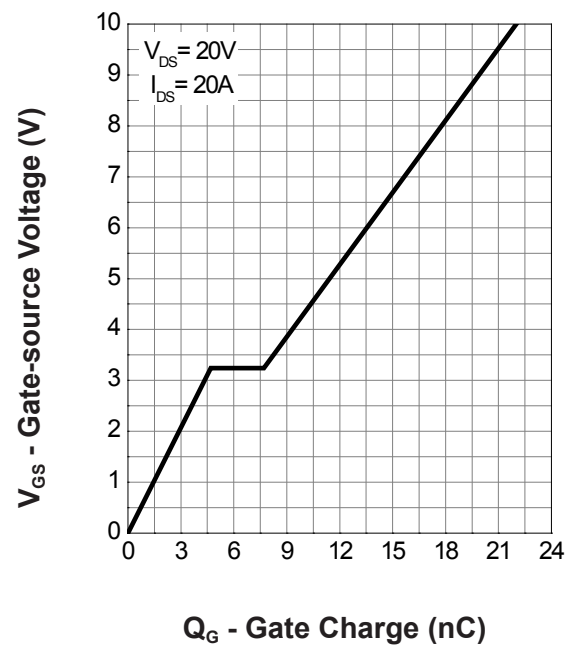
Source-Drain Diode Forward



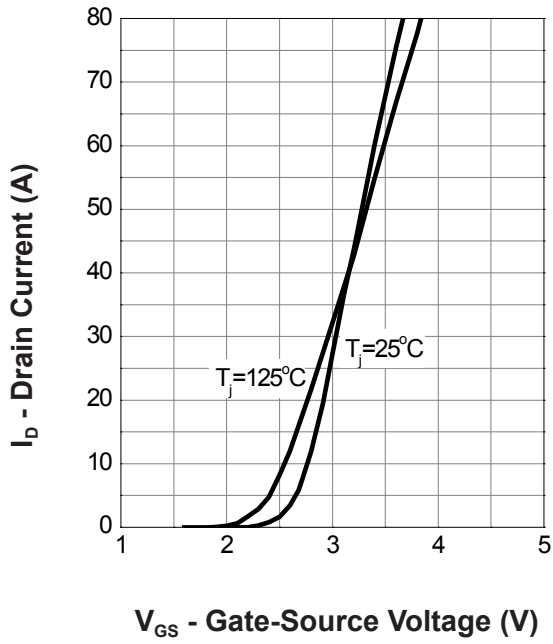
Capacitance



Gate Charge



Transfer Characteristics



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