

### General Description

The WSD4080DN56 is the highest performance trench N-ch MOSFET with extreme high cell density, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The WSD4080DN56 meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

### Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

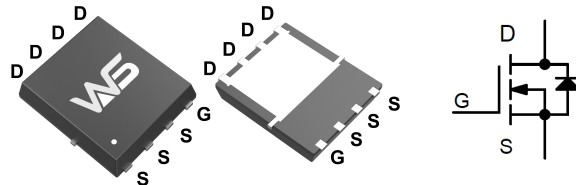
### Product Summary

BVDSS	RDSON	ID
40V	4.5mΩ	85A

### Applications

- Battery protection
- Load switch
- Uninterruptible power supply

### DFN5X6-8 Pin Configuration



### Absolute Maximum Ratings (Tc=25°C unless otherwise noted)

Symbol	Parameter	Rating	Units
V <sub>DS</sub>	Drain-Source Voltage	40	V
V <sub>GS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub> @T <sub>c</sub> =25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sub>1</sub>	85	A
I <sub>D</sub> @T <sub>c</sub> =100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sub>1</sub>	58	A
I <sub>DM</sub>	Pulsed Drain Current <sub>2</sub>	100	A
EAS	Single Pulse Avalanche Energy <sub>3</sub>	110.5	mJ
I <sub>AS</sub>	Avalanche Current	47	A
P <sub>D</sub> @T <sub>c</sub> =25°C	Total Power Dissipation <sub>4</sub>	52.1	W
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	°C
T <sub>J</sub>	Operating Junction Temperature Range	-55 to 150	°C
R <sub>θJA</sub>	Thermal Resistance Junction-Ambient <sub>1</sub>	62	°C/W
R <sub>θJC</sub>	Thermal Resistance Junction-Case <sub>1</sub>	2.4	°C/W

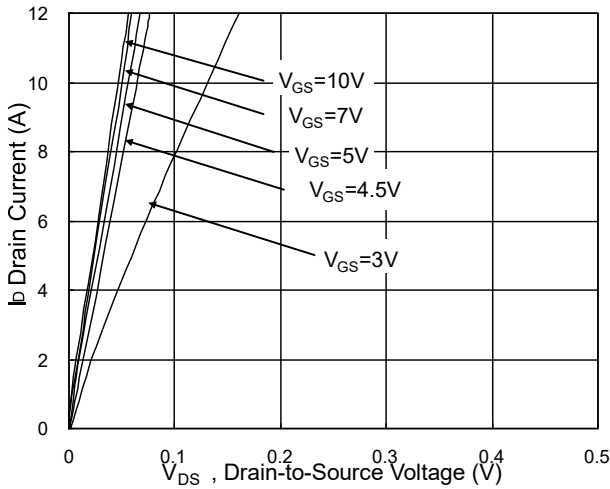
**Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
B <sub>VDS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	40	---	---	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =10A	---	4.5	6.5	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =5A	---	6.4	8.5	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.0	---	2.5	V
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =32V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =32V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	5	
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =5A	---	27	---	S
Q <sub>g</sub>	Total Gate Charge (4.5V)	V <sub>DS</sub> =20V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A	---	20	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	5.8	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	9.5	---	
T <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =15V, V <sub>GS</sub> =10V R <sub>G</sub> =3.3Ω I <sub>D</sub> =1A	---	15.2	---	ns
T <sub>r</sub>	Rise Time		---	8.8	---	
T <sub>d(off)</sub>	Turn-Off Delay Time		---	74	---	
T <sub>f</sub>	Fall Time		---	7	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz	---	2354	---	pF
C <sub>oss</sub>	Output Capacitance		---	215	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	175	---	
I <sub>s</sub>	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	70	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>s</sub> =1A, T <sub>J</sub> =25°C	---	---	1	V

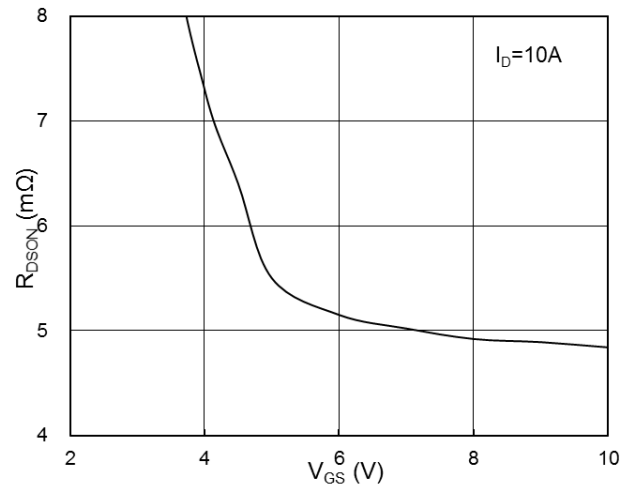
Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
- 3.The EAS data shows Max. rating . The test condition is V<sub>DD</sub>=25V,V<sub>GS</sub>=10V,L=0.1mH,I<sub>AS</sub>=47A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation.

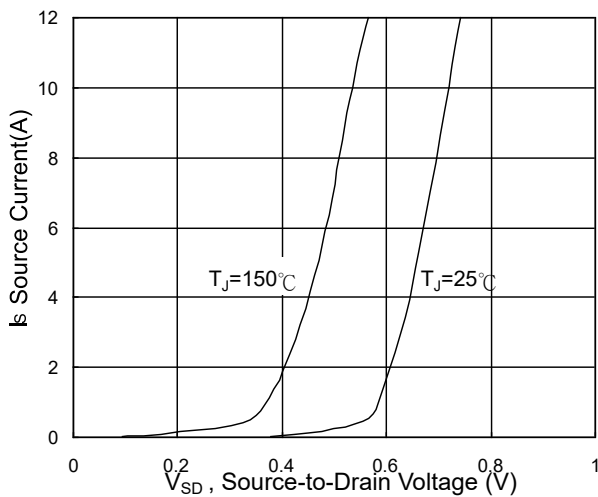
**Typical Characteristics**



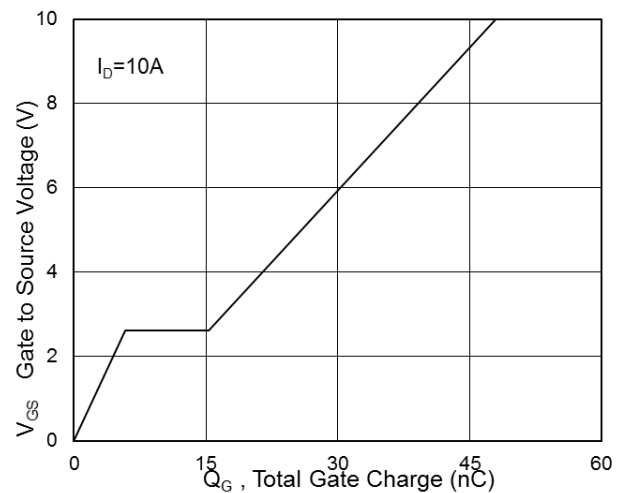
**Fig.1 Typical Output Characteristics**



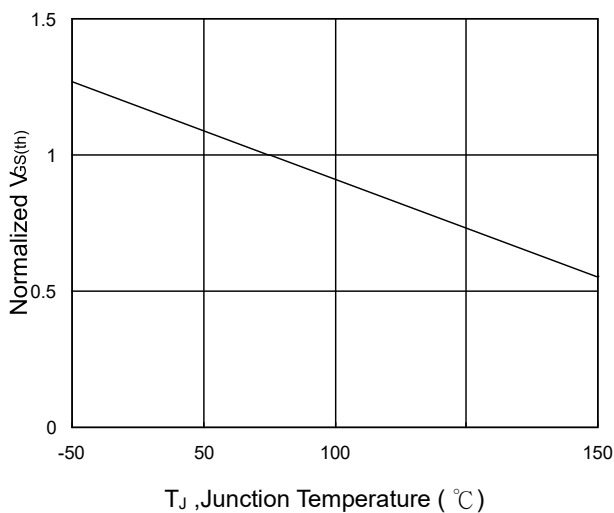
**Fig.2 On-Resistance vs. G-S Voltage**



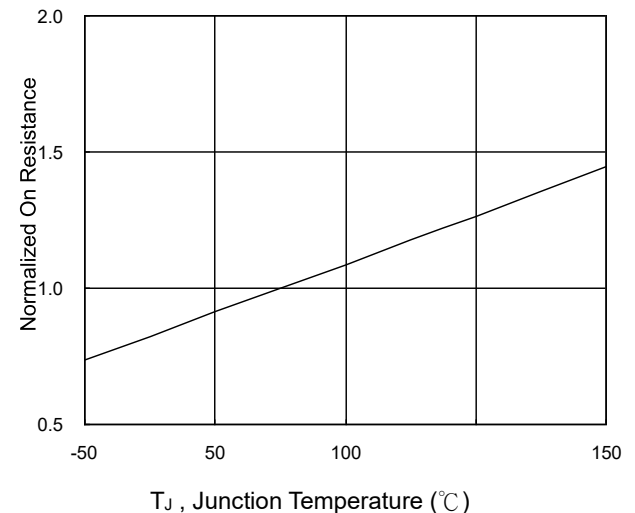
**Fig.3 Forward Characteristics of Reverse**



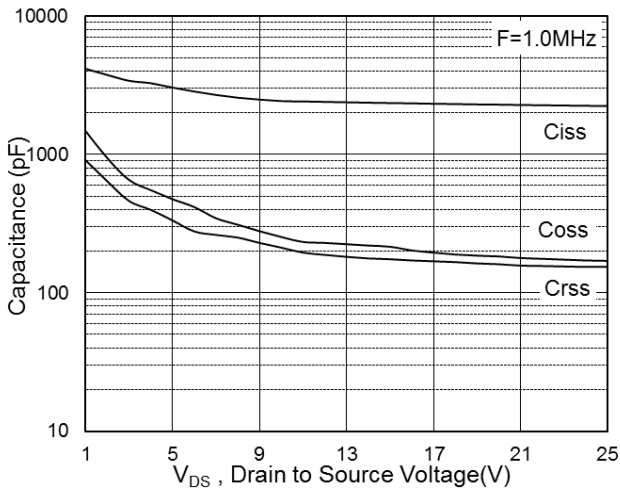
**Fig.4 Gate-Charge Characteristics**



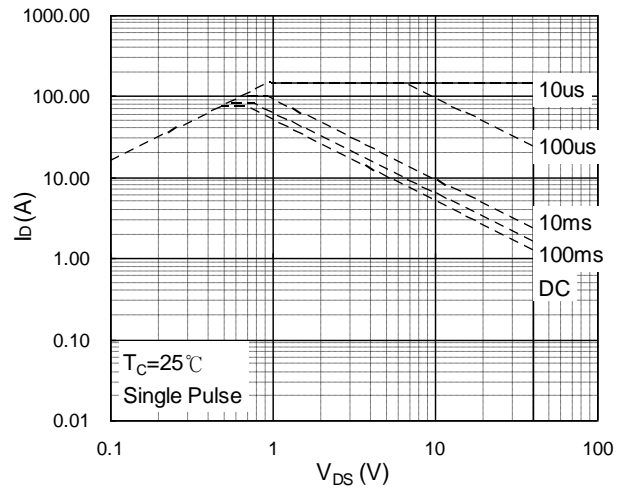
**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**



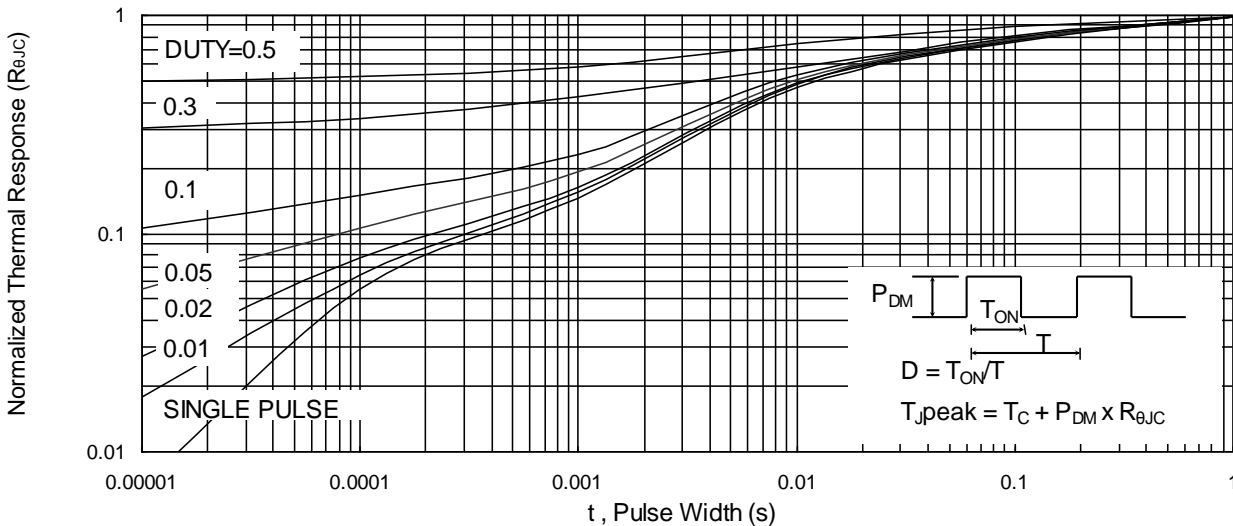
**Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$**



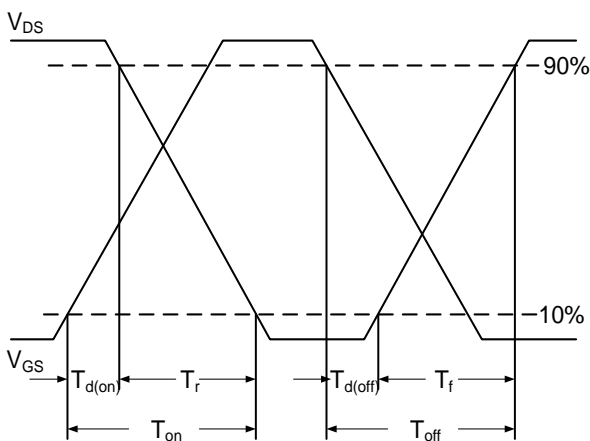
**Fig.7 Capacitance**



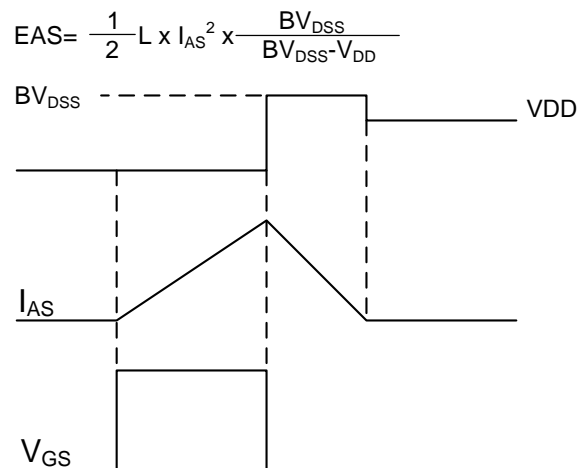
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching Wave**

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