General Description

This P-Channel enhancement mode power FETs are produced with high cell density, DMOS trench technology, which is especially used to minimize on-state resistance. This device is particularly suited for low voltage application such as portable equipment, power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

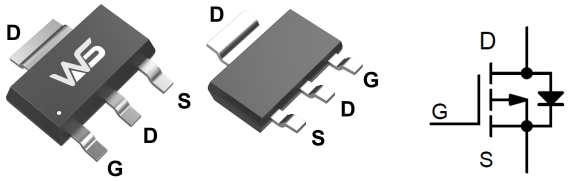
Product Summery

BVDSS	RDSON	ID
-60V	215mΩ	-2A

Applications

- High Frequency Point-of-Load Synchronous Buck Converter.
- Networking DC-DC Power System
- Load Switch

SOT-223 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-60	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_A=25℃	Continuous Drain Current, V_{GS} @ -10V	-2	A
I_D@T_A=70℃	Continuous Drain Current, V_{GS} @ -10V	-1.6	A
I_{DM}	Pulsed Drain Current	-10	A
P_D@T_A=25℃	Total Power Dissipation	2	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient	---	62	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case	---	5.4	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-60	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BV_{DSS} Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	-0.03	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V , I_D=-2A	---	175	215	mΩ
		V_{GS}=-4.5V , I_D=-2A	---	205	260	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-1.2	-1.9	-3.0	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4.56	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-60V , V_{GS}=0V , T_J=25℃	---	---	-1	uA
		V_{DS}=-60V , V_{GS}=0V , T_J=55℃	---	---	-5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=-15V , I_D=-2A	---	5	---	S
Q_g	Total Gate Charge	V_{DS}=-48V , V_{GS}=-4.5V , I_D=-1A	---	6.3	---	nC
Q_{gs}	Gate-Source Charge		---	2.3	---	
Q_{gd}	Gate-Drain Charge		---	1.8	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=-30V , V_{GS}=-10V , R_{GEN}=3.3Ω,RL=30Ω.	---	20	---	ns
T_r	Rise Time		---	. 3	---	
$T_{d(off)}$	Turn-Off Delay Time		---	5.2	---	
T_f	Fall Time		---	3.8	---	
C_{iss}	Input Capacitance	V_{DS}=-15V , V_{GS}=0V , f=1MHz	---	364	---	pF
C_{oss}	Output Capacitance		---	41	---	
C_{rss}	Reverse Transfer Capacitance		---	12	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current	V_G=V_D=0V , Force Current	---	---	-2	A
V_{SD}	Diode Forward Voltage	V_{GS}=0V , I_S=-1.2A , T_J=25℃	---	---	-1.2	V

A: The value of RθJA is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with TA =25°C. The value in any given application depends on the user's specific board design.

B: The power dissipation PD is based on TJ(MAX)=150℃, using ≤10s junction-to-ambient thermal resistance.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150℃. Ratings are based on low frequency and duty cycles to keep initial T_J=25℃.

D: The RθJA is the sum of the thermal impedence from junction to lead RθJA and lead to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F:These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in^2 FR-4 board with2oz. Copper, assuming a maximum junction temperature of TJ(MAX)=150℃. The SOA curve provides a single pulse rating.

Typical Characteristics

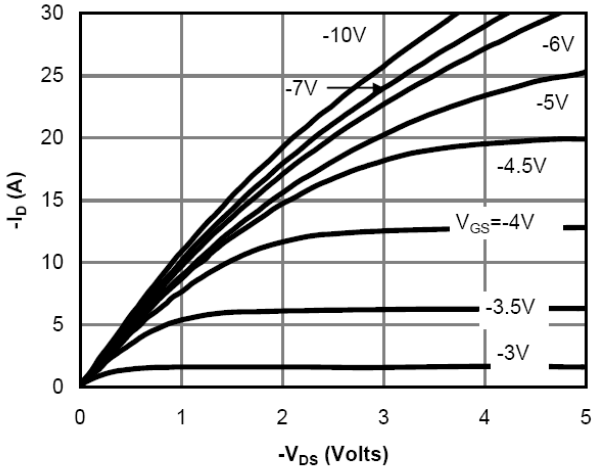


Fig 1: On-Region Characteristics

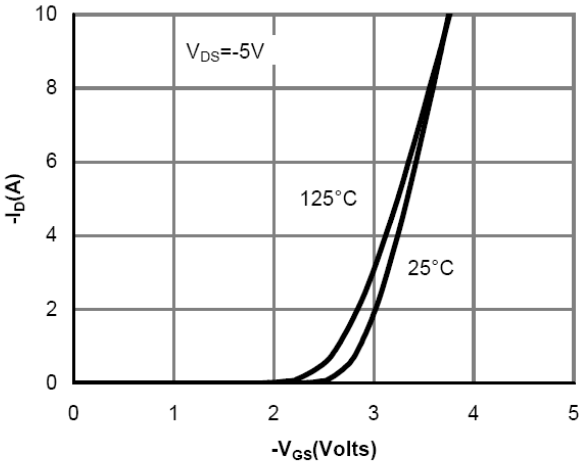


Figure 2: Transfer Characteristics

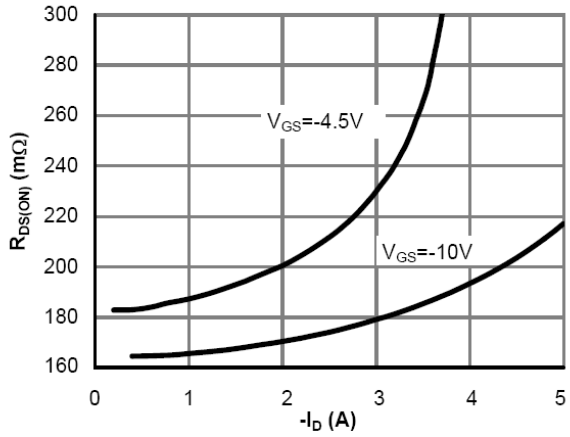


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

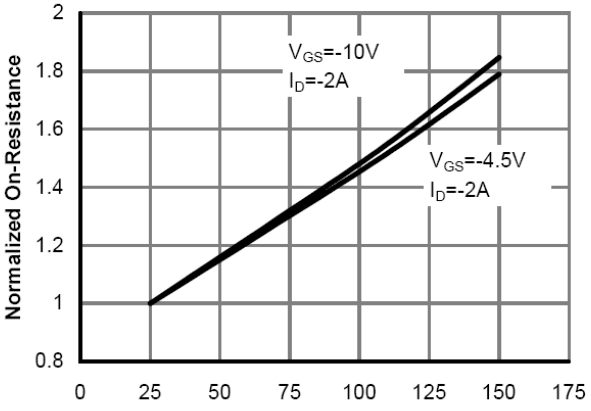


Figure 4: On-Resistance vs. Junction Temperature

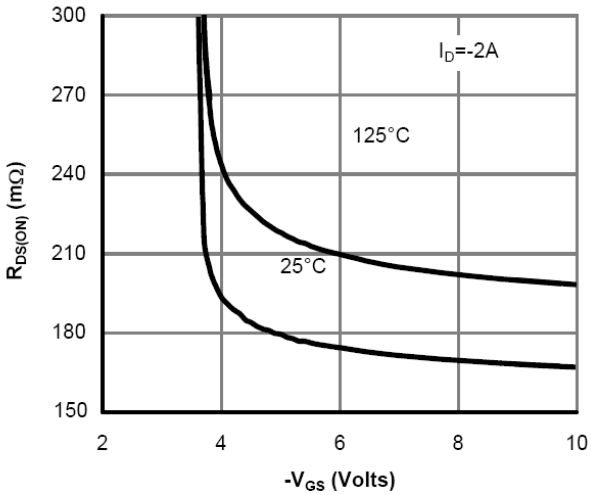


Figure 5: On-Resistance vs. Gate-Source Voltage

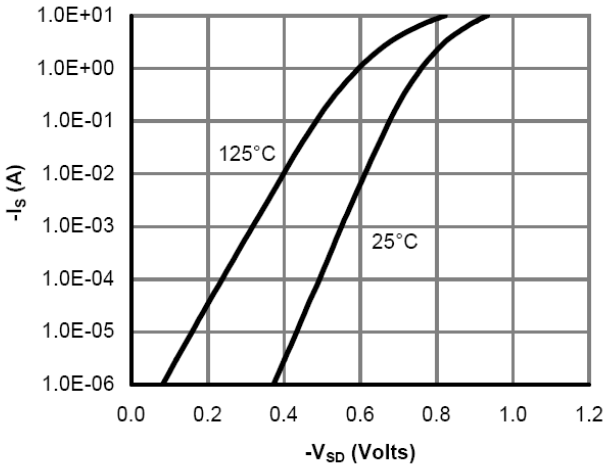


Figure 6: Body-Diode Characteristics

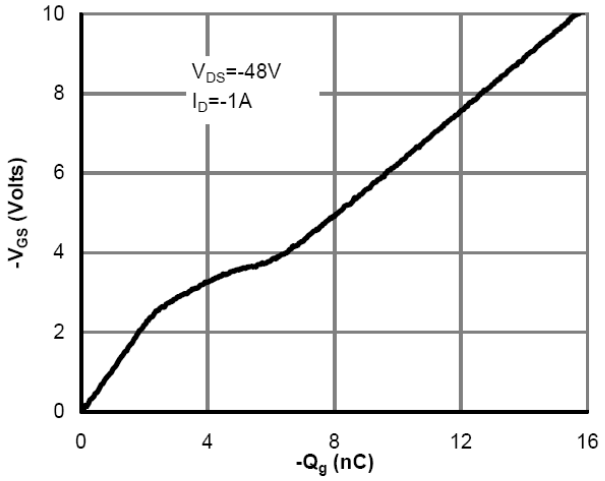


Figure 7: Gate-Charge Characteristics

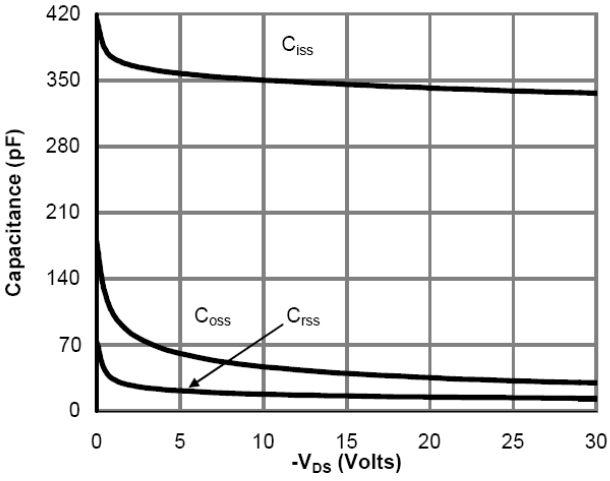


Figure 8: Capacitance Characteristics

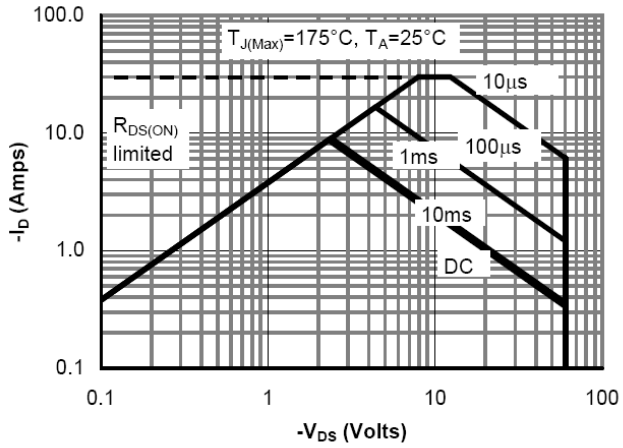


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

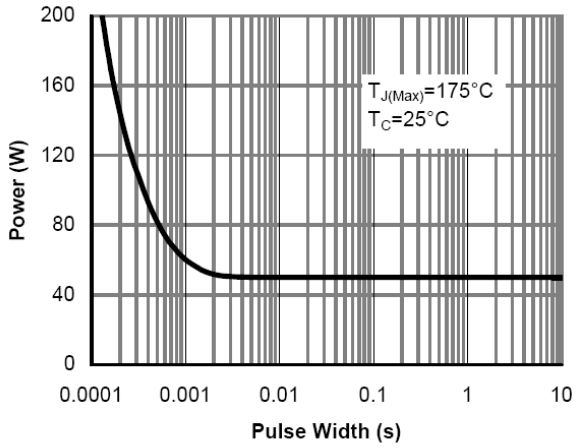


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

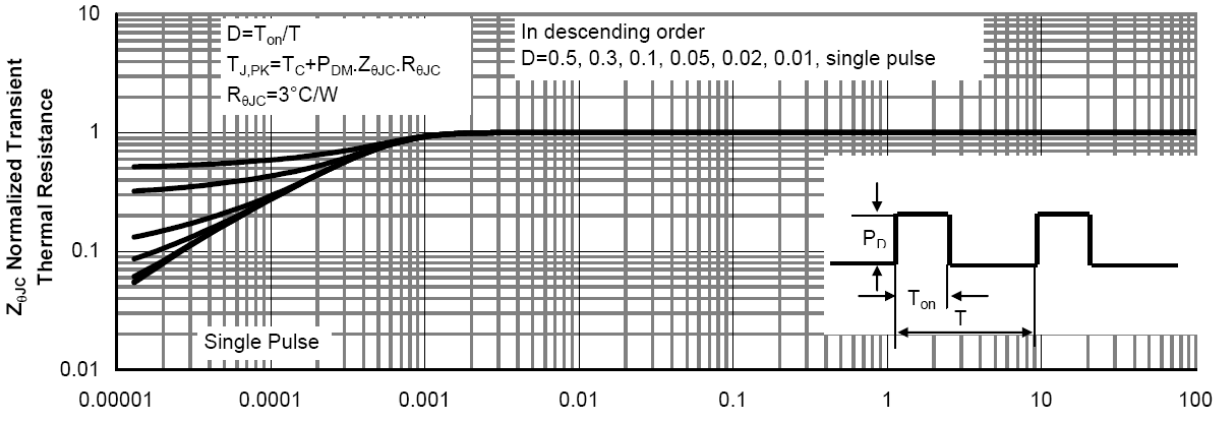


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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