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XINBOLE

Product Specification

XBLW SN74LS190

Presettable Synchronous
BCD Decade up/down Counter

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Presettable Synchronous
BCD Decade up/down Counter

Description

The SN74LS190 is a asynchronously presettable up/down BCD decade counters. They contain four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation.

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel data inputs (D0 to D3) is loaded into the counter and appears on the outputs when the parallel load ($\overline{PL}$) input is LOW. As indicated in the function table, this operation overrides the counting function.

Counting is inhibited by a HIGH level on the count enable ($\overline{CE}$) input. When $\overline{CE}$ is LOW internal state changes are initiated synchronously by the LOW-to-HIGH transition ofthe clock input. The up/down ($\overline{U}$/D) input signal determines the direction of counting as indicated in the function table. The $\overline{CE}$ input may go LOW when the clock is in either state, however, the LOW-to-HIGH $\overline{CE}$ transition must occur only when the clock is HIGH. Also, the U/D input should be changed only when either $\overline{CE}$ or CP is HIGH.

Overflow/underflow indications are provided by two types of outputs, the terminal count (TC) and ripple clock ($\overline{RC}$). The TC output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches "9" in the count-up-mode. The TC output will remain HIGH until a state change occurs, either by counting or presetting, or until $\overline{U}$/D is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the $\overline{RC}$ output. When TC is HIGH and $\overline{CE}$ is LOW, the $\overline{RC}$ output follows the clock pulse (CP). This feature simplifies the design ofmultistage counters as shown in Figure 5 and 6.

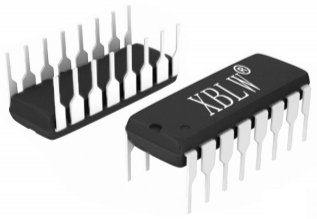
In Figure5,each $\overline{RC}$ output is used as the clock input to the next higher stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a HIGH On $\overline{CE}$ inhibits the $\overline{RC}$ output pulse as indicated in the function table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This can be a disadvantage ofthis configuration in some applications.

Figure 6 shows a method of causing state changes to occur simultaneously in all stages. The $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion and all clock inputs are driven in parallel. In this configuration the duration ofthe clock LOW state must be long enough to allow the negative-going edge ofthe carry/borrow signal to ripple through to the last stage before the clock goes HIGH. Since the $\overline{RC}$ output of any package goes HIGH shortly after its CP input goes HIGH there is no such restriction on the HIGH- state duration ofthe clock.

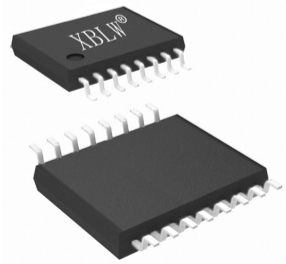
In Figure.7, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the $\overline{CE}$ input for a given stage. An enable must be included in each carry gate in order to inhibit counting. The TC output of a given stage it not affected by its own $\overline{CE}$ signal therefore the simple inhibit scheme ofFigure 5 and 6 does not apply.

Features

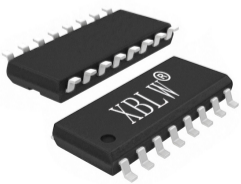
- Synchronous reversible counting
- Asynchronous parallel load
- Count enable control for synchronous expansion
- Single up/down control input
- Specified from -20℃ to +85℃
- Packaging information: DIP-16/SOP-16/TSSOP-16



DIP-16



TSSOP-16



SOP-16

Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW SN74LS190N	DIP-16	74LS190N	Tube	1000Pcs/Box
XBLW SN74LS190DTR	SOP-16	74LS190	Tape	2500Pcs/Reel
XBLW SN74LS190TDTR	TSSOP-16	74LS190	Tape	3000Pcs/Reel

Block Diagram

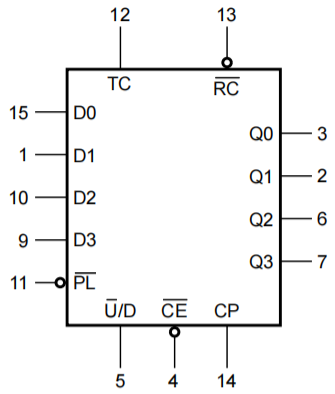


Figure 1. Logic symbol

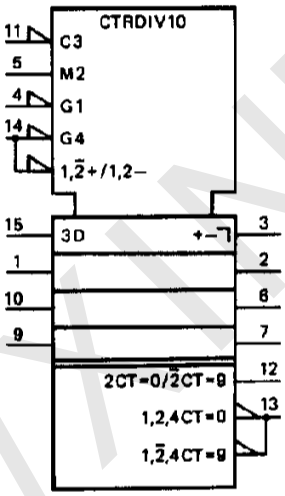


Figure 2. IEC logic symbol

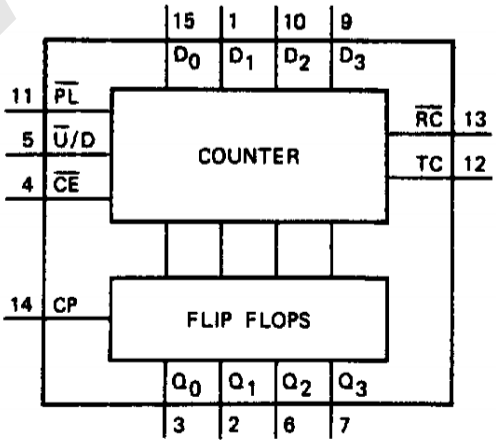


Figure 3.Functional diagram

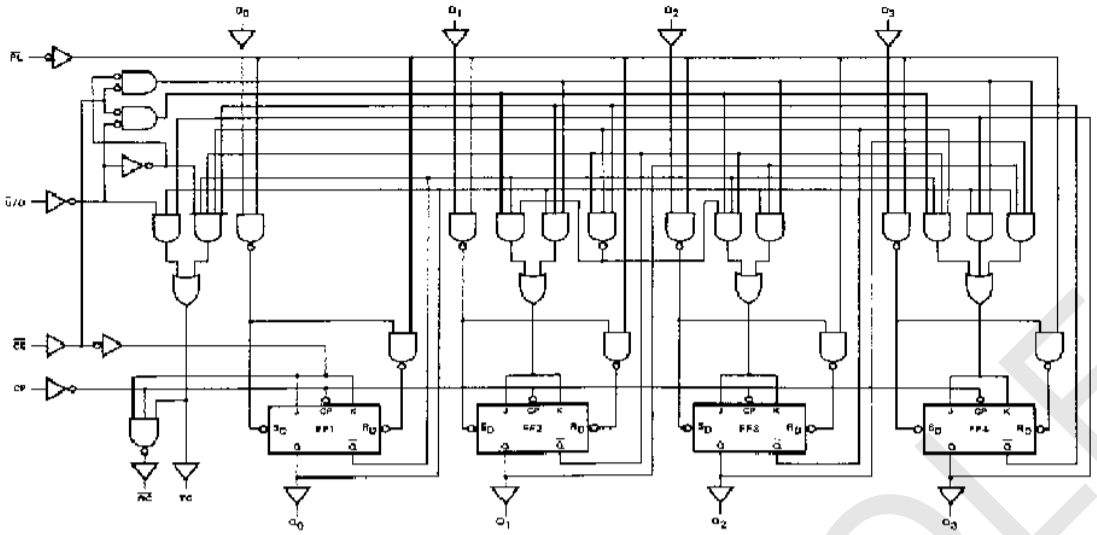


Figure 4. Logic diagram

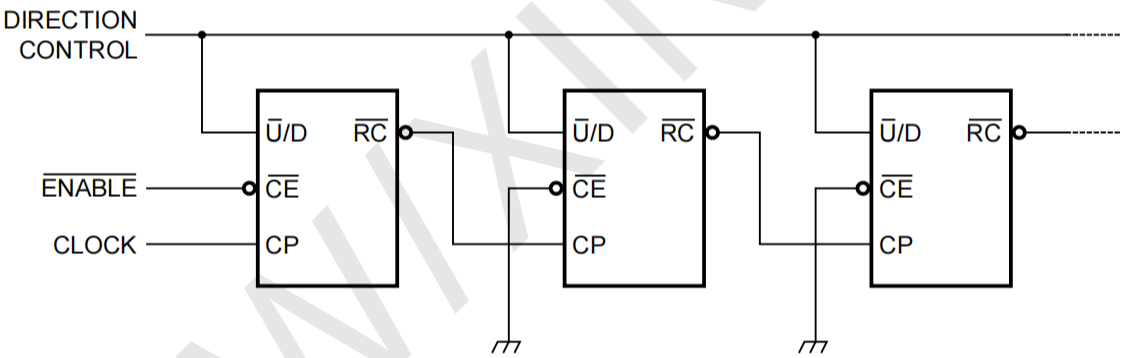


Figure 5.N-stage ripple counter using ripple clock

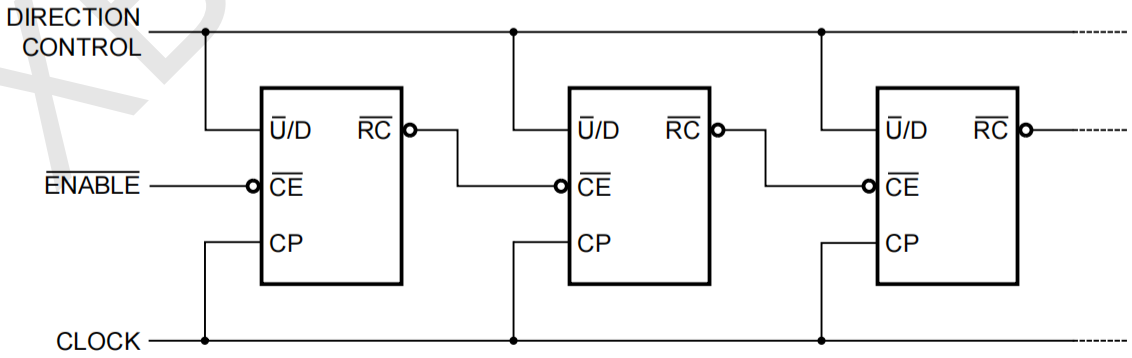


Figure 6. Synchronous n-stage counter using ripple carry/borrow

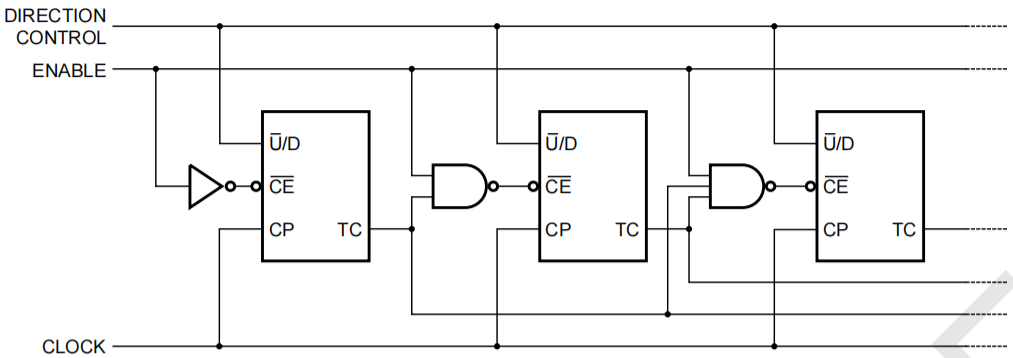


Figure 7. Synchronous n-stage counter with parallel gated carry/borrow

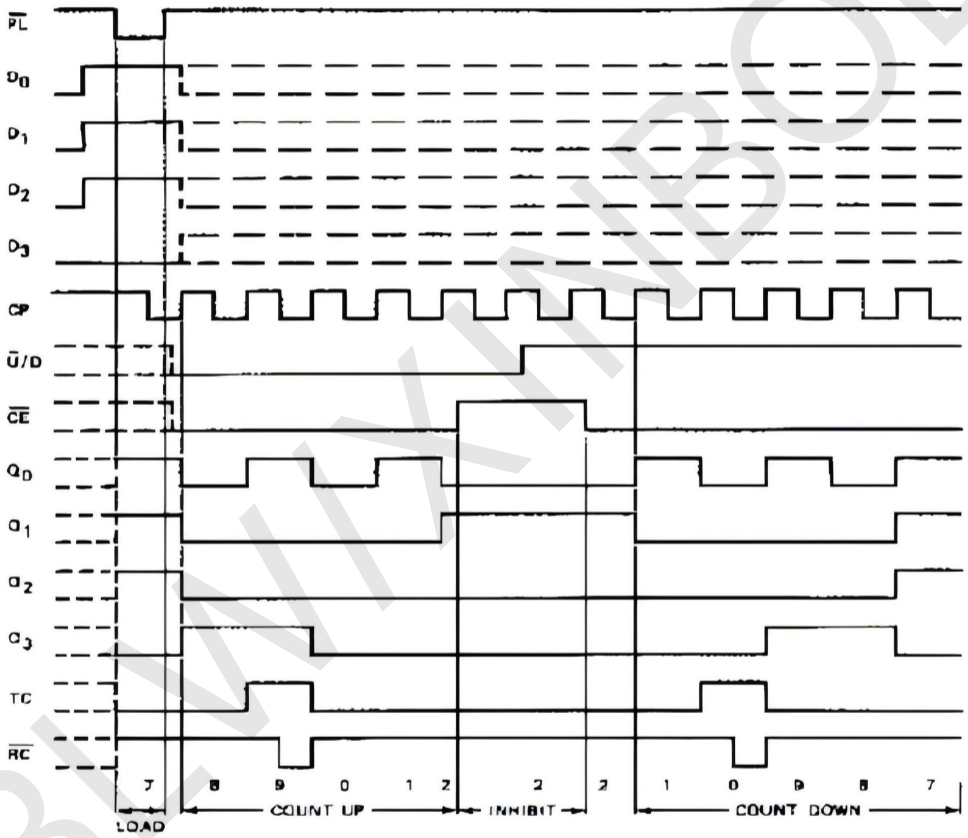
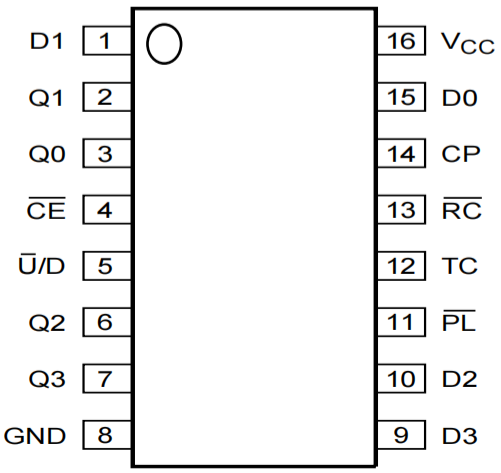


Figure 8. Typical timing sequence

Pin Configurations



Pin Description

Pin No.	Pin Name	Description
1	D1	data input
2	Q1	flip-flop output
3	Q0	flip-flop output
4	$\overline{CE}$	count enable input (active LOW)
5	$\overline{U}$/D	up/down input
6	Q2	flip-flop output
7	Q3	flip-flop output
8	GND	ground (0V)
9	D3	data input
10	D2	data input
11	$\overline{PL}$	parallel load input (active LOW)
12	TC	terminal count output
13	$\overline{RC}$	ripple clock output (active LOW)
14	CP	clock input (LOW-to-HIGH, edge-triggered)
15	D0	data input
16	V_{CC}	supply voltage

Function Table

Operating mode	Input					Output
	$\overline{PL}$	$\overline{U}$/D	CE	CP	Dn	Qn
parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
count up	H	L	l	↑	X	count up
countdown	H	H	l	↑	X	countdown
hold (do nothing)	H	X	H	X	X	no change

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care;
↑=LOW-to-HIGH clock;l=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.

Input			Terminal count state				Output	
$\overline{U}$/D	$\overline{CE}$	CP	Q0	Q1	Q2	Q3	TC	RC
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	⊓	H	X	X	H	⌐	⊓
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊓	L	L	L	L	⌐	⊓

Note:
[1] H=HIGH voltage level; L=LOW voltage level; X=don't care.
[2] ⊓ =one LOW level output pulse
[3] ⌐ =TC goes LOW on a LOW-to-HIGH clock transition.

Electrical Parameter

Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{CC}	-		-0.5	+7.0	V
input clamping current	I_{IK}	V_I < -0.5V or V_I > V_{CC}+0.5V		-	±20	mA
output clamping current	I_{OK}	V_O < -0.5V or V_O > V_{CC}+0.5V		-	±20	mA
output current	I_O	V_O= -0.5V to V_{CC}+0.5V		-	±25	mA
supply current	I_{CC}	-		-	+50	mA
ground current	I_{GND}	-		-50	-	mA
storage temperature	T_{stg}	-		-65	+150	℃
total power dissipation	P_{tot}	-		-	500	mW
Soldering temperature	T_L	10s	DIP	245		℃
			SOP/TSSOP	260		

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	Δt/ΔV	V_{CC}=2.0V	-	-	625	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	83	ns/V
ambient temperature	T_{amb}	-	-20	-	+85	℃

DC Characteristics 1

(T_{amb}=25°C, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	1.2	-	V
		V_{CC}=4.5V		3.15	2.4	-	V
		V_{CC}=6.0V		4.2	3.2	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	0.8	0.5	V
		V_{CC}=4.5V		-	2.1	1.35	V
		V_{CC}=6.0V		-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.98	4.32	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.48	5.81	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	0.15	0.26	V
			I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.26	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	8.0	uA
input capacitance	C_I	-		-	3.5	-	pF

DC Characteristics 2

(T_{amb}=-20℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.84	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.34	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	-	0.33	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA

AC Characteristics 1

(T_{amb}=25°C, GND=0V; t_r=t_f=6ns; C_L=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
propagation delay	t_{pd}	CP to Qn; see Figure 10	V_{CC}=2.0V	-	72	220	ns
			V_{CC}=4.5V	-	26	44	ns
			V_{CC}=5.0V; C_L= 15pF	-	22	-	ns
			V_{CC}=6.0V	-	21	37	ns
		CP to TC; see Figure 10	V_{CC}=2.0V	-	83	255	ns
			V_{CC}=4.5V	-	30	51	ns
			V_{CC}=6.0V	-	24	43	ns
		CP to $\overline{RC}$; see Figure 11	V_{CC}=2.0V	-	44	150	ns
			V_{CC}=4.5V	-	16	30	ns
			V_{CC}=6.0V	-	13	26	ns
		$\overline{CE}$ to $\overline{RC}$; see Figure 11	V_{CC}=2.0V	-	33	130	ns
			V_{CC}=4.5V	-	12	26	ns
			V_{CC}=6.0V	-	10	22	ns
		Dn to Qn; see Figure 12	V_{CC}=2.0V	-	63	220	ns
			V_{CC}=4.5V	-	23	44	ns
			V_{CC}=6.0V	-	18	37	ns
		$\overline{PL}$ to Qn; see Figure 13	V_{CC}=2.0V	-	63	220	ns
			V_{CC}=4.5V	-	23	44	ns
			V_{CC}=6.0V	-	18	37	ns
		$\overline{U}$/D to TC; see Figure 14	V_{CC}=2.0V	-	44	190	ns
			V_{CC}=4.5V	-	16	38	ns
			V_{CC}=6.0V	-	13	32	ns
		$\overline{U}$/D to $\overline{RC}$; see Figure 14	V_{CC}=2.0V	-	50	210	ns
			V_{CC}=4.5V	-	18	42	ns
			V_{CC}=6.0V	-	14	36	ns
transition time	t_t	see Figure 15	V_{CC}=2.0V	-	19	75	ns
			V_{CC}=4.5V	-	7	15	ns
			V_{CC}=6.0V	-	6	13	ns
pulse width	t_W	CP; HIGH or LOW; see Figure 10	V_{CC}=2.0V	155	28	-	ns
			V_{CC}=4.5V	31	10	-	ns
			V_{CC}=6.0V	26	8	-	ns
		$\overline{PL}$; LOW; see Figure 15	V_{CC}=2.0V	100	25	-	ns
			V_{CC}=4.5V	20	9	-	ns
			V_{CC}=6.0V	17	7	-	ns
recovery time	t_{rec}	$\overline{PL}$ to CP; see Figure 15	V_{CC}=2.0V	35	8	-	ns
			V_{CC}=4.5V	7	3	-	ns
			V_{CC}=6.0V	6	2	-	ns
set-up time	t_{su}	$\overline{U}$/D to CP;	V_{CC}=2.0V	205	61	-	ns

		see Figure 16	V_{CC}=4.5V	41	22	-	ns
			V_{CC}=6.0V	35	18	-	ns
		Dn to $\overline{PL}$; see Figure 17	V_{CC}=2.0V	100	19	-	ns
			V_{CC}=4.5V	20	7	-	ns
			V_{CC}=6.0V	17	6	-	ns
		$\overline{CE}$ to CP; see Figure 16	V_{CC}=2.0V	140	39	-	ns
			V_{CC}=4.5V	28	14	-	ns
			V_{CC}=6.0V	24	11	-	ns
hold time	t_h	$\overline{U}$/D to CP; see Figure 16	V_{CC}=2.0V	0	-44	-	ns
			V_{CC}=4.5V	0	-16	-	ns
			V_{CC}=6.0V	0	-13	-	ns
		Dn to $\overline{PL}$; see Figure 17	V_{CC}=2.0V	0	-14	-	ns
			V_{CC}=4.5V	0	-5	-	ns
			V_{CC}=6.0V	0	-4	-	ns
		$\overline{CE}$ to CP; see Figure 16	V_{CC}=2.0V	0	-19	-	ns
			V_{CC}=4.5V	0	-7	-	ns
			V_{CC}=6.0V	0	-6	-	ns
maximum frequency	f_{max}	CP; see Figure 10	V_{CC}=2.0V	3.0	8.3	-	MHz
			V_{CC}=4.5V	15	25	-	MHz
			V_{CC}=5.0V; C_L= 15pF	-	28	-	MHz
			V_{CC}=6.0V	18	30	-	MHz
power dissipation capacitance	C_{PD}	V_I=GND to V_{CC}		-	36	-	pF

Note:
[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
[2] t_t is the same as t_{THL} and t_{TLH}.
[3] C_{PD} isused to determine the dynamic power dissipation (P_D in uW).
$P_D=C_{PD}\times V_{CC}^2\times f_i+\Sigma(C_L\times V_{CC}^2\times f_o)$ where:
f_i=input frequency in MHz;
f_o=output frequency in MHz;
C_L=output load capacitance in pF;
V_{CC}=supply voltage in V;
$\Sigma(C_L\times V_{CC}^2\times f_o)$=sum of outputs.

AC Characteristics 2

(T_{amb}=-20℃ to +85℃, GND=0V; t_r=t_f=6ns; C_L=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
propagation delay	t_{pd}	CP to Qn; see Figure 10	V_{CC}=2.0V	-	-	275	ns
			V_{CC}=4.5V	-	-	55	ns
			V_{CC}=6.0V	-	-	47	ns
		CP to TC; see Figure 10	V_{CC}=2.0V	-	-	320	ns
			V_{CC}=4.5V	-	-	64	ns
			V_{CC}=6.0V	-	-	54	ns
		CP to $\overline{RC}$; see Figure 11	V_{CC}=2.0V	-	-	190	ns
			V_{CC}=4.5V	-	-	38	ns
			V_{CC}=6.0V	-	-	33	ns
		$\overline{CE}$ to $\overline{RC}$; see Figure 11	V_{CC}=2.0V	-	-	165	ns
			V_{CC}=4.5V	-	-	33	ns
			V_{CC}=6.0V	-	-	28	ns
		Dn to Qn; see Figure 12	V_{CC}=2.0V	-	-	275	ns
			V_{CC}=4.5V	-	-	55	ns
			V_{CC}=6.0V	-	-	47	ns
		$\overline{PL}$ to Qn; see Figure 13	V_{CC}=2.0V	-	-	275	ns
			V_{CC}=4.5V	-	-	55	ns
			V_{CC}=6.0V	-	-	47	ns
		$\overline{U}$/D to TC; see Figure 14	V_{CC}=2.0V	-	-	240	ns
			V_{CC}=4.5V	-	-	48	ns
			V_{CC}=6.0V	-	-	41	ns
		$\overline{U}$/D to $\overline{RC}$; see Figure 14	V_{CC}=2.0V	-	-	265	ns
			V_{CC}=4.5V	-	-	53	ns
			V_{CC}=6.0V	-	-	45	ns
transition time	t_t	see Figure 15	V_{CC}=2.0V	-	-	95	ns
			V_{CC}=4.5V	-	-	19	ns
			V_{CC}=6.0V	-	-	16	ns
pulse width	t_W	CP; HIGH or LOW; see Figure 10	V_{CC}=2.0V	195	-	-	ns
			V_{CC}=4.5V	39	-	-	ns
			V_{CC}=6.0V	33	-	-	ns
		$\overline{PL}$; LOW; see Figure 15	V_{CC}=2.0V	125	-	-	ns
			V_{CC}=4.5V	25	-	-	ns
			V_{CC}=6.0V	21	-	-	ns
recovery time	t_{rec}	$\overline{PL}$ to CP; see Figure 15	V_{CC}=2.0V	45	-	-	ns
			V_{CC}=4.5V	9	-	-	ns
			V_{CC}=6.0V	8	-	-	ns
set-up time	t_{su}	$\overline{U}$/D to CP; see Figure 16	V_{CC}=2.0V	255	-	-	ns
			V_{CC}=4.5V	51	-	-	ns
			V_{CC}=6.0V	43	-	-	ns
		Dn to $\overline{PL}$; see Figure 17	V_{CC}=2.0V	125	-	-	ns
			V_{CC}=4.5V	25	-	-	ns
			V_{CC}=6.0V	21	-	-	ns
		$\overline{CE}$ to CP; see Figure 16	V_{CC}=2.0V	175	-	-	ns
			V_{CC}=4.5V	35	-	-	ns

			V_{CC}=6.0V	30	-	-	ns
hold time	t_h	$\overline{U}$/D to CP; see Figure 16	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
		Dn to $\overline{PL}$; see Figure 17	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
		$\overline{CE}$ to CP; see Figure 16	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
maximum frequency	f_{max}	CP; see Figure 10	V_{CC}=2.0V	2.4	-	-	MHz
			V_{CC}=4.5V	12	-	-	MHz
			V_{CC}=6.0V	14	-	-	MHz

Note:
[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
[2] t_t is the same as t_{THL} and t_{TLH}.

Testing Circuit

AC Testing Circuit

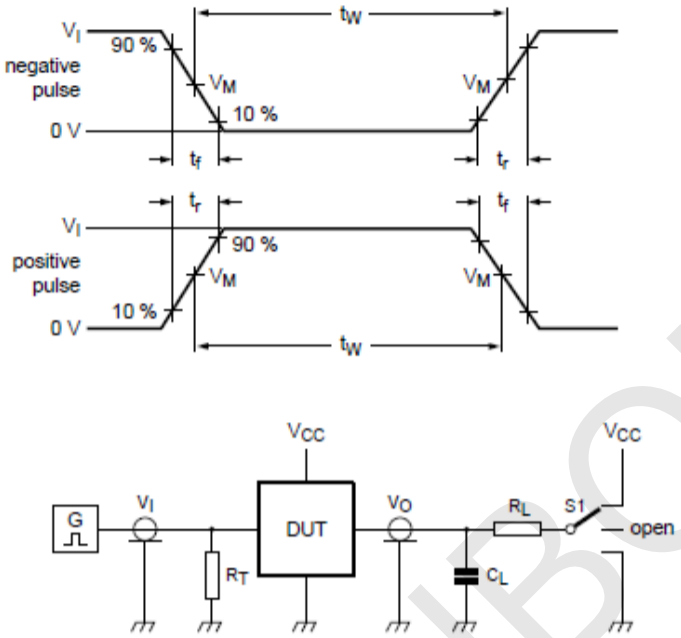


Figure 9. Test circuit for measuring switching times

Definitions for test circuit:
C_L=Load capacitance including jig and probe capacitance.
R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.
R_L=Load resistance.
S1=Test selection switch

AC Testing Waveforms

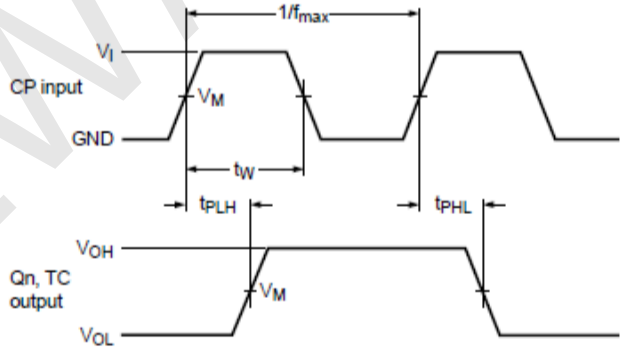


Figure 10. The clock input (CP) to outputs (Qn, TC) propagation delays, clock pulse width and maximum clock frequency

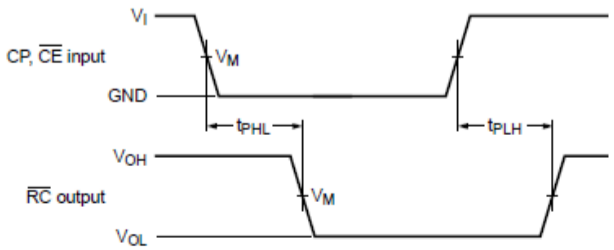


Figure 11. The clock and count enable inputs (CP, $\overline{CE}$) to ripple clock output ($\overline{RC}$) propagation delays

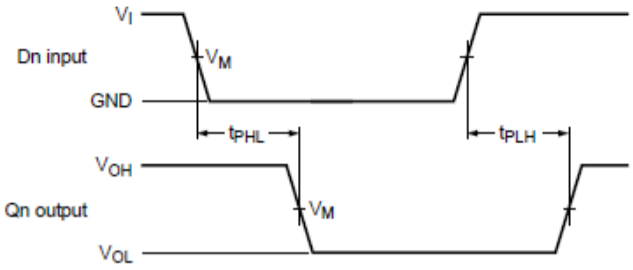


Figure 12. The input (Dn) to output (Qn) propagation delays

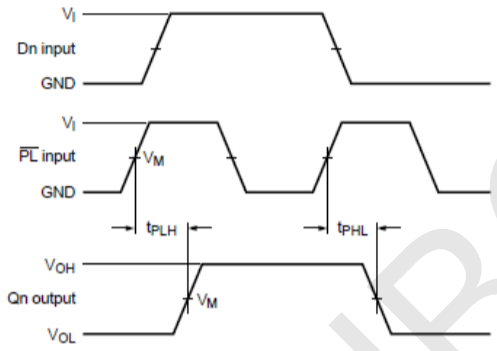


Figure 13. The parallel load input ($\overline{PL}$) to output (Qn) propagation delays

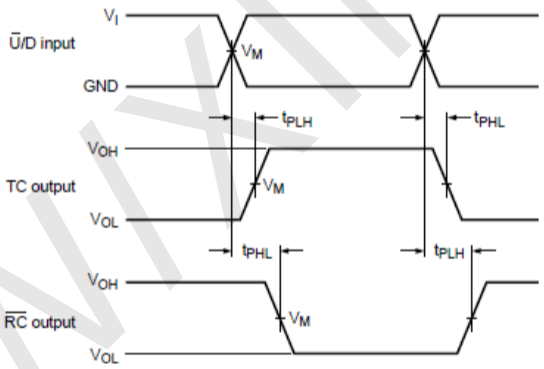


Figure 14. The up/down count input ($\overline{U}$/D) to terminal count and ripple clock output (TC, $\overline{RC}$) propagation delays

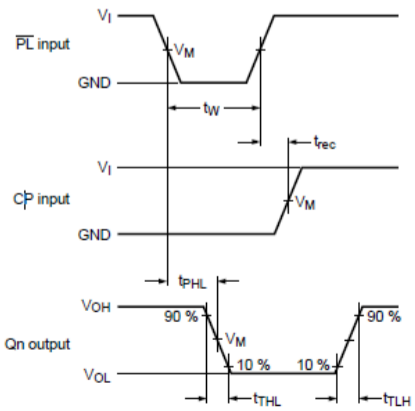


Figure 15. The parallel load input ($\overline{PL}$) to clock (CP) recovery times, parallel load pulse width and output (Qn) transition times

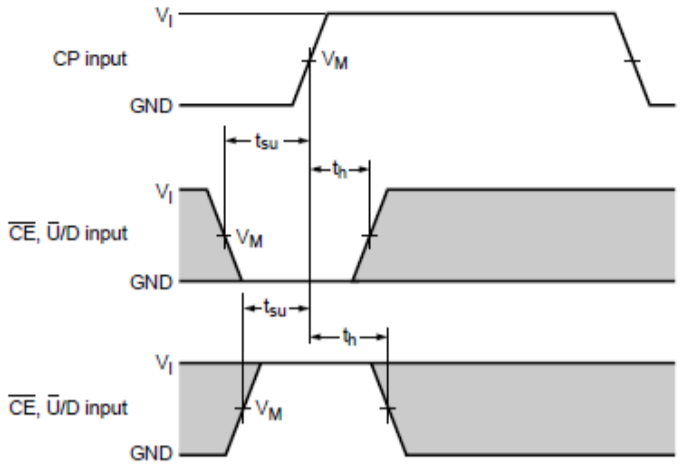


Figure 16. The count enable and up/down count inputs ($\overline{CE}$, $\overline{U}$/D) to clock input (CP) set-up and hold times

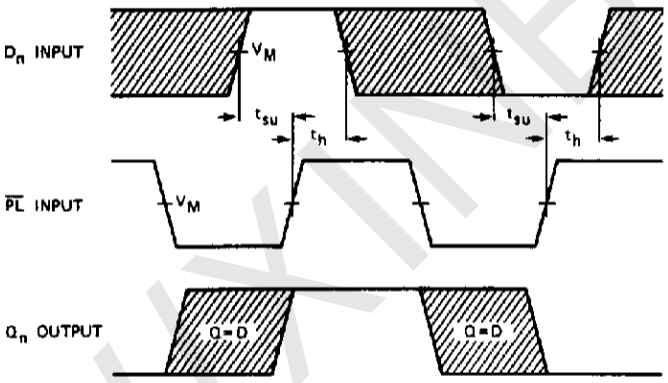


Figure 17. Waveforms showing the set-up and hold times from the parallel load input ($\overline{PL}$) to the data input (Dn)

Measurement Points

Type	Input	Output
	V_M	V_M
SN74LS190	0.5 ×V_{CC}	0.5 ×V_{CC}

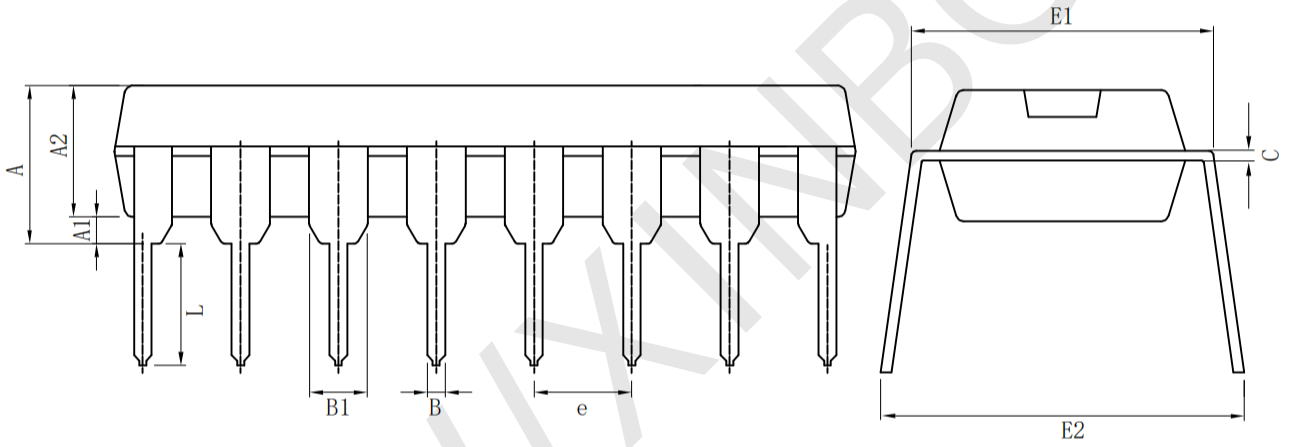
Test Data

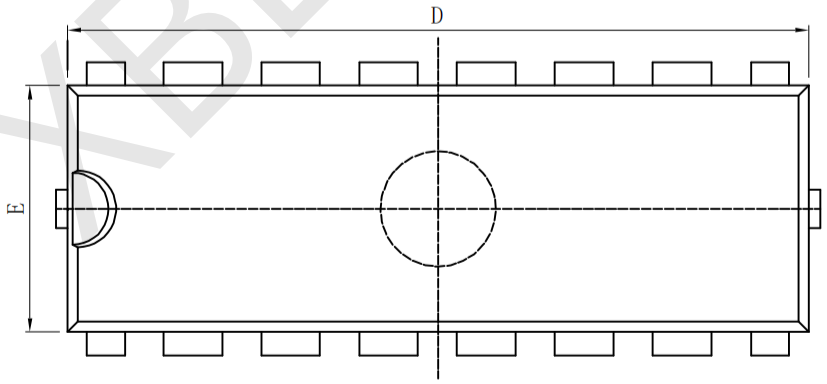
Type	Input		Load		S1 position
	V_I	t_r ,t_f	C_L	R_L	t_{PLH}, t_{PHL}
SN74LS190	V_{CC}	6ns	15pF, 50pF	1kΩ	open

PackageInformation

· DIP-16

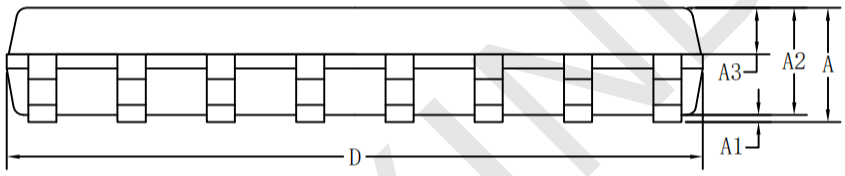
Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	3.710	4.310	A	0.146	0.170
A1	0.510		A1	0.020	
A2	3.200	3.600	A2	0.126	0.142
B	0.380	0.570	B	0.015	0.022
B1	1.524(BSC)		B1	0.060(BSC)	
C	0.204	0.360	C	0.008	0.014
D	18.80	19.20	D	0.740	0.756
E	6.200	6.600	E	0.244	0.260
E1	7.320	7.920	E1	0.288	0.312
e	2.540(BSC)		e	0.100(BSC)	
L	3.000	3.600	L	0.118	0.142
E2	8.400	9.000	E2	0.331	0.354

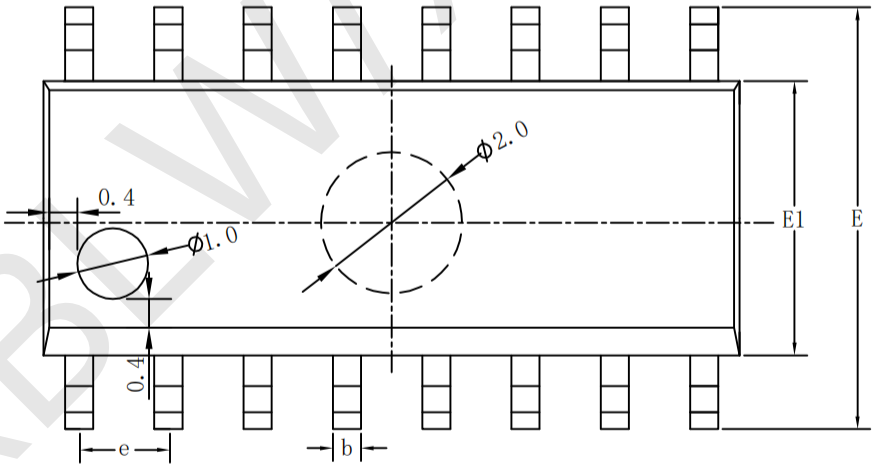


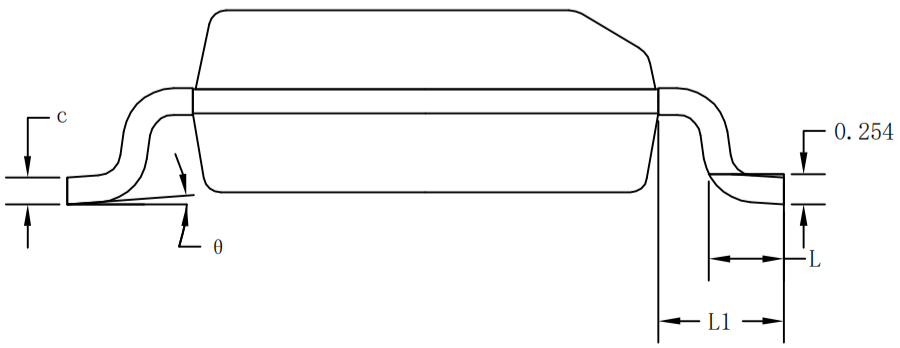


· SOP-16

Size / Symbol	Dimensions In Millimeters			Size / Symbol	Dimensions In Inches		
	Min(mm)	Nom(mm)	Max(mm)		Min(in)	Nom(in)	Max(in)
A	1.500	1.600	1.700	A	0.059	0.063	0.067
A1	0.100	0.150	0.250	A1	0.004	0.006	0.010
A2	1.400	1.450	1.500	A2	0.055	0.057	0.059
A3	0.600	0.650	0.700	A3	0.024	0.026	0.028
b	0.300	0.400	0.500	b	0.012	0.016	0.020
c	0.150	0.200	0.250	c	0.006	0.008	0.010
D	9.800	9.900	10.00	D	0.386	0.390	0.394
E	5.800	6.000	6.200	E	0.228	0.236	0.244
E1	3.850	3.900	3.950	E1	0.152	0.154	0.156
e	1.27(BSC)			e	0.050(BSC)		
L	0.500	0.600	0.700	L	0.020	0.024	0.028
L1	1.05(BSC)			L1	0.041(BSC)		
θ	0°	4°	8°	θ	0°	4°	8°

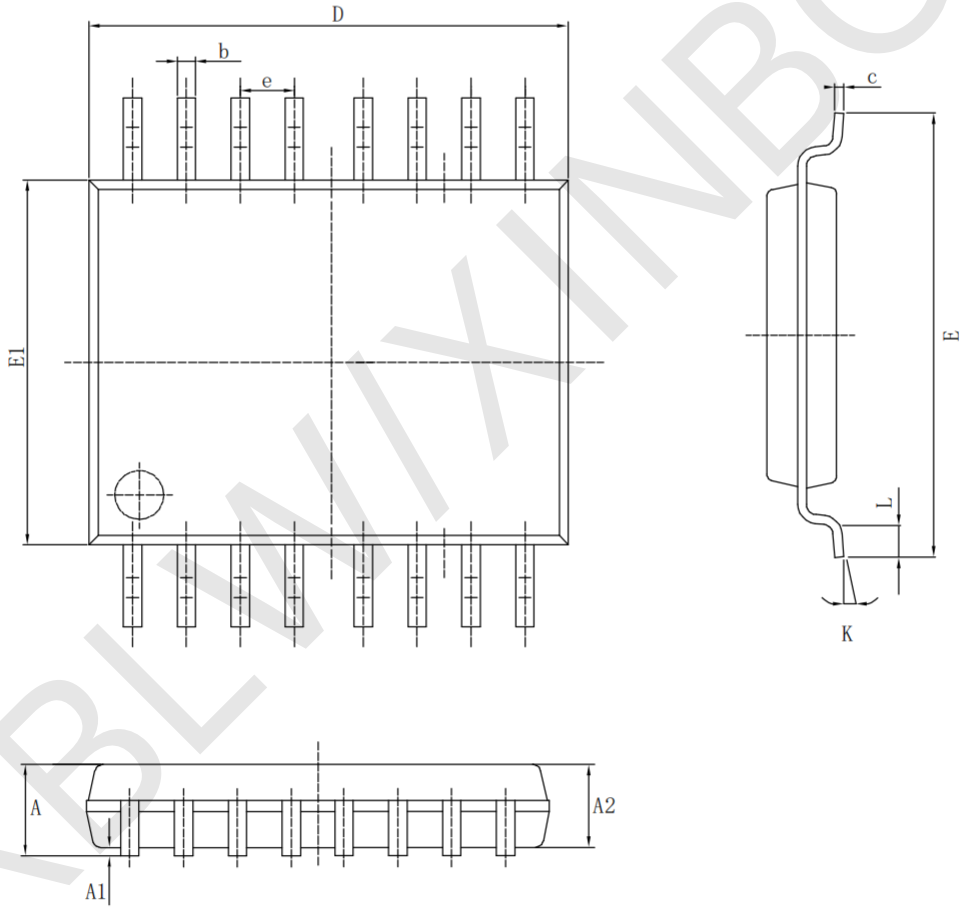






· TSSOP-16

Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A		1.200	A		0.047
A1	0.050	0.150	A1	0.002	0.006
A2	0.800	1.050	A2	0.031	0.041
b	0.190	0.300	b	0.007	0.012
c	0.090	0.200	c	0.004	0.0089
D	4.900	5.100	D	0.193	0.201
E	6.200	6.600	E	0.244	0.260
E1	4.300	4.480	E1	0.169	0.176
e	0.65(BSC)		e	0.0256(BSC)	
K	0°	8°	K	0°	8°
L	0.450	0.750	L	0.018	0.030



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