General Description

The CD4021 is an 8-bit static shift register (parallel-to-serial converter) with a synchronous serial data input (DS), a clock input (CP), an asynchronous active HIGH parallel load input (PL), eight asynchronous parallel data inputs (D0 to D7) and buffered parallel outputs from the last three stages (Q5 to Q7). Each register stage is a D-type master-slave flip-flop with a set direct (SD) and clear direct (CD) input. Information on D0 to D7 is asynchronously loaded into the register while PL is HIGH, independent of CP and DS. When PL is LOW, data on DS is shifted into the first register position and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of CP. Schmitt trigger action makes the clock input highly tolerant of slower rise and fall times.

It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

Features

- Tolerant of slower rise and fall times
- Fully static operation
- 5V, 10V, and 15V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40℃ to +105℃
- Packaging information: DIP16/SOP16/TSSOP16

ORDERING INFORMATION

DEVICE	Package Type	MARKING	Packing	Packing QTY
CD4021BE	DIP-16	CD4021BE	Tube	1000/Box
CD4021BDTR	SOP-16	CD4021B	Tape	2500/Reel
CD4021BTDTR	TSSOP-16	CD4021B	Tape	3000/Reel

Block Diagram And Pin Description

Block Diagram

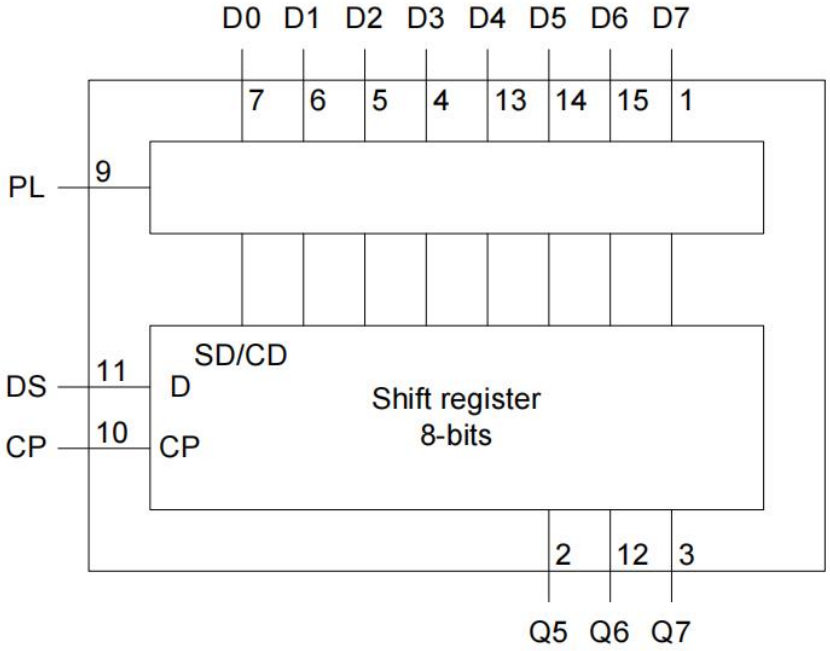


Figure 1. Functional diagram

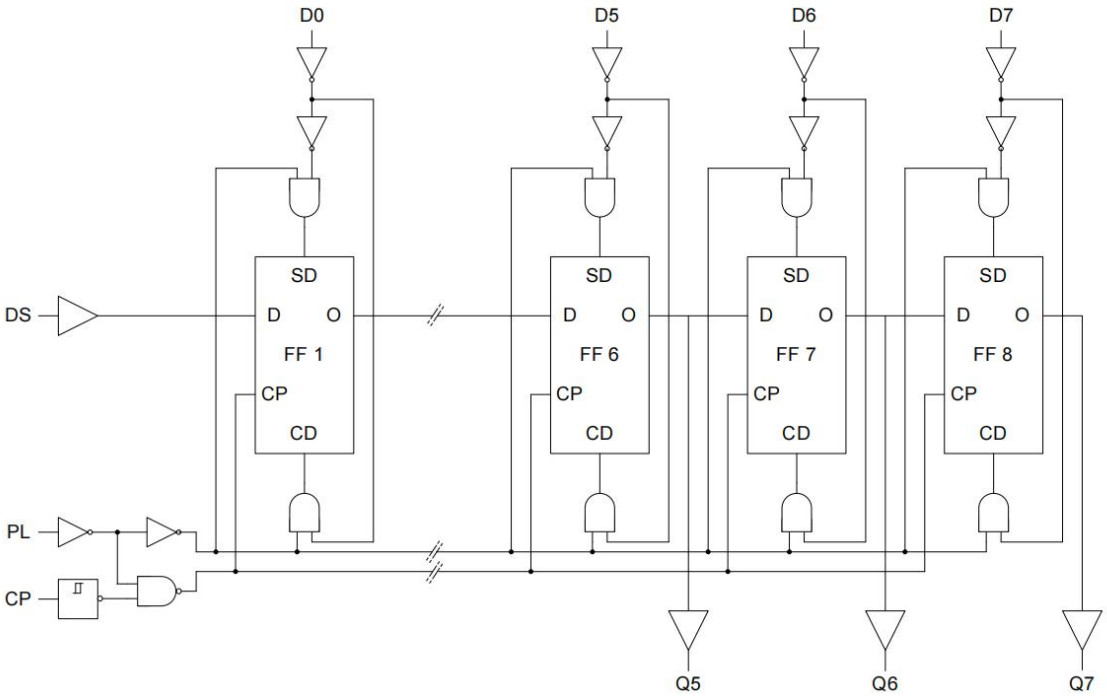
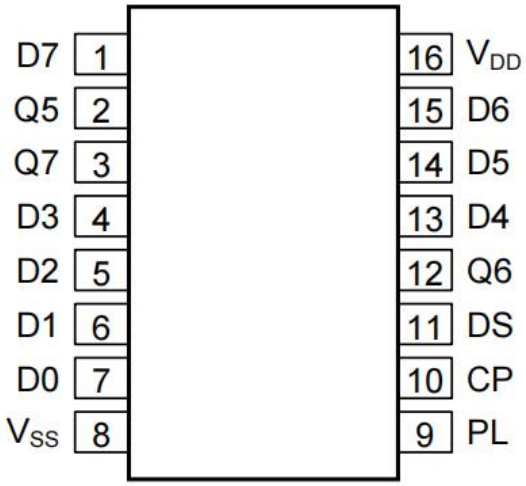


Figure 2. Logic diagram

Pin Configurations



Pin Description

Pin No.	Pin Name	Description
1	D7	parallel data input
2	Q5	buffered parallel output from the last three stages
3	Q7	buffered parallel output from the last three stages
4	D3	parallel data input
5	D2	parallel data input
6	D1	parallel data input
7	D0	parallel data input
8	V_{SS}	ground supply voltage
9	PL	parallel load input
10	CP	clock input (LOW-to-HIGH edge-triggered)
11	DS	serial data input
12	Q6	buffered parallel output from the last three stages
13	D4	parallel data input
14	D5	parallel data input
15	D6	parallel data input
16	V_{DD}	supply voltage

Function Table

Number of clock transitions	Inputs			Outputs		
	CP	DS	PL	Q5	Q6	Q7
Serial operation						
1	↑	data 1	L	X	X	X
2	↑	data 2	L	X	X	X
3	↑	data 3	L	X	X	X
6	↑	X	L	data 1	X	X
7	↑	X	L	data 2	data 1	X
8	↑	X	L	data 3	data 2	data 1
	↓	X	L	no change	no change	no change
Parallel operation						
	X	X	H	D5	D6	D7

Note:

[1] H=HIGH voltage level; L=LOW voltage level; X=don't care;

↑=LOW to HIGH clock transition; ↓=HIGH to LOW clock transition;

data n=data (HIGH or LOW) on the DS input at the n^{th} ↑ CP transition.

Electrical Parameter

Absolute Maximum Ratings (T_{amb}=25℃, unless otherwise specified.)

Characteristic	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{DD}	-		-0.5	+18	**V**
input clamping current	I_{IK}	V_I < -0.5V or V_I > V_{DD} +0.5V		-	±10	mA
input voltage	V_I	-		-0.5	V_{DD} +0.5	V
output clamping current	I_{OK}	V_I < -0.5V or V_I > V_{DD} +0.5V		-	±10	mA
input/output current	$I_{I/O}$	-		-	±10	mA
supply current	I_{DD}	-		-	50	mh
operating temperature	T_{amb}	-		-40	+105	℃
storage temperature	T_{stg}	-		-65	+150	℃
total power dissipation	P_{tot}	-		500		mW
power dissipation	P_D	per output		100		mW
soldering temperature	T_L	10s	DIP	245		℃
			SOP/TSSOP	260		℃

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{DD}	-	3	-	15	V
input voltage	V_I	-	0	-	V_{DD}	V
operating temperature	T_{amb}	-	-40	-	+105	℃

Electrical Characteristics

DC Characteristics 1 (Tamb=25℃, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions(V)			T_{amb}=25℃			Unit
		V_O	V_{IN}	V_{DD}	Min.	Typ.	Max.	
supply current	I_{DD}	-	0, 5	5	-	-	5	μA
		-	0, 10	10	-	-	10	μA
		-	0, 15	15	-	-	20	μA
LOW-level output current	I_{OL}	0.4	0, 5	5	0.5	-	-	mA
		0.5	0, 10	10	1.3	-	-	mA
		1.5	0, 15	15	3.4	-	-	mA
HIGH-level output current	I_{OH}	4.6	0, 5	5	-	-	-0.5	mA
		2.5	0, 5	5	-	-	-1.4	mA
		9.5	0, 10	10	-	-	-1.3	mA
		13.5	0, 15	15	-	-	-3.4	mA
LOW-level output voltage	V_{OL}	-	0, 5	5	-	-	0.05	V
		-	0, 10	10	-	-	0.05	V
		-	0, 15	15	-	-	0.05	V
HIGH-level output voltage	V_{OH}	-	0, 5	5	4.95	-	-	V
		-	0, 10	10	9.95	-	-	V
		-	0, 15	15	14.95	-	-	V
LOW-level input voltage	V_{IL}	4.5	-	5	-	-	1.5	V
		9	-	10	-	-	3	V
		13.5	-	15	-	-	4	V
HIGH-level input voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	-	V
		1, 9	-	10	7	-	-	V
		1.5, 13.5	-	15	11	-	-	V
input leakage current	I_I	-	0, 15	15	-	-	±1.0	μA
input capacitance	C_I	-	-	-	-	-	7.5	pF

DC Characteristics 2

(Tamb=-40℃ to +105℃, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions(V)			T_{amb}=-40℃		T_{amb}=+85℃		T_{amb}=+105℃		Unit
		V_O	V_{IN}	V_{DD}	Min.	Max.	Min.	Max.	Min.	Max.	
supply current	I_{DD}	-	0, 5	5	-	5	-	150	-	15	μA
		-	0, 10	10	-	10	-	300	-	300	μA
		-	0, 15	15	-	20	-	600	-	600	μA
LOW-level output current	I_{OL}	0.4	0, 5	5	0.64	-	0.36	-	0.36	-	mA
		0.5	0, 10	10	1.6	-	0.9	-	0.9	-	mA
		1.5	0, 15	15	4.2	-	2.4	-	2.4	-	mA
HIGH-level output current	I_{OH}	4.6	0, 5	5	-	-0.64	-	-0.36	-	-0.36	mA
		2.5	0, 5	5	-	-1.7	-	-1.1	-	-1.1	mA
		9.5	0, 10	10	-	-1.6	-	-0.9	-	-0.9	mA
		13.5	0, 15	15	-	-4.2	-	-2.4	-	-2.4	mA
LOW-level output voltage	V_{OL}	-	0, 5	5	-	0.05	-	0.05	-	0.05	V
		-	0, 10	10	-	0.05	-	0.05	-	0.05	V
		-	0, 15	15	-	0.05	-	0.05	-	0.05	V
HIGH-level output voltage	V_{OH}	-	0, 5	5	4.95	-	4.95	-	4.95	-	V
		-	0, 10	10	9.95	-	9.95	-	9.95	-	V
		-	0, 15	15	14.95	-	14.95	-	14.95	-	V
LOW-level input voltage	V_{IL}	4.5	-	5	-	1.5	-	1.5	-	1.5	V
		9	-	10	-	3	-	3	-	3	V
		13.5	-	15	-	4	-	4	-	4	V
HIGH-level input voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	3.5	-	3.5	-	V
		1, 9	-	10	7	-	7	-	7	-	V
		1.5, 13.5	-	15	11	-	11	-	11	-	V
input leakage current	I_I	-	0, 15	15	-	±0.1	-	±1.0	-	±1.0	μA

AC Characteristics (T_{amb}=25℃, V_{SS}=0V, unless otherwise specified.)

Parameter	Symbol	Conditions	VDD	Min.	Typ.	Max.	Unit
HIGH to LOW propagation delay	t_{PHL}	CP to Qn; see Figure 4	5	-	125	250	ns
			10	-	55	110	ns
			15	-	40	80	ns
		PL to Qn; see Figure 4	5	-	135	240	ns
			10	-	78	110	ns
			15	-	65	80	ns
LOW to HIGH propagation delay	t_{PLH}	CP to Qn; see Figure 4	5	-	115	230	ns
			10	-	50	100	ns
			15	-	40	80	ns
		PL to Qn; see Figure 4	5	-	135	210	ns
			10	-	78	100	ns
			15	-	72	80	ns
transition time	t_t	Qn; see Figure 4	5	-	60	120	ns
			10	-	30	60	ns
			15	-	20	40	ns
set-up time	t_{SU}	DS to CP; see Figure 5	5	+25	+4	-	ns
			10	+25	0	-	ns
			15	+15	0	-	ns
		Dn to PL; see Figure 6	5	50	-11	-	ns
			10	30	-7	-	ns
			15	20	-3	-	ns
hold time	t_h	DS to CP; see Figure 5	5	40	8	-	ns
			10	20	3	-	ns
			15	15	0	-	ns
		Dn to PL; see Figure 6	5	+15	-13	-	ns
			10	15	-9	-	ns
			15	15	-4	-	ns
pulse width	t_W	CP=LOW; minimum width; see Figure 5	5	70	35	-	ns
			10	30	15	-	ns
			15	24	12	-	ns
		PL=HIGH; minimum width; see Figure 6	5	70	35	-	ns
			10	30	15	-	ns
			15	24	12	-	ns
recovery time	t_{rec}	PL input; see Figure 6	5	50	10	-	ns
			10	40	5	-	ns
			15	35	5	-	ns
maximum clock frequency	$F_{clk(max)}$	CP input; see Figure 5	5	-	13	-	MHz
			10	-	30	-	MHz
			15		40	-	MHz

Testing Circuit

AC Testing Circuit

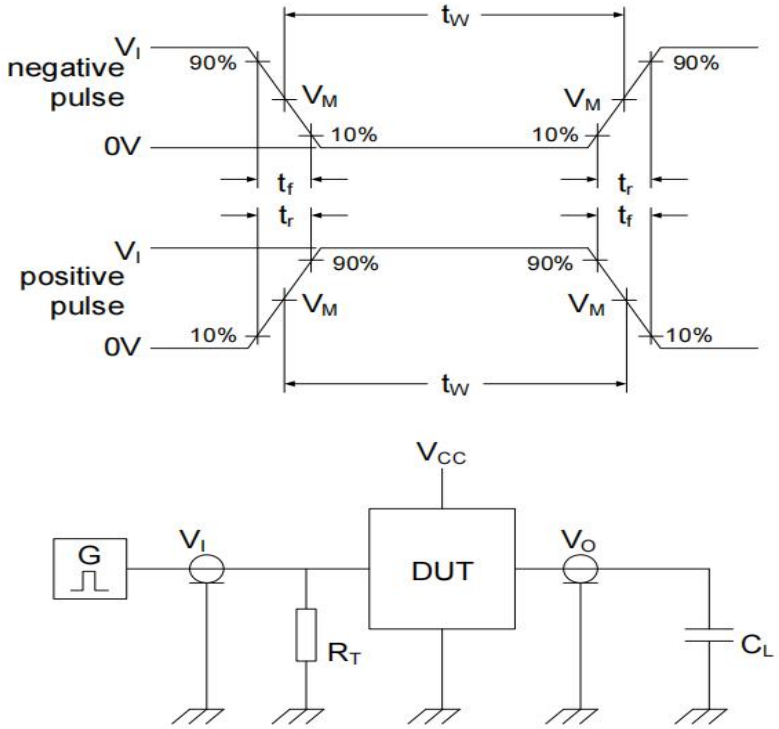


Figure 3. Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

AC Testing Waveforms

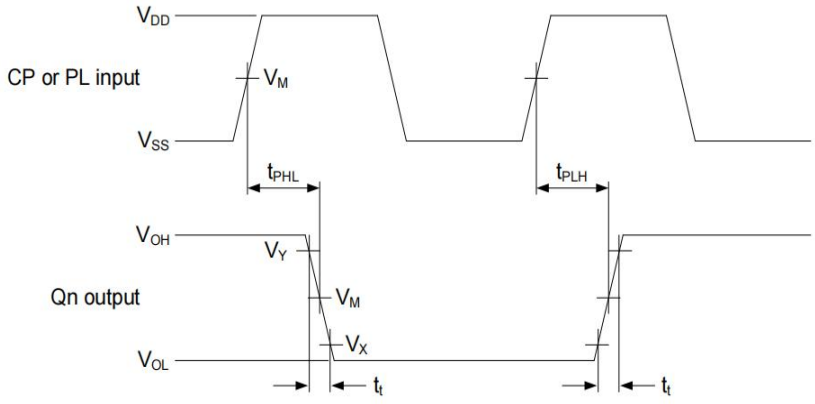


Figure 4. Waveforms showing propagation delays for CP and PL inputs to Qn output and Qn transition times

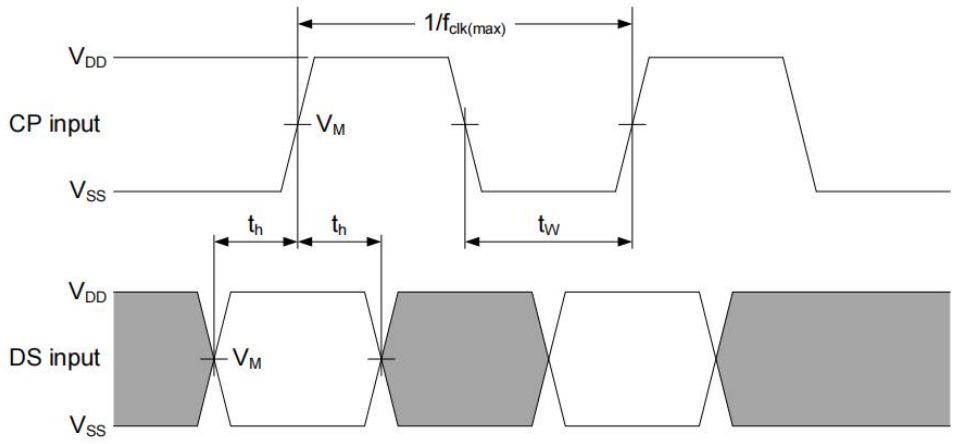


Figure 5. Waveforms showing minimum clock pulse width, set-up time, and hold time for CP and DS.

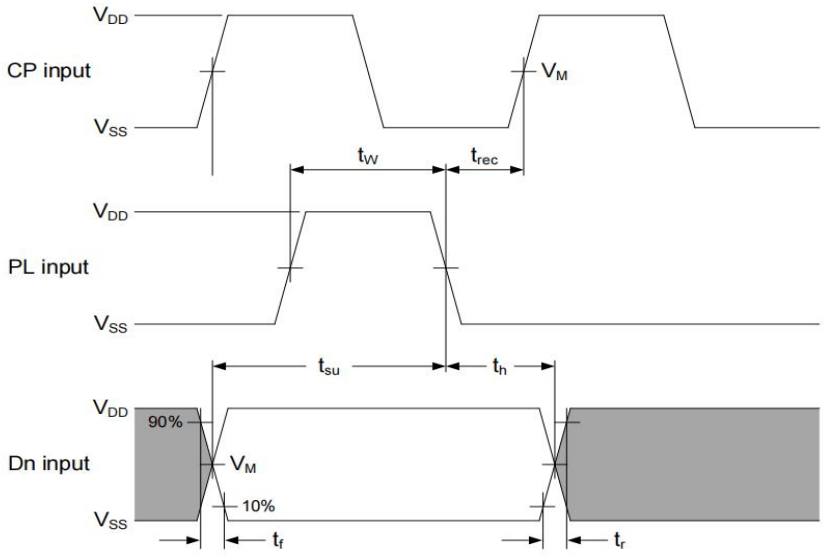


Figure 6. Waveforms showing minimum pulse width and recovery time for PL; set-up and hold times for Dn to PL.

Measurement Points

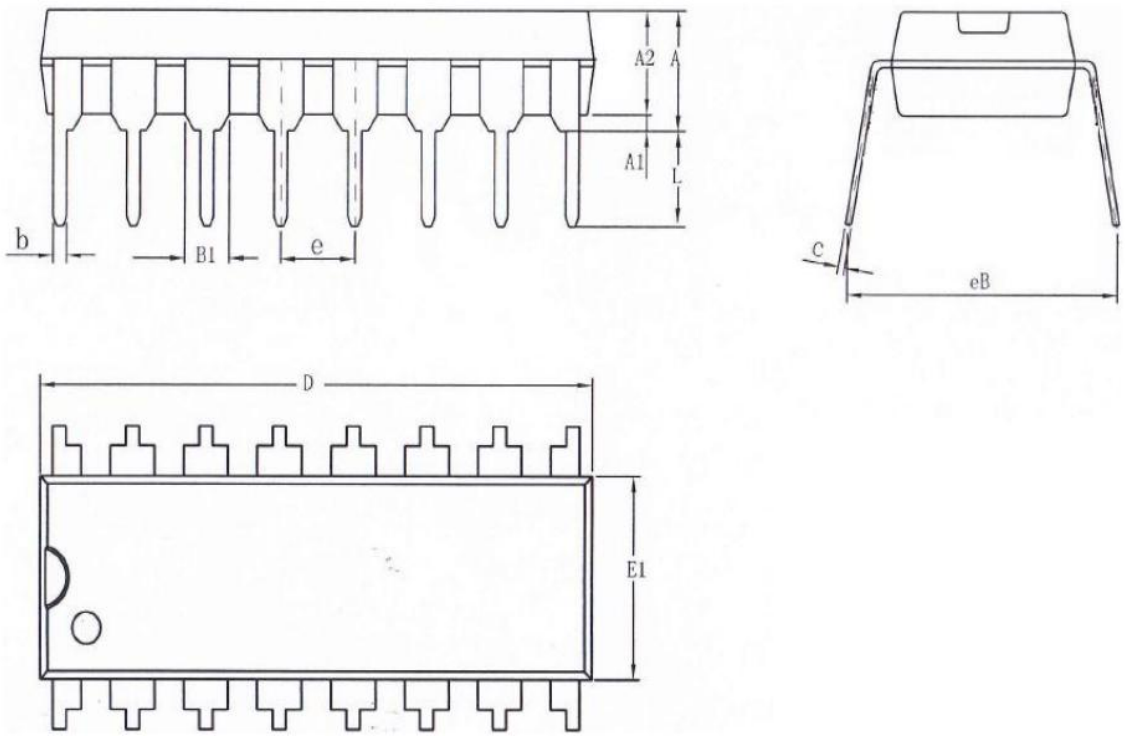
Supply voltage	Input	Output		
V_{DD}	V_M	V_M	V_X	V_Y
5V to 15V	0.5×V_{DD}	0.5×V_{DD}	0.1×V_{DD}	0.9×V_{DD}

Test Data

Supply voltage	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5V to 15V	V_{SS} or V_{DD}	≤20ns	50pF

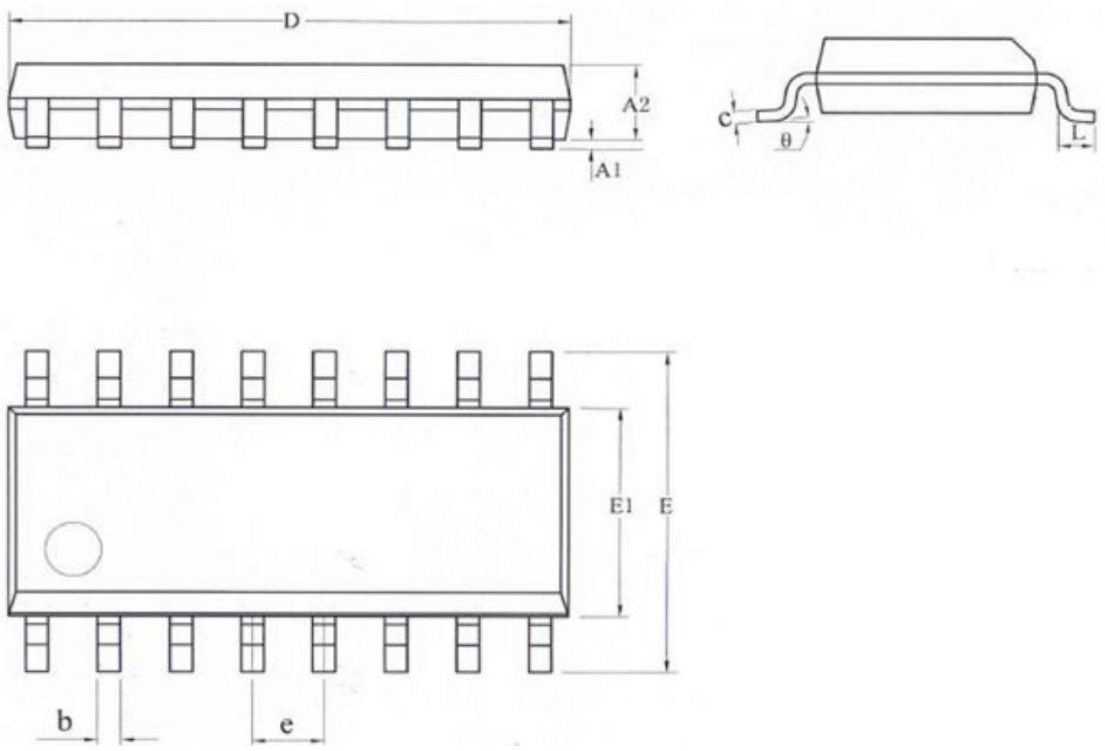
Package Information

DIP16



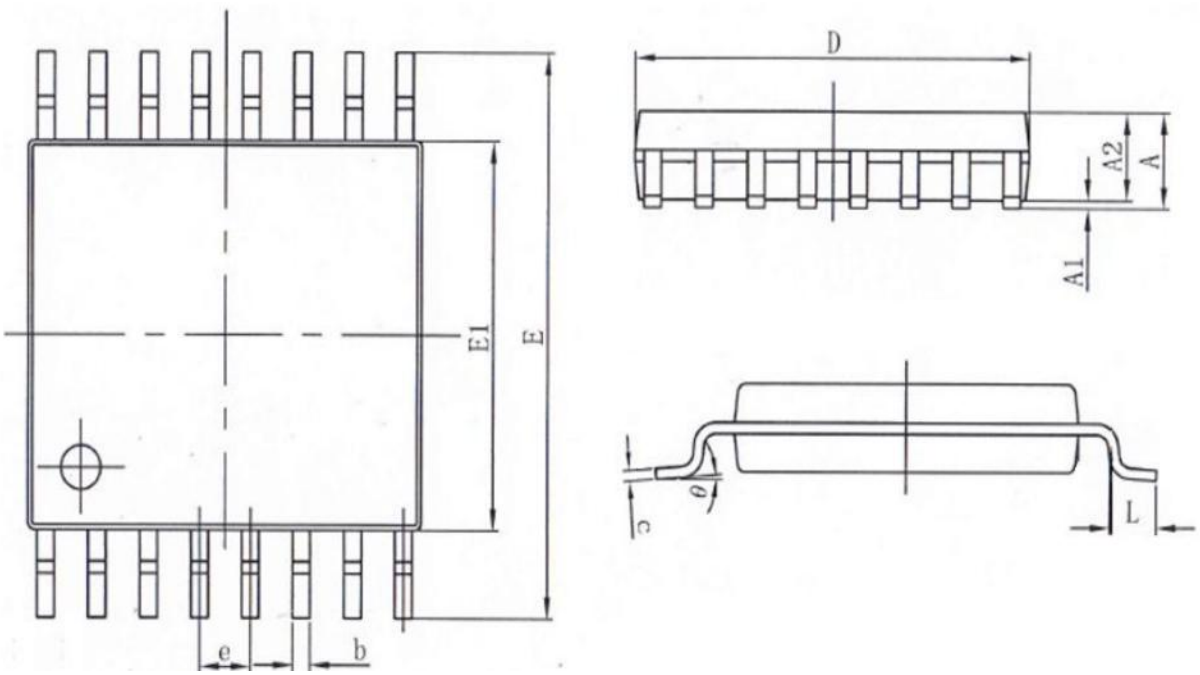
Symbol	Dimensions(mm)	
	Min.	Max.
A2	3.20	3.60
A1	0.51	-
A	3.60	5.33
L	3.00	3.60
b	0.36	0.56
B1	1.52	
D	18.80	19.94
E1	6.20	6.60
e	2.54	
c	0.20	0.36
eB	7.62	9.30

SOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
θ	0°	8°

TSSOP16



SYMBOL	MILLIMETER	
	MIN	MAX
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
θ	0°	8°

Statements And Notes

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butyl benzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements									

Statement：

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