

General Description

The CD4066 provides four single-pole, single-throw analog switch functions. Each switch has two input/output terminals (nY and nZ) and an active HIGH enable input (nE). When nE is LOW, the analog switch is turned off.

The CD4066 is pin compatible with the CD4016 but exhibits a much lower ON resistance. In addition the ON resistance is relatively constant over the full input signal range.

Features

- Wide supply voltage range from 3V to 9V
- Fully static operation
- 5V and 9V parametric ratings
- Standardized symmetrical output characteristics
- Inputs and outputs are protected against electrostatic effects
- Specified from -40 °C to +85 °C
- Packaging information: DIP14/SOP14/TSSOP14

Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
CD4066BE	DIP-14	CD4066BE	Tube	1000/Box
CD4066BDTR	SOP-14	CD4066B	Tape	2500/Reel
CD4066BDTR	TSSOP-14	CD4066B	Tape	3000/Reel

2、Block Diagram And Pin Description

2.1、Block Diagram

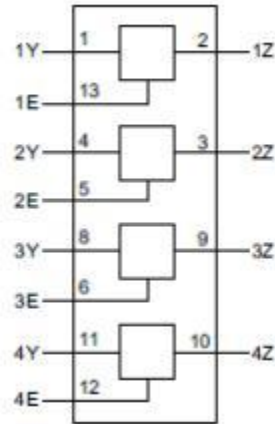


Figure 1. Functional diagram

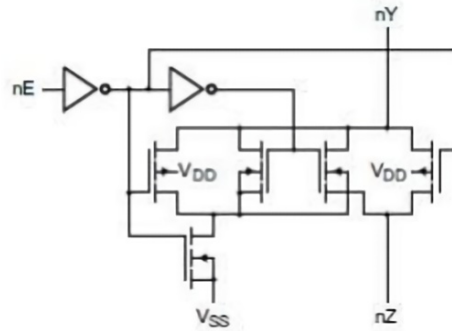
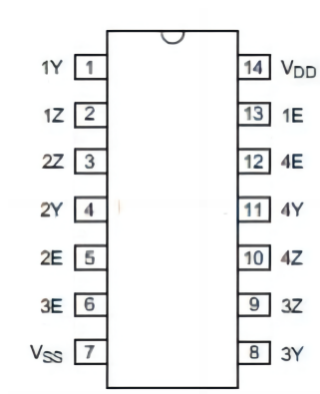


Figure 2. Logic diagram (one switch)

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	1Y	independent input or output
2	1Z	independent input or output
3	2Z	independent input or output
4	2Y	independent input or output
5	2E	enable input (active HIGH)
6	3E	enable input (active HIGH)
7	V _{SS}	ground (0V)
8	3Y	independent input or output
9	3Z	independent input or output
10	4Z	independent input or output
11	4Y	independent input or output
12	4E	enable input (active HIGH)
13	1E	enable input (active HIGH)
14	V _{DD}	supply voltage

2.4、Function Table

Input	Switch
nE	
H	ON
L	OFF

Note: H=HIGH voltage level; L=LOW voltage level.

3 Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V _{DD}	-	-0.5	+12	V
input voltage	V _I	-	-0.5	V _{DD} +0.5	V
input clamping current	I _{IK}	V _I <0.5V or V _I >V _{DD} +0.5V	-	±10	mA
input/output current	I _{I/O}	-	-	±10	mA
storage temperature	T _{stg}	-	-65	+150	°C
total power dissipation	P _{tot}	-	-	500	mW
device dissipation	P	per output transistor	-	100	mW
Soldering temperature	T _L	10s	DIP	245	°C
			SOP	250	°C

Note:

[1] For DIP14 packages: above 70°C the value of P_{tot} derates linearly with 12mW/K.

[2] For SOP14 packages: above 70°C the value of P_{tot} derates linearly with 8mW/K.

[3] For (T)SSOP14 packages: above 60°C the value of P_{tot} derates linearly with 5.5mW/K.

3.2、Recommended Operating Conditions

($T_{amb}=25^{\circ}\text{C}$; $R_L=10\text{k}\Omega$; $C_L=50\text{pF}$; $nE=V_{DD}$; $V_{IS}=V_{DD}=5\text{V}$.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{DD}	-	3	5	9	V
ambient temperature	T_{amb}	in free air	-40	-	+85	$^{\circ}\text{C}$
input voltage	V_I	-	0	-	V_{DD}	V
Disable output time (High level→turn off)	t_{PHZ}	nE to nZ or nE to nY	-	80	160	ns
Disable output time (Low level→turn off)	t_{PLZ}	nE to nZ or nE to nY	-	80	160	ns
Enable output time (turn off→high/low level)	t_{PZH} , t_{PZL}	-	-	45	90	ns
input capacitance	C_I	-	-	-	7.5	pF

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

($T_{amb}=25^{\circ}\text{C}$, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)		$T_{amb}=25^{\circ}\text{C}$			Unit
				Min.	Typ.	Max.	
supply current	I_{DD}	$V_I=V_{DD}$ or V_{SS} , $I_O=0\text{A}$	$V_{DD}=5\text{V}$	-	-	1.0	μA
			$V_{DD}=9\text{V}$	-	-	2.0	μA
HIGH-level input voltage	V_{IH}	$ I_O <1\mu\text{A}$	$V_{DD}=5\text{V}$, $V_O=0.5\text{V}$ or 4.5V	3.5	-	-	V
			$V_{DD}=9\text{V}$, $V_O=0.5\text{V}$ or 8V	7.0	-	-	V
LOW-level input voltage	V_{IL}	$ I_O <1\mu\text{A}$	$V_{DD}=5\text{V}$, $V_O=0.5\text{V}$ or 4.5V	-	-	1.5	V
			$V_{DD}=9\text{V}$, $V_O=0.5\text{V}$ or 8V	-	-	3.0	V
input leakage current	I_I	$V_I=0\text{V}$ or 9V , $V_{DD}=9\text{V}$		-	-	0.3	μA
ON resistance (rail)	R_{ON}	$V_I=0\text{V}$ to $V_{DD}-V_{EE}$	$V_{DD}-V_{EE}=5\text{V}$	-	350	2500	Ω
			$V_{DD}-V_{EE}=9\text{V}$	-	80	245	Ω
		$V_I=0\text{V}$	$V_{DD}-V_{EE}=5\text{V}$	-	115	340	Ω
			$V_{DD}-V_{EE}=9\text{V}$	-	50	160	Ω
		$V_I=V_{DD}-V_{EE}$	$V_{DD}-V_{EE}=5\text{V}$	-	120	365	Ω
			$V_{DD}-V_{EE}=9\text{V}$	-	65	200	Ω
ON resistance mismatch between channels	ΔR_{ON}	$V_I=0\text{V}$ to $V_{DD}-V_{EE}$	$V_{DD}-V_{EE}=5\text{V}$	-	25	-	Ω
			$V_{DD}-V_{EE}=9\text{V}$	-	10	-	Ω

Note: On resistance waveform and test circuit see Figure 9 and Figure 10.

3.3.2、DC Characteristics 2

($T_{amb}=-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)	$T_{amb}=-40^{\circ}\text{C}$		$T_{amb}+85^{\circ}\text{C}$		Unit	
			Min.	Max.	Min.	Max.		
supply current	I_{DD}	$V_I=V_{DD}$ or V_{SS} , $I_O=0\text{A}$	$V_{DD}=5\text{V}$	-	1.0	-	7.5	μA
			$V_{DD}=9\text{V}$	-	2.0	-	15.0	μA
HIGH-level input voltage	V_{IH}	$ I_O <1\mu\text{A}$	$V_{DD}=5\text{V}$, $V_O=0.5\text{V}$ or 4.5V	3.5	-	3.5	-	V
			$V_{DD}=9\text{V}$, $V_O=0.5\text{V}$ or 8V	7.0	-	7.0	-	V
LOW-level input voltage	V_{IL}	$ I_O <1\mu\text{A}$	$V_{DD}=5\text{V}$, $V_O=0.5\text{V}$ or 4.5V	-	1.5	-	1.5	V
			$V_{DD}=9\text{V}$, $V_O=0.5\text{V}$ or 8V	-	3.0	-	3.0	V
input leakage current	I_I	$V_I=0\text{V}$ or 9V , $V_{DD}=9\text{V}$	-	-	-	1.0	μA	

3.3.3、AC Characteristics 1

($T_{amb}=25^{\circ}\text{C}$, $V_{EE}=V_{SS}=0\text{V}$, $t_r, t_f \leq 20\text{ns}$, $C_L=50\text{pF}$, $R_L=10\text{k}\Omega$, unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
HIGH to LOW propagation delay time	t_{PHL}	nY to nZ; nZ to nY; see Figure 4	$V_{DD}=5\text{V}$	-	10	20	ns
			$V_{DD}=9\text{V}$	-	5	10	ns
LOW to HIGH propagation delay	t_{PLH}	nY to nZ; nZ to nY; see Figure 4	$V_{DD}=5\text{V}$	-	10	20	ns
			$V_{DD}=9\text{V}$	-	5	10	ns
HIGH to OFF-state propagation delay	t_{PHZ}	nE to nY, nZ; see Figure 5	$V_{DD}=5\text{V}$	-	80	160	ns
			$V_{DD}=9\text{V}$	-	65	130	ns
LOW to OFF-state propagation delay	t_{PLZ}	nE to nY, nZ; see Figure 5	$V_{DD}=5\text{V}$	-	80	160	ns
			$V_{DD}=9\text{V}$	-	70	140	ns
OFF-state to HIGH propagation delay	t_{PZH}	nE to nY, nZ; see Figure 5	$V_{DD}=5\text{V}$	-	40	80	ns
			$V_{DD}=9\text{V}$	-	20	40	ns
OFF-state to LOW propagation delay	t_{PZL}	nE to nY, nZ; see Figure 5	$V_{DD}=5\text{V}$	-	45	90	ns
			$V_{DD}=9\text{V}$	-	20	40	ns

3.3.4、AC Characteristics 2

($T_{amb}=25^{\circ}\text{C}$, $V_{EE}=V_{SS}=0\text{V}$, $V_I=0.5V_{DD}$ (p-p), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Square wave distortion	d_{sin}	see Figure 6; $R_L=10\text{k}\Omega$; $C_L=15\text{pF}$; channel ON; $f_i=1\text{kHz}$	$V_{DD}=5\text{V}$	0.25	-	-	%
			$V_{DD}=9\text{V}$	0.04	-	-	%
any two channel crosstalk	f_{ct}	$V_{DD}=9\text{V}$, see note2	1	-	-	MHz	
crosstalk voltage (nE to nY to nZ)	V_{ct}	see Figure 7; $R_L=10\text{k}\Omega$; $C_L=15\text{pF}$; \bar{E} or Sn= V_{DD} (square-wave)	50	-	-	mV	
OFF frequency	f_{OFF}	$V_{DD}=9\text{V}$, see note3	1	-	-	MHz	
conduction frequency	f_{ON}	$V_{DD}=5\text{V}$, see note4	-	-	-	MHz	
		$V_{DD}=9\text{V}$, see note4	90	-	-	MHz	

Note:

- [1] f_i is biased at $0.5V_{DD}$; $V_i=0.5V_{DD}$ (p-p).
- [2] $R_L=1k\Omega$; $20\log V_{os}/V_{is}=-50\text{dB}$, see Figure 8.
- [3] $R_L=1k\Omega$; $C_L=5\text{pF}$, channel off, $20\log V_{os}/V_{is}=-50\text{dB}$, see Figure 6.
- [4] $R_L=1k\Omega$; $C_L=5\text{pF}$, channel on, $20\log V_{os}/V_{is}=-3\text{dB}$, see Figure 6.

4、Testing Circuit

4.1、AC Testing Circuit 1

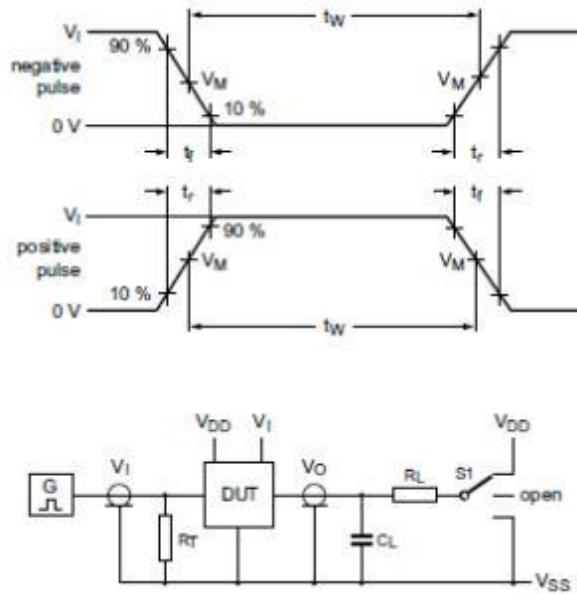


Figure 3. Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator. R_L =Load resistance.

4.2、AC Testing Waveforms

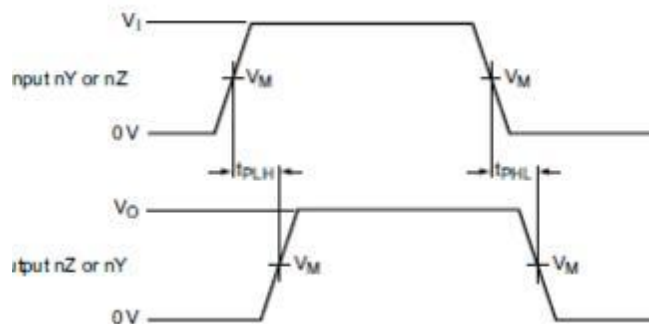


Figure 4. nY or nZ to nZ or nY propagation delays

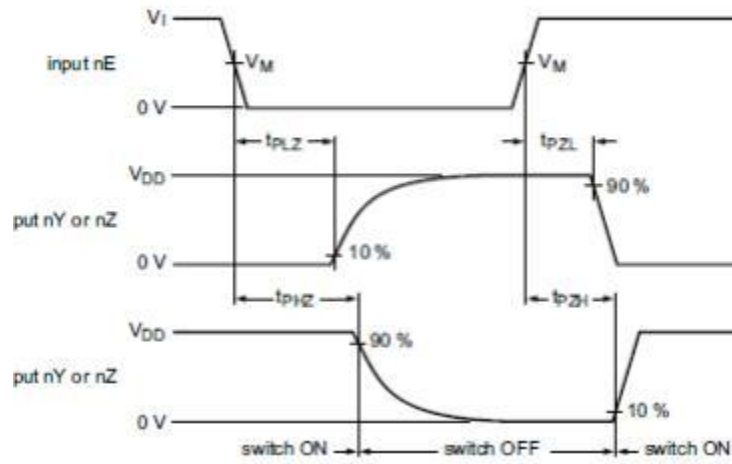


Figure 5. Enable and disable times

4.3、AC Testing Circuit 2

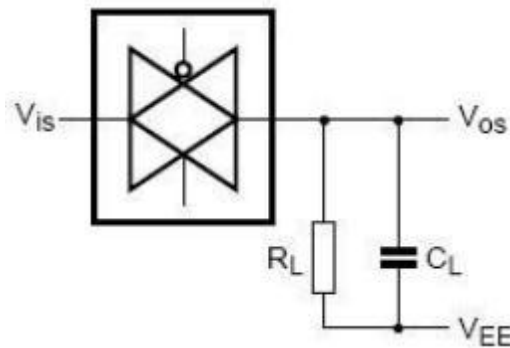


Figure 6. Square wave distortion degree of cut-off frequency and conduction frequency test pattern

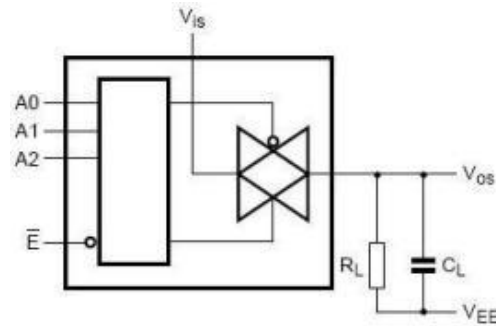


Figure 7. Crosstalk logical input/output test

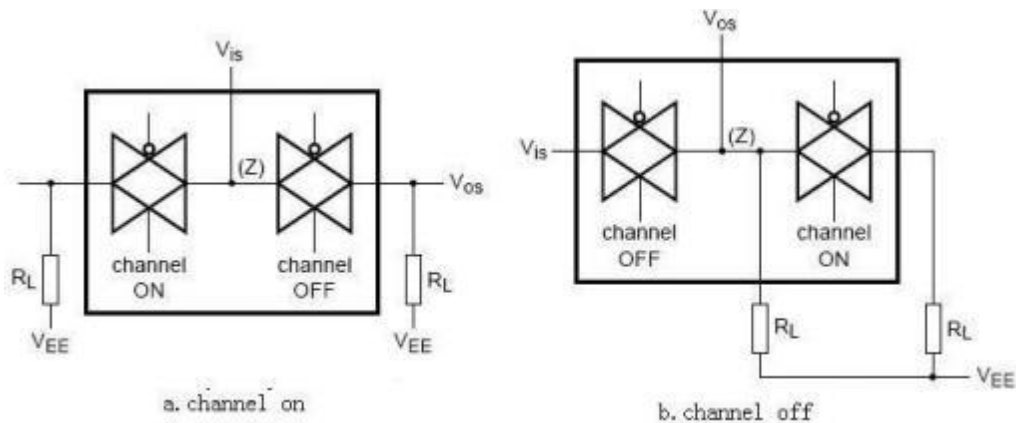
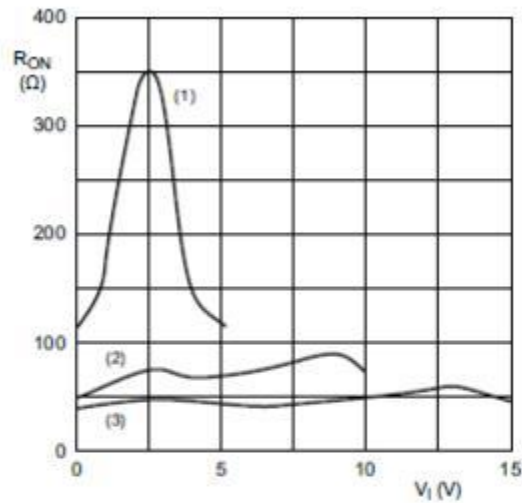


Figure 8. Inter channel Crosstalk



$I_{SW} = 200 \mu A.$
 (1) $V_{DD} = 5 V$
 (2) $V_{DD} = 10 V$
 (3) $V_{DD} = 15 V$

Figure 10. Typical R_{ON} as a function of input voltage

4.5、 Measurement Points

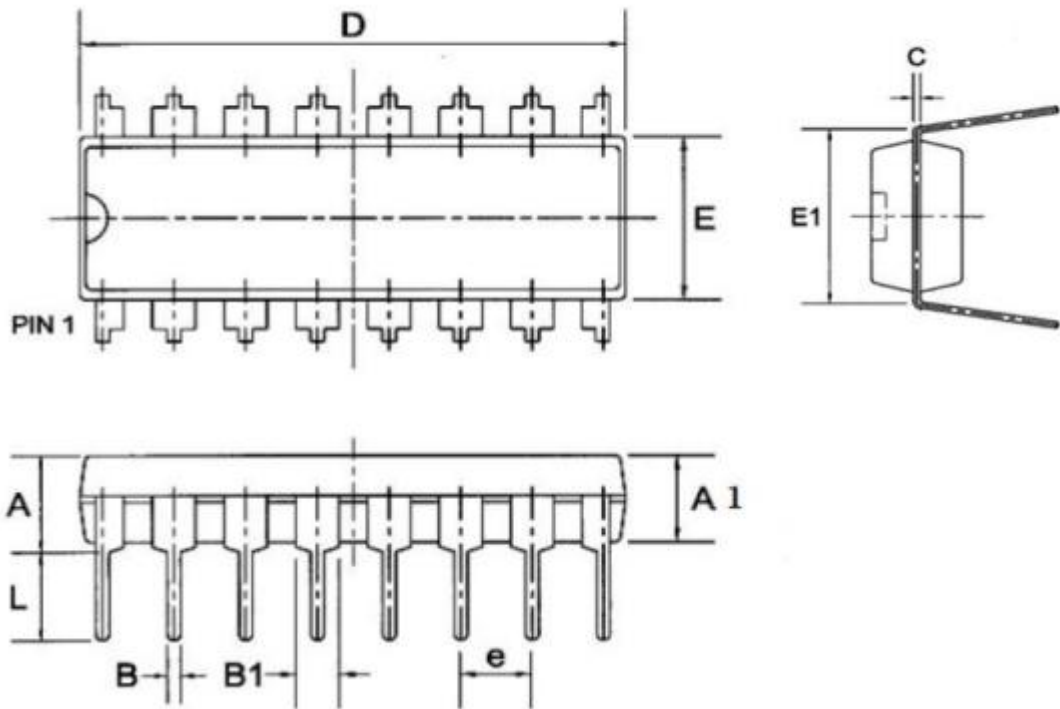
Supply voltage	Input	Output
V_{DD}	V_M	V_M
3V to 9V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$

4.6、 Test Data

Test	Input		Load		Switch
	V_{is}	t_r, t_f	C_L	R_L	
t_{PHL}	V_{EE}	20ns	50pF	10kΩ	V_{DD}
t_{PLH}	V_{DD}	20ns	50pF	10kΩ	V_{EE}
t_{PZH}, t_{PHZ}	V_{DD}	20ns	50pF	10kΩ	V_{EE}
t_{PZL}, t_{PLZ}	V_{EE}	20ns	50pF	10kΩ	V_{DD}
others	pulse	20ns	50pF	10kΩ	open

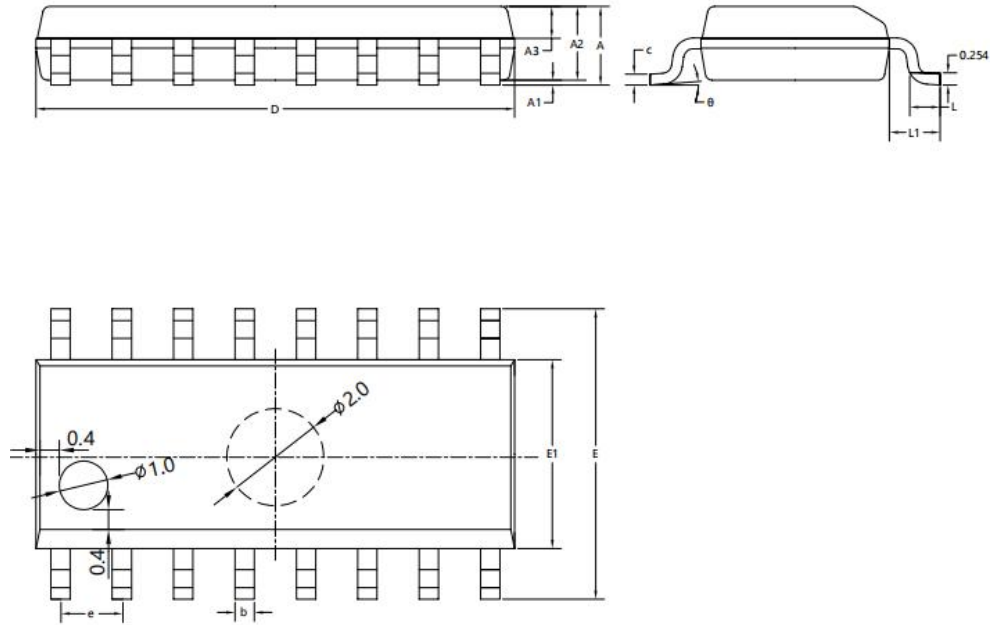
5、Package Information

5.1 DIP16



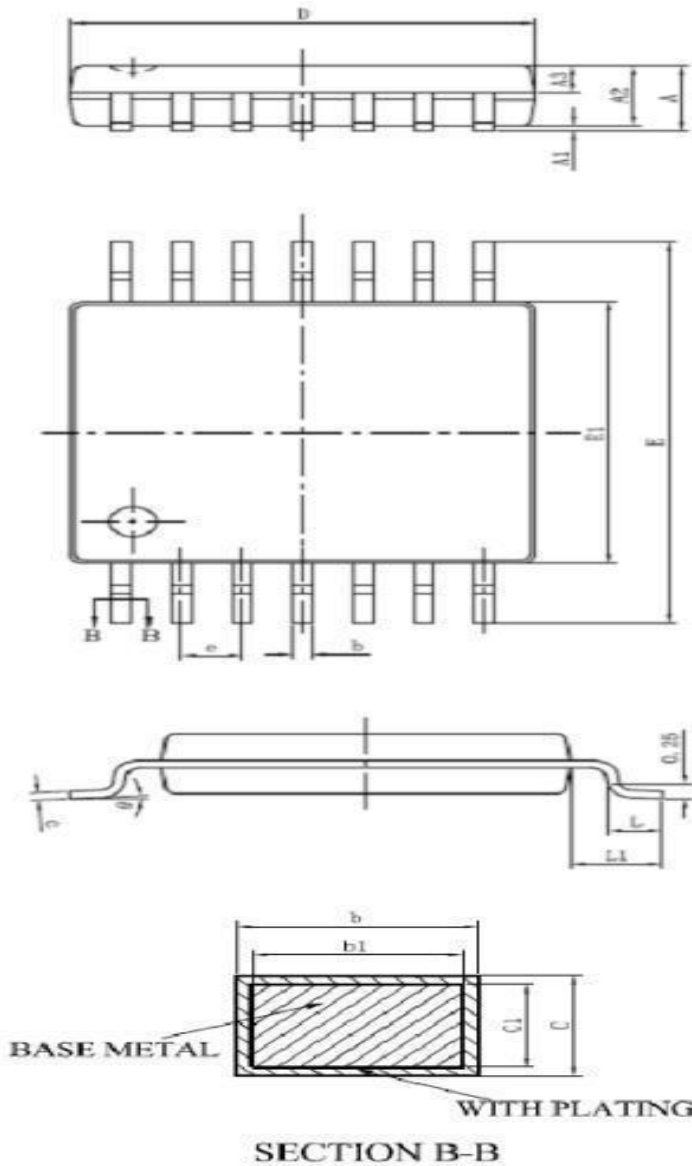
Symbol	Dimensions in Millimeters		
	Min	Nom	Max
A	--	--	4.31
A1	3.15	3.30	3.65
B	--	0.50	--
B1	--	1.6	--
C	--	0.27	--
D	19.00	19.20	19.60
E	6.20	6.50	6.60
E1	--	8.0	--
e	--	2.3	--
L	3.00	3.20	3.60

5.2 SOP16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.50	1.60	1.70
A1	0.10	0.15	0.25
A2	1.40	1.45	1.50
A3	0.60	0.65	0.70
b	0.30	0.40	0.50
c	0.15	0.20	0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.85	3.90	3.95
e	1.27BSC		
L	0.50	0.60	0.70
L1	1.05BSC		
θ	0°	4°	8°

5.3TSSOP-14



SYMBOL	MILLIMETER	
	MIN	MAX
A	—	1.20
A1	0.05	0.15
A2	0.90	1.05
A3	0.39	0.49
b	0.20	0.30
b1	0.19	0.25
c	0.13	0.19
c1	0.12	0.14
D	4.86	5.06
E1	4.30	4.50
E	6.20	6.60
e	0.65BSC	
L	0.45	0.75
L1	1.00BSC	
θ	0	8°

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