General Description

The SN74HC/HCT163 is a synchronous presettable binary counter with an internal look-head carry. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP). The outputs (Q0 to Q3) of the counters maybe preset to a HIGH or LOW. A LOW at the parallel enable input ($\overline{PE}$) disables the counting action. It causes the data at the data inputs (D0 to D3) to be loaded into the counter on the positive-going edge of the clock. Preset takes place regardless of the levels at count enable inputs (CEP and CET). A LOW at the master reset input ($\overline{MR}$) sets Q0 to Q3 LOW after the next positive-going transition on the clock input (CP). This action occurs regardless of the levels at input pins $\overline{PE}$, CET and CEP. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate. The look-ahead carry simplifies serial cascading of the counters. Both CEP and CET must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH output of Q0. This pulse can be used to enable the next cascaded stage. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

The CP to TC propagation delay and CEP to CP set-up time determine the maximum clock frequency for the cascaded counters according to the following formula:

$f_{max}=1/(t_{P(max)}(\text{CP to TC})+t_{SU}(\text{CEP to CP}))$

Features

- Input levels:
  For SN74HC163: CMOS level
  For SN74HCT163: TTL level
- Synchronous counting and loading
- 2 count enable inputs for n-bit cascading
- Synchronous reset
- Positive-edge triggered clock
- Specified from -40℃ to +125℃
- Packaging information: DIP16/SOP16/TSSOP16

Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW SN74HC163N	DIP-16	74HC163N	Tube	1000Pcs/Box
XBLW SN74HC163DTR	SOP-16	74HC163	Tape	2500Pcs/Reel
XBLW SN74HC163TDTR	TSSOP-16	74HC163	Tape	3000Pcs/Reel
XBLW SN74HCT163N	DIP-16	74HCT163N	Tube	1000Pcs/Box
XBLW SN74HCT163DTR	SOP-16	74HCT163	Tape	2500Pcs/Reel
XBLW SN74HCT163TDTR	TSSOP-16	74HCT163	Tape	3000Pcs/Reel

Block Diagram And Pin Description

Block Diagram

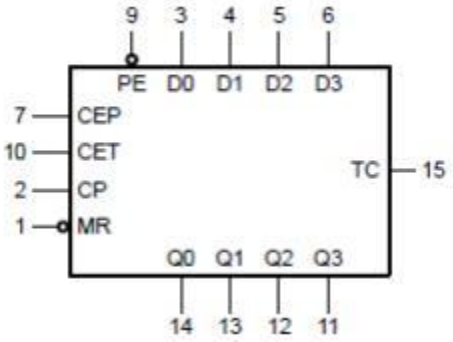


Figure 1. Logic symbol

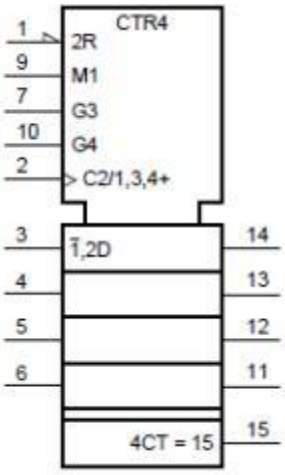


Figure 2. IEC logic symbol

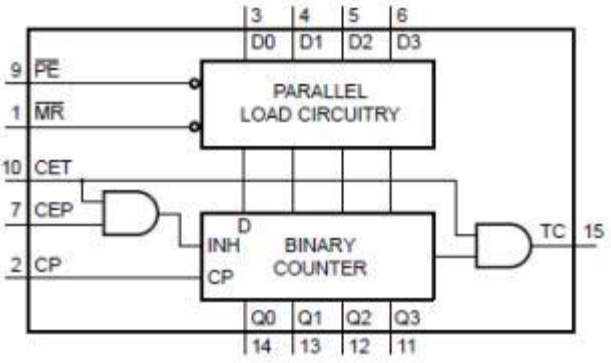


Figure 3.Functional diagram

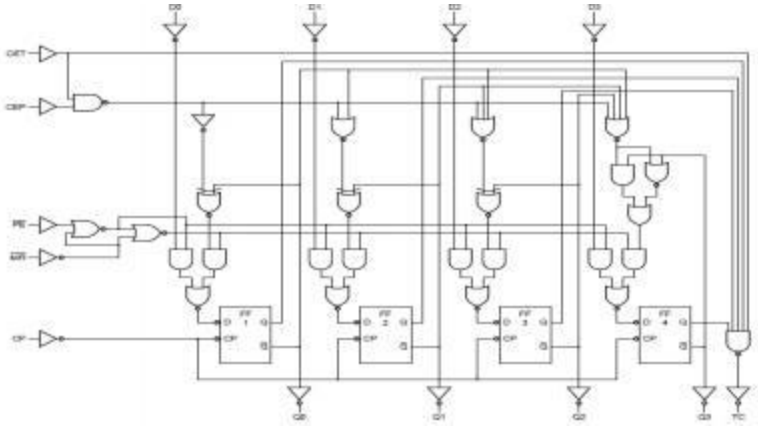


Figure 4. Logic diagram

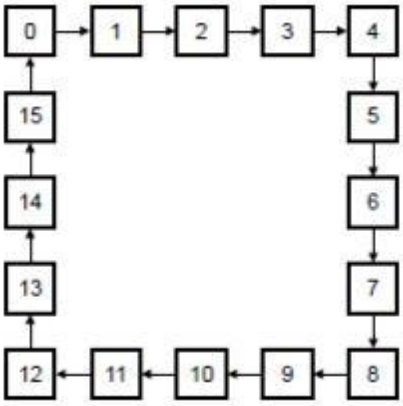


Figure 5. State diagram

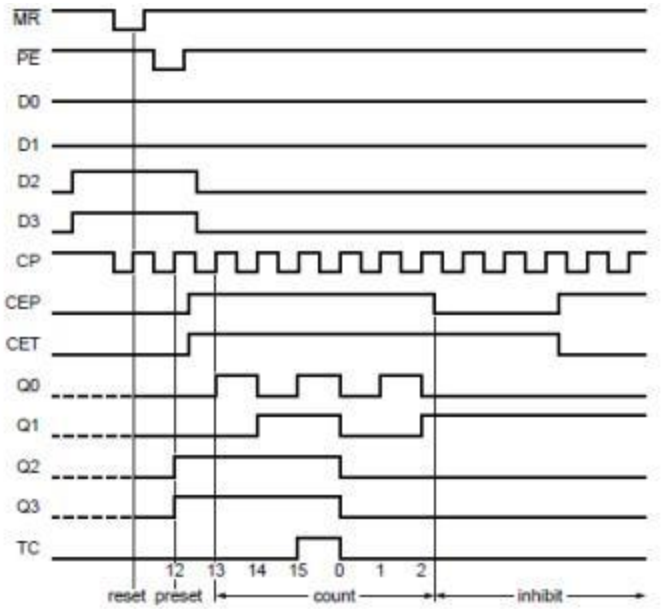
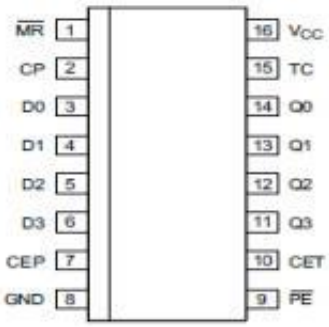


Figure 6. Typical timing sequence

Pin Configurations



Pin Description

Pin No.	Pin Name	Description
1	MR	asynchronous master reset (active LOW)
2	CP	clock input (LOW-to-HIGH, edge triggered)
3	D0	data input
4	D1	data input
5	D2	data input
6	D3	data input
7	CEP	count enable input
8	GND	ground (0V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CET	count enable carry input
11	Q3	flip-flop output
12	Q2	flip-flop output
13	Q1	flip-flop output
14	Q0	flip-flop output
15	TC	terminal count output
16	V_{CC}	supply voltage

Function Table

Operating mode	Input						Output	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	Dn	Qn	TC
reset (clear)	l	↑	X	X	X	X	L	L
parallel load	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	L
count	h	↑	h	h	h	X	count	[2]
hold (do nothing)	h	X	l	X	h	X	q_n	L

	h	X	X	l	h	X	q_n	L

Note:

[1] H=HIGH voltage level; L=LOW voltage level; X=don't care; ↑=LOW-to-HIGH clock transition;
l=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
h=HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;
q=lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition.

[2] The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH).

Electrical Parameter

Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{CC}	-		-0.5	+7.0	V
input clamping current	I_{IK}	V_I < -0.5V or V_I > V_{CC}+0.5V		-	±20	mA
output clamping current	I_{OK}	V_O < -0.5V or V_O > V_{CC}+0.5V		-	±20	mA
output current	I_O	-0.5V < V_O < V_{CC}+0.5V		-	±25	mA
supply current	I_{CC}	-		-	+50	mA
ground current	I_{GND}	-		-50	-	mA
storage temperature	T_{stg}	-		-65	+150	℃
total power dissipation	P_{tot}	-		-	500	mW
Soldering temperature	T_L	10s	DIP	245		℃
			SOP/TSSOP	260		

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SN74HC163						
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	Δt/ΔV	V_{CC}=2.0V	-	-	625	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	83	ns/V
ambient temperature	T_{amb}	-	-40	-	+125	℃
SN74HCT163						
supply voltage	V_{CC}	-	4.5	5.0	5.5	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	Δt/ΔV	V_{CC}=4.5V	-	1.67	139	ns/V
ambient temperature	T_{amb}	-	-40	-	+125	℃

DC Characteristics 1

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
SN74HC163							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	1.2	-	V
		V_{CC}=4.5V		3.15	2.4	-	V
		V_{CC}=6.0V		4.2	3.2	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	0.8	0.5	V
		V_{CC}=4.5V		-	2.1	1.35	V
		V_{CC}=6.0V		-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.98	4.32	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.48	5.81	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	0.15	0.26	V
			I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.26	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	8.0	uA
input capacitance	C_I	-		-	3.5	-	pF
SN74HCT163							
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V		2.0	1.6	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	1.2	0.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	4.5	-	V
			I_O=-4.0mA	3.98	4.32	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=20uA	-	0	0.1	V
			I_O=4.0mA	-	0.15	0.26	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	8.0	uA
additional supply current	ΔI_{CC}	per input pin; V_I=V_{CC}-2.1V; other inputs at V_{CC} or GND; I_O=0A; V_{CC}=4.5V to 5.5V	pin $\overline{MR}$	-	-	342	uA
			pin CP	-	-	396	uA
			pin CEP and Dn	-	-	90	uA
			pin CET	-	-	270	uA
			pin $\overline{PE}$	-	-	108	uA
input capacitance	C_I	-		-	3.5	-	pF

DC Characteristics 2

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
SN74HC163							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.84	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.34	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	-	0.33	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA
SN74HCT163							
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V		2.0	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	-	-	V
			I_O=-4.0mA	3.84	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=20uA	-	-	0.1	V
			I_O=4.0mA	-	-	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	80	uA
additional supply current	ΔI_{CC}	per input pin; V_I=V_{CC}-2.1V; other inputs at V_{CC} or GND; I_O=0A; V_{CC}=4.5V to 5.5V	pin $\overline{MR}$	-	-	427.5	uA
			pin CP	-	-	495	uA
			pin CEP and Dn	-	-	112.5	uA
			pin CET	-	-	337.5	uA
			pin $\overline{PE}$	-	-	135	uA

DC Characteristics 3

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
SN74HC163							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.7	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.2	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	-	0.4	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.4	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	160	uA
SN74HCT163							
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V		2.0	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	-	-	V
			I_O=-4.0mA	3.7	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=20uA	-	-	0.1	V
			I_O=4.0mA	-	-	0.4	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	160	uA
additional supply current	ΔI_{CC}	per input pin; V_I=V_{CC}-2.1V; other inputs at V_{CC} or GND; I_O=0A; V_{CC}=4.5V to 5.5V	pin $\overline{MR}$	-	-	465.5	uA
			pin CP	-	-	539	uA
			pin CEP and Dn	-	-	122.5	uA
			pin CET	-	-	367.5	uA
			pin $\overline{PE}$	-	-	147	uA

AC Characteristics 1

(T_{amb}=25℃, GND=0V, C_L=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
SN74HC163							
propagation delay	t_{pd}	CP to Qn; see Figure 8	V_{CC}=2.0V	-	55	185	ns
			V_{CC}=4.5V	-	20	37	ns
			V_{CC}=5.0V; C_L=15pF	-	17	-	ns
			V_{CC}=6.0V	-	16	31	ns
		CP to TC; see Figure 8	V_{CC}=2.0V	-	69	215	ns
			V_{CC}=4.5V	-	25	43	ns
			V_{CC}=5.0V; C_L=15pF	-	21	-	ns
			V_{CC}=6.0V	-	20	37	ns
		CET to TC; see Figure 9	V_{CC}=2.0V	-	36	120	ns
			V_{CC}=4.5V	-	13	24	ns
			V_{CC}=5.0V; C_L=15pF	-	11	-	ns
			V_{CC}=6.0V	-	10	20	ns
transition time	t_t	see Figure 8 and Figure 9	V_{CC}=2.0V	-	19	75	ns
			V_{CC}=4.5V	-	7	15	ns
			V_{CC}=6.0V	-	6	13	ns
pulse width	t_W	CP HIGH or LOW; see Figure 8	V_{CC}=2.0V	80	17	-	ns
			V_{CC}=4.5V	16	6	-	ns
			V_{CC}=6.0V	14	5	-	ns
set-up time	t_{su}	$\overline{MR}$, Dn to CP; see Figure 10, 11	V_{CC}=2.0V	80	22	-	ns
			V_{CC}=4.5V	16	8	-	ns
			V_{CC}=6.0V	14	6	-	ns
		$\overline{PE}$ to CP; see Figure 10	V_{CC}=2.0V	80	17	-	ns
			V_{CC}=4.5V	16	6	-	ns
			V_{CC}=6.0V	14	5	-	ns
		CEP, CET to CP; see Figure 12	V_{CC}=2.0V	175	58	-	ns
			V_{CC}=4.5V	35	21	-	ns
			V_{CC}=6.0V	30	17	-	ns
hold time	t_h	Dn, $\overline{PE}$, CEP, CET, $\overline{MR}$ to CP; see Figure 10, 11, 12	V_{CC}=2.0V	0	-14	-	ns
			V_{CC}=4.5V	0	-5	-	ns
			V_{CC}=6.0V	0	-4	-	ns
maximum frequency	f_{max}	CP; see Figure 8	V_{CC}=2.0V	5	15	-	MHz
			V_{CC}=4.5V	27	46	-	MHz
			V_{CC}=5.0V; C_L=15pF	-	51	-	MHz
			V_{CC}=6.0V	32	55	-	MHz
power dissipation capacitance	C_{PD}	f_i=1MHz; V_{CC}=5.0V; V_I=GND to V_{CC}		-	33	-	pF
SN74HCT163							
propagation delay	t_{pd}	CP to Qn; see Figure 8	V_{CC}=4.5V	-	23	39	ns
			V_{CC}=5.0V; C_L=15pF	-	20	-	ns
		CP to TC; see Figure 8	V_{CC}=4.5V	-	29	49	ns
			V_{CC}=5.0V; C_L=15pF	-	25	-	ns
		CET to TC; see Figure 9	V_{CC}=4.5V	-	17	32	ns
			V_{CC}=5.0V; C_L=15pF	-	14	-	ns
transition time	t_t	V_{CC}=4.5V; see Figure 8, 9		-	7	15	ns
pulse width	t_W	CP HIGH or LOW; V_{CC}=4.5V; see Figure 8		20	6	-	ns

set-up time	t_{su}	$\overline{MR}$, Dn to CP; V_{CC}=4.5V; see Figure 10, 11		20	9	-	ns
		$\overline{PE}$ to CP; V_{CC}=4.5V; see Figure 10		20	11	-	ns
		CEP, CET to CP; V_{CC}=4.5V;see Figure 12		40	24	-	ns
hold time	t_h	Dn, $\overline{PE}$, CEP, CET, $\overline{MR}$ to CP; V_{CC}=4.5V; see Figure 10, 11, 12		0	-5	-	ns
maximum frequency	f_{max}	CP; see Figure 8	V_{CC}=4.5V	26	45	-	MHz
			V_{CC}=5.0V; C_L=15pF	-	50	-	MHz
power dissipation capacitance	C_{PD}	f_i=1MHz; V_{CC}=5.0V; V_I=GND to V_{CC}-1.5V		-	35	-	pF

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the sameast$_{THL}$ and t_{TLH}.

[3] C_{PD} isused to determine the dynamic power dissipation (P_D in uW).

$P_D=C_{PD}\times V_{CC}^2\times f_i\times N+\Sigma(C_L\times V_{CC}^2\times f_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

$\Sigma(C_L\times V_{CC}^2\times f_o)$=sum of outputs.

AC Characteristics 2

(T_{amb}=-40℃ to +85℃, GND=0V, C_L=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
SN74HC163							
propagation delay	t_{pd}	CP to Qn; see Figure 8	V_{CC}=2.0V	-	-	230	ns
			V_{CC}=4.5V	-	-	46	ns
			V_{CC}=6.0V	-	-	39	ns
		CP to TC; see Figure 8	V_{CC}=2.0V	-	-	270	ns
			V_{CC}=4.5V	-	-	54	ns
			V_{CC}=6.0V	-	-	46	ns
		CET to TC; see Figure 9	V_{CC}=2.0V	-	-	150	ns
			V_{CC}=4.5V	-	-	30	ns
			V_{CC}=6.0V	-	-	26	ns
transition time	t_t	see Figure 8 and Figure 9	V_{CC}=2.0V	-	-	95	ns
			V_{CC}=4.5V	-	-	19	ns
			V_{CC}=6.0V	-	-	16	ns
pulse width	t_W	CP HIGH or LOW; see Figure 8	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
set-up time	t_{su}	$\overline{MR}$, Dn to CP; see Figure 10, 11	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
		$\overline{PE}$ to CP;	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns

		see Figure 10	V_{CC}=6.0V	17	-	-	ns
		CEP, CET to CP; see Figure 12	V_{CC}=2.0V	220	-	-	ns
			V_{CC}=4.5V	44	-	-	ns
			V_{CC}=6.0V	37	-	-	ns
hold time	t_h	Dn, $\overline{PE}$, CEP, CET $\overline{MR}$ to CP; see Figure 10, 11, 12	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
maximum frequency	f_{max}	CP; see Figure 8	V_{CC}=2.0V	4	-	-	MHz
			V_{CC}=4.5V	22	-	-	MHz
			V_{CC}=6.0V	26	-	-	MHz
SN74HCT163							
propagation delay	t_{pd}	CP to Qn; see Figure 8	V_{CC}=4.5V	-	-	49	ns
		CP to TC; see Figure 8	V_{CC}=4.5V	-	-	61	ns
		CET to TC; see Figure 9	V_{CC}=4.5V	-	-	44	ns
transition time	t_t	V_{CC}=4.5V; see Figure 8, 9		-	-	19	ns
pulse width	t_W	CP HIGH or LOW; V_{CC}=4.5V; see Figure 8		25	-	-	ns
set-up time	t_{su}	$\overline{MR}$, Dn to CP; V_{CC}=4.5V; see Figure 10, 11		25	-	-	ns
		$\overline{PE}$ to CP; V_{CC}=4.5V; see Figure 10		25	-	-	ns
		CEP, CET to CP; V_{CC}=4.5V;see Figure 12		50	-	-	ns
hold time	t_h	Dn, $\overline{PE}$, CEP, CET, $\overline{MR}$to CP; V_{CC}=4.5V; see Figure 10, 11, 12		0	-	-	ns
maximum frequency	f_{max}	CP; see Figure 8	V_{CC}=4.5V	21	-	-	MHz

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the sameast$_{THL}$ and t_{TLH}.

AC Characteristics 3

(T_{amb}=-40℃ to +125℃, GND=0V, C_L=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
SN74HC163							
propagation delay	t_{pd}	CP to Qn; see Figure 8	V_{CC}=2.0V	-	-	280	ns
			V_{CC}=4.5V	-	-	56	ns
			V_{CC}=6.0V	-	-	48	ns
		CP to TC; see Figure 8	V_{CC}=2.0V	-	-	320	ns
			V_{CC}=4.5V	-	-	65	ns
			V_{CC}=6.0V	-	-	55	ns
		CET to TC; see Figure 9	V_{CC}=2.0V	-	-	180	ns
			V_{CC}=4.5V	-	-	36	ns
			V_{CC}=6.0V	-	-	31	ns
transition time	t_t	see Figure 8	V_{CC}=2.0V	-	-	110	ns
			V_{CC}=4.5V	-	-	22	ns

		and Figure 9	V_{CC}=6.0V	-	-	19	ns
pulse width	t_W	CP HIGH or LOW; see Figure 8	V_{CC}=2.0V	120	-	-	ns
			V_{CC}=4.5V	24	-	-	ns
			V_{CC}=6.0V	20	-	-	ns
set-up time	t_{su}	$\overline{MR}$, Dn to CP; see Figure 10, 11	V_{CC}=2.0V	120	-	-	ns
			V_{CC}=4.5V	24	-	-	ns
			V_{CC}=6.0V	20	-	-	ns
		$\overline{PE}$ to CP; see Figure 10	V_{CC}=2.0V	120	-	-	ns
			V_{CC}=4.5V	24	-	-	ns
			V_{CC}=6.0V	20	-	-	ns
		CEP, CET to CP; see Figure 12	V_{CC}=2.0V	265	-	-	ns
			V_{CC}=4.5V	53	-	-	ns
			V_{CC}=6.0V	45	-	-	ns
hold time	t_h	Dn, $\overline{PE}$, CEP, CET $\overline{MR}$ to CP; see Figure 10, 11, 12	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
maximum frequency	f_{max}	CP; see Figure 8	V_{CC}=2.0V	4	-	-	MHz
			V_{CC}=4.5V	18	-	-	MHz
			V_{CC}=6.0V	21	-	-	MHz
SN74HCT163							
propagation	t_{pd}	CP to Qn;	V_{CC}=4.5V	-	-	59	ns
delay		see Figure 8					
		CP to TC; see Figure 8	V_{CC}=4.5V	-	-	74	ns
		CET to TC; see Figure 9	V_{CC}=4.5V	-	-	48	ns
transition time	t_t	V_{CC}=4.5V; see Figure 8, 9		-	-	22	ns
pulse width	t_W	CP HIGH or LOW; V_{CC}=4.5V; see Figure 8		30	-	-	ns
set-up time	t_{su}	$\overline{MR}$, Dn to CP; V_{CC}=4.5V; see Figure 10, 11		30	-	-	ns
		$\overline{PE}$ to CP; V_{CC}=4.5V; see Figure 10		30	-	-	ns
		CEP, CET to CP; V_{CC}=4.5V;see Figure 12		60	-	-	ns
hold time	t_h	Dn, $\overline{PE}$, CEP, CET, $\overline{MR}$to CP; V_{CC}=4.5V; see Figure 10, 11, 12		0	-	-	ns
maximum frequency	f_{max}	CP; see Figure 8	V_{CC}=4.5V	17	-	-	MHz

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the sameast$_{THL}$ and t_{TLH}.

Testing Circuit

AC Testing Circuit

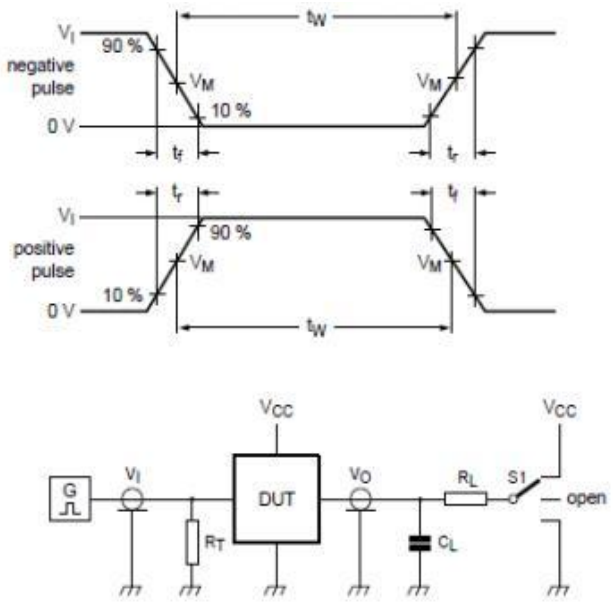


Figure 7. Test circuit for measuring switching times

Definitions for test circuit:
C_L=Load capacitance including jig and probe capacitance.
R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.
R_L=Load resistance.
S1=Test selection switch

AC Testing Waveforms

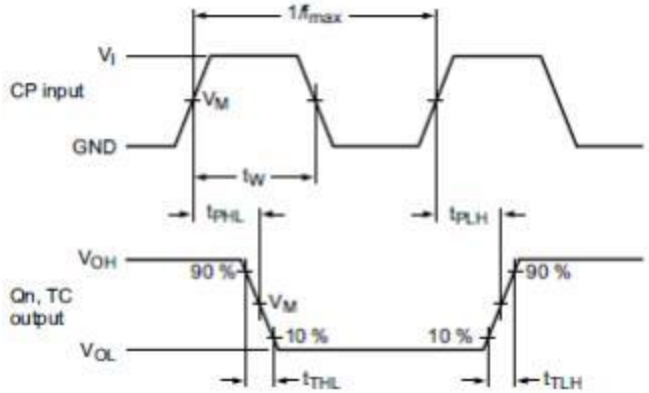


Figure 8. The clock (CP) to outputs (Qn, TC) propagation delays, pulse width, output transition times and maximum frequency

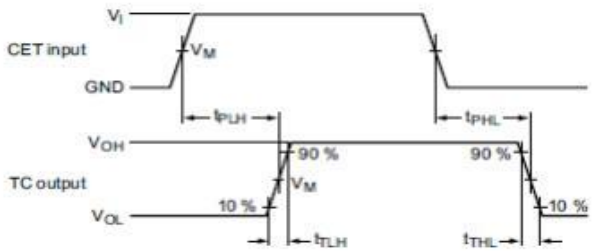


Figure 9. The count enable carry input (CET) to terminal count output (TC) propagation delays and output transition times

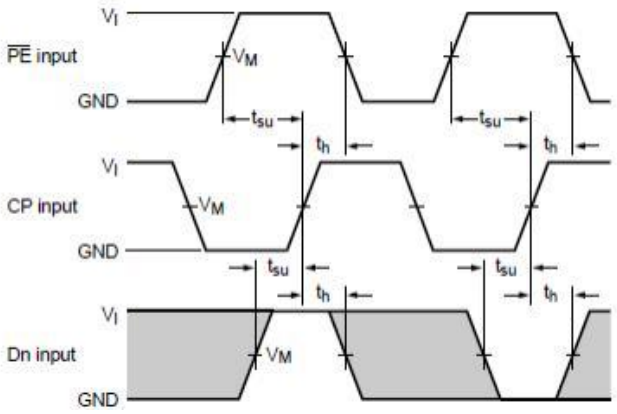


Figure 10. The data input (Dn) and parallel enable input ($\overline{PE}$) set-up and hold times

Measurement Points

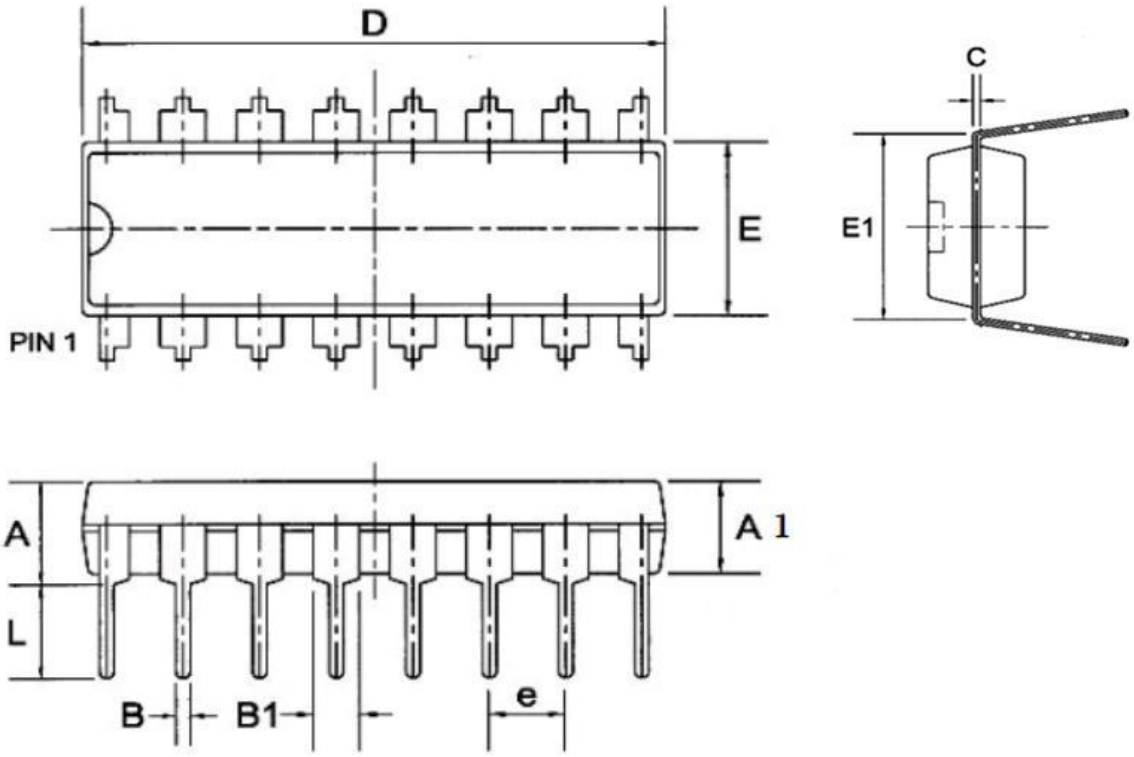
Type	Input		Output
	V_I	V_M	V_M
SN74HC163	GND to V_{CC}	0.5×V_{CC}	0.5×V_{CC}
SN74HCT163	GND to 3V	1.3V	1.3V

Test Data

Type	Input		Load		S1 position
	V_I	t_r ,t_f	C_L	R_L	t_{PHL}, t_{PLH}
SN74HC163	V_{CC}	6ns	15pF, 50pF	1kΩ	open
SN74HCT163	3V	6ns	15pF, 50pF	1kΩ	open

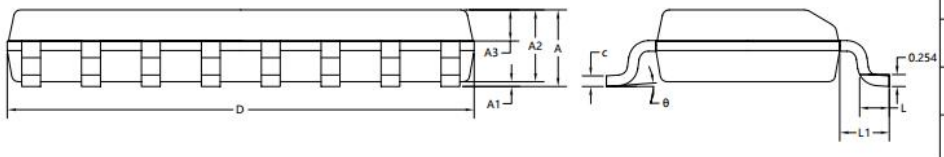
Package Information

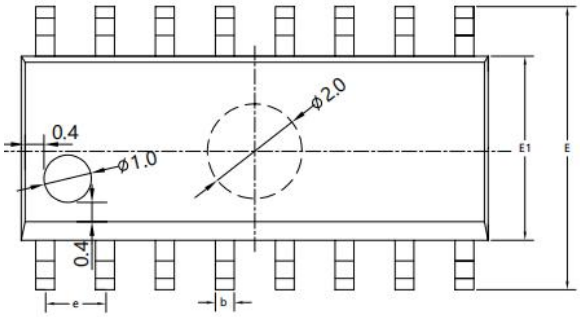
DIP16



Symbol	Dimensions in Millimeters		
	Min	Nom	Max
A	--	--	4.31
A1	3.15	3.30	3.65
B	--	0.50	--
B1	--	1.6	--
C	--	0.27	--
D	19.00	19.20	19.60
E	6.20	6.50	6.60
E1	--	8.0	--
e	--	2.3	--
L	3.00	3.20	3.60

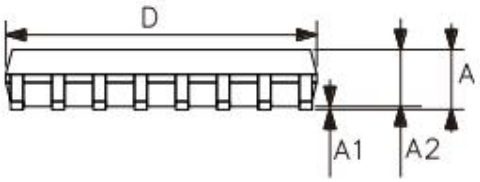
SOP16

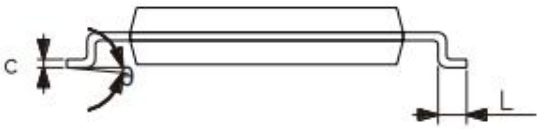


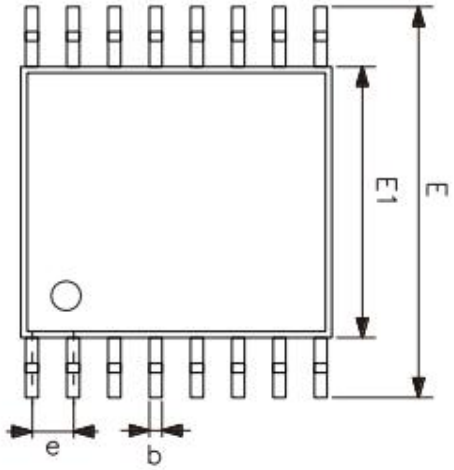


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.50	1.60	1.70
A1	0.10	0.15	0.25
A2	1.40	1.45	1.50
A3	0.60	0.65	0.70
b	0.30	0.40	0.50
c	0.15	0.20	0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.85	3.90	3.95
e	1.27BSC		
L	0.50	0.60	0.70
L1	1.05BSC		
θ	0°	4°	8°

TSSOP16







Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
θ	0°	8°

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