

## General Description

The SN74HC/HCT165 is 8-bit serial or parallel-in/serial-out shift registers. The device features a serial data input (DS), eight parallel data inputs (D0 to D7) and two complementary serial outputs (Q7 and  $\bar{Q}7$ ). When the parallel load input ( $\bar{P}L$ ) is LOW the data from D0 to D7 is loaded into the shift register asynchronously. When  $\bar{P}L$  is HIGH data enters the register serially at DS. When the clock enable input ( $\bar{C}E$ ) is LOW data is shifted on the LOW-to-HIGH transitions of the CP input. A HIGH on  $\bar{C}E$  will disable the CP input. Inputs are overvoltage tolerant to 15V. This enables the device to be used in HIGH-to-LOW level shifting applications.

## Features

- Input levels:  
For SN74HC165: CMOS level  
For SN74HCT165: TTL level
- Asynchronous 8-bit parallel load
- Synchronous serial input
- Specified from -40°C to +85°C
- Packaging information: DIP16/SOP16/TSSOP16

## Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing QTY
SN74HC165N	DIP-16	74HC165N	Tube	1000/Box
SN74HC165DTR	SOP-16	74HC165	Tape	2500/Reel
SN74HCT165DTR	SOP-16	74HCT165	Tape	2500/Reel
SN74HCT165TDTR	TSSOP-16	74HCT165	Tape	3000/Reel

## 2、Block Diagram And Pin Description

### 2.1、Block Diagram

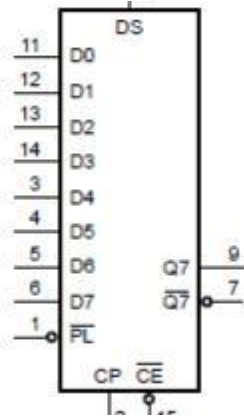


Figure 1. Logic symbol

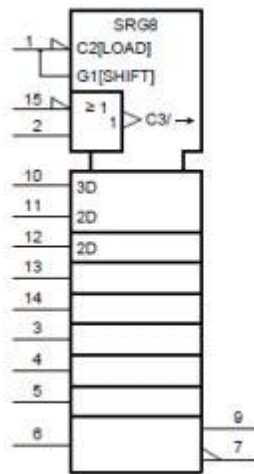


Figure 2. Functional diagram

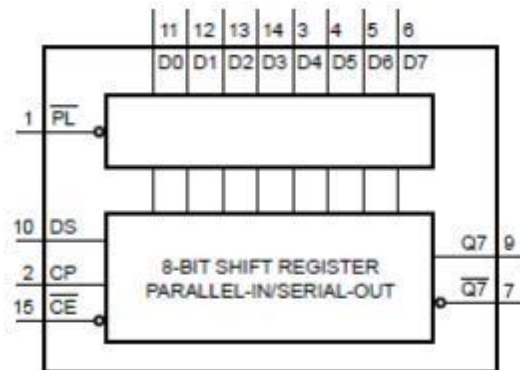


Figure 3. Functional diagram

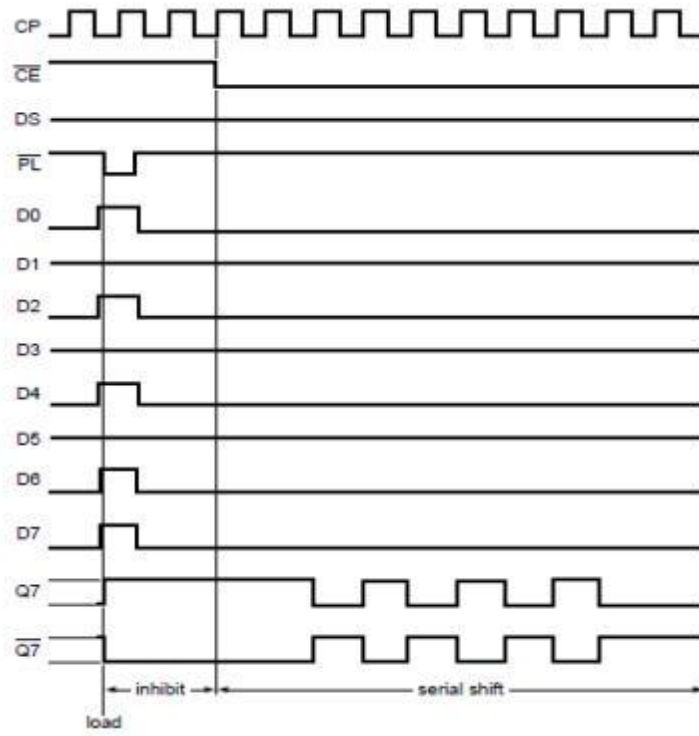
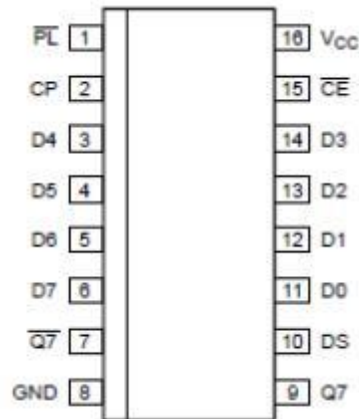


Figure 4. Timing diagram

## 2.2、Pin Configurations



### 2.3、Pin Description

Pin No.	Pin Name	Description
1	$\bar{P}L$	asynchronous parallel load input (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3	D4	parallel data input (also referred to as Dn)
4	D5	parallel data input (also referred to as Dn)
5	D6	parallel data input (also referred to as Dn)
6	D7	parallel data input (also referred to as Dn)
7	$\bar{Q}7$	complementary output from the last stage
8	GND	ground (0V)
9	Q7	serial output from the last stage
10	DS	serial data input
11	D0	parallel data input (also referred to as Dn)
12	D1	parallel data input (also referred to as Dn)
13	D2	parallel data input (also referred to as Dn)
14	D3	parallel data input (also referred to as Dn)
15	$\bar{C}E$	clock enable input (active LOW)
16	V <sub>CC</sub>	supply voltage

### 2.4、Function Table

Operating mode	Input					Qn register		Output	
	$\bar{P}L$	$\bar{C}E$	CP	DS	D0 to D7	Q0	Q1 to Q6	Q7	$\bar{Q}7$
parallel load	L	X	X	X	L	L	L to L	L	H
	L	X	X	X	H	H	H to H	H	L
serial shift	H	L	t	l	X	L	q0 to q5	q6	$\bar{q}6$
	H	L	t	h	X	H	q0 to q5	q6	$\bar{q}6$
	H	t	L	l	X	L	q0 to q5	q6	$\bar{q}6$
	H	t	L	h	X	H	q0 to q5	q6	$\bar{q}6$
hold "do nothing"	H	H	X	X	X	q0	q1 to q6	q7	$\bar{q}7$
	H	X	H	X	X	q0	q1 to q6	q7	$\bar{q}7$

Note: H=HIGH voltage level;

h=HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;

L=LOW voltage level; t=LOW-to-HIGH clock transition;

l=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;

q=state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition;

X=don't care;

t=LOW-to-HIGH clock transition.

### 3、Electrical Parameter

#### 3.1、Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	$V_{CC}$	-	-0.5	+7	V
input clamping current	$I_{IK}$	$V_I < -0.5V$ or $V_I > V_{CC}+0.5V$	-	$\pm 20$	mA
output clamping current	$I_{OK}$	$V_O < -0.5V$ or $V_O > V_{CC}+0.5V$	-	$\pm 20$	mA
output current	$I_O$	$-0.5V < V_O < V_{CC}+0.5V$	-	$\pm 25$	mA
supply current	$I_{CC}$	-	-	50	mA
ground current	$I_{GND}$	-	-50	-	mA
total power dissipation	$P_{tot}$	-	-	500	mW
storage temperature	$T_{stg}$	-	-65	+150	$^{\circ}C$
soldering temperature	$T_L$	10s	DIP	245	$^{\circ}C$
			SOP	250	$^{\circ}C$

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Note:

[1] For DIP16 packages: above  $70^{\circ}C$  the value of  $P_{tot}$  derates linearly with 12mW/K.

[2] For SOP16 packages: above  $70^{\circ}C$  the value of  $P_{tot}$  derates linearly with 8mW/K.

[3] For (T)SSOP16 packages: above  $60^{\circ}C$  the value of  $P_{tot}$  derates linearly with 5.5mW/K.

#### 3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SN74HC165						
supply voltage	$V_{CC}$	-	2.0	5.0	6.0	V
input voltage	$V_I$	-	0	-	$V_{CC}$	V
output voltage	$V_O$	-	0	-	$V_{CC}$	V
input transition rise and fall rate	$\Delta t/\Delta V$	$V_{CC}=2.0V$	-	-	625	ns/V
		$V_{CC}=4.5V$	-	1.67	139	ns/V
		$V_{CC}=6.0V$	-	-	83	ns/V
ambient temperature	$T_{amb}$	-	-40	-	+85	$^{\circ}C$
SN74HCT165						
supply voltage	$V_{CC}$	-	4.5	5.0	5.5	V
input voltage	$V_I$	-	0	-	$V_{CC}$	V
output voltage	$V_O$	-	0	-	$V_{CC}$	V
input transition rise and fall rate	$\Delta t/\Delta V$	$V_{CC}=2.0V$	-	-	-	ns/V
		$V_{CC}=4.5V$	-	1.67	139	ns/V
		$V_{CC}=6.0V$	-	-	-	ns/V
ambient temperature	$T_{amb}$	-	-40	-	+85	$^{\circ}C$

### 3.3、Electrical Characteristics

#### 3.3.1、DC Characteristics 1

( $T_{amb}=25^{\circ}C$ , voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
SN74HC165							
HIGH-level input voltage	$V_{IH}$	$V_{CC}=2.0V$	1.5	1.2	-	V	
		$V_{CC}=4.5V$	3.15	2.4	-	V	
		$V_{CC}=6.0V$	4.2	3.2	-	V	
LOW-level input voltage	$V_{IL}$	$V_{CC}=2.0V$	-	0.8	0.5	V	
		$V_{CC}=4.5V$	-	2.1	1.35	V	
		$V_{CC}=6.0V$	-	2.8	1.8	V	
HIGH-level output voltage	$V_{OH}$	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O=-20\mu A; V_{CC}=2.0V$	1.9	2.0	-	V
			$I_O=-20\mu A; V_{CC}=4.5V$	4.4	4.5	-	V
			$I_O=-20\mu A; V_{CC}=6.0V$	5.9	6.0	-	V
			$I_O=-4.0mA; V_{CC}=4.5V$	3.98	4.32	-	V
			$I_O=-5.2mA; V_{CC}=6.0V$	5.48	5.81	-	V
LOW-level output voltage	$V_{OL}$	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O=20\mu A; V_{CC}=2.0V$	-	0	0.1	V
			$I_O=20\mu A; V_{CC}=4.5V$	-	0	0.1	V
			$I_O=20\mu A; V_{CC}=6.0V$	-	0	0.1	V
			$I_O=4.0mA; V_{CC}=4.5V$	-	0.15	0.26	V
			$I_O=5.2mA; V_{CC}=6.0V$	-	0.16	0.26	V
input leakage current	$I_I$	$V_I = V_{CC} \text{ or } GND;$ $V_{CC}=6.0V$	-	-	$\pm 0.1$	$\mu A$	
supply current	$I_{CC}$	$V_I = V_{CC} \text{ or } GND; I_O=0A;$ $V_{CC}=6.0V$	-	-	8	$\mu A$	
input capacitance	$C_I$	-	-	3.5	-	pF	
SN74HCT165							
HIGH- level input voltage	$V_{IH}$	$V_{CC}=4.5V \text{ to } 5.5V$	2.0	1.6	-	V	
LOW- level input voltage	$V_{IL}$	$V_{CC}=4.5V \text{ to } 5.5V$	-	1.2	0.8	V	
HIGH-level output voltage	$V_{OH}$	$V_I = V_{IH} \text{ or } V_{IL};$ $V_{CC}=4.5V$	$I_O=-20\mu A$	4.4	4.5	-	V
			$I_O=-4.0mA$	3.98	4.32	-	V
LOW-level output voltage	$V_{OL}$	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O=20\mu A; V_{CC}=4.5V$	-	0	0.1	V
			$I_O=5.2mA; V_{CC}=6.0V$	-	0.16	0.26	V
input leakage current	$I_I$	$V_I = V_{CC} \text{ or } GND;$ $V_{CC}=6.0V$	-	-	$\pm 0.1$	$\mu A$	
supply current	$I_{CC}$	$V_I = V_{CC} \text{ or } GND; I_O=0A;$ $V_{CC}=6.0V$	-	-	8.0	$\mu A$	
additional supply current	$\Delta I_{CC}$	per input pin; $V_I = V_{CC} - 2.1V;$ other inputs at $V_{CC}$ or GND; $V_{CC}=4.5V \text{ to } 5.5V$	Dn and DS inputs	-	35	126	$\mu A$
			CP, $\bar{CE}$ , and $\bar{PL}$ inputs	-	65	234	$\mu A$
input capacitance	$C_I$	-	-	3.5	-	pF	

**3.3.2、DC Characteristics 2**

( $T_{amb} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
SN74HC165							
HIGH-level input voltage	$V_{IH}$	$V_{CC}=2.0\text{V}$	1.5	-	-	V	
		$V_{CC}=4.5\text{V}$	3.15	-	-	V	
		$V_{CC}=6.0\text{V}$	4.2	-	-	V	
LOW-level input voltage	$V_{IL}$	$V_{CC}=2.0\text{V}$	-	-	0.5	V	
		$V_{CC}=4.5\text{V}$	-	-	1.35	V	
		$V_{CC}=6.0\text{V}$	-	-	1.8	V	
HIGH-level output voltage	$V_{OH}$	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O = -20\mu\text{A}; V_{CC} = 2.0\text{V}$	1.9	-	-	V
			$I_O = -20\mu\text{A}; V_{CC} = 4.5\text{V}$	4.4	-	-	V
			$I_O = -20\mu\text{A}; V_{CC} = 6.0\text{V}$	5.9	-	-	V
			$I_O = -4.0\text{mA}; V_{CC} = 4.5\text{V}$	3.84	-	-	V
			$I_O = -5.2\text{mA}; V_{CC} = 6.0\text{V}$	5.34	-	-	V
LOW-level output voltage	$V_{OL}$	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O = 20\mu\text{A}; V_{CC} = 2.0\text{V}$	-	-	0.1	V
			$I_O = 20\mu\text{A}; V_{CC} = 4.5\text{V}$	-	-	0.1	V
			$I_O = 20\mu\text{A}; V_{CC} = 6.0\text{V}$	-	-	0.1	V
			$I_O = 4.0\text{mA}; V_{CC} = 4.5\text{V}$	-	-	0.33	V
			$I_O = 5.2\text{mA}; V_{CC} = 6.0\text{V}$	-	-	0.33	V
input leakage current	$I_I$	$V_I = V_{CC} \text{ or } \text{GND};$ $V_{CC} = 6.0\text{V}$	-	-	$\pm 1$	$\mu\text{A}$	
supply current	$I_{CC}$	$V_I = V_{CC} \text{ or } \text{GND}; I_O = 0\text{A};$ $V_{CC} = 6.0\text{V}$	-	-	80	$\mu\text{A}$	
SN74HCT165							
HIGH- level input voltage	$V_{IH}$	$V_{CC} = 4.5\text{V} \text{ to } 5.5\text{V}$	2.0	-	-	V	
LOW- level input voltage	$V_{IL}$	$V_{CC} = 4.5\text{V} \text{ to } 5.5\text{V}$	-	-	0.8	V	
HIGH-level output voltage	$V_{OH}$	$V_I = V_{IH} \text{ or } V_{IL};$ $V_{CC} = 4.5\text{V}$	$I_O = -20\mu\text{A}$	4.4	-	-	V
			$I_O = -4.0\text{mA}$	3.84	-	-	V
LOW-level output voltage	$V_{OL}$	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O = 20\mu\text{A}; V_{CC} = 4.5\text{V}$	-	-	0.1	V
			$I_O = 5.2\text{mA}; V_{CC} = 6.0\text{V}$	-	-	0.33	V
input leakage current	$I_I$	$V_I = V_{CC} \text{ or } \text{GND};$ $V_{CC} = 6.0\text{V}$	-	-	$\pm 1$	$\mu\text{A}$	
supply current	$I_{CC}$	$V_I = V_{CC} \text{ or } \text{GND}; I_O = 0\text{A};$ $V_{CC} = 6.0\text{V}$	-	-	80	$\mu\text{A}$	
additional supply current	$\Delta I_{CC}$	per input pin; $V_I = V_{CC} - 2.1\text{V};$ other inputs at $V_{CC}$ or GND; $V_{CC} = 4.5\text{V} \text{ to } 5.5\text{V}$	Dn and DS inputs	-	-	157.5	$\mu\text{A}$
			CP, $\bar{\text{CE}}$ , and $\bar{\text{PL}}$ inputs	-	-	292.5	$\mu\text{A}$

**3.3.3、DC Characteristics 3**

 (T<sub>amb</sub>=25°C, GND=0V, C<sub>L</sub>=50pf, unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
SN74HC165							
propagation delay	t <sub>pd</sub>	CP, $\overline{CE}$ to Q7, $\overline{Q7}$ ; see Figure 6	V <sub>CC</sub> =2.0V	-	52	165	ns
			V <sub>CC</sub> =4.5V	-	19	33	ns
			V <sub>CC</sub> =5.0V; C <sub>L</sub> =15pF	-	16	-	ns
		PL to Q7, $\overline{Q7}$ ; see Figure 7	V <sub>CC</sub> =2.0V	-	50	165	ns
			V <sub>CC</sub> =4.5V	-	18	33	ns
			V <sub>CC</sub> =5.0V; C <sub>L</sub> =15pF	-	15	-	ns
		D7 to Q7, $\overline{Q7}$ ; see Figure 8	V <sub>CC</sub> =2.0V	-	36	120	ns
			V <sub>CC</sub> =4.5V	-	13	24	ns
			V <sub>CC</sub> =5.0V; C <sub>L</sub> =15pF	-	11	-	ns
		transition time	t <sub>t</sub>	Q7, $\overline{Q7}$ output; see Figure 6	V <sub>CC</sub> =2.0V	-	19
V <sub>CC</sub> =4.5V	-				7	15	ns
V <sub>CC</sub> =6.0V	-				6	13	ns
pulse width	t <sub>w</sub>	CP input HIGH or LOW; see Figure 6	V <sub>CC</sub> =2.0V	80	17	-	ns
			V <sub>CC</sub> =4.5V	16	6	-	ns
			V <sub>CC</sub> =6.0V	14	5	-	ns
		$\overline{PL}$ input LOW; see Figure 7	V <sub>CC</sub> =2.0V	80	14	-	ns
			V <sub>CC</sub> =4.5V	16	5	-	ns
			V <sub>CC</sub> =6.0V	14	4	-	ns
recovery time	t <sub>rec</sub>	$\overline{PL}$ to CP, $\overline{CE}$ ; see Figure 7	V <sub>CC</sub> =2.0V	100	22	-	ns
			V <sub>CC</sub> =4.5V	20	8	-	ns
			V <sub>CC</sub> =6.0V	17	6	-	ns
set-up time	t <sub>su</sub>	DS to CP, $\overline{CE}$ ; see Figure 9	V <sub>CC</sub> =2.0V	80	11	-	ns
			V <sub>CC</sub> =4.5V	16	4	-	ns
			V <sub>CC</sub> =6.0V	14	3	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$ ; see Figure 9	V <sub>CC</sub> =2.0V	80	17	-	ns
			V <sub>CC</sub> =4.5V	16	6	-	ns
			V <sub>CC</sub> =6.0V	14	5	-	ns
		Dn to $\overline{PL}$ ; see Figure 10	V <sub>CC</sub> =2.0V	80	22	-	ns
			V <sub>CC</sub> =4.5V	16	8	-	ns
			V <sub>CC</sub> =6.0V	14	6	-	ns
hold time	t <sub>h</sub>	DS to CP, $\overline{CE}$ and Dn to $\overline{PL}$ ; see Figure 9	V <sub>CC</sub> =2.0V	5	2	-	ns
			V <sub>CC</sub> =4.5V	5	2	-	ns
			V <sub>CC</sub> =6.0V	5	2	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$ ; see Figure 9	V <sub>CC</sub> =2.0V	5	-17	-	ns
			V <sub>CC</sub> =4.5V	5	-6	-	ns
			V <sub>CC</sub> =6.0V	5	-5	-	ns
maximum frequency	f <sub>max</sub>	CP input; see Figure 6	V <sub>CC</sub> =2.0V	6	17	-	MHz
			V <sub>CC</sub> =4.5V	30	51	-	MHz



			$V_{CC}=5.0V; C_L=15pF$	-	56	-	MHz
			$V_{CC}=6.0V$	35	61	-	MHz
power dissipation capacitance	$C_{PD}$	per package; $V_I = GND \text{ to } V_{CC}$		-	35	-	pF
SN74HCT165							
propagation delay	$t_{pd}$	CP, $\overline{CE}$ to Q7, $\overline{Q7}$ ; see Figure 6	$V_{CC}=4.5V$	-	17	34	ns
			$V_{CC}=5.0V; C_L=15pF$	-	14	-	ns
		PL to Q7, $\overline{Q7}$ ; see Figure 7	$V_{CC}=4.5V$	-	20	40	ns
			$V_{CC}=5.0V; C_L=15pF$	-	17	-	ns
D7 to Q7, $\overline{Q7}$ ; see Figure 8	$V_{CC}=4.5V$	-	14	28	ns		
	$V_{CC}=5.0V; C_L=15pF$	-	11	-	ns		
transition time	$t_t$	Q7, $\overline{Q7}$ output; see Figure 6	$V_{CC}=4.5V$	-	7	15	ns
pulse width	$t_w$	CP input; see Figure 6	$V_{CC}=4.5V$	16	6	-	ns
		$\overline{PL}$ input; see Figure 7	$V_{CC}=4.5V$	20	9	-	ns
recovery time	$t_{rec}$	$\overline{PL}$ to CP, $\overline{CE}$ ; see Figure 7	$V_{CC}=4.5V$	20	8	-	ns
set-up time	$t_{su}$	DS to CP, $\overline{CE}$ ; see Figure 9	$V_{CC}=4.5V$	20	2	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$ ; see Figure 9	$V_{CC}=4.5V$	20	7	-	ns
		Dn to $\overline{PL}$ ; see Figure 10	$V_{CC}=4.5V$	20	10	-	ns
hold time	$t_h$	DS to CP, $\overline{CE}$ and Dn to $\overline{PL}$ ; see Figure 9	$V_{CC}=4.5V$	7	-1	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$ ; see Figure 9	$V_{CC}=4.5V$	0	-7	-	ns
maximum frequency	$f_{max}$	CP input; see Figure 6	$V_{CC}=4.5V$	26	44	-	MHz
			$V_{CC}=5.0V; C_L=15pF$	-	48	-	MHz
power dissipation capacitance	$C_{PD}$	per package; $V_I = GND \text{ to } V_{CC} - 1.5V$		-	35	-	pF

Note:

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[2]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in uW).

$$P_D = (C_{PD} \times V_{CC}^2 \times f_i \times N) + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$ =input frequency in MHz;

$f_o$ =output frequency in MHz;

$C_L$ =output load capacitance in pF;

$V_{CC}$ =supply voltage in V;

N=number of inputs switching;

$\sum (C_L \times V_{CC}^2 \times f_o)$ =sum of outputs.

**3.3.4、AC Characteristics 2**

( $T_{amb}=-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $GND=0\text{V}$ ,  $C_L=50\text{pf}$ , unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
SN74HC165							
propagation delay	$t_{pd}$	CP, $\overline{CE}$ to Q7, $\overline{Q7}$ ; see Figure 6	$V_{CC}=2.0\text{V}$	-	-	205	ns
			$V_{CC}=4.5\text{V}$	-	-	41	ns
			$V_{CC}=6.0\text{V}$	-	-	35	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$ ; see Figure 7	$V_{CC}=2.0\text{V}$	-	-	205	ns
			$V_{CC}=4.5\text{V}$	-	-	41	ns
			$V_{CC}=6.0\text{V}$	-	-	35	ns
		D7 to Q7, $\overline{Q7}$ ; see Figure 8	$V_{CC}=2.0\text{V}$	-	-	150	ns
			$V_{CC}=4.5\text{V}$	-	-	30	ns
			$V_{CC}=6.0\text{V}$	-	-	26	ns
transition time	$t_t$	Q7, $\overline{Q7}$ output; see Figure 6	$V_{CC}=2.0\text{V}$	-	-	95	ns
			$V_{CC}=4.5\text{V}$	-	-	19	ns
			$V_{CC}=6.0\text{V}$	-	-	16	ns
pulse width	$t_w$	CP input HIGH or LOW; see Figure 6	$V_{CC}=2.0\text{V}$	100	-	-	ns
			$V_{CC}=4.5\text{V}$	20	-	-	ns
			$V_{CC}=6.0\text{V}$	17	-	-	ns
		$\overline{PL}$ input LOW; see Figure 7	$V_{CC}=2.0\text{V}$	100	-	-	ns
			$V_{CC}=4.5\text{V}$	20	-	-	ns
			$V_{CC}=6.0\text{V}$	17	-	-	ns
recovery time	$t_{rec}$	$\overline{PL}$ to CP, $\overline{CE}$ ; see Figure 7	$V_{CC}=2.0\text{V}$	125	-	-	ns
			$V_{CC}=4.5\text{V}$	25	-	-	ns
			$V_{CC}=6.0\text{V}$	21	-	-	ns
set-up time	$t_{su}$	DS to CP, $\overline{CE}$ ; see Figure 9	$V_{CC}=2.0\text{V}$	100	-	-	ns
			$V_{CC}=4.5\text{V}$	20	-	-	ns
			$V_{CC}=6.0\text{V}$	17	-	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$ ; see Figure 9	$V_{CC}=2.0\text{V}$	100	-	-	ns
			$V_{CC}=4.5\text{V}$	20	-	-	ns
			$V_{CC}=6.0\text{V}$	17	-	-	ns
		Dn to $\overline{PL}$ ; see Figure 10	$V_{CC}=2.0\text{V}$	100	-	-	ns
			$V_{CC}=4.5\text{V}$	20	-	-	ns
			$V_{CC}=6.0\text{V}$	17	-	-	ns
hold time	$t_h$	DS to CP, $\overline{CE}$ and Dn to $\overline{PL}$ ; see Figure 9	$V_{CC}=2.0\text{V}$	5	-	-	ns
			$V_{CC}=4.5\text{V}$	5	-	-	ns
			$V_{CC}=6.0\text{V}$	5	-	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$ ; see Figure 9	$V_{CC}=2.0\text{V}$	5	-	-	ns
			$V_{CC}=4.5\text{V}$	5	-	-	ns
			$V_{CC}=6.0\text{V}$	5	-	-	ns

maximum frequency	$f_{\max}$	CP input; see Figure 6	$V_{CC}=2.0V$	5	-	-	MHz
			$V_{CC}=4.5V$	24	-	-	MHz
			$V_{CC}=6.0V$	28	-	-	MHz
SN74HCT165							
propagation delay	$t_{pd}$	CP, $\overline{CE}$ to Q7, $\overline{Q7}$ ; see Figure 6	$V_{CC}=4.5V$	-	-	43	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$ ; see Figure 7	$V_{CC}=4.5V$	-	-	50	ns
		D7 to Q7, $\overline{Q7}$ ; see Figure 8	$V_{CC}=4.5V$	-	-	35	ns
transition time	$t_t$	Q7, $\overline{Q7}$ output; see Figure 6	$V_{CC}=4.5V$	-	-	19	ns
pulse width	$t_w$	CP input; see Figure 6	$V_{CC}=4.5V$	20	-	-	ns
		$\overline{PL}$ input; see Figure 7	$V_{CC}=4.5V$	25	-	-	ns
recovery time	$t_{rec}$	$\overline{PL}$ to CP, $\overline{CE}$ ; see Figure 7	$V_{CC}=4.5V$	25	-	-	ns
set-up time	$t_{su}$	DS to CP, $\overline{CE}$ ; see Figure 9	$V_{CC}=4.5V$	25	-	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$ ; see Figure 9	$V_{CC}=4.5V$	25	-	-	ns
		Dn to $\overline{PL}$ ; see Figure 10	$V_{CC}=4.5V$	25	-	-	ns
hold time	$t_h$	DS to CP, $\overline{CE}$ and Dn to $\overline{PL}$ ; see Figure 9	$V_{CC}=4.5V$	9	-	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$ ; see Figure 9	$V_{CC}=4.5V$	0	-	-	ns
maximum frequency	$f_{\max}$	CP input; see Figure 6	$V_{CC}=4.5V$	21	-	-	MHz

Note:

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[2]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in uW).

$$P_D = (C_{PD} \times V_{CC}^2 \times f_i \times N) + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$ =input frequency in MHz;

$f_o$ =output frequency in MHz;

$C_L$ =output load capacitance in pF;

$V_{CC}$ =supply voltage in V;

N=number of inputs switching;

$\sum (C_L \times V_{CC}^2 \times f_o)$ =sum of outputs.

## 4、Testing Circuit

### 4.1、AC Testing Circuit

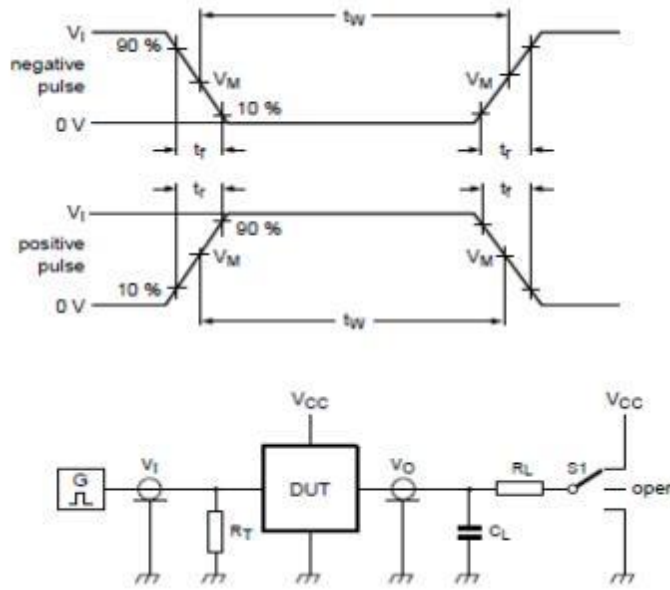


Figure 5. Test circuit for measuring switching times

Definitions for test circuit:

$C_L$ =load capacitance including jig and probe capacitance.

$R_T$ =termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.  $R_L$ =Load resistance.

$S1$ =Test selection switch.

### 4.2、AC Testing Waveforms

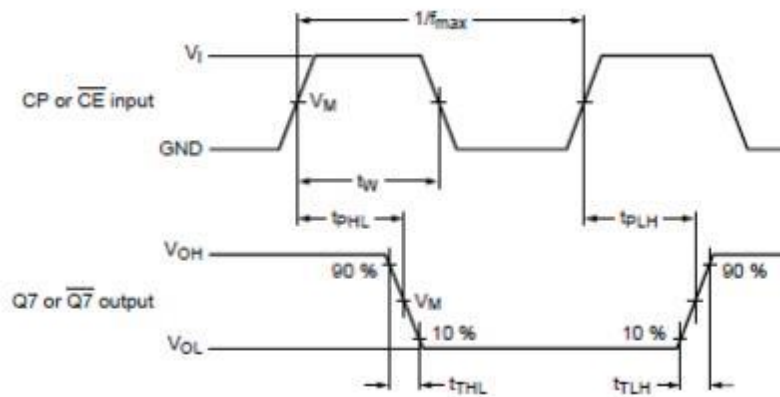


Figure 6. The clock (CP) or clock enable ( $\overline{CE}$ ) to output ( $Q7$  or  $\overline{Q7}$ ) propagation delays, the clock pulse width, the maximum clock frequency and the output transition times

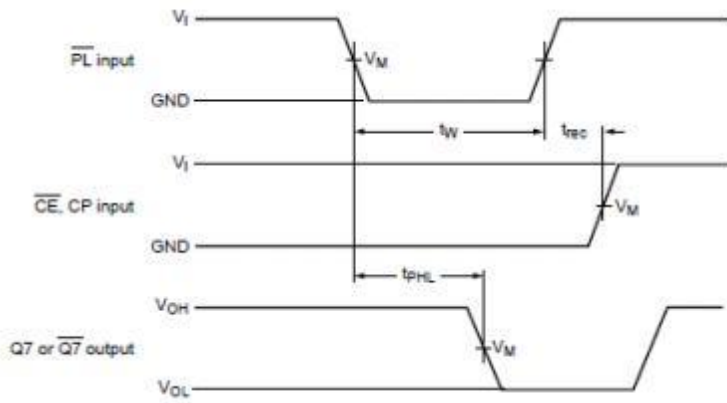


Figure 7. The parallel load ( $\overline{PL}$ ) pulse width, the parallel load to output (Q7 or  $\overline{Q7}$ ) propagation delays, the parallel load to clock (CP) and clock enable ( $\overline{CE}$ ) recovery time

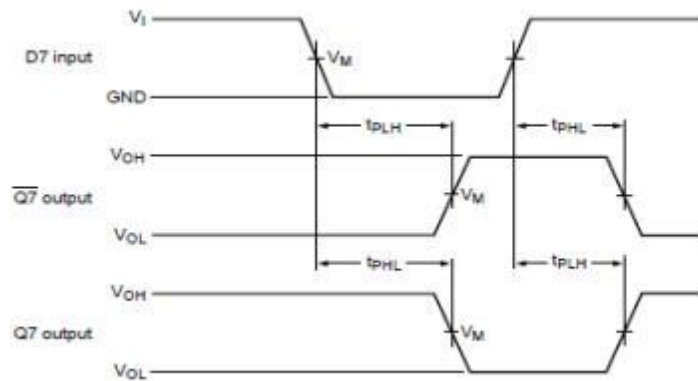


Figure 8. The data input (D7) to output (Q7 or  $\overline{Q7}$ ) propagation delays when  $\overline{PL}$  is LOW

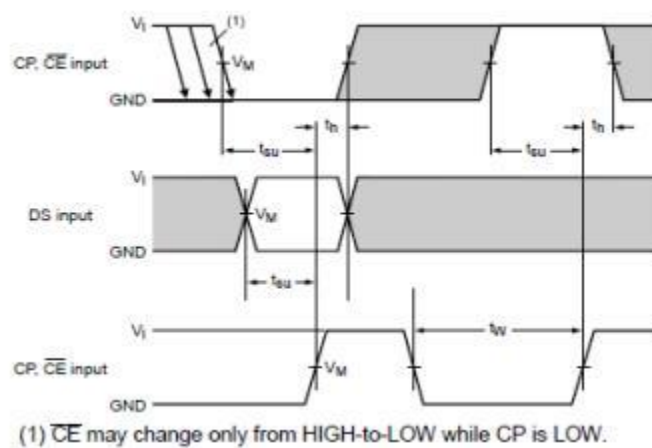


Figure 9. The set-up and hold times from the serial data input (DS) to the clock (CP) and clock enable ( $\overline{CE}$ ) inputs, from the clock enable input ( $\overline{CE}$ ) to the clock input (CP) and from the clock input (CP) to the clock enable input (CE)

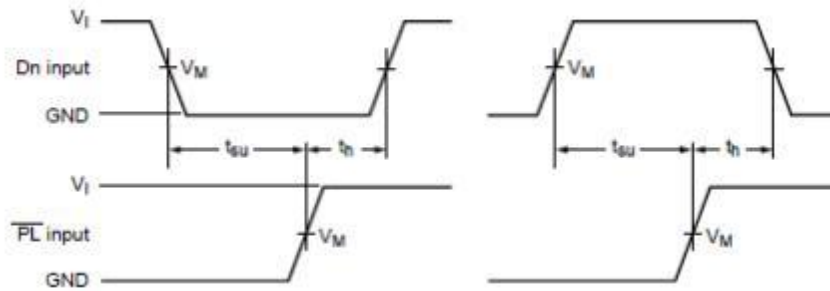


Figure 10. The set-up and hold times from the data inputs (Dn) to the parallel load input ( $\overline{PL}$ )

#### 4.3 、 Measurement Points

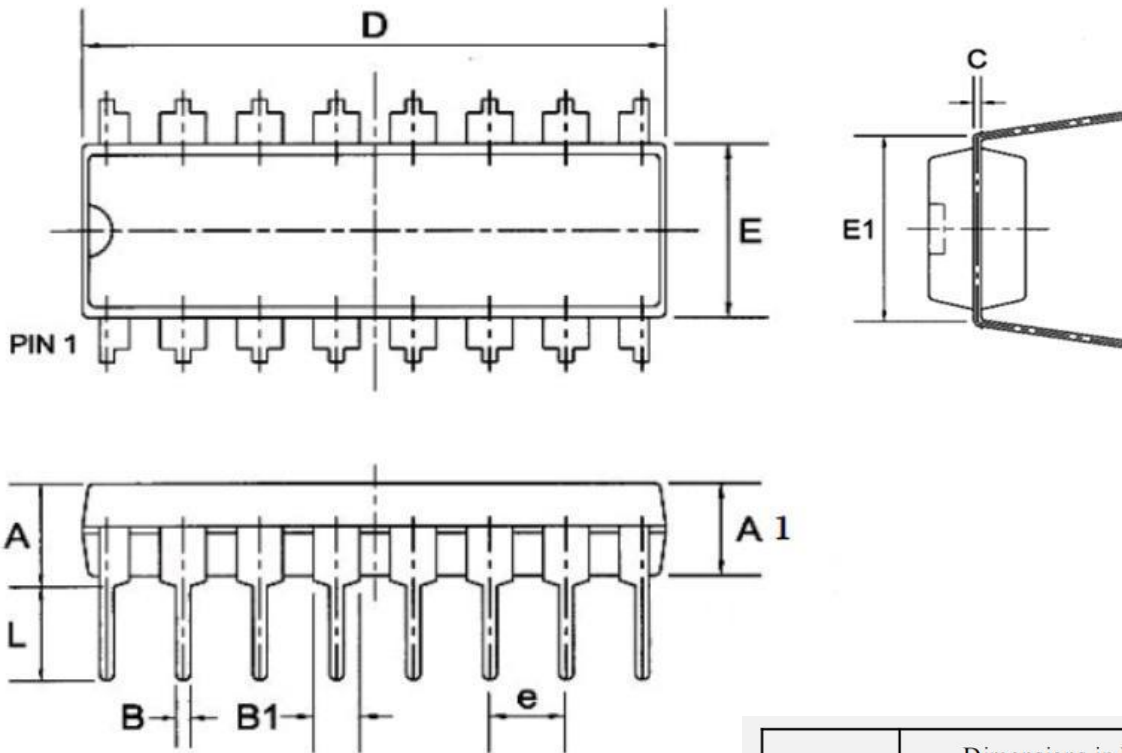
Type	Input		Output
	$V_I$	$V_M$	$V_M$
SN74HC165	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
SN74HCT165	3V	1.3V	1.3V

#### 4.4 、 Test Data

Type	Input		Load		S1 position
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$
SN74HC165	$V_{CC}$	6.0ns	15pF, 50pF	1k $\Omega$	open
SN74HCT165	3.0V	6.0ns	15pF, 50pF	1k $\Omega$	open

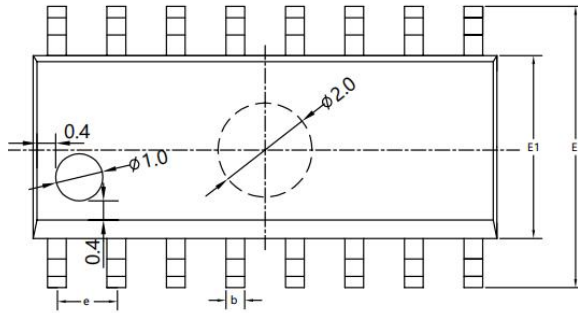
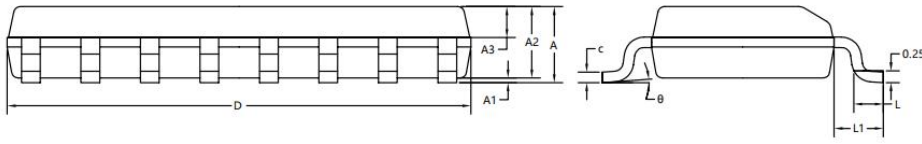
## 5、Package Information

### 5.1、DIP16



Symbol	Dimensions in Millimeters		
	Min	Nom	Max
A	--	--	4.31
A1	3.15	3.30	3.65
B	--	0.50	--
B1	--	1.6	--
C	--	0.27	--
D	19.00	19.20	19.60
E	6.20	6.50	6.60
E1	--	8.0	--
e	--	2.3	--
L	3.00	3.20	3.60

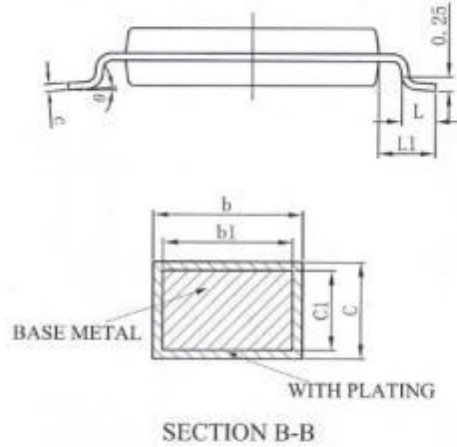
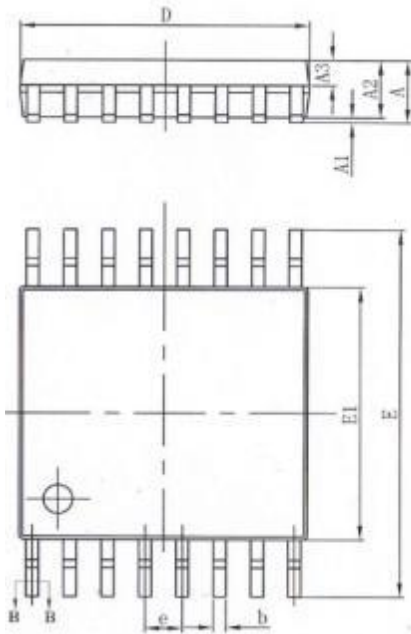
5.2、SOP16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.50	1.60	1.70
A1	0.10	0.15	0.25
A2	1.40	1.45	1.50
A3	0.60	0.65	0.70
b	0.30	0.40	0.50
c	0.15	0.20	0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.85	3.90	3.95
e	1.27BSC		
L	0.50	0.60	0.70
L1	1.05BSC		
θ	0°	4°	8°



5.3, TSSOP16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°

Statement:

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- ◇ Any semiconductor product is liable to fail or malfunction under certain conditions, and the buyer shall be responsible for complying with safety standards in the system design and whole machine manufacturing using Shenzhen xinbole electronics co., ltd products, and take appropriate security measures to avoid the potential risk of failure may result in personal injury or property losses of the situation occurred!
- ◇ Product performance is never ending, Shenzhen xinbole electronics co., ltd will be dedicated to provide customers with better performance, better quality of integrated circuit products.

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