

Product Specification

XBLW AO4435

P-Channel Enhancement Mode MOSFET

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Description

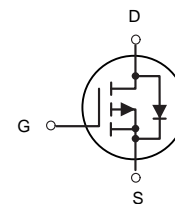
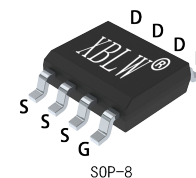
The AO4435 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

- $V_{DS} = -30\text{ V}$ $I_D = -11\text{ A}$
- $R_{DS(ON)} < 16\text{ m}\Omega$ @ $V_{GS} = 10\text{ V}$

Application

- Battery protection
- Load switch
- Uninterruptible power supply



P-Channel MOSFET

Package Marking and Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW AO4435	SOP-8	AO4435	Tape	3000Pcs/Reel

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	- 30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_A = 25^\circ\text{C}$	Drain Current ³ , $V_{GS} @ 10\text{ V}$	-11	A
IDM	Pulsed Drain Current ¹	-40	A
$P_D @ T_A = 25^\circ\text{C}$	Total Power Dissipation	3.7	W
TSTG	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$
R_{thj-a}	Maximum Thermal Resistance, Junction-ambient ³	33.8	$^\circ\text{C/W}$

Electrical Characteristics (T_J = 25°C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D = -250μA	-30	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -30V, V _{GS} =0V,	-	-	-1	μA
I _{GSS}	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} = ±20V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D = -250μA	-1.0	-1.6	-2.5	V
R _{DS(on)}	Static Drain-Source on-Resistance <small>Note3</small>	V _{GS} = -10V, I _D = -10A	-	13	16	mΩ
		V _{GS} = -4.5V, I _D = -5A	-	18	27	
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = -15V, V _{GS} =0V, f=1.0MHz	-	1330	-	pF
C _{oss}	Output Capacitance		-	183	-	pF
C _{rss}	Reverse Transfer Capacitance		-	156	-	pF
Q _g	Total Gate Charge	V _{DS} = -15V, I _D = -5A, V _{GS} = -10V	-	22	-	nC
Q _{gs}	Gate-Source Charge		-	1.0	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	1.8	-	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} = -15V, I _D = -10A, V _{GS} =-10V, R _{GEN} =2.5Ω	-	9	-	ns
t _r	Turn-on Rise Time		-	13	-	ns
t _{d(off)}	Turn-off Delay Time		-	48	-	ns
t _f	Turn-off Fall Time		-	20	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	-11	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-40	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S = -15A	-	-0.8	-1.2	V
t _{rr}	Reverse Recovery Time	T _J =25°C,	-	64	-	ns
Q _{rr}	Reverse Recovery Charge	V _{DD} = -24V, I _F =-2.8A, dI/dt=-100A/μs	-	25	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: T_J=25°C, V_{GS}=10V, R_G=25Ω, L=0.5mH, I_{AS}=-12.7A

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

Typical Characteristics

Figure 1: Output Characteristics

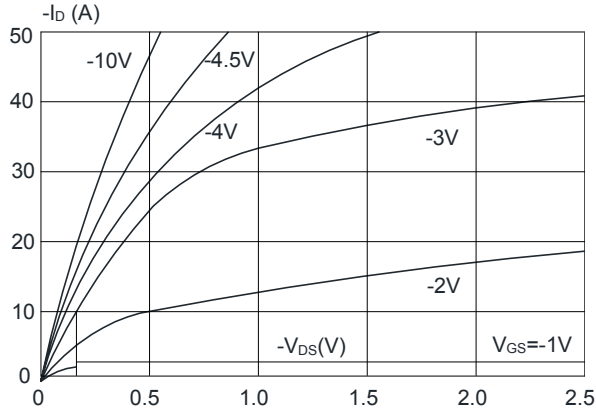


Figure 2: Typical Transfer Characteristics

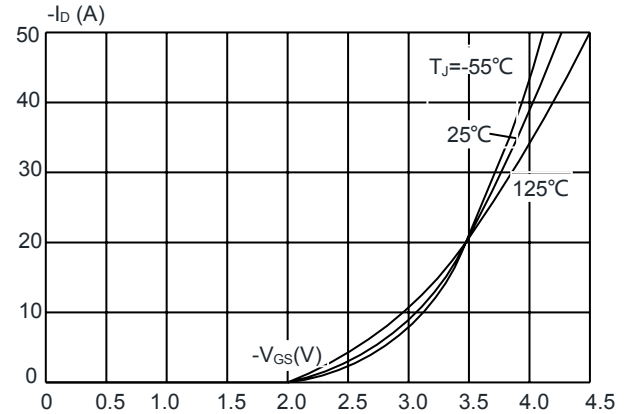


Figure 3: On-resistance vs. Drain Current

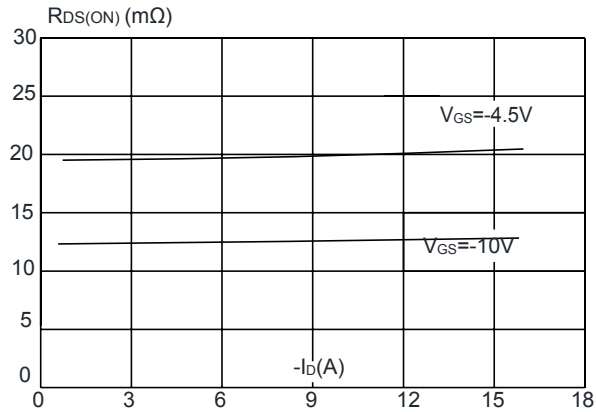


Figure 4: Body Diode Characteristics

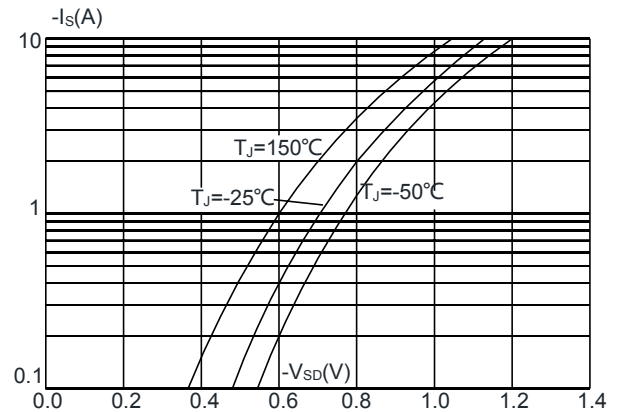


Figure 5: Gate Charge Characteristics

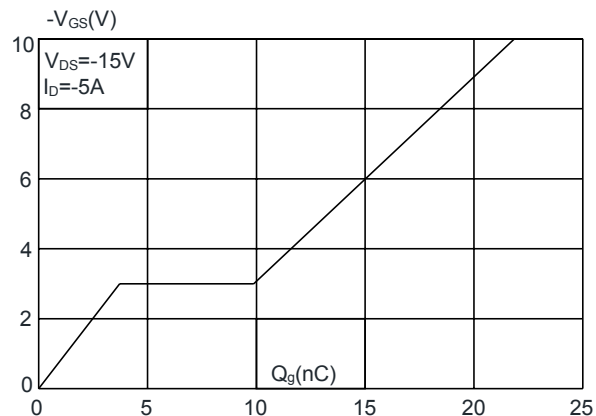


Figure 6: Capacitance Characteristics

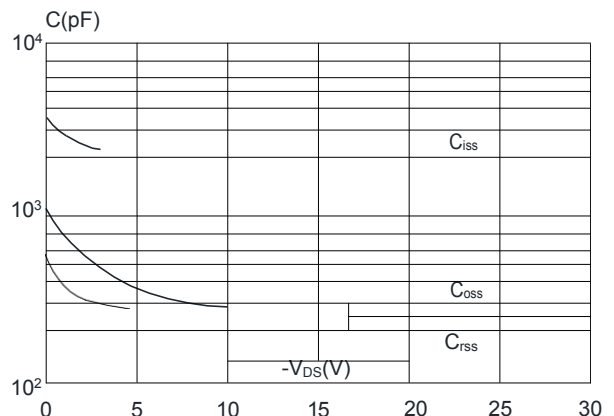


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

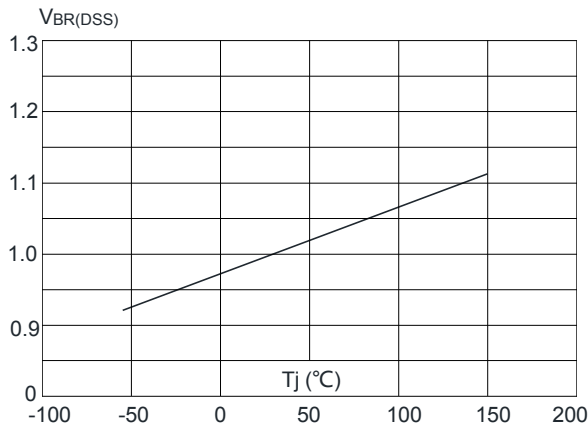


Figure 8: Normalized on Resistance vs. Junction Temperature

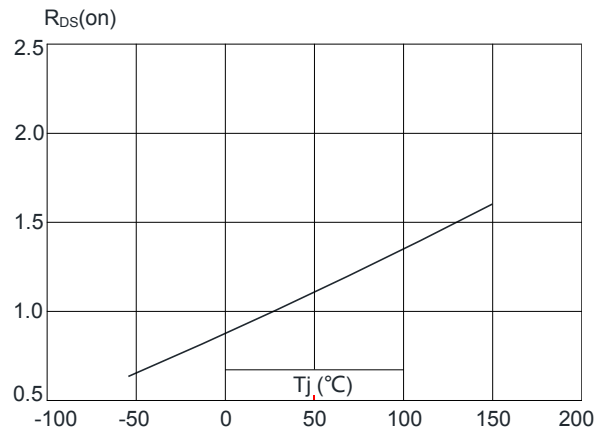


Figure 9: Maximum Safe Operating Area

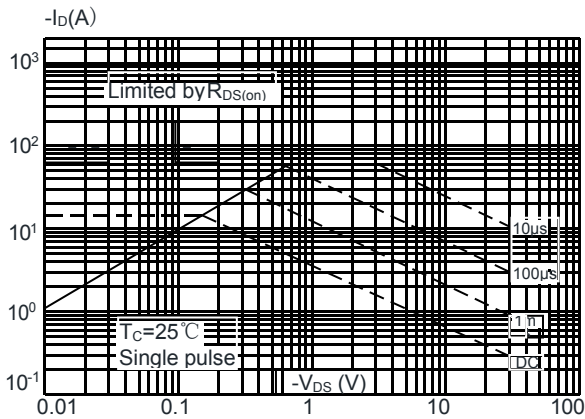


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

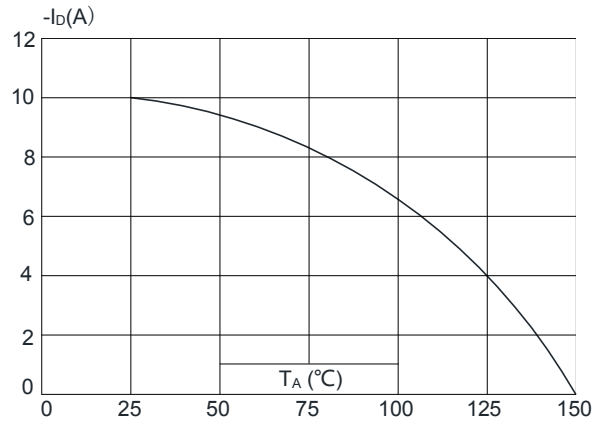
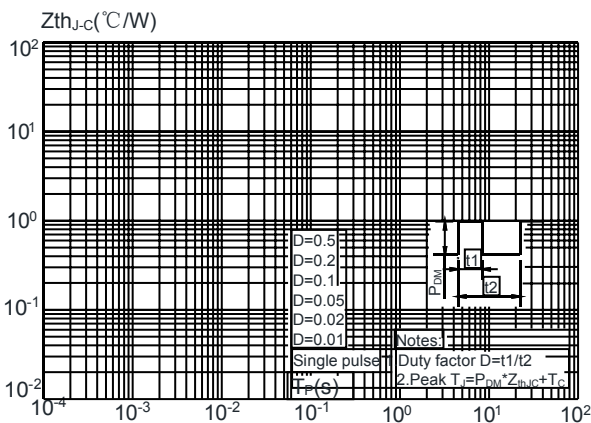
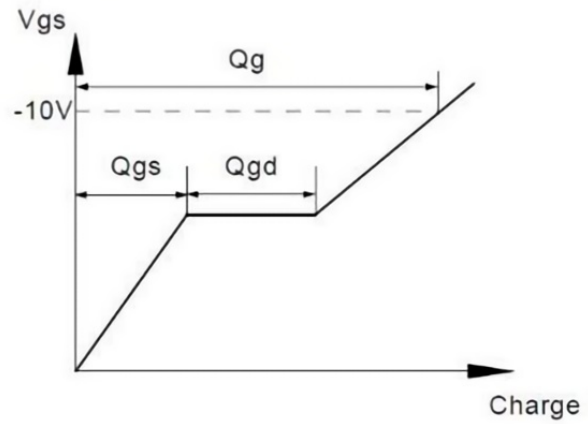
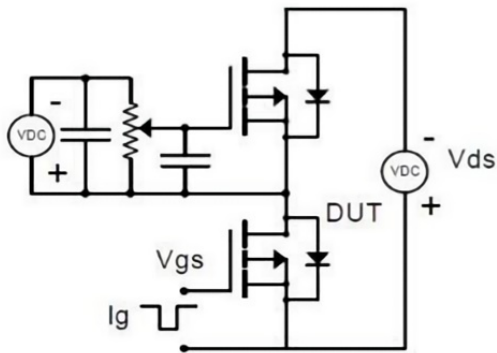


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

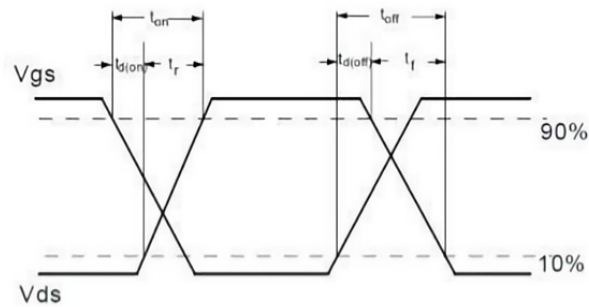
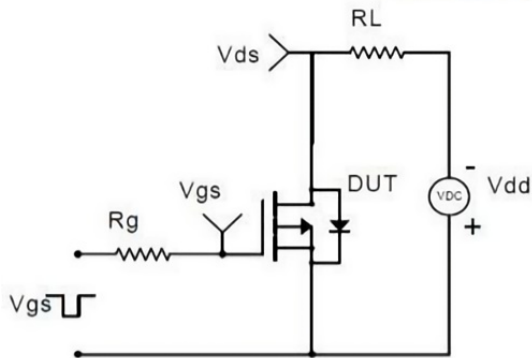


Test Circuit

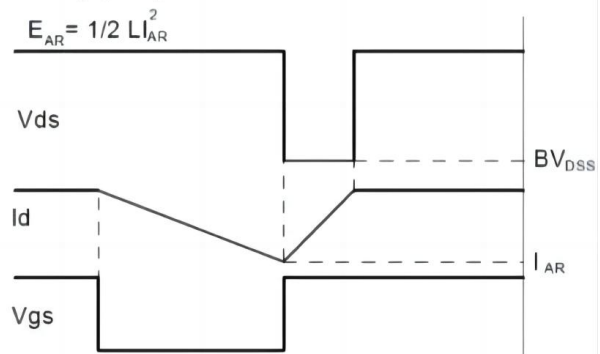
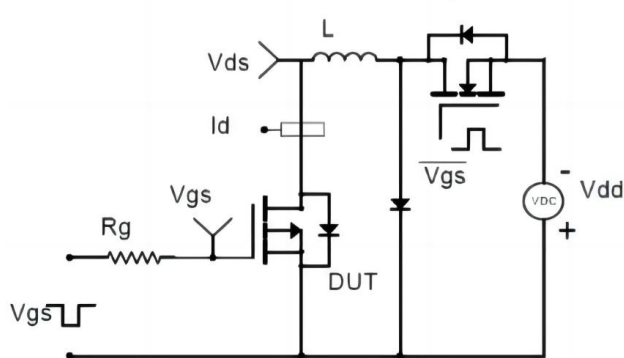
Gate Charge Test Circuit & Waveform



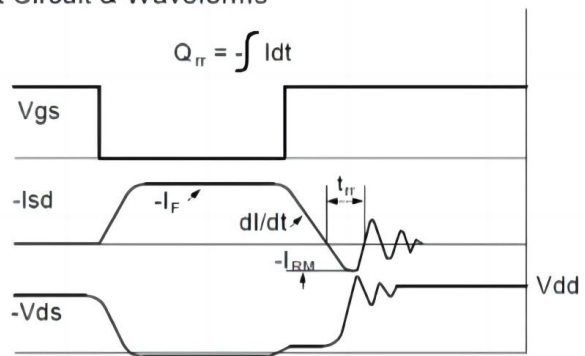
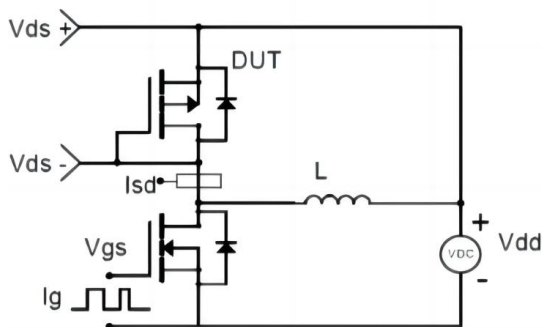
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

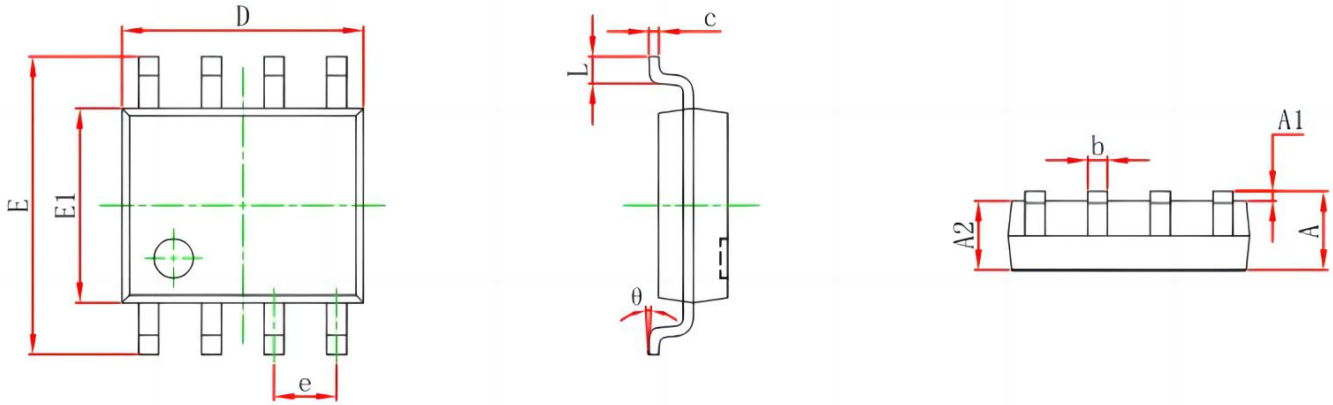


Diode Recovery Test Circuit & Waveforms

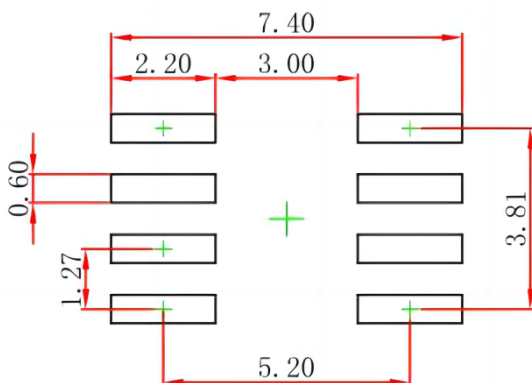


Package Outline Dimensions

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Note:

1. Controlling dimension: In millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.

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