芯伯乐®
XINBOLE

Product Specification

XBLW TLV6001/6002/6004

Low-Power, Rail-to-Rail In/Out
1-MHz Operational Amplifier

WEB | www.xinboleic.com

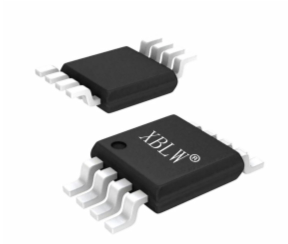
RoHS

Description

The XBLW TLV6001(single), XBLW TLV6002(dual) and XBLW TLV6004(quad) are general purpose,low offset, high frequency response and micro power operational amplifiers. With an excellent bandwidth of 1MHz, a slew rate of 0.8V/μs, and a quiescent current of 80μA per amplifier at 5V, the XBLW TLV6001/6002/6004 family can be designed into a wide range of applications.

The XBLW TLV6001/6002/6004 op-amps are designed to provide optimal performance in low voltage and low power systems. The input common-mode voltage range includes ground, and the maximum input offset voltage are 4.5mV. These parts provide rail-to-rail output swing into heavy loads. The XBLW TLV6001/6002/6004 family is specified for single or dual power supplies of +1.8V to +5.5V.

The XBLW TLV6001 is available in 5-lead SOT-23 and SC70-5 package. The XBLW TLV6002 is available in8 -lead SOP-8 and MSOP-8 package. The XBLW TLV6004 is available in 14-lead SOP and TSSOP package.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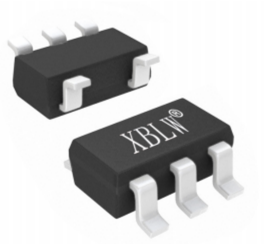
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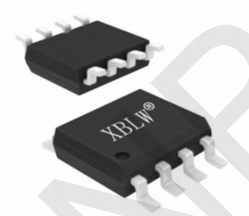
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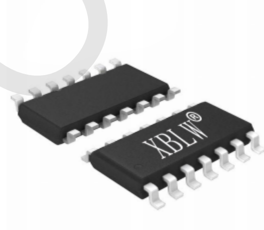
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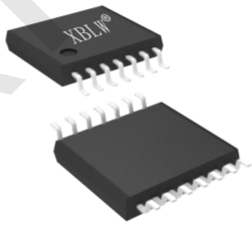
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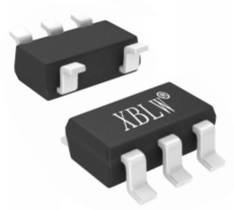
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Feature

- Rail-to-Rail Input and Output
- General Purpose 1MHz Amplifiers, Low Cost
- Low Offset Voltage: 4.5 mV Maximum
- Low Power: 80μA per Amplifier Supply Current
- Unit Gain Stable
- Input Voltage Range: -0.1V to +5.1V at 5V Supply
- Operating Power Supply: +1.8V to +5.5V
- Operating Temperature Range: -40℃ to +125℃
- ESD Rating: HBM-4kV, CDM-2kV
- Settling Time to 0.1% with 2V Step: 4.2 μs
- High Slew Rate: 0.8V/μs

Applications

- Active Filters
- Audio Outputs
- Medical Instrumentation
- Sensor Interfaces
- Smoke/Gas/Environment Sensors
- Portable Equipment and Mobile Devices
- Battery and Power Supply Control
- Battery-Powered Instrumentation

Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW TLV6001IDCKR	SC70-5	13X	Tape	3000Pcs/Reel
XBLW TLV6001IDBVR	SOT23-5	14W2	Tape	3000Pcs/Reel
XBLW TLV6001RIDBVR	SOT23-5	16O2	Tape	3000Pcs/Reel
XBLW TLV6001UIDBVR	SOT23-5	16P2	Tape	3000Pcs/Reel
XBLW TLV6002IDR	SOP-8	TL6002	Tape	3000Pcs/Reel
XBLW TLV6002IDGKR	MSOP-8	6002	Tape	3000Pcs/Reel
XBLW TLV6004IDR	SOP-14	TLV6004	Tape	3000Pcs/Reel
XBLW TLV6004IPWR	TSSOP-14	TLV6004	Tape	3000Pcs/Reel

Pin Configurations

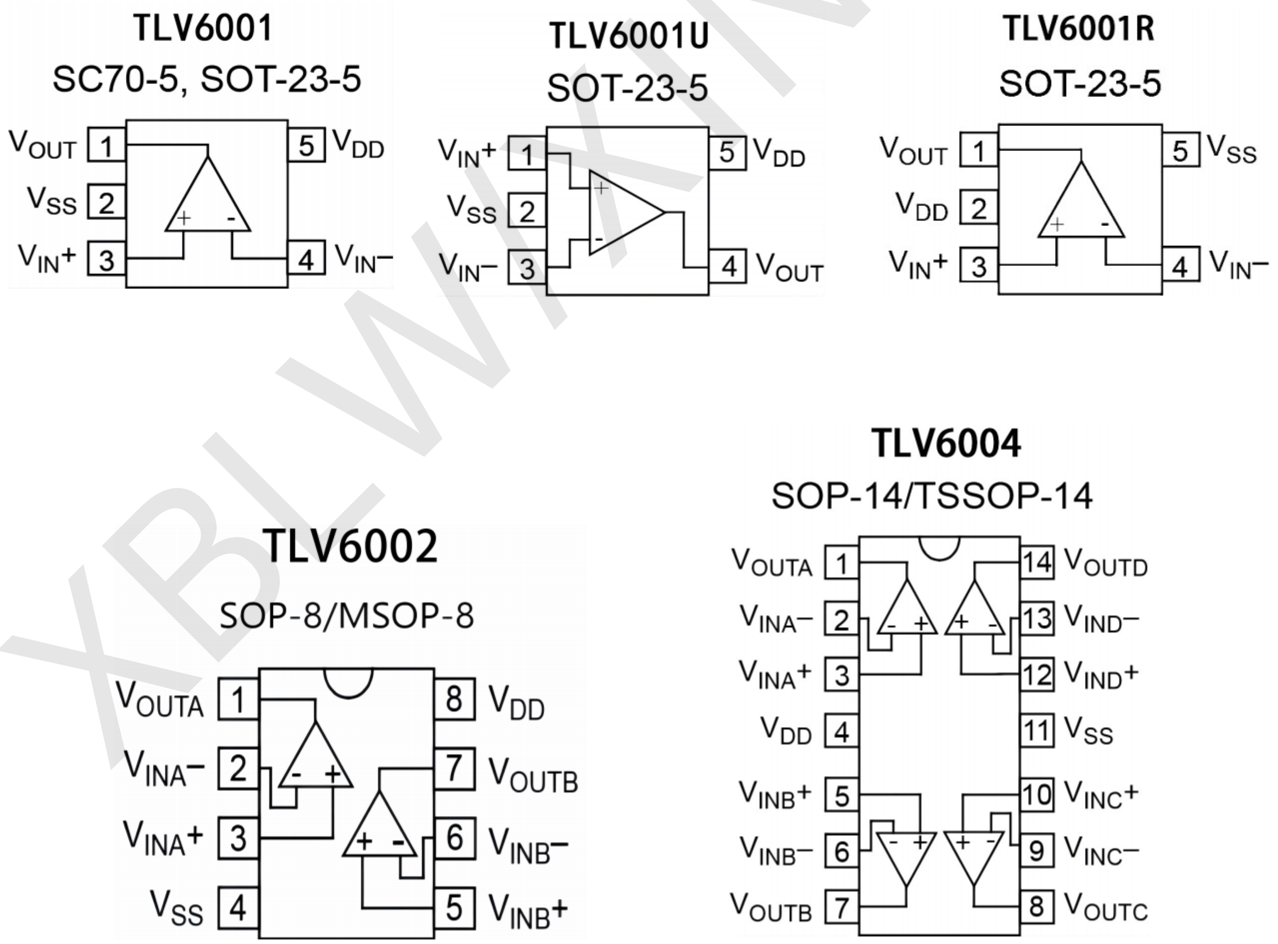


Figure 1 Pin Configurations

Pin Description

Symbol	Description
V_{IN-}	Negative (inverting) input.
V_{IN+}	Positive (noninverting) input.
V_{INA-}, V_{INB-} V_{INC-}, V_{IND-}	Inverting Input of the Amplifier. The Voltage range can go from (V_{S-} – 0. 1V) to (V_{S+} + 0. 1V).
V_{INA+}, V_{INB+} V_{INC+}, V_{IND+}	Non-Inverting Input ofAmplifier. This pin has the same voltage range as -IN.
V_{DD}	Positive Power Supply. The voltage is from 1.8V to 5.5V. Split supplies are possible as long as the voltage between V_{S+} and V_{S-} is between 1.8V and 5.5V. A bypass capacitor of 0. 1μF as close to the part as possible should be used between power supply pins or between supply pins and ground
V_{SS}	Negative Power Supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V_{S+} and V_{S-} is from 1.8V to 5.5V. If it is not connected to ground, bypass it with a capacitor of 0. 1μF as close to the part as possible.
V_{OUT}	Output.
V_{OUTA}, V_{OUTB} V_{OUTC}, V_{OUTD}	Amplifier Output

Absolute Maximum Ratings (TA= 25℃)

Symbol	Description	Value	Units
V_{S+}, V_{S-}	Supply Voltage, V_{S+} to V_{S-}	7.0	V
V_{CM}	Common-Mode Input Voltage	V_{S-} – 0.3 to V_{S+} + 0.3	V
ESD	Electrostatic Discharge Voltage	HBM ±4000	V
		CDM ±2000	V
T_J	Junction Temperature	160	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C(T_J)
T_{JL}	Lead Temperature Range (Soldering 10sec)	260	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. Provided device does not exceed maximum junction temperature (TJ) at any time.

Electrical Characteristics

V_S = 5.0V, T_A = +25℃, V_{CM} = V_S/2, V_O = V_S/2, and R_L = 10kΩ connected to V_S/2, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
INPUT CHARACTERISTICS						
V_{OS}	Input offset voltage		-4.5	±1.0	+4.5	mV
	Over temperature		-4.8		+4.8	
V_{OS} TC	Offset voltage drift	Over Temperature		2.3		μV/°C
I_B	Input bias current			1		pA
	Over temperature			500		
I_{OS}	Input offset current			1		pA
V_{CM}	Common-mode voltage range		V_{S-}–0.1		V_{S+}+0.1	V
CMRR	Common-mode rejection ratio	V_{CM} = 0.05V to 3.5V		90		dB
	Over temperature			85		
		V_{CM} = V_{S-}–0.1 to V_{S+}+0.1 V		80		
	Over temperature			75		
A_{VOL}	Open-loop voltage gain	V_O = 0.05 to 3.5 V		110		dB
	Over temperature			100		
R_{IN}	Input resistance		100			GΩ
C_{IN}	Input capacitance	Differential		2.0		pF
		Common mode		3.5		
OUTPUT CHARACTERISTICS						
V_{OH}	High output voltage swing			V_{S+}–8		mV
V_{OL}	Low output voltage swing			8		mV
Z_{OUT}	Closed-loop output impedance	f = 200kHz, G = +1		0.4		Ω
	Open-loop output impedance	f = 1MHz, I_O = 0		2.6		
I_{SC}	Short-circuit current	Source current through 10Ω		40		mA
		Sink current through 10Ω		40		
DYNAMIC PERFORMANCE						
GBW	Gain bandwidth product	f = 1kHz		1.0		MHz
$Φ_M$	Phase margin	C_L = 100pF		62		°
SR	Slew rate	G = +1, C_L = 100pF, V_O = 1.5V to 3.5V		0.8		V/μs

Electrical Characteristics

V_S = 5.0V, T_A = +25℃, V_{CM} = V_S/2, V_O = V_S/2, and R_L = 10kΩ connected to V_S/2, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_S	Settling time	To 0. 1%, G = +1, 2V step		4.2		μs
		To 0.01%, G = +1, 2V step		5.2		
t_{OR}	Overload recovery time	V_{IN} * Gain > V_S		2		μs
THD+N	Total harmonic distortion+Nois e	f= 1kHz, G = +1, V_O=3V_{PP}		0.003		%
NOISE PERFORMANCE						
V_n	Input voltage noise	f = 0.1 to 10 Hz		13		μV_{P-P}
e_n	Input voltage noise density	f= 1kHz		35		nV/√Hz
I_n	Input current noise density	f= 10kHz		6		fA/√Hz
POWER SUPPLY						
V_S	Operating supply voltage		1.8		5.5	V
PSRR	Power supply rejection ratio	V_S = 1.8V to 6.0V, V_{CM} < V_{S+} − 2V		98		dB
	Over temperature			85		
I_Q	Quiescent current (peramplifier)			80	120	μA
	Over temperature			85	130	
THERMAL CHARACTERISTICS						
T_A	Operating temperature range		-40		+125	°C
$θ_{JA}$	Package thermal resistance	SOT23-5		190		℃/W
		SOP-8/MSOP-8		125		
		SOP-14/TSSOP-14		115		

Specifications subject to changes without notice

Typical Performance Characteristics

At T_A = +25℃, V_{CM} = V_S/2, and R_L = 10kΩ connected to V_S/2, unless otherwise noted.

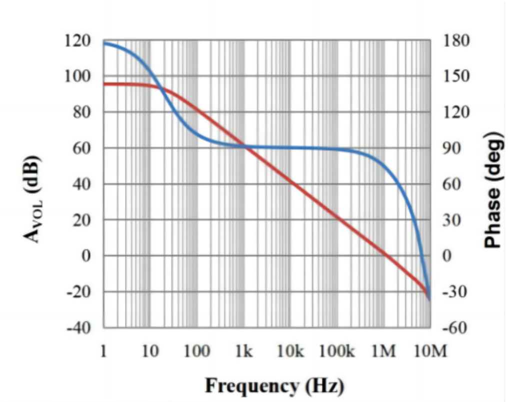


Figure 2 Open-loop Gain and Phase as function of Frequency

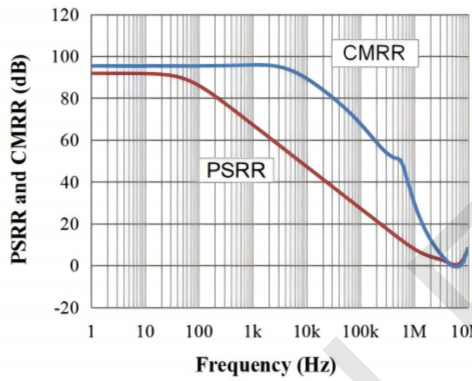


Figure 3 Power Supply and Common-mode RejectionRatio a as a function of Frequency

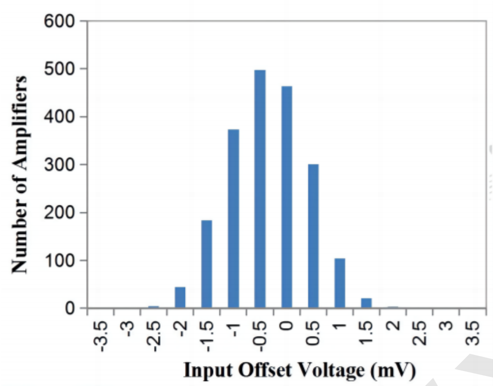


Figure 4 Input Offset Voltage Production Distribution

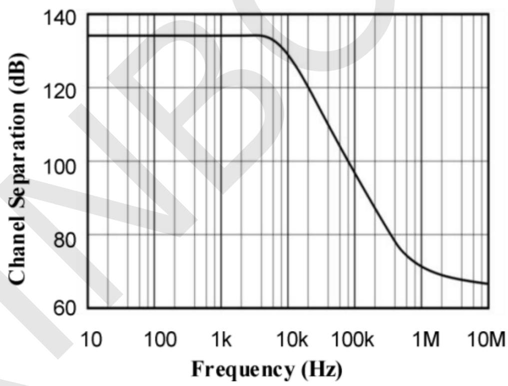


Figure 5 Channel Separation as a function of Frequency

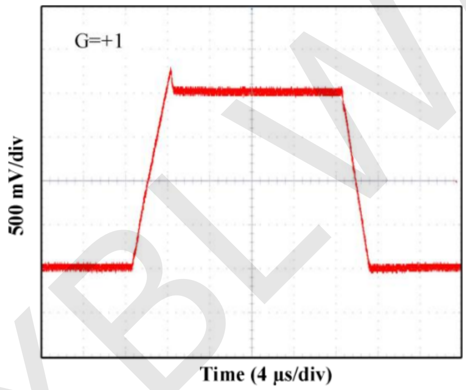


Figure 6 Large-Signal Step Response at 2.7V

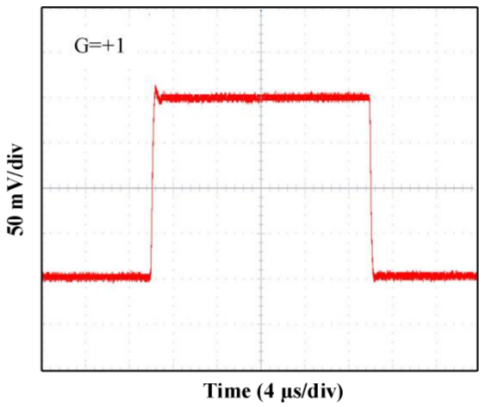


Figure 7 Small-Signal Step Response at 2.7V

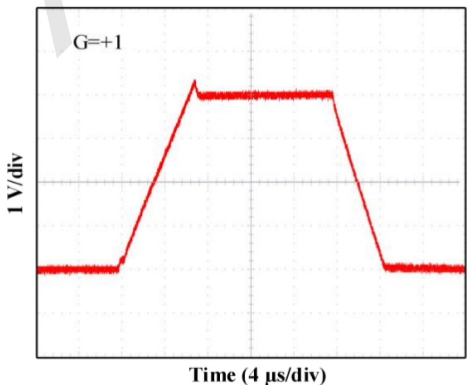


Figure 8 Large-Signal Step Response at 5V

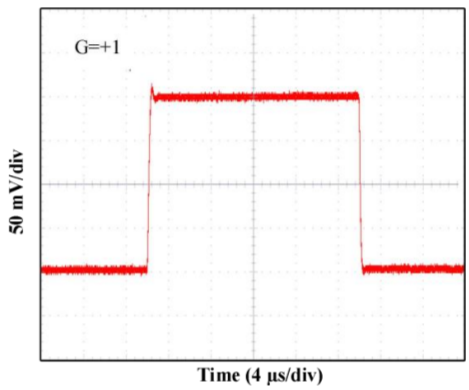


Figure 9 Small-Signal Step Response at 5V

Application Notes

1. LOW INPUT BIAS CURRENT

The XBLW TLV6001/6002/6004 family is a CMOS op-amp family and features very low input bias current in pA range. The low input bias current allows the amplifiers to be used in applications with high resistance sources. Care must be taken to minimize PCB Surface Leakage. See below section on "PCB Surface Leakage" for more details.

2. PCB SURFACE LEAKAGE

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5pA of current to flow, which is greater than the XBLW TLV6001/6002/6004's input bias current at +25℃ (±1fA, typical). It is recommended to use multi-layer PCB layout and route the op-amp's -IN and +IN signal under the PCB surface.

The effective way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 10 for Inverting Gain application.

1. For Non-Inverting Gain and Unity-Gain Buffer:

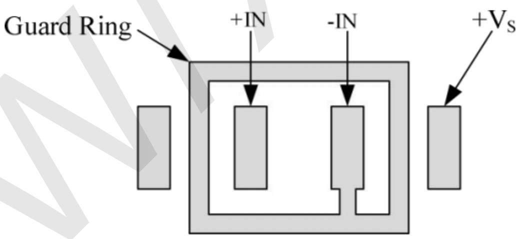
a) Connect the non-inverting pin (+IN) to the input with a wire that does not touch the PCB surface.

b) Connect the guard ring to the inverting input pin (-IN). This biases the guard ring to the Common Mode input voltage.

2. For Inverting Gain and Trans-impedance Gain Amplifiers (convert current to voltage, such as photo detectors):

a) Connect the guard ring to the non-inverting input pin (+IN). This biases the guard ring to the same reference voltage as the op-amp (e.g., $V_S/2$ or ground).

b) Connect the inverting pin (-IN) to the input with a wire that does not touch the PCB surface.



3. GROUND SENSING AND RAIL TO RAIL

The input common-mode voltage range of the XBLW TLV6001/6002/6004 series extends 100mV beyond the supply rails. This is achieved with a complementary input stage—an N- channel input differential pair in parallel with a P -channel differential pair. For normal operation, inputs should be limited to this range. The absolute maximum input voltage is 300mV beyond the supplies. Inputs greater than the input common-mode range but less than the maximum input voltage, while not valid, will not cause any damage to the op-amp. Unlike some other op-amps, if input current is limited, the inputs may go beyond the supplies without phase inversion, as shown in Figure 11. Since the input common- mode range extends from (V_{S-} − 0.1V) to (V_{S+} + 0.1V), the XBLW TLV6001/6002/6004 op-amps can easily perform 'true ground' sensing.

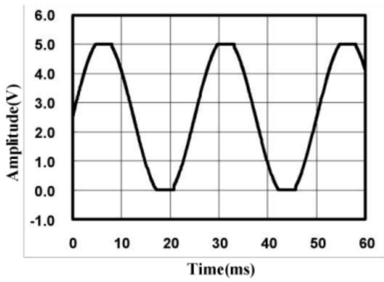


Figure 11 No Phase Inversion with Inputs Greater Than the Power-Supply Voltage

A topology of class AB output stage with common-source transistors is used to achieve ail-to-rail output. For light resistive loads (e.g. 100kΩ), the output voltage can typically swing to within 5mV from the supply rails. With moderate resistive loads (e.g. 10kΩ), the output can typically swing to within 10mV from the supply rails and maintain high open-loop gain.

The maximum output current is a function of total supply voltage. As the supply voltage to the amplifier increases, the output current capability also increases. Attention must be paid to keep the junction temperature of the IC below 150°C when the output is in continuous short-circuit. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.5V beyond either supply, otherwise current will flow through these diodes.

4. CAPACITIVE LOAD AND STABILITY

The XBLW TLV6001/6002/6004 can directly drive 1nF in unity-gain without oscillation. The unity-gain follower (buffer) is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers and this results in ringing or even oscillation. Applications that require greater capacitive drive capability should use an isolation resistor between the output and the capacitive load like the circuit in Figure 12. The isolation resistor RISO and the load capacitor CL form a zero to increase stability. The bigger the RISO resistor value, the more stable VOUT will be. Note that this method results in a loss of gain accuracy because RISO forms a voltage divider with the RL.

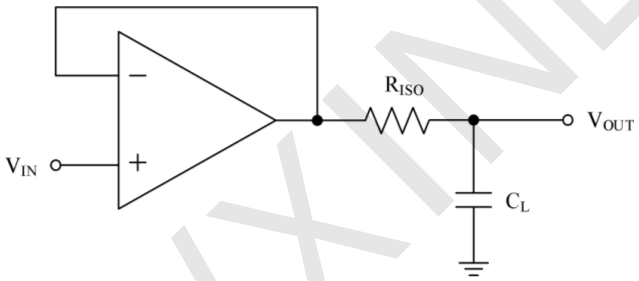


Figure 12 Indirectly Driving Heavy Capacitive Load

An improvement circuit is shown in Figure 13. It provides DC accuracy as well as AC stability. The R_F provides the DC accuracy by connecting the inverting signal with the output. The C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

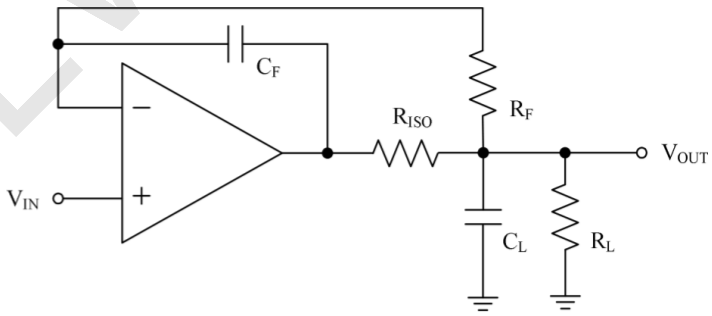


Figure 13 Indirectly Driving Heavy Capacitive Load with DC Accuracy

For no-buffer configuration, there are two others ways to increase the phase margin: (a) by increasing the amplifier's gain, or (b) by placing a capacitor in parallel with the feedback resistor to counteract the parasitic capacitance associated with inverting node.

5. POWER SUPPLY LAYOUT AND BYPASS

The XBLW TLV6001/6002/6004 family operates from either a single +1.8V to +5.5V supply or dual ±0.9V to ±3.0V supplies. For single-supply operation, bypass the power supply V_S with a ceramic capacitor (i.e. 0.01μF to 0.1μF) which should be placed close (within 2mm for good high frequency performance) to the V_S pin. For dual-supply operation, both the V_{S+} and the V_{S-} supplies should be bypassed to ground with separate 0.1μF ceramic capacitors. A bulk capacitor (i.e. 2.2μF or larger tantalum capacitor) within 100mm to provide large, slow currents and better performance. This bulk capacitor can be shared with other analog parts.

Good PC board layout techniques optimize performance by decreasing the amount of stray capacitance at the op - amp's inputs and output. To decrease stray capacitance, minimize trace lengths and widths by placing external components as close to the device as possible. Use surface-mount components whenever possible. For the op-amp, soldering the part to the board directly is strongly recommended. Try to keep the high frequency big current loop area small to minimize the EMI (electromagnetic interfacing).

6. GROUNDING

A ground plane layer is important for the XBLW TLV6001/6002/6004 circuit design. The length of the current path speed currents in an inductive ground return will create an unwanted voltage noise. Broad ground plane areas will reduce the parasitic inductance.

7. INPUT-TO-OUTPUT COUPLING

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

Typical Application Circuits

1. DIFFERENTIAL AMPLIFIER

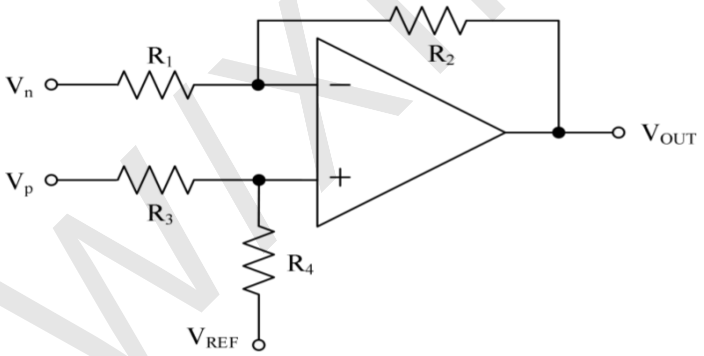
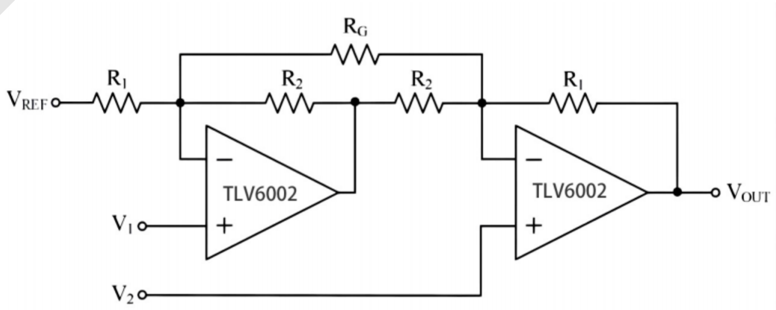


Figure 14 Differential Amplifier

The circuit shown in Figure 14 performs the difference function. If the resistors ratios are equal $R_4/R_3 = R_2/R_1$, then:

$$V_{OUT} = (V_p - V_n) \times R_2/R_1 + V_{REF}$$

2. INSTRUMENTATION AMPLIFIER



$$V_{OUT} = (V_1 - V_2) \times (1 + R_1/R_2 + 2R_1/R_G) + V_{REF}$$

Figure 15 Instrumentation Amplifier

The XBLW TLV6001/6002/6004 family is well suited for conditioning sensor signals in battery-powered applications. Figure 15 shows a two op-amp instrumentation amplifier, using the XBLW TLV6002op-amps. The circuit works well for applications requiring rejection of common-mode noise at higher gains. The reference voltage (V_{REF}) is supplied by a low- impedance source. In single voltage supply applications, the V_{REF} is typically $V_S/2$.

3. BUFFERED CHEMICAL SENSORS

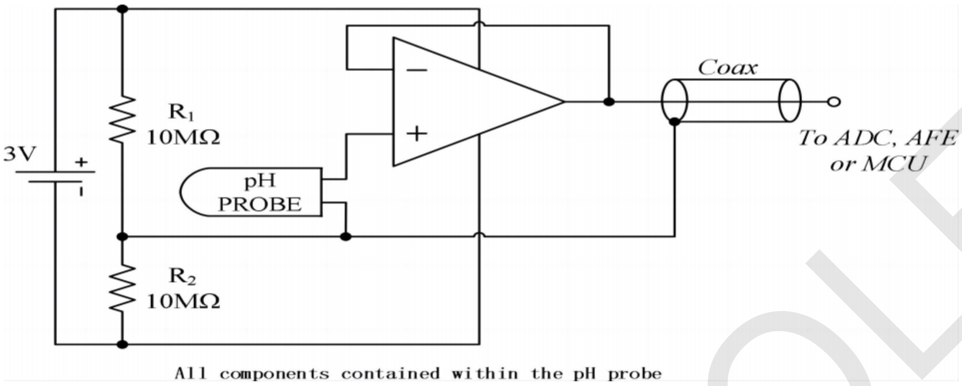
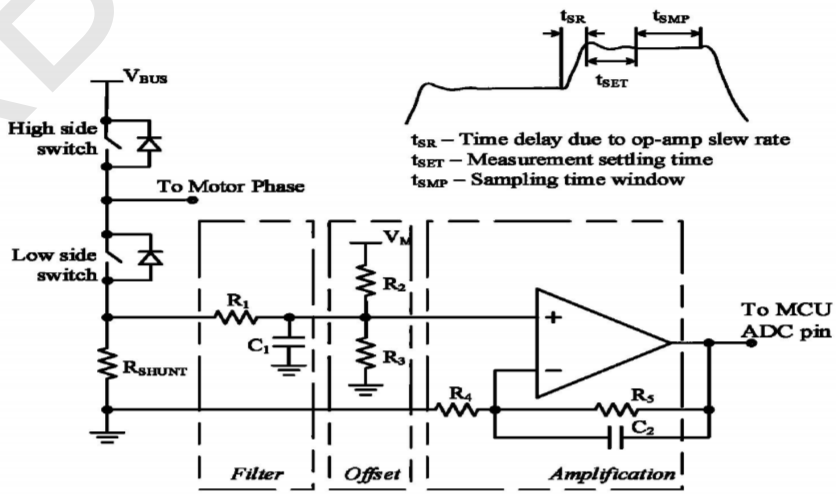


Figure 16 Buffered pH Probe

The XBLW TLV6001/6002/6004 family has input bias current in the pA range. This is ideal in buffering high impedance chemical sensors, such as pH probes. As an example, the circuit in Figure 16 eliminates expansive low-leakage cables that is required to connect a pH probe (general purpose combination pH probes, e.g Corning 476540) to metering ICs such as ADC, AFE and/or MCU. An XBLW TLV6001/6002/6004 op-amp and a lithium battery are housed in the probe assembly. A conventionallow-cost coaxial cable can be used to carry the op-amp's output signal to subsequent ICs for pH reading.

4. SHUNT-BASED CURRENT SENSING AMPLIFIER

The current sensing amplification shown in Figure 8 has a slew rate of 2πfVPP for the output of sine wave signal, and has a slew rate of 2fVPP for the output of triangular wave signal. In most of motor control systems, the PWM frequency is at 10kHz to 20kHz, and one cycle time is 100µs for a 10kHz of PWM frequency. In current shunt monitoring for a motor phase, the phase current is converted to a phase voltage signal for ADC sampling. This sampling voltage signal must be settled before entering the ADC. As the Figure 19 shown, the total settling time of a current shunt monitor circuit includes: the rising edge delay time (tSR) due to the op-amp's slew rate, and the measurement settling time (tSET). For a 3-shunt solution in motor phase current sensing, if the smaller duty cycle of the PWM is defined at 45% (In fact, the phase with minimum PWM duty cycle, such as 5%, is not detected current directly, and it can be calculated from the other two phase currents), and the tSR is required at 20% of a total time window for a phase current monitoring, in case of a 3.3V motor control system(3.3V MCU with 12-bit ADC), the op-amp's slew rate should be more than:



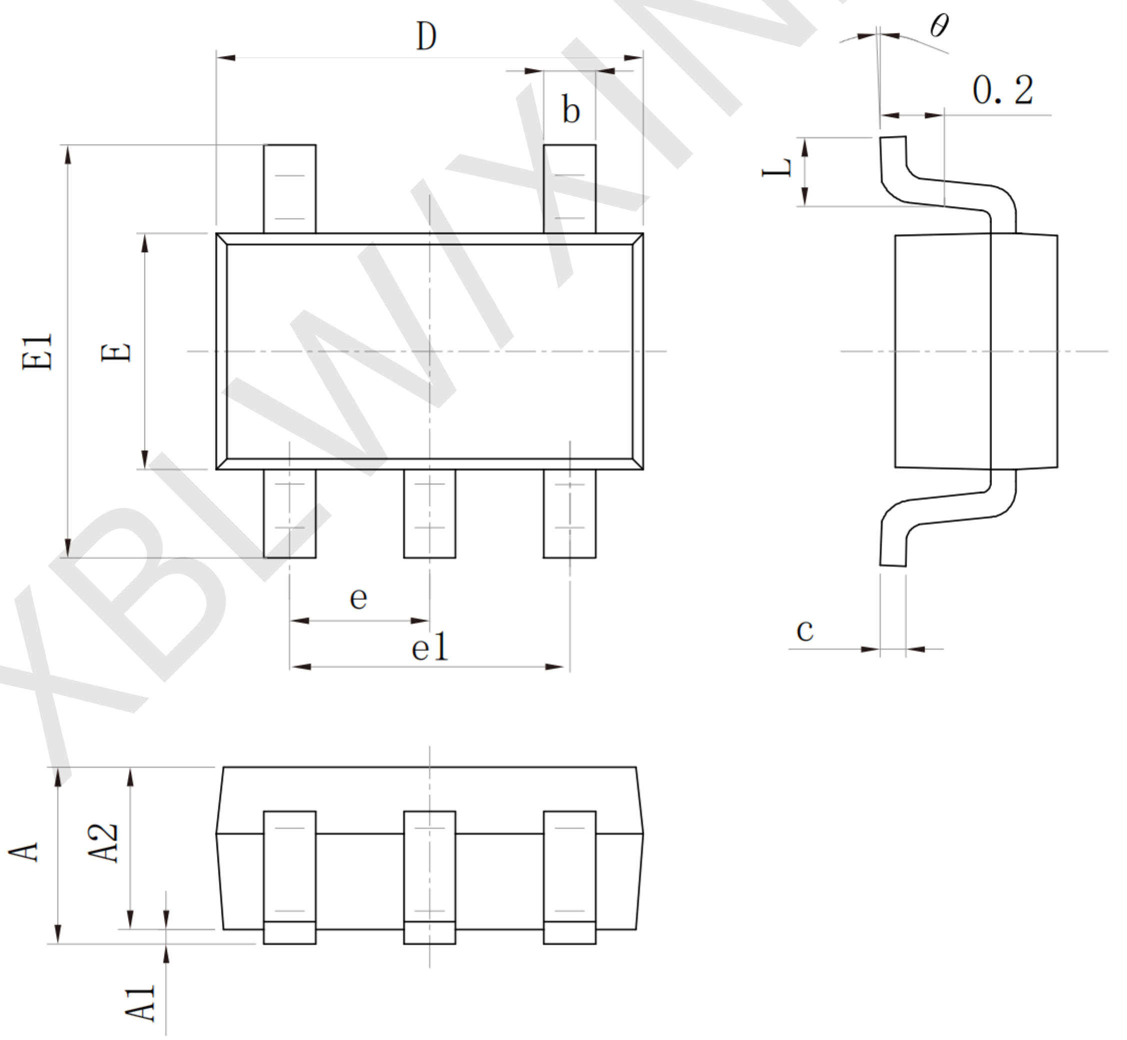
$$3.3V / (100\mu s \times 45\% \times 20\%) = 0.37\ V/\mu s$$

At the same time, the op-amp's bandwidth should be much greater than the PWM frequency, like 10 time at least.

Package Information

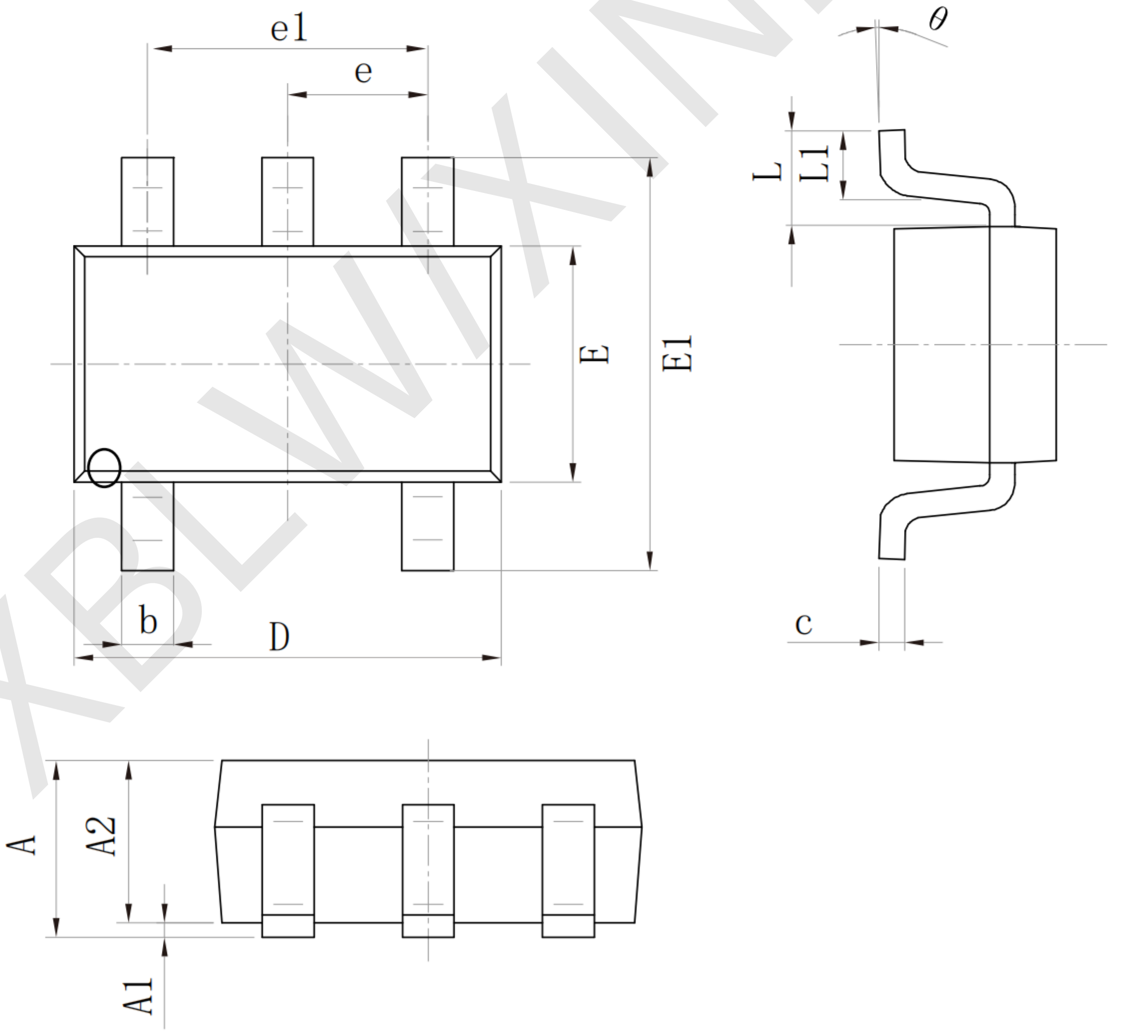
- SOT23-5

SIZE SYMBOL	Dimensions In Millimeters MIN(mm)	MAX(mm)	SIZE SYMBOL	Dimensions In Inches MIN(in)	MAX(in)
A	1.050	1.250	A	0.041	0.049
A1	0.000	0.100	A1	0.000	0.004
A2	1.050	1.150	A2	0.041	0.045
b	0.300	0.500	b	0.012	0.020
c	0.100	0.200	c	0.004	0.008
D	2.820	3.020	D	0.111	0.119
E	1.500	1.700	E	0.059	0.067
E1	2.650	2.950	E1	0.104	0.116
e	0.95(BSC)		e	0.037(BSC)	
e1	1.800	2.000	e1	0.071	0.079
L	0.300	0.600	L	0.012	0.024
θ	0°	8°	θ	0°	8°



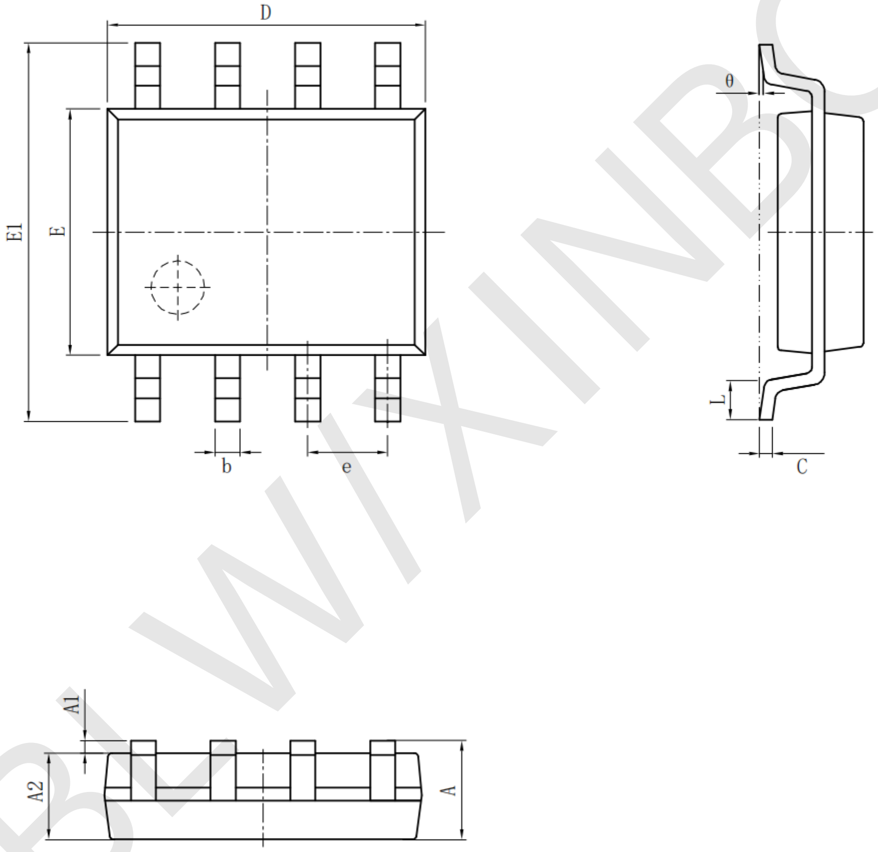
- SC70-5

Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	0.800	1.100	A	0.035	0.043
A1	0.000	0.100	A1	0.000	0.004
A2	0.800	0.900	A2	0.035	0.039
b	0.150	0.350	b	0.006	0.014
C	0.080	0.150	C	0.003	0.006
D	1.850	2.150	D	0.079	0.087
E	1.100	1.400	E	0.045	0.053
E1	1.950	2.200	E1	0.085	0.096
e	0.85(typ)		e	0.026(typ)	
e1	1.200	1.400	e1	0.047	0.055
L	0.42(ref)		L	0.021(ref)	
L1	0.260	0.460	L1	0.010	0.018
θ	0°	8°	θ	0°	8°



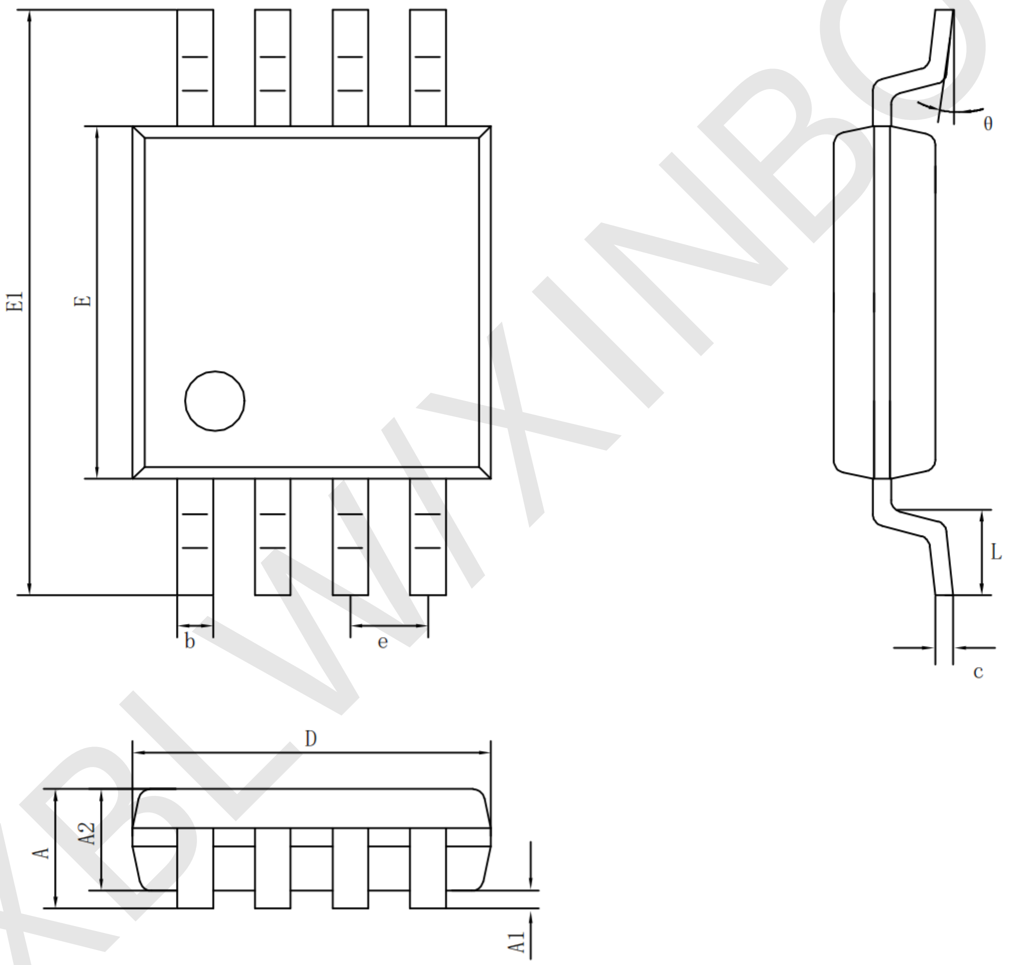
- SOP-8

Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	1.350	1.750	A	0.053	0.069
A1	0.100	0.250	A1	0.004	0.010
A2	1.350	1.550	A2	0.053	0.061
b	0.330	0.510	b	0.013	0.020
c	0.170	0.250	c	0.006	0.010
D	4.700	5.100	D	0.185	0.200
E	3.800	4.000	E	0.150	0.157
E1	5.800	6.200	E1	0.228	0.224
e	1.270(BSC)		e	0.050(BSC)	
L	0.400	1.270	L	0.016	0.050
θ	0°	8°	θ	0°	8°



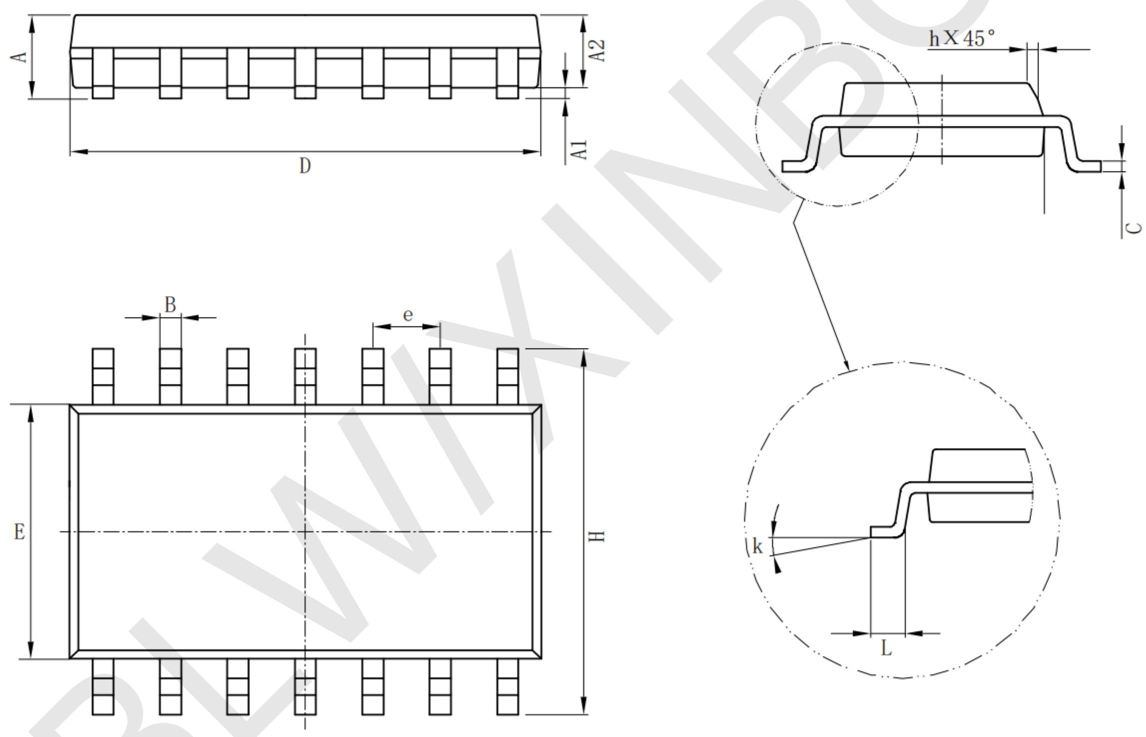
· MSOP-8

Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	0.820	1.100	A	0.320	0.043
A1	0.020	0.150	A1	0.001	0.006
A2	0.750	0.950	A2	0.030	0.037
b	0.250	0.380	b	0.010	0.015
c	0.090	0.230	c	0.004	0.009
D	2.900	3.100	D	0.114	0.122
e	0.65 (BSC)		e	0.026(BSC)	
E	2.900	3.100	E	0.114	0.122
E1	4.750	5.050	E1	0.187	0.199
L	0.400	0.800	L	0.016	0.031
θ	0°	6°	θ	0°	6°



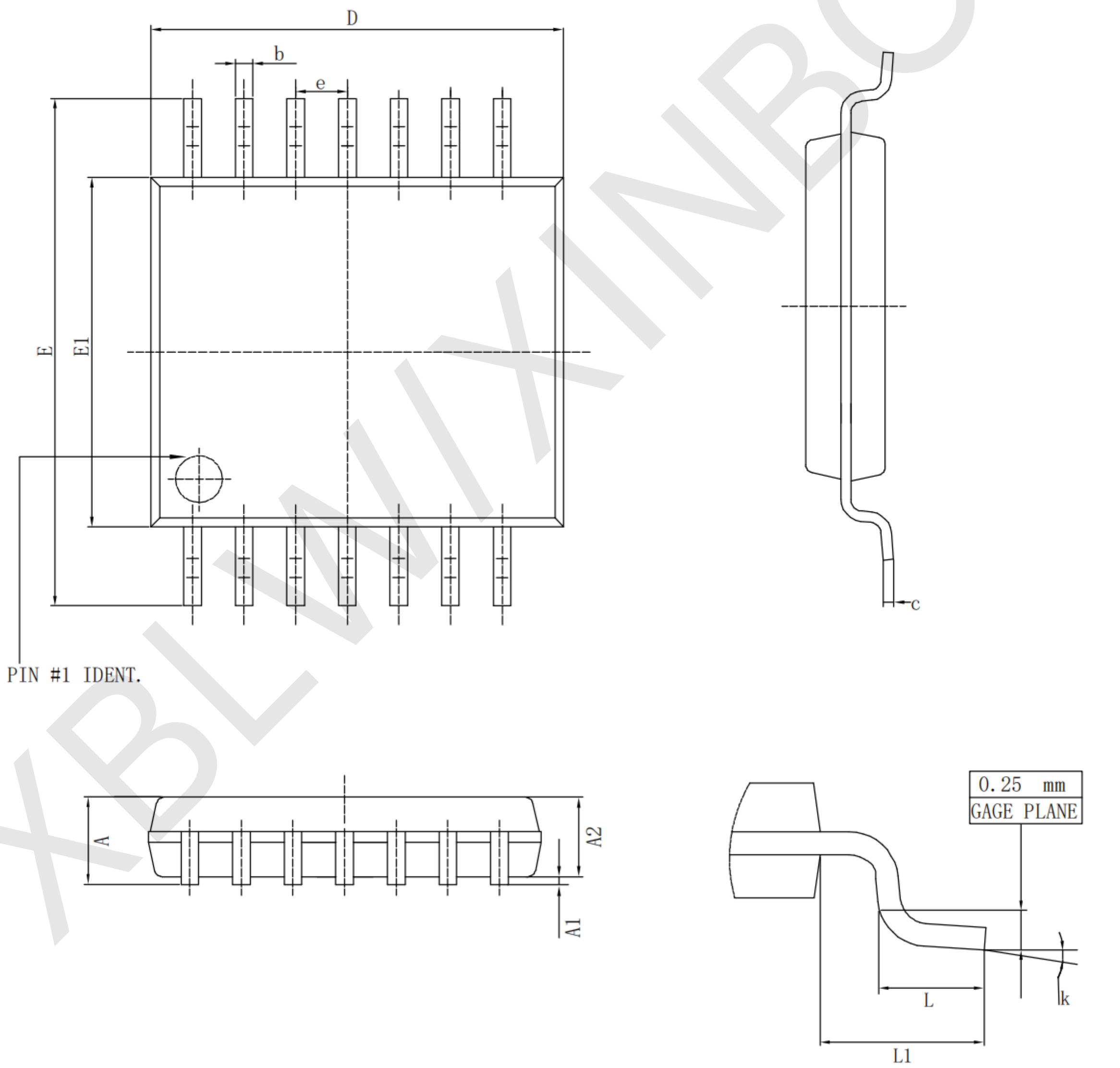
· SOP-14

Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	1.350	1.750	A	0.050	0.068
A1	0.100	0.250	A1	0.004	0.009
A2	1.100	1.650	A2	0.040	0.060
B	0.330	0.510	B	0.010	0.020
C	0.190	0.250	C	0.007	0.009
D	8.550	8.750	D	0.330	0.340
E	3.800	4.000	E	0.150	0.150
e	1.27		e	0.05	
H	5.800	6.200	H	0.220	0.240
h	0.250	0.500	h	0.009	0.020
L	0.400	1.270	L	0.015	0.050
k	8° (max)		k	8° (max)	



· TSSOP-14

Symbol \ Size	Dimensions In Millimeters		Symbol \ Size	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A		1.200	A		0.047
A1	0.050	0.150	A1	0.002	0.006
A2	0.800	1.050	A2	0.031	0.041
b	0.190	0.300	b	0.007	0.012
c	0.090	0.200	c	0.004	0.0089
D	4.900	5.100	D	0.193	0.201
E	6.200	6.600	E	0.244	0.260
E1	4.300	4.500	E1	0.169	0.176
e	0.65		e	0.0256	
L	0.450	0.750	L	0.018	0.030
L1	1.00		L1	0.039	
k	0°	8°	k	0°	8°



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