芯伯乐®
XINBOLE

# Product Specification

## XBLW SN74LS123

Dual Retriggerable Monostable Multivibrator with Reset

WEB | www.xinboleic.com

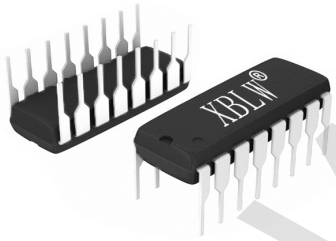
## Description

The SN74LS123 is high-speed Si-gate CMOS devices .
The SN74LS123 is dual retriggerable monostable multivibrators with output pulse width control by three methods:

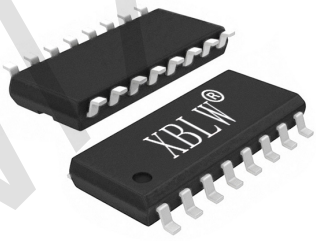
1. The basic pulse is programmed by selection of an external resistor ($R_{EXT}$) and capacitor ($C_{EXT}$).
2. Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ($n\bar{A}$) or the active HIGH-going edge input (nB). By repeating this process, the output pulse period (nQ=HIGH, $n\bar{Q}$=LOW) can be made as long as desired. Alternatively an output delay can be terminated at anytime by a LOW-going edge on input $n\bar{R}D$, which also inhibits the triggering.
3. An internal connection from $n\bar{R}D$ to the input gates makes it possible to trigger the circuit by a HIGH-going signal at input $n\bar{R}D$.

## Features

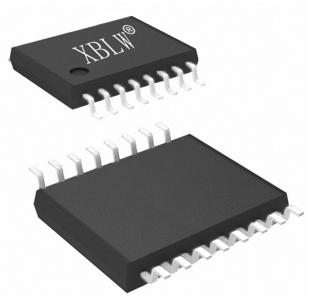
- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100% duty factor
- Direct reset terminates output pulse
- Specified from -20℃ to +85℃
- Packaging information: DIP-16/SOP-16/TSSOP-16



DIP-16



SOP-16



TSSOP-16

## Ordering Information

| Product Model | Package Type | Marking | Packing | Packing Qty |
|---|---|---|---|---|
| XBLW SN74LS123N | DIP-16 | 74LS123N | Tube | 1000Pcs/Box |
| XBLW SN74LS123DTR | SOP-16 | 74LS123 | Tape | 2500Pcs/Reel |
| XBLW SN74LS123TDTR | TSSOP-16 | 74LS123 | Tape | 3000Pcs/Reel |

## Block Diagram

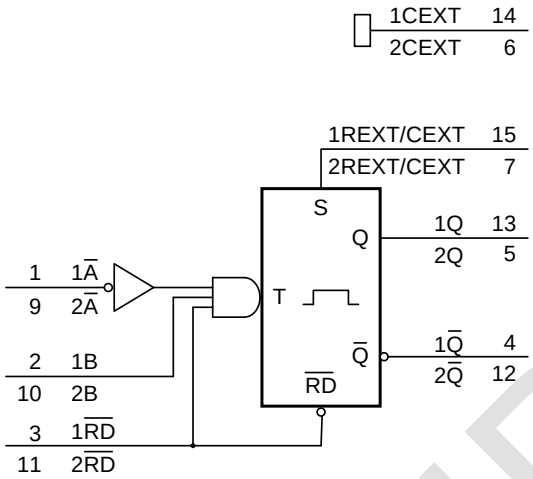



Figure 1. Logic symbol

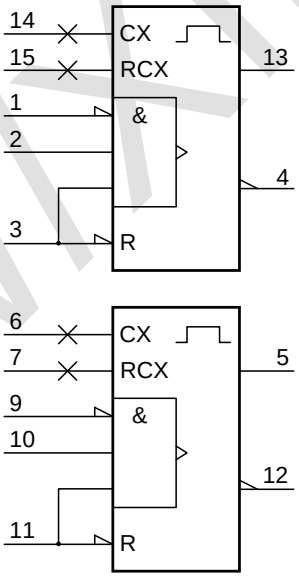



Figure 2. IEC logic symbol

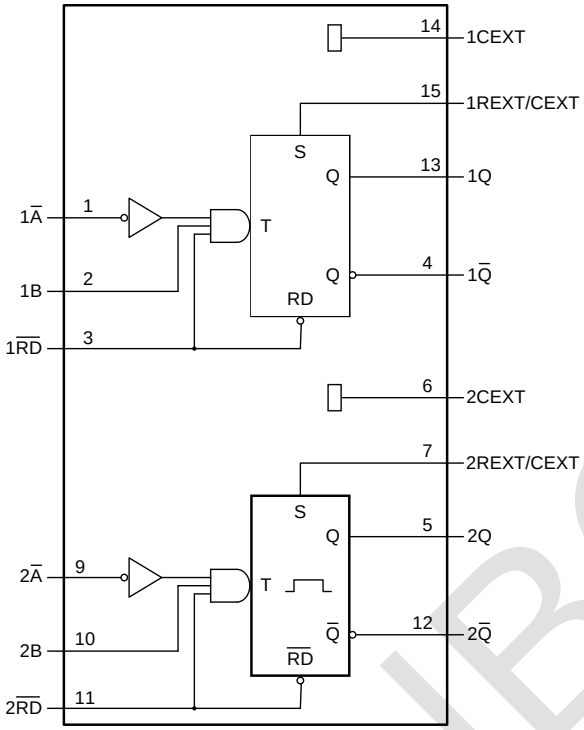



Figure 3. Functional diagram

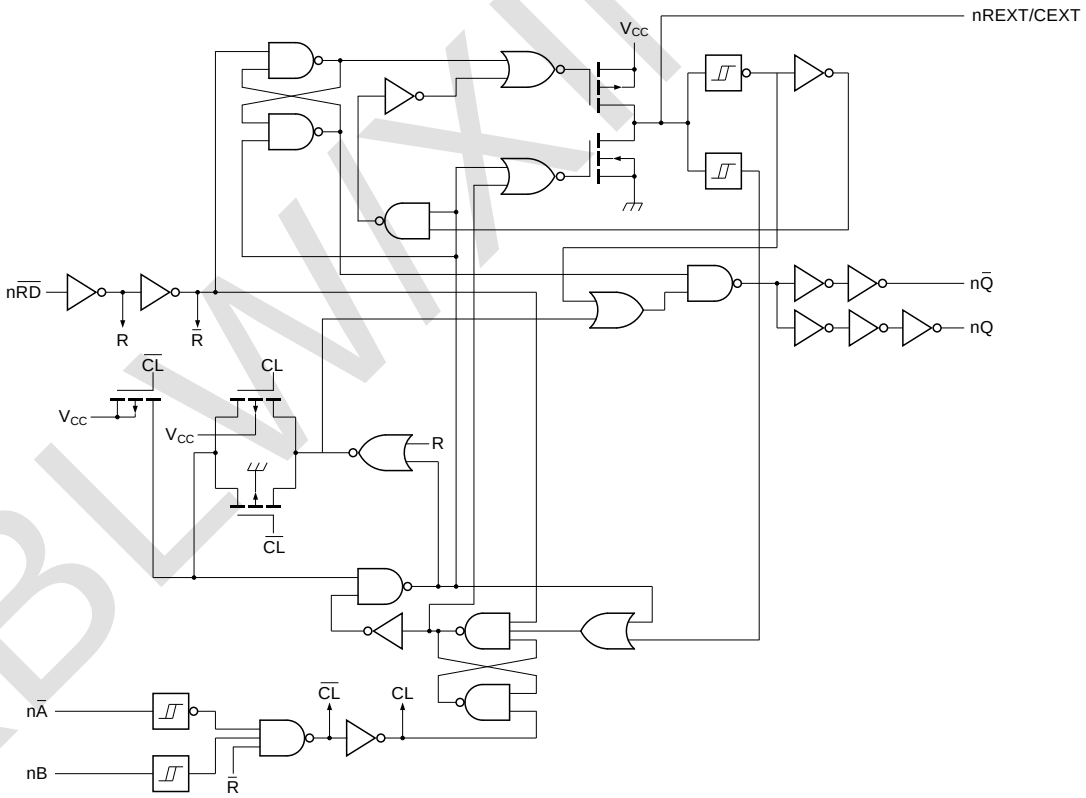
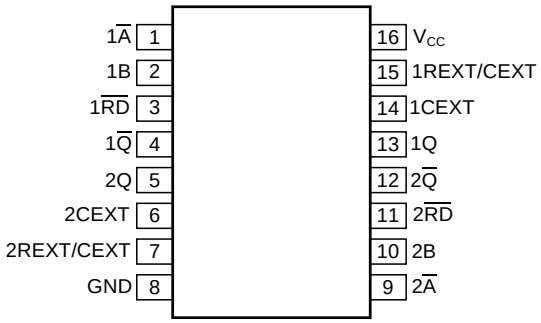



Figure 4. Logic diagram

## Pin Configurations




## Pin Description

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | 1$\overline{A}$ | negative-edge triggered input 1 |
| 2 | 1B | positive-edge triggered input 1 |
| 3 | 1$\overline{RD}$ | direct reset LOW and positive-edge triggered input 1 |
| 4 | 1$\overline{Q}$ | active LOW output 1 |
| 5 | 2Q | active HIGH output 2 |
| 6 | 2CEXT | external capacitor connection 2 |
| 7 | 2REXT/CEXT | external resistor and capacitor connection 2 |
| 8 | GND | ground (0V) |
| 9 | 2$\overline{A}$ | negative-edge triggered input 2 |
| 10 | 2B | positive-edge triggered input 2 |
| 11 | 2$\overline{RD}$ | direct reset LOW and positive-edge triggered input 2 |
| 12 | 2$\overline{Q}$ | active LOW output 2 |
| 13 | 1Q | active HIGH output 1 |
| 14 | 1CEXT | external capacitor connection 1 |
| 15 | 1REXT/CEXT | external resistor and capacitor connection 1 |
| 16 | $V_{CC}$ | supply voltage |

## Function Table

| Input | | | Output | |
|---|---|---|---|---|
| n$\overline{RD}$ | n$\overline{A}$ | nB | nQ | n$\overline{Q}$ |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | ↑ | ⊓ | ⊔ |
| H | ↓ | H | ⊓ | ⊔ |
| ↑ | L | H | ⊓ | ⊔ |

Note:
[1] H=HIGH voltage level; L=LOW voltage level; X=don't care.
[2] ↑=LOW-to-HIGH transition; ↓=HIGH-to-LOW transition.
[3] ⊓ =one HIGH level output pulse; ⊔ =one LOW level output pulse.
[4] If the monostable was triggered before this condition was established, the pulse will continue as programmed.

# Electrical Parameter

## Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

| Parameter | Symbol | Conditions | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| supply voltage | $V_{CC}$ | - | | -0.5 | +7.0 | V |
| input clamping current | $I_{IK}$ | $V_I$ < -0.5V or $V_I$ > $V_{CC}$+0.5V | | - | ±20 | mA |
| output clamping current | $I_{OK}$ | $V_O$ < -0.5V or $V_O$ > $V_{CC}$+0.5V | | - | ±20 | mA |
| output current | $I_O$ | except for pinsnREXT/CEXT; $V_O$= -0.5V to ($V_{CC}$+0.5V) | | - | ±25 | mA |
| supply current | $I_{CC}$ | - | | - | 50 | mA |
| ground current | $I_{GND}$ | - | | - | -50 | mA |
| storage temperature | $T_{stg}$ | - | | -65 | +150 | °C |
| total power dissipation | $P_{tot}$ | - | | - | 500 | mW |
| soldering temperature | $T_L$ | 10s | DIP | 245 | | °C |
| | | | SOP/TSSOP | 260 | | °C |

## Recommended Operating Conditions

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| supply voltage | $V_{CC}$ | - | | 2.0 | 5.0 | 6.0 | V |
| input voltage | $V_I$ | - | | 0 | - | $V_{CC}$ | V |
| output voltage | $V_O$ | - | | 0 | - | $V_{CC}$ | V |
| input transition rise and fall rate | △t/△V | nRD input | $V_{CC}$=2.0V | - | - | 625 | ns/V |
| | | | $V_{CC}$=4.5V | - | 1.67 | 139 | ns/V |
| | | | $V_{CC}$=6.0V | - | - | 83 | ns/V |
| ambient temperature | $T_{amb}$ | - | | -20 | - | +85 | °C |

# Electrical Characteristics

## DC Characteristics 1

($T_{amb}$=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| HIGH-level input voltage | $V_{IH}$ | $V_{CC}$=2.0V | | 1.5 | 1.2 | - | V |
| | | $V_{CC}$=4.5V | | 3.15 | 2.4 | - | V |
| | | $V_{CC}$=6.0V | | 4.2 | 3.2 | - | V |
| LOW-level input voltage | $V_{IL}$ | $V_{CC}$=2.0V | | - | 0.8 | 0.5 | V |
| | | $V_{CC}$=4.5V | | - | 2.1 | 1.35 | V |
| | | $V_{CC}$=6.0V | | - | 2.8 | 1.8 | V |
| HIGH-level output voltage | $V_{OH}$ | $V_I$=$V_{IH}$ or $V_{IL}$ | $I_O$=-20uA; $V_{CC}$=2.0V | 1.9 | 2.0 | - | V |
| | | | $I_O$=-20uA; $V_{CC}$=4.5V | 4.4 | 4.5 | - | V |
| | | | $I_O$=-20uA; $V_{CC}$=6.0V | 5.9 | 6.0 | - | V |
| | | | $I_O$=-4mA; $V_{CC}$=4.5V | 3.98 | 4.32 | - | V |
| | | | $I_O$=-5.2mA; $V_{CC}$=6.0V | 5.48 | 5.81 | - | V |
| LOW-level output voltage | $V_{OL}$ | $V_I$=$V_{IH}$ or $V_{IL}$ | $I_O$=20uA; $V_{CC}$=2.0V | - | 0 | 0.1 | V |
| | | | $I_O$=20uA; $V_{CC}$=4.5V | - | 0 | 0.1 | V |
| | | | $I_O$=20uA; $V_{CC}$=6.0V | - | 0 | 0.1 | V |
| | | | $I_O$=4mA; $V_{CC}$=4.5V | - | 0.15 | 0.26 | V |
| | | | $I_O$=5.2mA; $V_{CC}$=6.0V | - | 0.16 | 0.26 | V |
| input leakage current | $I_I$ | $V_I$=$V_{CC}$ or GND; $V_{CC}$=6.0V | | - | - | ±1.0 | uA |
| supply current | $I_{CC}$ | $V_I$=$V_{CC}$ or GND; $I_O$=0A; $V_{CC}$=6.0V | | - | - | 8.0 | uA |
| input capacitance | $C_I$ | - | | - | 3.5 | - | pF |

## DC Characteristics 2

($T_{amb}$=-20℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| HIGH-level input voltage | $V_{IH}$ | $V_{CC}$=2.0V | | 1.5 | - | - | V |
| | | $V_{CC}$=4.5V | | 3.15 | - | - | V |
| | | $V_{CC}$=6.0V | | 4.2 | - | - | V |
| LOW-level input voltage | $V_{IL}$ | $V_{CC}$=2.0V | | - | - | 0.5 | V |
| | | $V_{CC}$=4.5V | | - | - | 1.35 | V |
| | | $V_{CC}$=6.0V | | - | - | 1.8 | V |
| HIGH-level output voltage | $V_{OH}$ | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_O$=-20uA; $V_{CC}$=2.0V | 1.9 | - | - | V |
| | | | $I_O$=-20uA; $V_{CC}$=4.5V | 4.4 | - | - | V |
| | | | $I_O$=-20uA; $V_{CC}$=6.0V | 5.9 | - | - | V |
| | | | $I_O$=-4mA; $V_{CC}$=4.5V | 3.84 | - | - | V |
| | | | $I_O$=-5.2mA; $V_{CC}$=6.0V | 5.34 | - | - | V |
| LOW-level output voltage | $V_{OL}$ | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_O$=20uA; $V_{CC}$=2.0V | - | - | 0.1 | V |
| | | | $I_O$=20uA; $V_{CC}$=4.5V | - | - | 0.1 | V |
| | | | $I_O$=20uA; $V_{CC}$=6.0V | - | - | 0.1 | V |
| | | | $I_O$=4mA; $V_{CC}$=4.5V | - | - | 0.33 | V |
| | | | $I_O$=5.2mA; $V_{CC}$=6.0V | - | - | 0.33 | V |
| input leakage current | $I_I$ | $V_I$=$V_{CC}$ or GND; $V_{CC}$=6.0V | | - | - | ±1.0 | uA |
| supply current | $I_{CC}$ | $V_I$=$V_{CC}$ or GND; $I_O$=0A; $V_{CC}$=6.0V | | - | - | 80 | uA |

**AC Characteristics 1**

($T_{amb}$=25°C, voltages are referenced to GND (ground=0V); $C_L$=50pF, unless otherwise specified.)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| propagation delay | $t_{pd}$ | $n\overline{RD}$, $n\overline{A}$, $n\overline{B}$ to nQ or $n\overline{Q}$; $C_{EXT}$=0pF; $R_{EXT}$=5kΩ; see Figure 6[1] | $V_{CC}$=2.0V | - | 83 | 255 | ns |
| | | | $V_{CC}$=4.5V | - | 30 | 51 | ns |
| | | | $V_{CC}$=5.0V; $C_L$=15pF | - | 26 | - | ns |
| | | | $V_{CC}$=6.0V | - | 24 | 43 | ns |
| | | $n\overline{RD}$(reset) to nQ or $n\overline{Q}$; $C_{EXT}$=0pF; $R_{EXT}$=5kΩ; see Figure 6 | $V_{CC}$=2.0V | - | 66 | 215 | ns |
| | | | $V_{CC}$=4.5V | - | 25 | 43 | ns |
| | | | $V_{CC}$=5.0V; $C_L$=15pF | - | 20 | - | ns |
| | | | $V_{CC}$=6.0V | - | 19 | 37 | ns |
| transition time | $t_t$ | see Figure 6[1] | $V_{CC}$=2.0V | - | 19 | 75 | ns |
| | | | $V_{CC}$=4.5V | - | 7 | 15 | ns |
| | | | $V_{CC}$=6.0V | - | 6 | 13 | ns |
| pulse width | $t_W$ | $n\overline{A}$ LOW; see Figure 7 | $V_{CC}$=2.0V | 100 | 8 | - | ns |
| | | | $V_{CC}$=4.5V | 20 | 3 | - | ns |
| | | | $V_{CC}$=6.0V | 17 | 2 | - | ns |
| | | nB HIGH; see Figure 7 | $V_{CC}$=2.0V | 100 | 17 | - | ns |
| | | | $V_{CC}$=4.5V | 20 | 6 | - | ns |
| | | | $V_{CC}$=6.0V | 17 | 5 | - | ns |
| | | $n\overline{RD}$ LOW; see Figure 8 | $V_{CC}$=2.0V | 100 | 14 | - | ns |
| | | | $V_{CC}$=4.5V | 20 | 5 | - | ns |
| | | | $V_{CC}$=6.0V | 17 | 4 | - | ns |
| | | nQ HIGH and $n\overline{Q}$ LOW; $V_{CC}$=5.0V; see Figure 7, 8[2] | $C_{EXT}$=100nF; $R_{EXT}$=10kΩ | - | 450 | - | us |
| | | | $C_{EXT}$=0pF; $R_{EXT}$=5kΩ | - | 75 | - | ns |
| retrigger time | $t_{rtrig}$ | $n\overline{A}$, nB; $C_{EXT}$=0pF; $R_{EXT}$=5kΩ; $V_{CC}$=5.0V; see Figure 7[3][4] | | - | 110 | - | ns |
| external timing resistor | $R_{EXT}$ | see Figure 7 | $V_{CC}$=2.0V | 10 | - | 1000 | kΩ |
| | | | $V_{CC}$=5.0V | 2 | - | 1000 | kΩ |
| external timing capacitor | $C_{EXT}$ | $V_{CC}$=5.0V; see Figure 9[4] | | - | - | - | pF |
| power dissipation capacitance | $C_{PD}$ | per monostable; $V_I$=GND to $V_{CC}$[5] | | - | 54 | - | pF |

Note:
[1] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$; $t_t$ is the same as $t_{THL}$ and $t_{TLH}$.
[2] For other $R_{EXT}$ and $C_{EXT}$ combinations see Figure 9. If $C_{EXT}$>10nF, the next formula is valid. $t_W=K\times R_{EXT}\times C_{EXT}$, where:$t_W$=typical output pulse width inns; $R_{EXT}$=external resistor inkΩ; $C_{EXT}$=external capacitor in pF; K=constant = 0.45 for $V_{CC}$=5.0V and 0.55 for $V_{CC}$=2.0V.The inherent test jig and pin capacitance at pins 15 and 7 (nREXT/CEXT) is approximately 7pF.
[3] The time toretrigger the monostable multivibrator depends on the values of $R_{EXT}$ and $C_{EXT}$. The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time. If $C_{EXT}$>10pF, the next formula (at $V_{CC}$=5.0V) for the setup time of aretrigger pulse is valid:$t_{rtrig}=30+0.19\times R_{EXT}\times C_{EXT}^{0.9}+13\times R_{EXT}^{1.05}$, where: $t_{rtrig}$=retrigger time inns;$C_{EXT}$=external capacitor in pF; $R_{EXT}$=external resistor inkΩ.
The inherent test jig and pin capacitance at pins 15 and 7 (nREXT/CEXT) is 7pF.
[4] When the device is powered-up, initiate the device via areset pulse, when $C_{EXT}$<50pF. [5] $C_{PD}$ isused to determine the dynamic power dissipation ($P_D$ in uW).$P_D=C_{PD}\times V_{CC}^2\times f_i+\sum(C_L\times V_{CC}^2\times f_o)+0.75\times C_{EXT}\times V_{CC}^2\times f_o+D\times 16\times V_{CC}$ where:$f_i$=input frequency in MHz; $f_o$=output frequency in MHz; D=duty factor in %; $C_L$=output load capacitance in pF;$V_{CC}$=supply voltage in V;$C_{EXT}$=timing capacitance in pF; $\sum(C_L\times V_{CC}^2\times f_o)$=sum ofoutputs.

**AC Characteristics 2**

($T_{amb}$=-20°C to +85°C, GND=0V; $C_L$=50pF, unless otherwise specified.)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| propagation delay | $t_{pd}$ | $n\bar{R}D$, $n\bar{A}$, nB to nQ or $n\bar{Q}$; $C_{EXT}$=0pF; $R_{EXT}$=5kΩ; see Figure 6[1] | $V_{CC}$=2.0V | - | - | 320 | ns |
| | | | $V_{CC}$=4.5V | - | - | 64 | ns |
| | | | $V_{CC}$=6.0V | - | - | 54 | ns |
| | | $n\bar{R}D$(reset) to nQ or $n\bar{Q}$; $C_{EXT}$=0pF; $R_{EXT}$=5kΩ; see Figure 6 | $V_{CC}$=2.0V | - | - | 270 | ns |
| | | | $V_{CC}$=4.5V | - | - | 54 | ns |
| | | | $V_{CC}$=6.0V | - | - | 46 | ns |
| transition time | $t_t$ | see Figure 6[1] | $V_{CC}$=2.0V | - | - | 95 | ns |
| | | | $V_{CC}$=4.5V | - | - | 19 | ns |
| | | | $V_{CC}$=6.0V | - | - | 16 | ns |
| pulse width | $t_W$ | $n\bar{A}$ LOW; see Figure 7 | $V_{CC}$=2.0V | 125 | - | - | ns |
| | | | $V_{CC}$=4.5V | 25 | - | - | ns |
| | | | $V_{CC}$=6.0V | 21 | - | - | ns |
| | | nB HIGH; see Figure 7 | $V_{CC}$=2.0V | 125 | - | - | ns |
| | | | $V_{CC}$=4.5V | 25 | - | - | ns |
| | | | $V_{CC}$=6.0V | 21 | - | - | ns |
| | | $n\bar{R}D$ LOW; see Figure 8 | $V_{CC}$=2.0V | 125 | - | - | ns |
| | | | $V_{CC}$=4.5V | 25 | - | - | ns |
| | | | $V_{CC}$=6.0V | 21 | - | - | ns |

Note:
[1] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$; $t_t$ is the same as $t_{THL}$ and $t_{TLH}$.

## Testing Circuit

### AC Testing Circuit

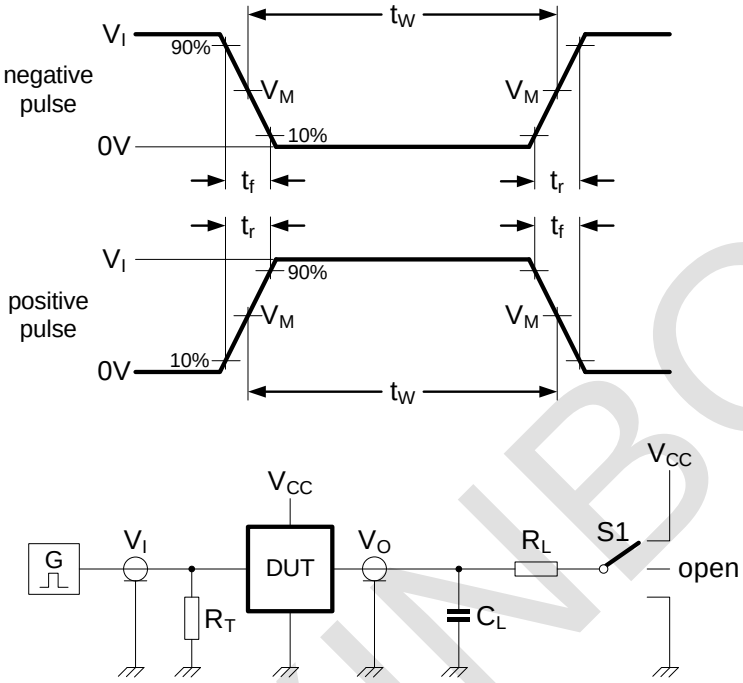






Figure 5. Test circuit for measuring switching times

Definitions for test circuit: $R_L$=Load resistance.

$C_L$=Load capacitance including jig and probe capacitance.

$R_T$=Termination resistance should be equal to the output impedance $Z_o$ of the pulse generator.

S1=Testselection switch.

**AC Testing Waveforms**

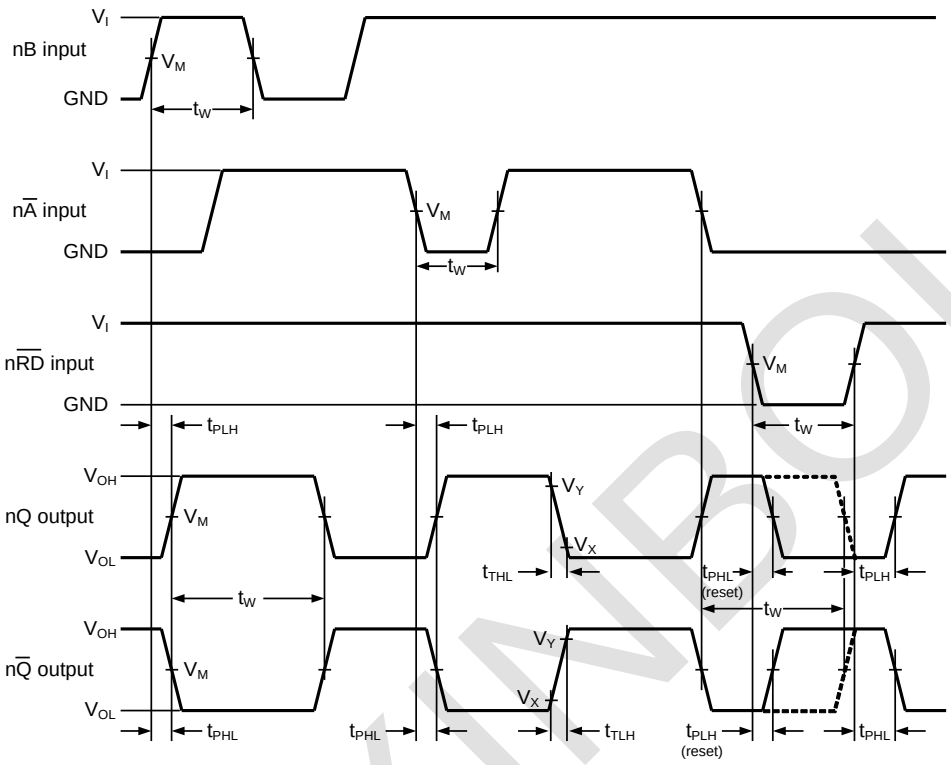



Figure 6. Propagation delays from inputs (nA̅, nB, nR̅D̅) to outputs (nQ, nQ̅) and output transition times

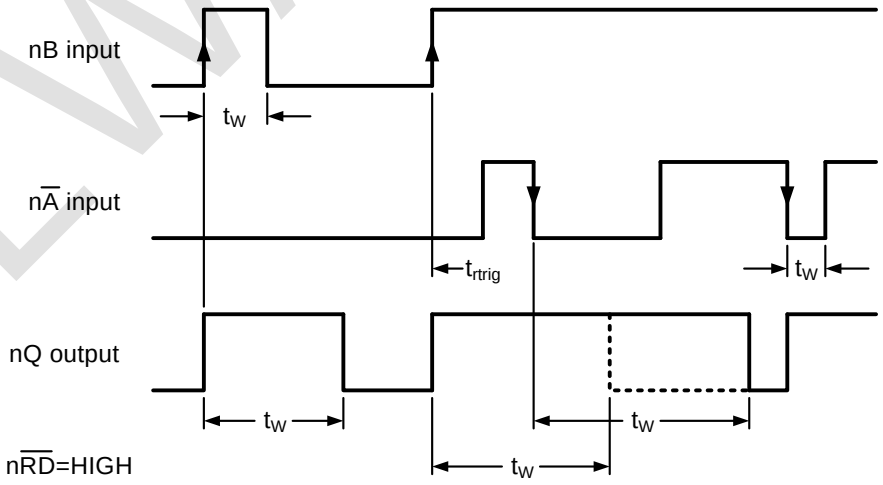



Figure 7. Output pulse control using retrigger pulse

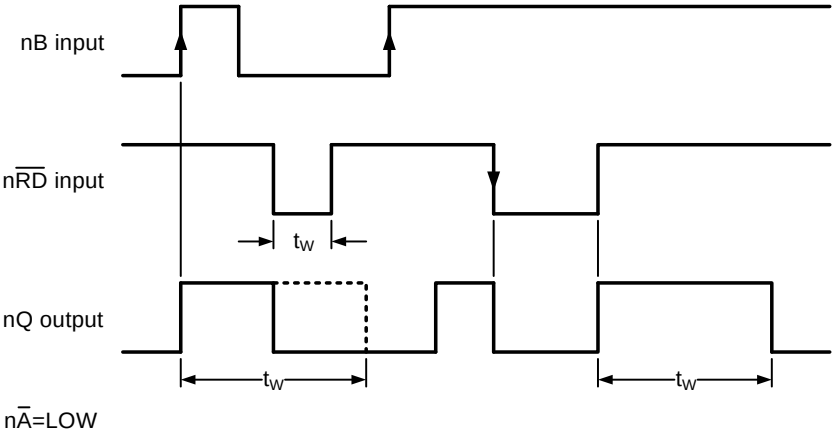
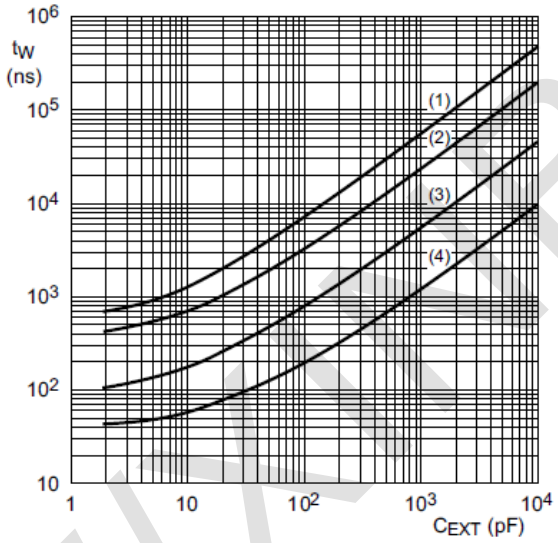



Figure 8. Output pulse control using reset input nRD




$V_{CC}$=5.0V; $T_{amb}$=25℃.

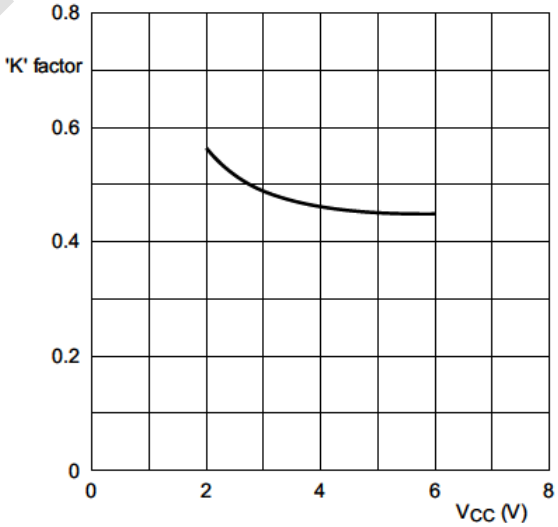
(1) $R_{EXT}$=100kΩ

(2) $R_{EXT}$=50kΩ

(3) $R_{EXT}$=10kΩ

(4) $R_{EXT}$=2kΩ

Figure 9.Typical output pulse width as a function of the external capacitor value




$C_{EXT}$=10nF; $R_{EXT}$=10kΩ to 100kΩ.$T_{amb}$=25℃.

Figure 10. SN74LS123 typical 'K' factor as function of $V_{CC}$

**Measurement Points**

| Type | Input | Output |
|---|---|---|
| | $V_M$ | $V_M$ |
| SN74LS123 | 0.5×$V_{CC}$ | 0.5×$V_{CC}$ |

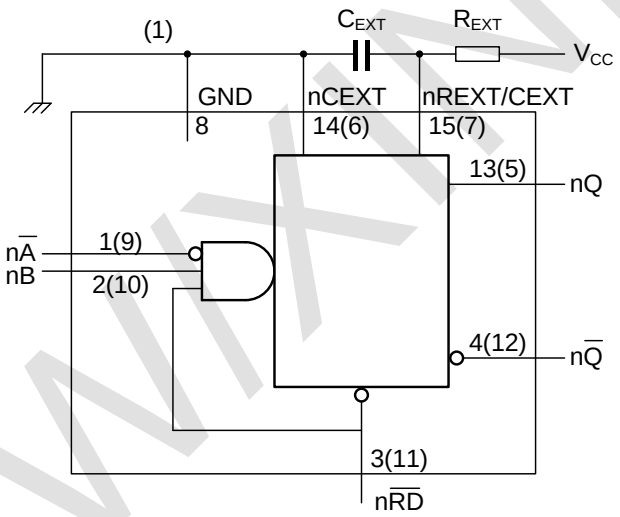
**Test Data**

| Type | Input | | Load | | S1 position |
|---|---|---|---|---|---|
| | $V_I$ | $t_r$ ,$t_f$ | $C_L$ | $R_L$ | $t_{PHL}$, $t_{PLH}$ |
| SN74LS123 | $V_{CC}$ | 6ns | 15pF, 50pF | 1kΩ | open |

## Typical Application Circuit And Application Note

### Timing component connections

The basic output pulse width is essentially determined by the values of the external timing componentsR$_{EXT}$ and C$_{EXT}$.




(1) For minimum noise generation it is recommended to ground pins 6 (2C$_{EXT}$) and 14 (1C$_{EXT}$) externally topin 8 (GND).

Figure 11. Timing component connections

**Power-up considerations**

When the monostable is powered-up it may produce an output pulse, with a pulse width defined by the values of $R_{EXT}$ and $C_{EXT}$. This output pulse can be eliminated using the circuit shown in Figure 12.

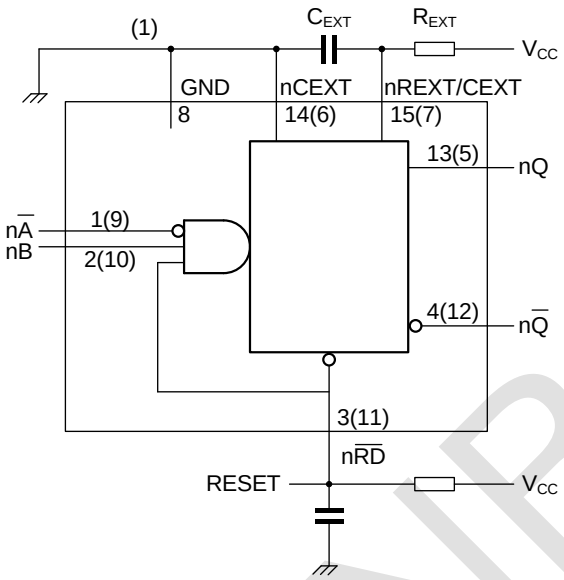



Figure 12. Power-up output pulse elimination circuit

**Power-down considerations**

A large capacitor $C_{EXT}$ may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of $V_{CC}$ to zero occurs, the monostable may sustain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode ($D_{EXT}$) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in Figure 13.

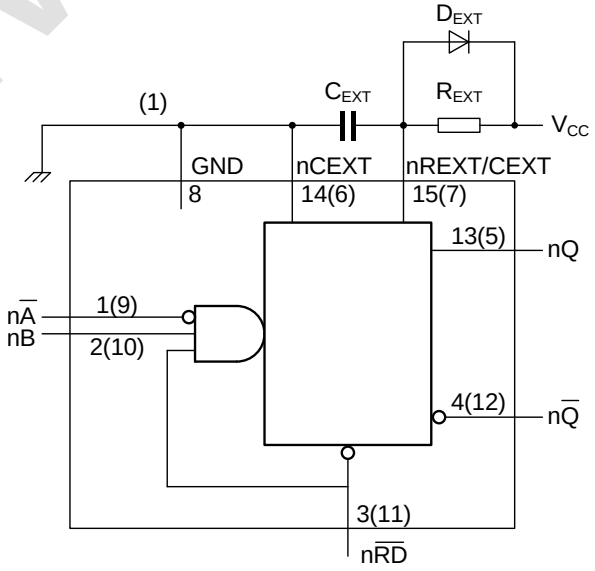
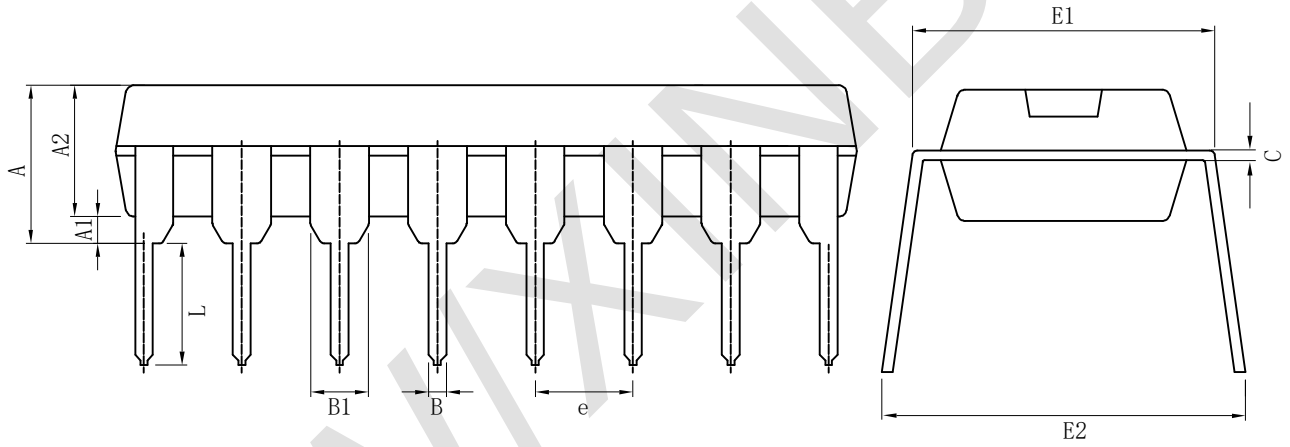


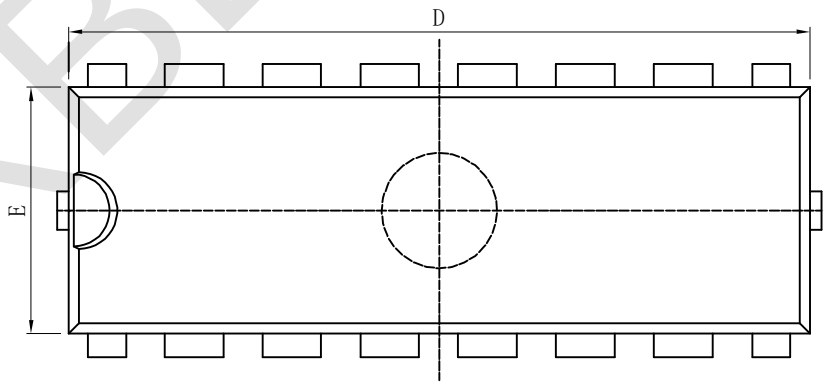

Figure 13. Power-down protection circuit

## Package Information

· DIP-16

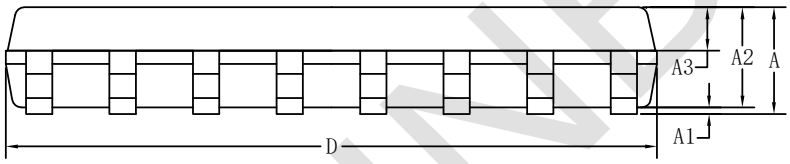
| Size / Symbol | Dimensions In Millimeters | | Size / Symbol | Dimensions In Inches | |
|---|---|---|---|---|---|
| | Min( mm) | Max( mm) | | Min( in) | Max( in) |
| A | 3.710 | 4.310 | A | 0.146 | 0.170 |
| A1 | 0.510 | | A1 | 0.020 | |
| A2 | 3.200 | 3.600 | A2 | 0.126 | 0.142 |
| B | 0.380 | 0.570 | B | 0.015 | 0.022 |
| B1 | 1.524(BSC) | | B1 | 0.060(BSC) | |
| C | 0.204 | 0.360 | C | 0.008 | 0.014 |
| D | 18.80 | 19.20 | D | 0.740 | 0.756 |
| E | 6.200 | 6.600 | E | 0.244 | 0.260 |
| E1 | 7.320 | 7.920 | E1 | 0.288 | 0.312 |
| e | 2.540(BSC) | | e | 0.100(BSC) | |
| L | 3.000 | 3.600 | L | 0.118 | 0.142 |
| E2 | 8.400 | 9.000 | E2 | 0.331 | 0.354 |

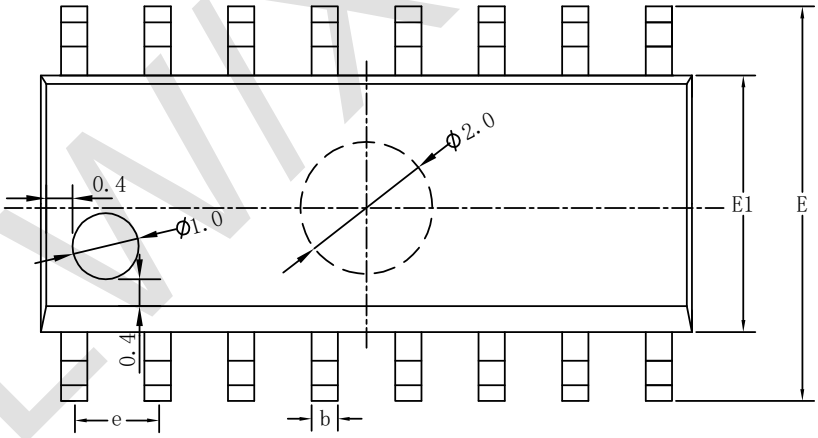


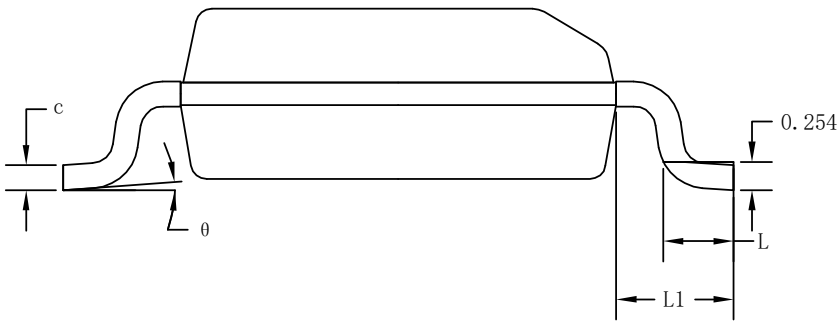



· SOP-16

| Size / Symbol | Dimensions In Millimeters | | | Size / Symbol | Dimensions In Inches | | |
|---|---|---|---|---|---|---|---|
| | Min(mm) | Nom(mm) | Max(mm) | | Min(in) | Nom(in) | Max(in) |
| A | 1.500 | 1.600 | 1.700 | A | 0.059 | 0.063 | 0.067 |
| A1 | 0.100 | 0.150 | 0.250 | A1 | 0.004 | 0.006 | 0.010 |
| A2 | 1.400 | 1.450 | 1.500 | A2 | 0.055 | 0.057 | 0.059 |
| A3 | 0.600 | 0.650 | 0.700 | A3 | 0.024 | 0.026 | 0.028 |
| b | 0.300 | 0.400 | 0.500 | b | 0.012 | 0.016 | 0.020 |
| c | 0.150 | 0.200 | 0.250 | c | 0.006 | 0.008 | 0.010 |
| D | 9.800 | 9.900 | 10.00 | D | 0.386 | 0.390 | 0.394 |
| E | 5.800 | 6.000 | 6.200 | E | 0.228 | 0.236 | 0.244 |
| E1 | 3.850 | 3.900 | 3.950 | E1 | 0.152 | 0.154 | 0.156 |
| e | 1.27(BSC) | | | e | 0.050(BSC) | | |
| L | 0.500 | 0.600 | 0.700 | L | 0.020 | 0.024 | 0.028 |
| L1 | 1.05(BSC) | | | L1 | 0.041(BSC) | | |
| θ | 0° | 4° | 8° | θ | 0° | 4° | 8° |

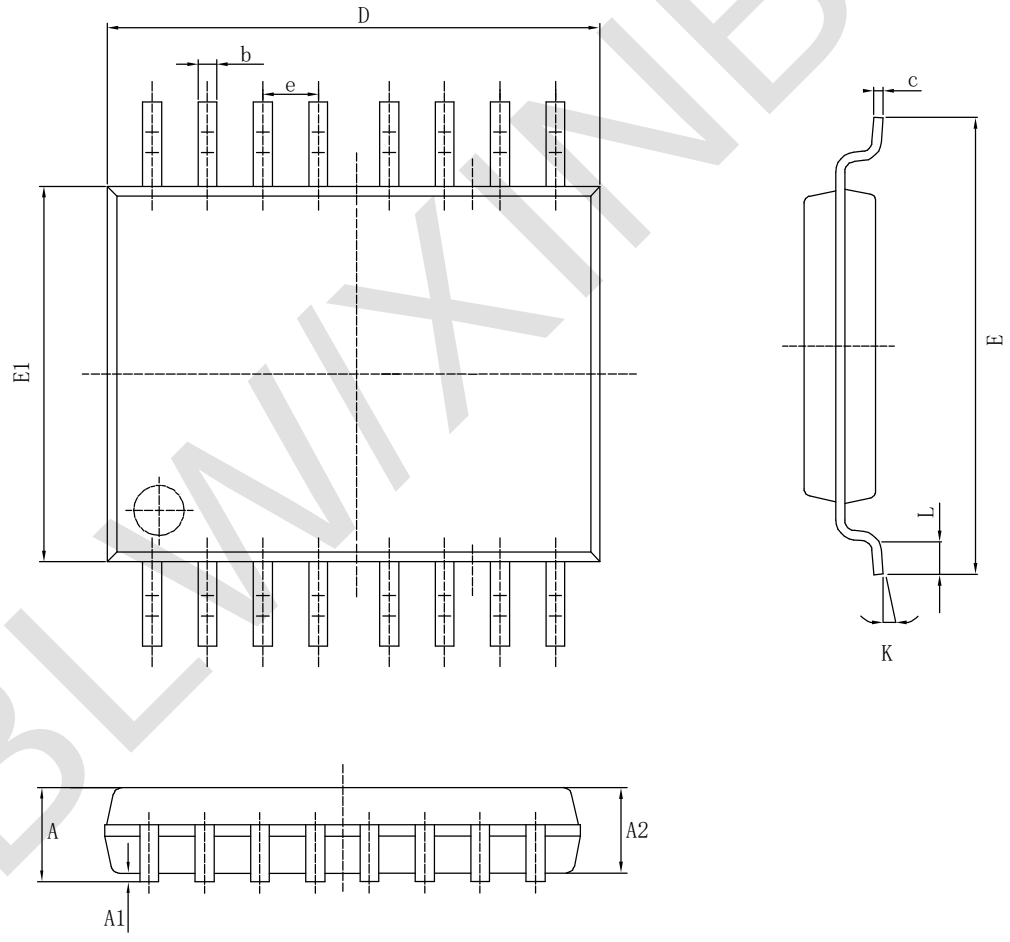


## · TSSOP-16

| Size / Symbol | Dimensions In Millimeters | | Size / Symbol | Dimensions In Inches | |
|---|---|---|---|---|---|
| | Min(mm) | Max(mm) | | Min(in) | Max(in) |
| A | | 1.200 | A | | 0.047 |
| A1 | 0.050 | 0.150 | A1 | 0.002 | 0.006 |
| A2 | 0.800 | 1.050 | A2 | 0.031 | 0.041 |
| b | 0.190 | 0.300 | b | 0.007 | 0.012 |
| c | 0.090 | 0.200 | c | 0.004 | 0.0089 |
| D | 4.900 | 5.100 | D | 0.193 | 0.201 |
| E | 6.200 | 6.600 | E | 0.244 | 0.260 |
| E1 | 4.300 | 4.480 | E1 | 0.169 | 0.176 |
| e | 0.65(BSC) | | e | 0.0256(BSC) | |
| K | 0° | 8° | K | 0° | 8° |
| L | 0.450 | 0.750 | L | 0.018 | 0.030 |



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