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XINBOLE

Product Specification

XBLW LMV721-722-724

10MHz, Rail-to-Rail Operational Amplifiers

WEB | www.xinboleic.com

RoHS

Description

The LMV721 (single), LMV722 (dual) and LMV724 (quad) are low noise, low voltage, and micro power operational amplifiers. With an excellent bandwidth of 10MHz, a slew rate of 9V/μs, and a quiescent current of 1000μA per amplifier at 5V, the LMV72X family can be designed into a wide range of applications.

The LMV72X op-amps are designed to provide optimal performance in low voltage and low noise systems. The input common-mode voltage range includes ground, and the maximum input offset voltage are 3.5mV. These parts provide rail-to-rail output swing into heavy loads. The LMV72X family is specified for single or dual power supplies of +2.5V to +5.5V.

The LMV721 is available in SOT-23-5 and SC70-5 packages.
The LMV722 is available in SOP-8, MSOP-8 and TSSOP-8 packages.
The LMV724 is available in SOP-14 and TSSOP-14 packages.

Feature:

- High Slew Rate: 9V/ μs
- Wide Bandwidth: 10MHz
- Low Power: 1000μA per Amplifier Supply Current
- Settling Time to 0.1% with 2V Step: 0.25 μs
- Low Noise: 20 nV/ Hz@ 10kHz
- Low Offset Voltage: 3.5 mV Maximum
- Unit Gain Stable
- Rail-to-Rail Input and Output
  Input Voltage Range: -0. 1V to +5. 1V at 5V Supply
- Operating Power Supply: +2.5V to +5.5V
- Operating Temperature Range: -40℃ to +125℃

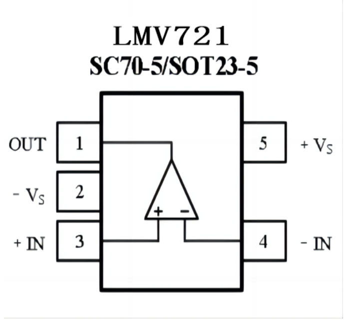
Applications

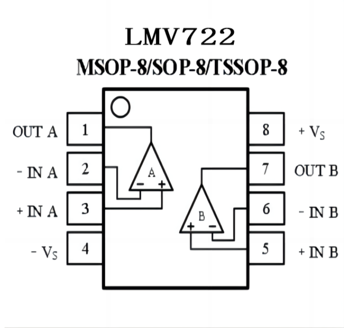
- Photodiode Amplification
- Sensor Interfaces
- Audio Outputs
- Active Filters
- Driving A/D Converters
- Portable Equipment & Battery-Powered Instrumentation

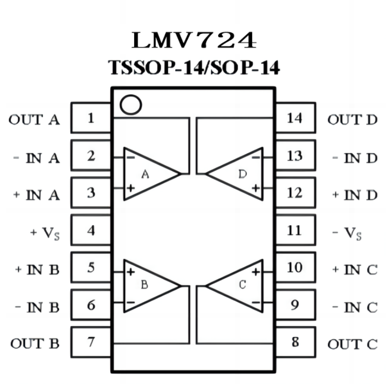
Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW LMV721IDBVR	SOT23-5	V721	Tape	3000Pcs/Reel
XBLW LMV721IDCKR	SC70-5	V721	Tape	3000Pcs/Reel
XBLW LMV722IDR	SOP-8	LMV722	Tape	2500Pcs/Reel
XBLW LMV722MMDTR	MSOP-8	V722	Tape	3000Pcs/Reel
XBLW LMV722MTDTR	TSSOP-8	V722	Tape	3000Pcs/Reel
XBLW LMV724MDTR	SOP-14	LMV724	Tape	2500Pcs/Reel
XBLW LMV724MTDTR	TSSOP-14	LMV724	Tape	2500Pcs/Reel

Pin Configurations







Pin Description

Symbol	Description
-IN	Negative (inverting) input.
+IN	Positive (noninverting) input.
-INA, -INB -INC, IND	Inverting Input ofthe Amplifier. The Voltage range can go from (V_{S-} – 0. 1V) to (V_{S+} + 0. 1V).
+INA, +INB +INC, +IND	Non-Inverting Input ofAmplifier. This pin has the same voltage range as –IN.
+V_S	Positive Power Supply. The voltage is from 2.5V to 5.5V. Split supplies are possible as long as the voltage between V_{S+} and V_{S-} is between 2.5V and 5.5V. A bypass capacitor of 0. 1μF as close to the part as possible should be used between power supply pins or between supply pins and ground.
-V_S	Negative Power Supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V_{S+} and V_{S-} is from 2.5V to 5.5V. If it is not connected to ground, bypass it with a capacitor of 0. 1μF as close to the part as possible.
OUT	Output.
OUTA,OUTB OUTC,OUTD	Amplifier Output.

Absolute Maximum Ratings（TA=25℃）

Symbol	Description	Value	Unit
V_{S+},V_{S-}	Supply Voltage, V_{S+} to V_{S-}	7.0	V
V_{CM}	Common-Mode Input Voltage	V_{S-} – 0.3 to V_{S+} + 0.3	V
ESD	Electrostatic Discharge Voltage	HBM ±4000	V
		CDM ±1000	V
T_J	Junction Temperature	160	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C(TJ)
T_{JL}	Lead Temperature Range (Soldering 10 sec)	260	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum- rated conditions for extended periods may affect device reliability.
2. Input terminals are diode-clamped to the power-supply rails.
3. Provided device does not exceed maximum junction temperature (T_J) at any time.

Electrical Characteristics（TA=25℃）

(V_S=5.0V ,T_A=+25℃ ,V_{CM}=V_S/2 ,V_O=V_S/2, R_L= 10kΩ connected to V_S/2, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
INPUT CHARACTERISTICS						
V_{OS}	Input offset voltage		-3.5	±0.8	+3.5	mV
		B Version	-0.9	±0.4	+0.9	mV
		C Version	-0.35	±0.1	+0.35	mV
$V_{OS}TC$	Offset voltage drift			3		μV/°C
I_B	Input bias current			1		pA
	Over temperature			800		
I_{OS}	Input offset current			1		pA
V_{CM}	Common-mode voltage range		V_{S-}–0. 1		V_{S+}+0. 1	V
CMRR	Common-mode rejection ratio	V_{CM} = 0.05V to 3.5V	70	84		dB
	Over temperature			80		
		V_{CM} = V_{S-}–0. 1 to V_{S+}+0. 1 V	60	76		
A_{VOL}	Open-loop voltage gain	R_L = 10kΩ, V_O = 0.1 to 4.9 V	90	102		
	Over temperature			90		
		R_L = 600Ω, V_O = 0.2 to 4.8 V	80	89		
	Over temperature			80		
R_{IN}	Input resistance			100		GΩ
C_{IN}	Input capacitance	Differential		2.0		pF
		Common mode		3.5		
OUTPUT CHARACTERISTICS						
V_{OH}	High output voltage swing	R_L = 600Ω		V_{S+}–100		mV
		R_L = 10kΩ		V_{S+}–8		
V_{OL}	Low output voltage swing	R_L = 600Ω		100		mV
		R_L = 10kΩ		8		
Z_{OUT}	Closed-loop output impedance	f = 200kHz, G = +1		0.8		Ω
	Open-loop output impedance	f = 1MHz, I_O = 0		3		
I_{SC}	Short-circuit current	Source current through 10Ω		40		mA
		Sink current through 10Ω		40		

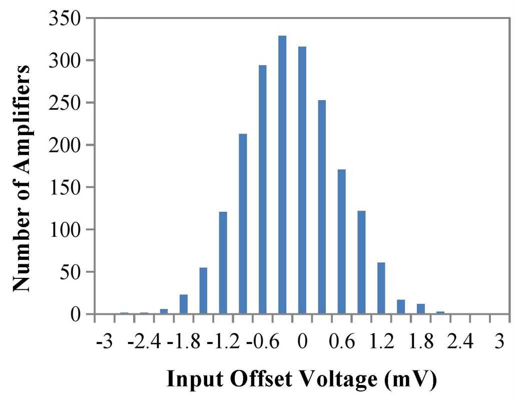
Electrical Characteristics（TA=25℃)

(V_S=5.0V, T_A=+25°C, V_{CM}=V_S/2, V_O=V_S/2, R_L= 10kΩ connected to V_S/2, unless otherwise noted.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DYNAMIC PERFORMANCE						
GBW	Gain bandwidth product	f = 1kHz		10		MHz
$Φ_M$	Phase margin	C_L = 100pF		60		°
SR	Slew rate	G = +1, C_L = 100pF, V_O = 1.5V to 3.5V		9		V/μs
BW_P	Full power bandwidth	<1% distortion		400		kHz
t_S	Settling time	To 0.1%, G = +1, 2V step		0.25		μs
		To 0.01%, G = +1, 2V step		0.28		
t_{OR}	Overload recovery time	V_{IN} * Gain > V_S		0.5		μs
NOISE PERFORMANCE						
V_n	Input voltage noise	f = 0.1 to 10 Hz		12		μV_{P-P}
e_n	Input voltage noise density	f = 10kHz		20		nV/√Hz
I_n	Input current noise density	f = 10kHz		5		fA/√Hz
POWER SUPPLY						
V_S	Operating supply voltage		2.5		5.5	V
PSRR	Power supply rejection ratio	V_S = 2.7V to 5.5V, V_{CM} < V_{S+} +0.5V	70	95		dB
	Over temperature			80		
I_Q	Quiescent current (per amplifier)			1000	1300	μA
	Over temperature			1200	1600	
THERMAL CHARACTERISTICS						
T_A	Operating temperature range		-40		+125	°C
$θ_{JA}$	Package thermal resistance	SOT23-5		190		°C/W
		SC70-5		333		
		SO-8		125		
		MSOP-8		216		
		TSSOP-8		153		
		SO-14		115		
		TSSOP-14		112		

Typical Performance Characteristics

(T_A = +25℃, V_{CM} = V_S/2, and R_L = 10kΩ connected to V_S/2, unless otherwise noted.)



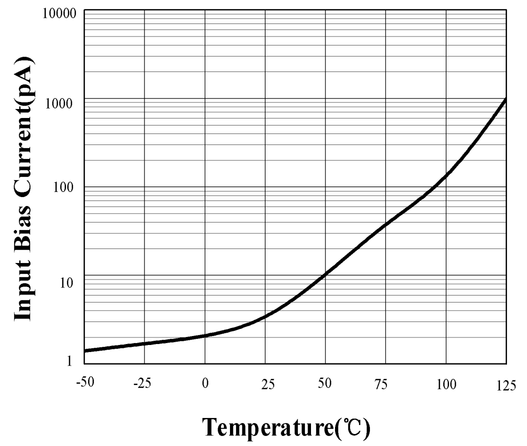


Fig. 2 Input Offset Voltage Production

Fig. 3 Input Bias Current as a Function of Temperature

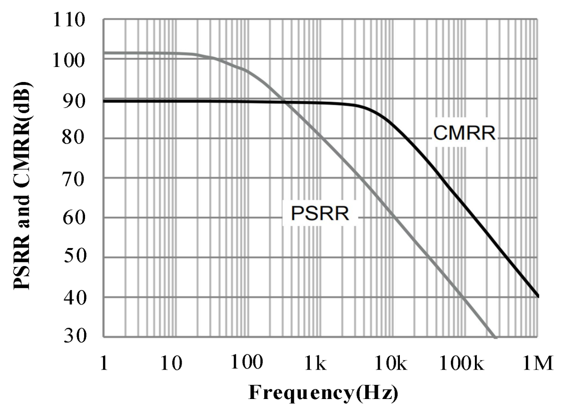


Fig. 4 Power Supply and Common-mode Rejection Ratio as a Function of Frequency

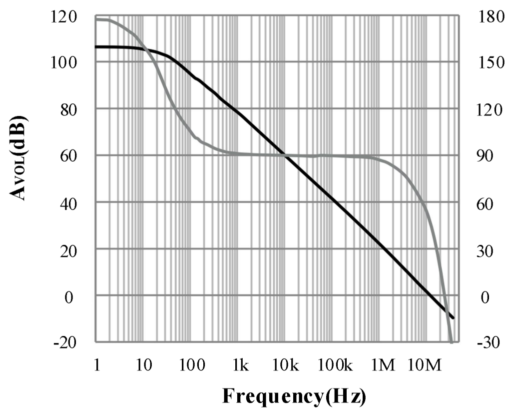


Fig. 5 Open-loop Gain and Phase as a function of Frequency

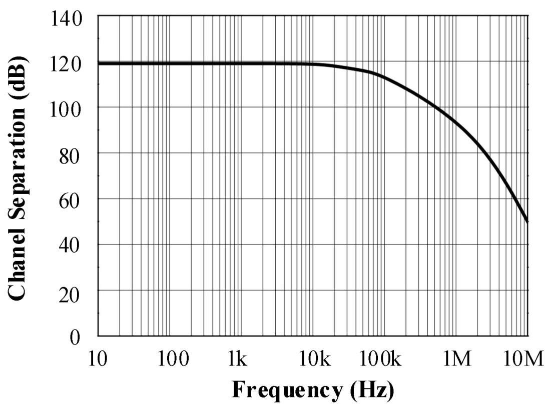


Fig. 6 Channel Separation as a function of Frequency

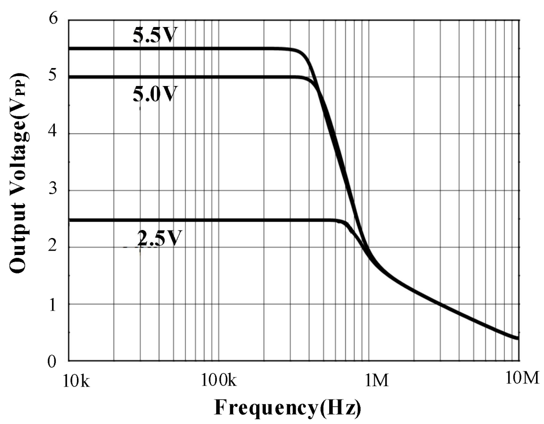


Fig. 7 Maximum Output Voltage as a function of Frequency

Typical Performance Characteristics

(T_A = +25℃, V_{CM} = V_S/2, and R_L = 10kΩ connected to V_S/2, unless otherwise noted.)

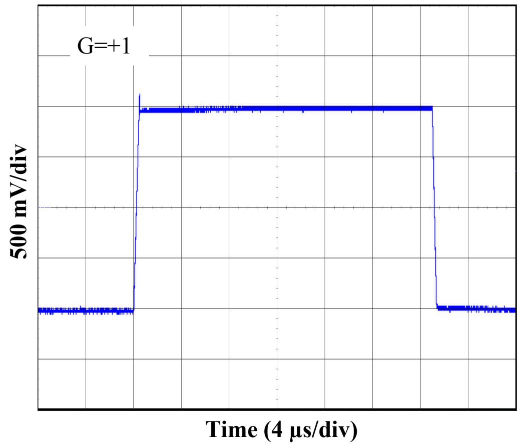


Fig. 8 Large-Signal Step Response at 2.7V

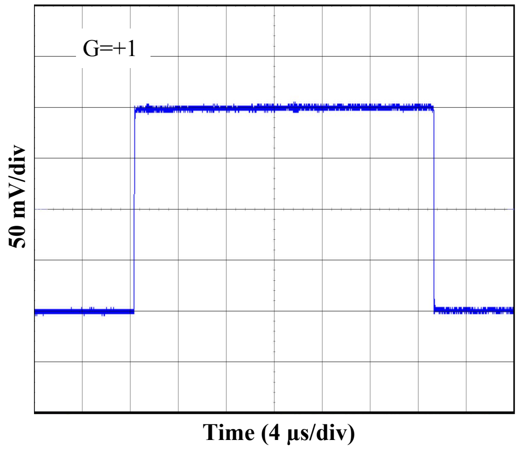


Fig. 9 Small-Signal Step Response at 2.7V

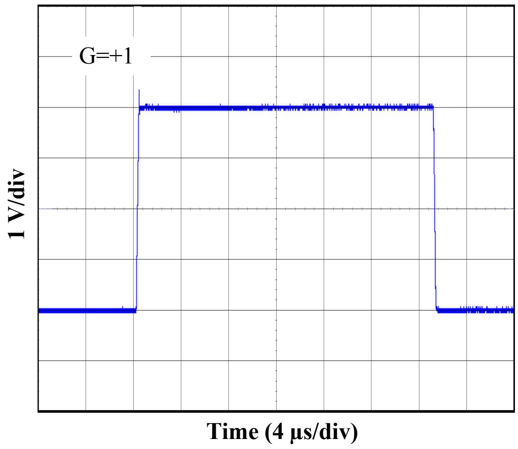


Fig. 10 Large-Signal Step Response at 5V

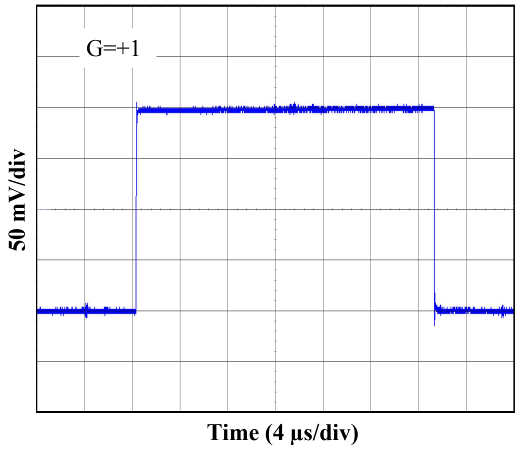


Fig. 11 Small-Signal Step Response at 5V

Application Notes

1. Low Input Bias Current

The LMV72X family is a CMOS op-amp family and features very low input bias current in pA range. The low input bias current allows the amplifiers to be used in applications with high resistance sources. Care must be taken to minimize PCB Surface Leakage. See below section on "PCB Surface Leakage" for more details.

2. PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5pA of current to flow, which is greater than the LMV72X's input bias current at +25℃ (±1pA, typical). It is recommended to use multi-layer PCB layout and route the op-amp's –IN and +IN signal under the PCB surface.

The effective way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 12 for Inverting Gain application.

1. For Non-Inverting Gain and Unity-Gain Buffer:

a) Connect the non-inverting pin (+IN) to the input with a wire that does not touch the PCB surface.

b) Connect the guard ring to the inverting input pin (-IN). This biases the guard ring to the Common Mode input voltage.

2. For Inverting Gain and Trans-impedance Gain Amplifiers (convert current to voltage, such as photo detectors):

a) Connect the guard ring to the non-inverting input pin (+IN). This biases the guard ring to the same reference voltage as the op-amp (e.g., $V_S/2$ or ground).

b) Connect the inverting pin (-IN) to the input with a wire that does not touch the PCB surface.

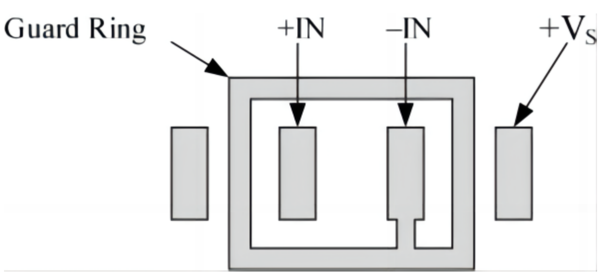


Fig. 12 Use a Guard Ring around Sensitive Pins

3. Ground Sensing And Rail To Rail

The input common-mode voltage range of the LMV72X series extends 300mV beyond the supply rails. This is achieved with a complementary input stage—a N-channel input differential pair in parallel with a P-channel differential pair. For normal operation, inputs should be limited to this range. The absolute maximum input voltage is 500mV beyond the supplies. Inputs greater than the input common-mode range but less than the maximum input voltage, while not valid, will not cause any damage to the op-amp. Unlike some other op- amps, if input current is limited, the inputs may go beyond the supplies without phase inversion, as shown in Figure 13. Since the input common-mode range extends from (V_{S-} − 0. 1V) to (V_{S+} + 0. 1V), the LMV72X op-amps can easily perform ‘true ground’ sensing.

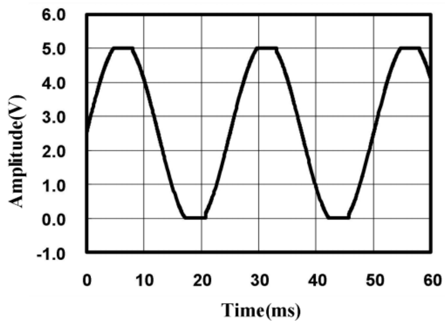


Fig. 13 No Phase Inversion with Inputs Greater Than the Power-Supply Voltage

A topology of class AB output stage with common-source transistors is used to achieve rail-to-rail output. For light resistive loads (e.g. 100kΩ), the output voltage can typically swing to within 5mV from the supply rails. With moderate resistive loads (e.g. 10kΩ), the output can typically swing to within 10mV from the supply rails and maintain high open-loop gain.

The maximum output current is a function of total supply voltage. As the supply voltage to the amplifier increases, the output current capability also increases. Attention must be paid to keep the junction temperature of the IC below 150℃ when the output is in continuous short-circuit. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.5V beyond either supply, otherwise current will flow through these diodes.

4. Capacitive Load And Stability

The LMV72X can directly drive 1nF in unity-gain without oscillation. The unity-gain follower (buffer) is the most sensitive configuration to capacitive loading.

Direct capacitive loading reduces the phase margin of amplifiers and this results in ringing or even oscillation. Applications that require greater capacitive drive capability should use an isolation resistor between the output and the capacitive load like the circuit in Figure 14. The isolation resistor R_{ISO} and the load capacitor C_L form a zero to increase stability. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Note that this method results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the R_L.

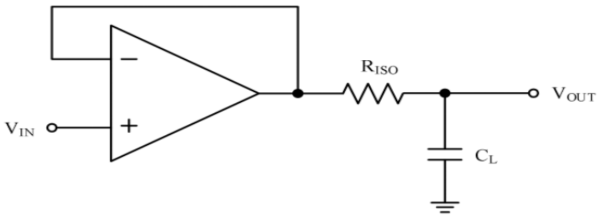


Fig. 14 Indirectly Driving Heavy Capacitive Load

An improvement circuit is shown in Figure 15. It provides DC accuracy as well as AC stability. The R_F provides the DC accuracy by connecting the inverting signal with the output.

The C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

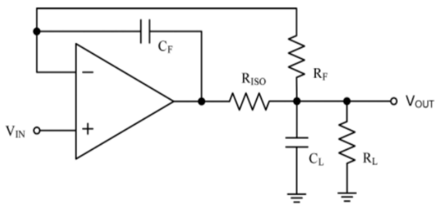


Fig. 15 Indirectly Driving Heavy Capacitive Load with DC Accuracy

For no-buffer configuration, there are two other ways to increase the phase margin: (a) by increasing the amplifier's gain, or (b) by placing a capacitor in parallel with the feedback resistor to counteract the parasitic capacitance associated with inverting node.

5. Power Supply Layout And Bypass

The LMV72X family operates from either a single +2.5V to +5.5V supply or dual ±1.25V to ±2.25V supplies. For single-supply operation, bypass the power supply V_S with a ceramic capacitor (i.e. 0.01μF to 0.1μF) which should be placed close (within 2mm for good high frequency performance) to the V_S pin. For dual-supply operation both the V_{S+} and the V_{S-} supplies should be bypassed to ground with separate 0.1μF ceramic capacitors. A bulk capacitor(i.e. 2.2 μF or larger tantalum capacitor) within 100mm to provide large, slow currents and better performance.This bulk capacitor can be shared with other analog parts.

Good PC board layout techniques optimize performance by decreasing the amount of stray capacitance at the op-amp's inputs and output. To decrease stray capacitance, minimize trace lengths and widths by placing external components as close to the device as possible. Use surface-mount components whenever possible. For the op-amp, soldering the part to the board directly is strongly recommended. Try to keep the high frequency big current loop area small to minimize the EMI (electromagnetic interfacing).

6. Grounding

A ground plane layer is important for the LMV72X circuit design. The length of the current path speed currents in an inductive ground return will create an unwanted voltage noise. Broad ground plane areas will reduce the parasitic inductance.

7. Input To Output Coupling

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

Typical Application Circuits

1. Differential Amplifier

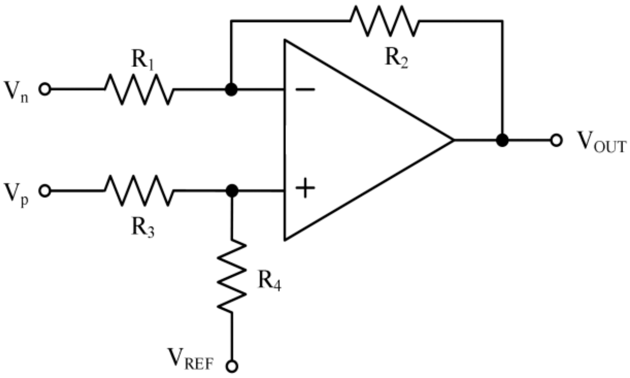
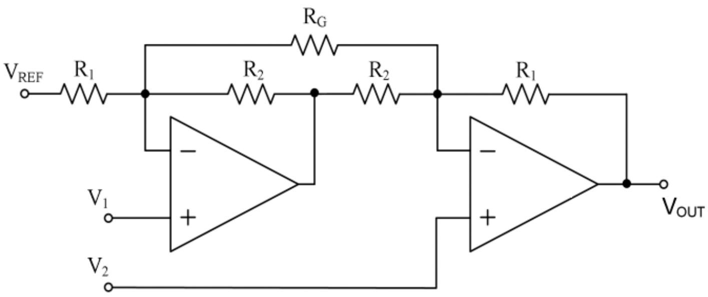


Fig. 16 Differential Amplifier

The circuit shown in Figure 16 performs the difference function. If the resistors ratios are equal $R_4/R_3 = R_2/R_1$, then:

$$\mathbf{V_{OUT} = (V_p - V_n) \times R_2/R_1 + V_{REF}}$$

2. Instrumentation Amplifier



$$V_{OUT} = (V_1 - V_2)(1 + \frac{R_1}{R_2} + \frac{2R_1}{R_G}) + V_{REF}$$

Fig. 17 Instrumentation Amplifier

The LMV72X family is well suited for conditioning sensor signals in battery-powered applications. Figure 17 shows a two op-amp instrumentation amplifier, using the LMV72X op-amps. The circuit works well for applications requiring rejection of common-mode noise at higher gains. The reference voltage (V_{REF}) is supplied by a low-impedance source. In single voltage supply applications, the V_{REF} is typically $V_S/2$.

3. Buffered Chemical Sensors

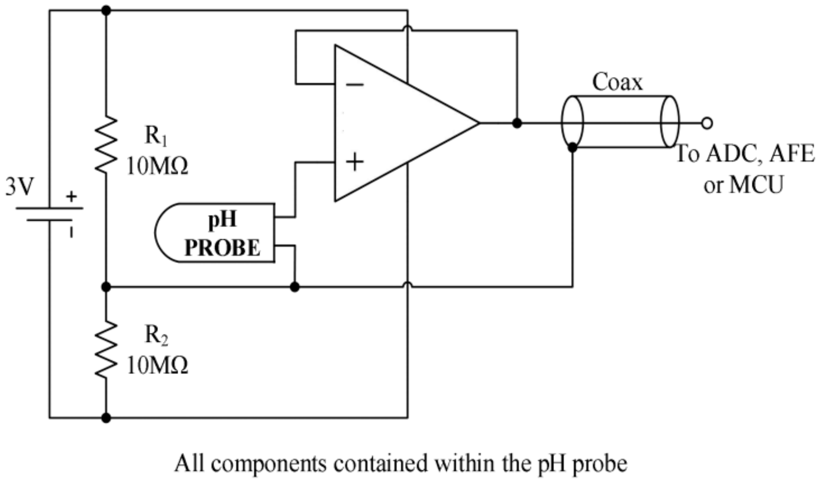


Fig. 18 Buffered pH Probe

The LMV72X family has input bias current in the pA range. This is ideal in buffering high impedance chemical sensors, such as pH probes. As an example, the circuit in Figure 7 eliminates expansive low-leakage cables that is required to connect a pH probe (general purpose combination pH probes, e.g Corning 476540) to metering ICs such as ADC, AFE and/or MCU. An LMV72X op-amp and a lithium battery are housed in the probe assembly. A conventional low-cost coaxial cable can be used to carry the op-amp's output signal to subsequent ICs for pH reading.

4. Shunt-Based Current Sensing Amplifier

The current sensing amplification shown in Figure 8 has a slew rate of $2\pi fV_{PP}$ for the output of sine wave signal, and has a slew rate of $2fV_{PP}$ for the output of triangular wave signal. In most of motor control systems, the PWM frequency is at 10kHz to 20kHz, and one cycle time is 100μs for a 10kHz of PWM frequency. In current shunt monitoring for a motor phase, the phase current is converted to a phase voltage signal for ADC sampling. This sampling voltage signal must be settled before entering the ADC. As the Figure 8 shown, the total settling time of a current shunt monitor circuit includes: the rising edge delay time (t_{SR}) due to the op-amp's slew rate, and the measurement settling time (t_{SET}). If the minimum duty cycle of the PWM is defined at 5%, and the t_{SR} is required at 20% of a total time window for a phase current monitoring, in case of a 3.3V motor control system (3.3V MCU with 12-bit ADC), the op-amp's slew rate should be more than:

$$3.3V / (100\mu s \times 5\% \times 20\%) = 3.3\ V/\mu s$$

At the same time, the op-amp's bandwidth should be much greater than the PWM frequency, like 10 time at least.

Typical Application Circuits

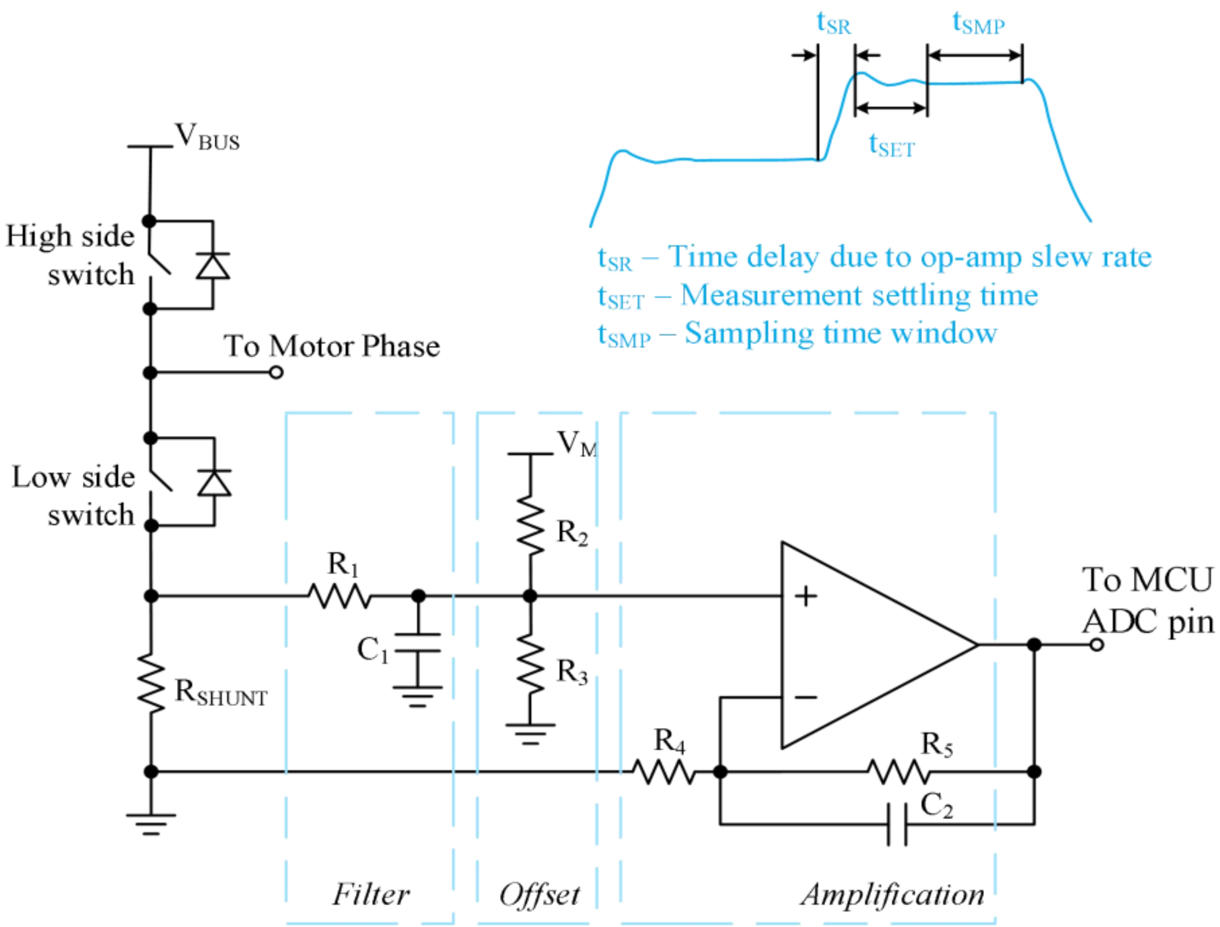
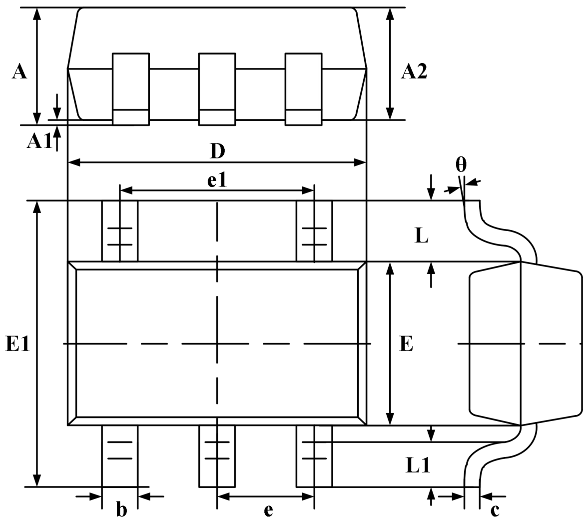


Fig. 19 Current Shunt Monitor Circuit

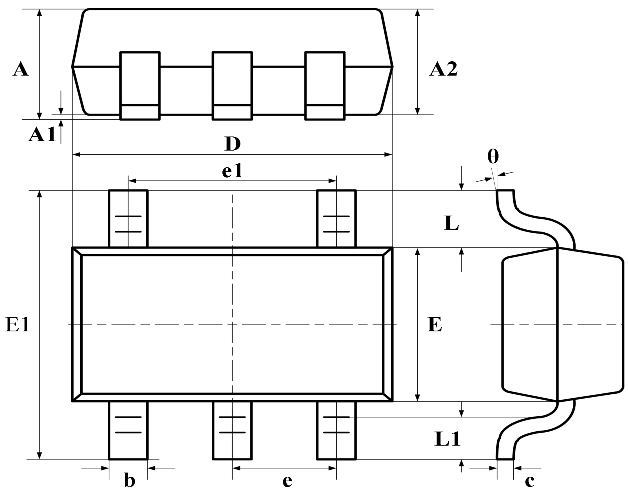
Package Information

SC70-5 (SOT353)



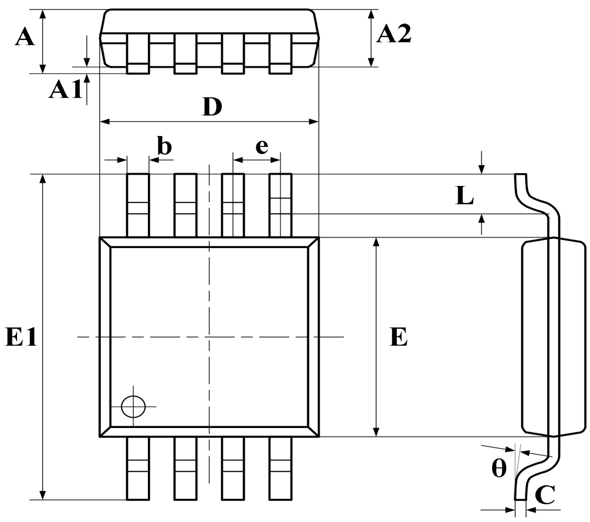
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.800	0.900	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.080	0.150	0.003	0.006
D	1.850	2.150	0.079	0.087
E	1.100	1.400	0.045	0.053
E1	1.950	2.200	0.085	0.096
e	0.850 typ.		0.026 typ.	
e1	1.200	1.400	0.047	0.055
L	0.42 ref.		0.021 ref.	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

SOT23-5



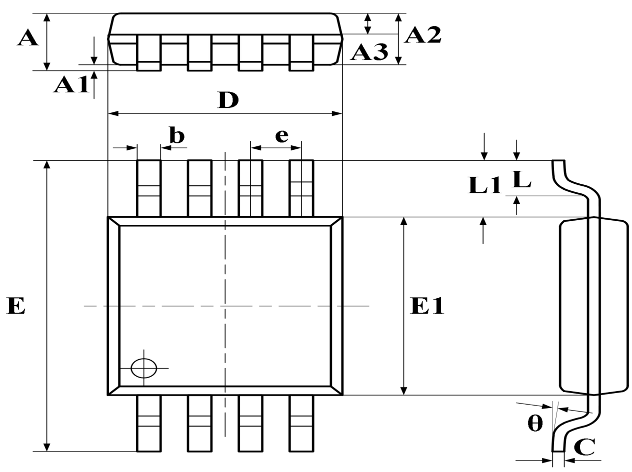
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.040	1.350	0.042	0.055
A1	0.040	0.150	0.002	0.006
A2	1.000	1.200	0.041	0.049
b	0.380	0.480	0.015	0.020
c	0.110	0.210	0.004	0.009
D	2.720	3.120	0.111	0.127
E	1.400	1.800	0.057	0.073
E1	2.600	3.000	0.106	0.122
e	0.950 typ.		0.037 typ.	
e1	1.900 typ.		0.078 typ.	
L	0.700 ref.		0.028 ref.	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

MSOP-8



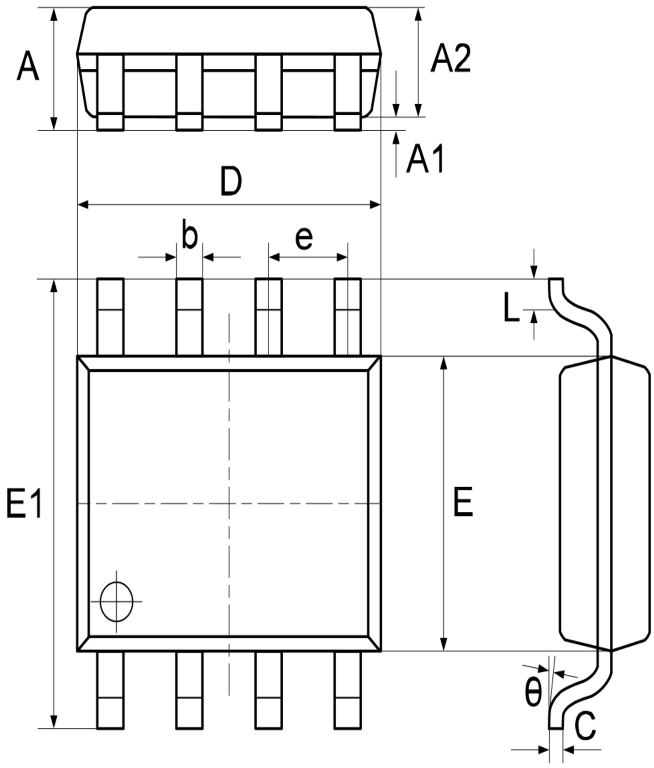
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.033	0.045
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.031	0.039
b	0.290	0.380	0.012	0.016
C	0.150	0.200	0.006	0.008
D	2.900	3.100	0.118	0.127
E	2.900	3.100	0.118	0.127
E1	4.700	5.100	0.192	0.208
e	0.650 typ.		0.026 typ.	
L	0.400	0.700	0.016	0.029
θ	0°	8°	0°	8°

TSSOP-8



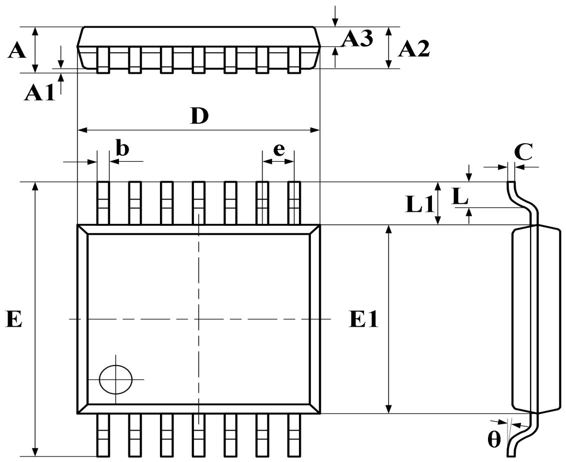
Symbol	Dimensions In Millimeters	Dimensions In Inches	
	Min	Nom	Max
A	-	-	1.200
A1	0.050	-	0.150
A2	0.900	1.000	1.050
A3	0.390	0.440	0.490
b	0.200	-	0.280
C	0.130	-	0.170
D	2.900	3.000	3.100
E	6.200	6.400	6.600
E1	4.300	4.400	4.500
e	0.65BSC		
L	0.450	-	0.750
L1	1.000 ref		
θ	0°	-	8°

SOP-8



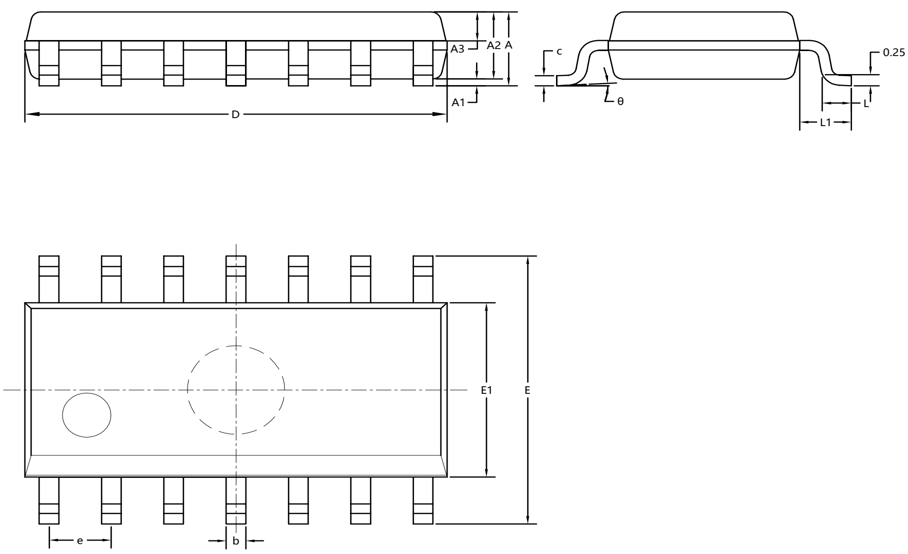
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.370	1.670	0.056	0.068
A1	0.070	0.170	0.003	0.007
A2	1.300	1.500	0.053	0.061
b	0.306	0.506	0.013	0.021
C	0.203 typ.		0.008 typ.	
D	4.700	5.100	0.192	0.208
E	3.820	4.020	0.156	0.164
E1	5.800	6.200	0.237	0.253
e	1.270 typ.		0.050 typ.	
L	0.450	0.750	0.018	0.306
θ	0°	8°	0°	8°

TSSOP-14



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	-	1.200	-	0.0472
A1	0.050	0.150	0.002	0.006
A2	0.900	1.050	0.037	0.043
A3	0.390	0.490	0.016	0.020
b	0.200	0.290	0.008	0.012
C	0.130	0.180	0.005	0.007
D	4.860	5.060	0.198	0.207
E	6.200	6.600	0.253	0.269
E1	4.300	4.500	0.176	0.184
e	0.650 typ.		0.0256 typ.	
L1	1.000 ref.		0.0393 ref.	
L	0.450	0.750	0.018	0.031
θ	0°	8°	0°	8°

SOP-14



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.50	1.60	1.70
A1	0.10	0.15	0.25
A2	1.40	1.45	1.50
A3	0.60	0.65	0.70
b	0.35	0.40	0.45
c	0.15	0.20	0.25
D	8.50	8.60	8.70
E	5.80	6.00	6.20
E1	3.85	3.90	3.95
e	1.27BSC		
L	0.50	0.60	0.70
L1	1.05REF		
θ	0°	4°	8°

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