General Description

The SN74HC/HCT190 are asynchronously presettable up/down BCD decade counters. They contain four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation.

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel data inputs (D0 to D3) is loaded into the counter and appears on the outputs when the parallel load ($\overline{PL}$) input is LOW. As indicated in the function table, this operation overrides the counting function.

Counting is inhibited by a HIGH level on the count enable ($\overline{CE}$) input. When $\overline{CE}$ is LOW internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The up/down ($\overline{U}$/D) input signal determines the direction of counting as indicated in the function table. The $\overline{CE}$ input may go LOW when the clock is in either state, however, the LOW-to-HIGH $\overline{CE}$ transition must occur only when the clock is HIGH. Also, the $\overline{U}$/D input should be changed only when either $\overline{CE}$ or CP is HIGH. Overflow/underflow indications are provided by two types of outputs, the terminal count (TC) and ripple clock ($\overline{RC}$). The TC output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches "9" in the count-up-mode. The TC output will remain HIGH until a state change occurs, either by counting or presetting, or until $\overline{U}$/D is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the $\overline{RC}$ output. When TC is HIGH and $\overline{CE}$ is LOW, the $\overline{RC}$ output follows the clock pulse (CP). This feature simplifies the design of multistage counters as shown in Figure 5 and 6.

In Figure 5, each $\overline{RC}$ output is used as the clock input to the next higher stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a HIGH on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse as indicated in the function table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This can be a disadvantage of this configuration in some applications.

Figure 6 shows a method of causing state changes to occur simultaneously in all stages. The $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion and all clock inputs are driven in parallel. In this configuration the duration of the clock LOW state must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. Since the $\overline{RC}$ output of any package goes HIGH shortly after its CP input goes HIGH there is no such restriction on the HIGH-state duration of the clock.

In Figure.7, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the $\overline{CE}$ input for a given stage. An enable must be included in each carry gate in order to inhibit counting. The TC output of a given stage it not affected by its own $\overline{CE}$ signal therefore the simple inhibit scheme of Figure 5 and 6 does not apply.

Features

- Input levels:
  For SN74HC190: CMOS level
  For SN74HCT190: TTL level
- Synchronous reversible counting
- Asynchronous parallel load
- Count enable control for synchronous expansion

- Single up/down control input
- Specified from -40℃ to +125℃
- Packaging information: DIP16/SOP16/TSSOP16

Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW SN74HC190N	DIP-16	74HC190N	Tube	1000Pcs/Box
XBLW SN74HC190DTR	SOP-16	74HC190	Tape	2500Pcs/Reel
XBLW SN74HC190TDTR	TSSOP-16	74HC190	Tape	3000Pcs/Reel
XBLW SN74HCT190N	DIP-16	74HCT190N	Tube	1000Pcs/Box
XBLW SN74HCT190DTR	SOP-16	74HCT190	Tape	2500Pcs/Reel
XBLW SN74HCT190TDTR	TSSOP-16	74HCT190	Tape	3000Pcs/Reel

Block Diagram And Pin Description

Block Diagram

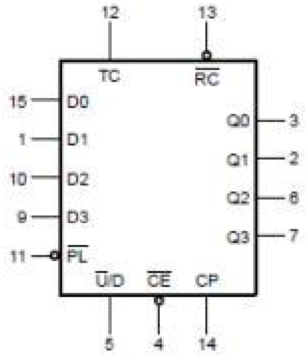


Figure 1. Logic symbol

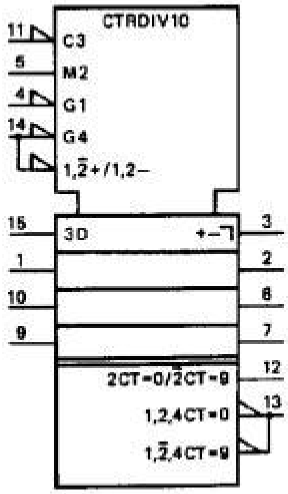


Figure 2. IEC logic symbol

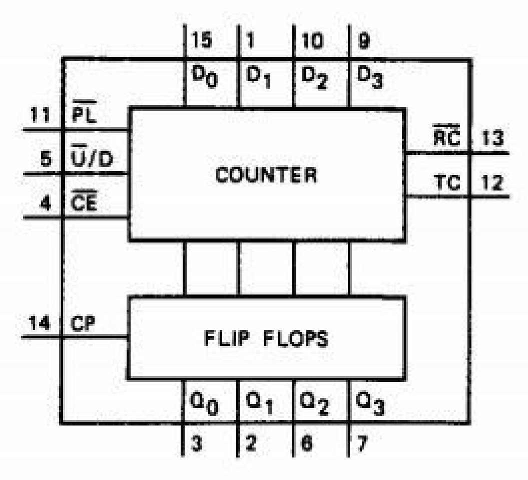


Figure 3.Functional diagram

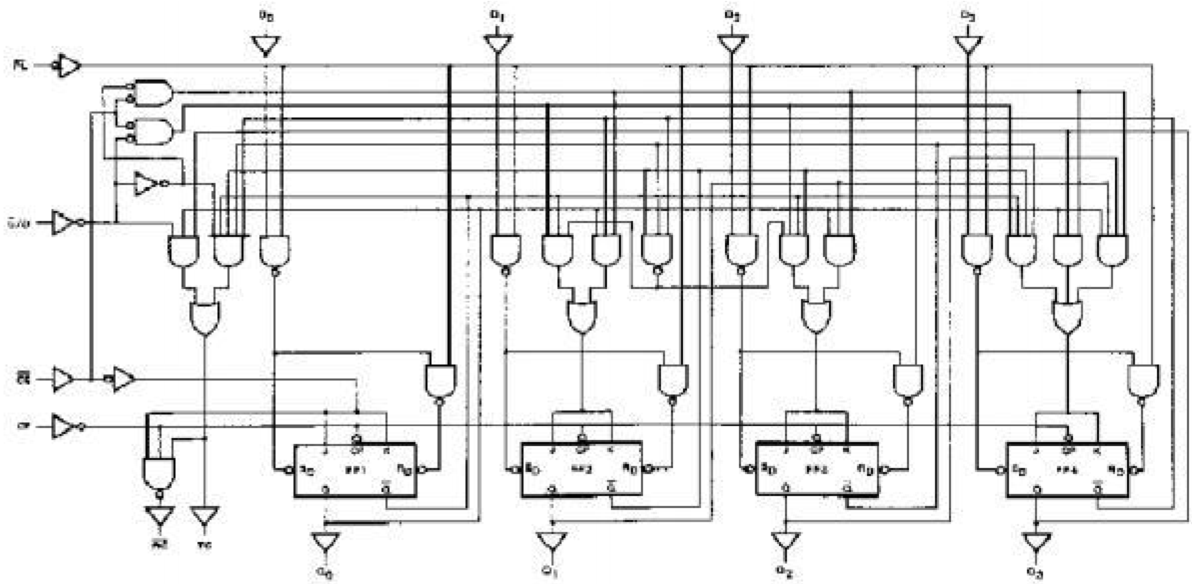


Figure 4. Logic diagram

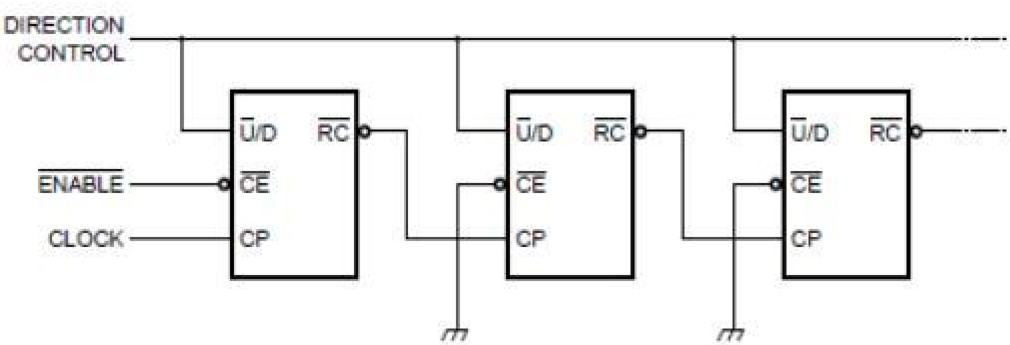


Figure 5.N-stage ripple counter using ripple clock

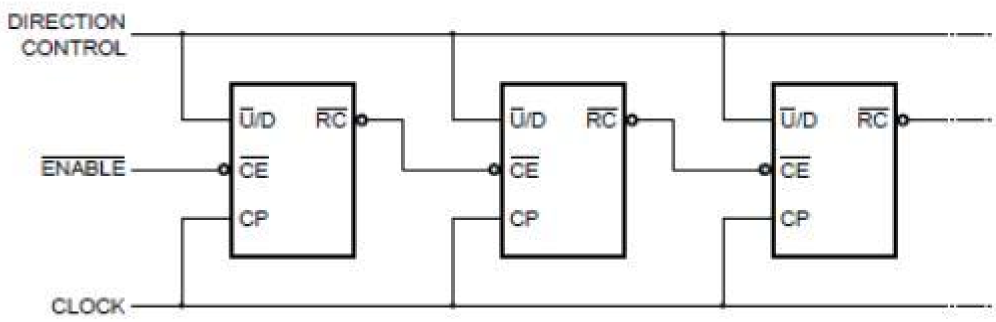


Figure 6. Synchronous n-stage counter using ripple carry/borrow

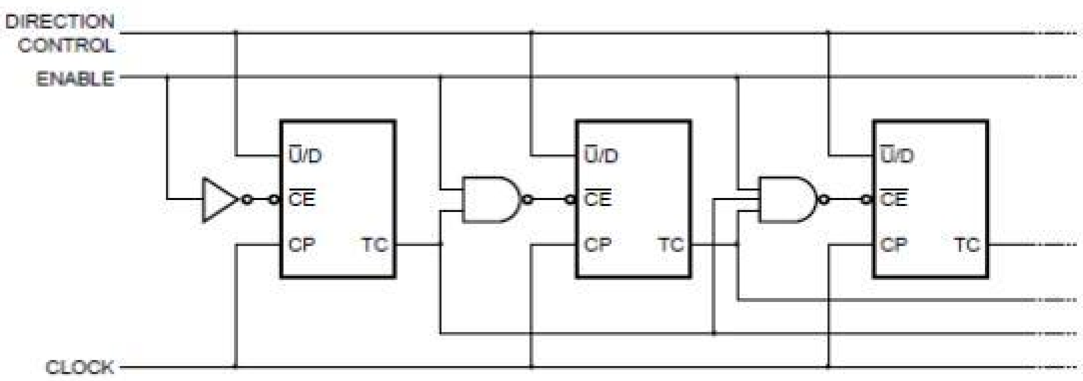


Figure 7. Synchronous n-stage counter with parallel gated carry/borrow

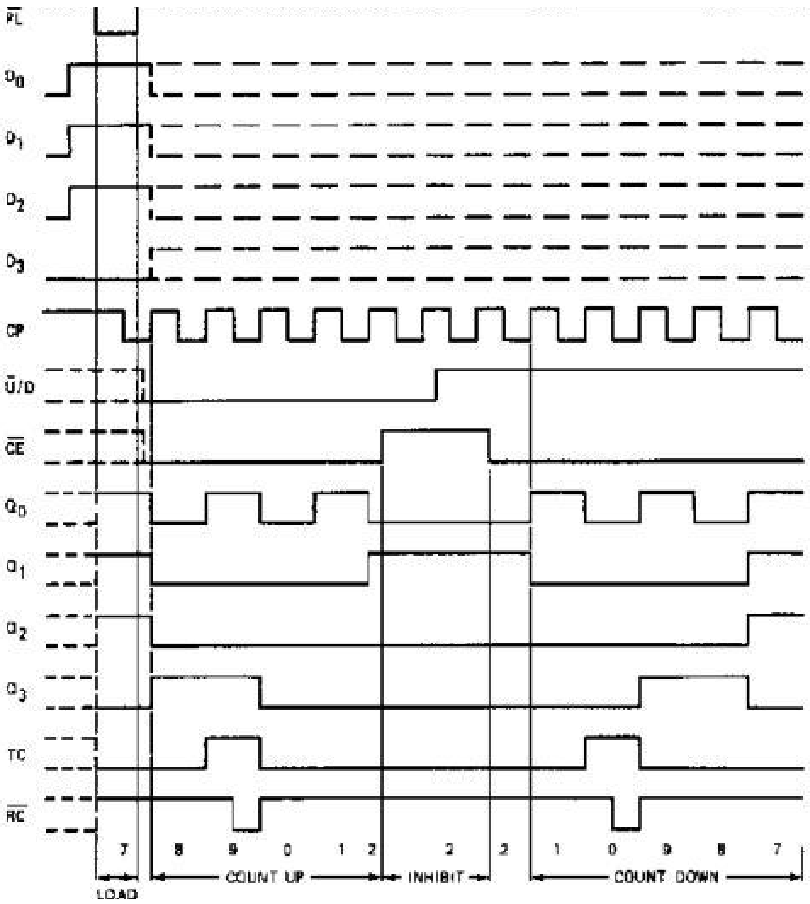
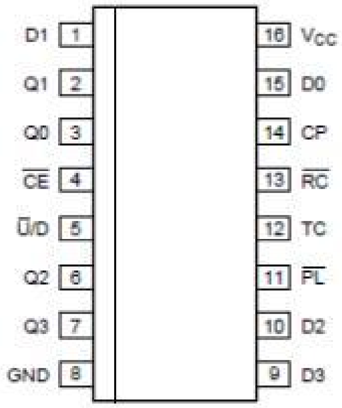


Figure 8. Typical timing sequence

Pin Configurations



Pin Description

Pin No.	Pin Name	Description
1	D1	data input
2	Q1	flip-flop output
3	Q0	flip-flop output
4	$\overline{CE}$	count enable input (active LOW)
5	$\overline{U}$/D	up/down input
6	Q2	flip-flop output
7	Q3	flip-flop output
8	GND	ground (0V)
9	D3	data input
10	D2	data input
11	$\overline{PL}$	parallel load input (active LOW)
12	TC	terminal count output
13	$\overline{RC}$	ripple clock output (active LOW)
14	CP	clock input (LOW-to-HIGH, edge-triggered)
15	D0	data input
16	V_{CC}	supply voltage

Function Table

Operating mode	Input					Output
	$\overline{PL}$	$\overline{U}$/D	$\overline{CE}$	CP	Dn	Qn
parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
count up	H	L	l	↑	X	count up
count down	H	H	l	↑	X	count down
hold (do nothing)	H	X	H	X	X	no change

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care; ↑=LOW-to-HIGH clock

l=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.

Input			Terminal count state				Output	
$\overline{U}$/D	$\overline{CE}$	CP	Q0	Q1	Q2	Q3	TC	$\overline{RC}$
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	⊔	H	X	X	H	⌉⌊	⊔
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊔	L	L	L	L	⌉⌊	⊔

Note:

[1] H=HIGH voltage level; L=LOW voltage level; X=don't care.

[2] ⊔ =one LOW level output pulse.

[3] ⌉⌊ =TC goes LOW on a LOW-to-HIGH clock transition.

Electrical Parameter

Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{CC}	-		-0.5	+7.0	V
input clamping current	I_{IK}	V_I < -0.5V or V_I > V_{CC}+0.5V		-	±20	mA
output clamping current	I_{OK}	V_O < -0.5V or V_O > V_{CC}+0.5V		-	±20	mA
output current	I_O	V_O= -0.5V to V_{CC}+0.5V		-	±25	mA
supply current	I_{CC}	-		-	+50	mA
ground current	I_{GND}	-		-50	-	mA
storage temperature	T_{stg}	-		-65	+150	℃
total power dissipation	P_{tot}	-		-	500	mW
Soldering temperatur e	T_L	10s	DIP	245		℃
			SOP/TSSOP	260		

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SN74HC190						
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	Δt/ΔV	V_{CC}=2.0V	-	-	625	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	83	ns/V
ambient temperature	T_{amb}	-	-40	-	+125	℃
SN74HCT190						
supply voltage	V_{CC}	-	4.5	5.0	5.5	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	Δt/ΔV	V_{CC}=2.0V	-	-	-	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	-	ns/V
ambient temperature	T_{amb}	-	-40	-	+125	℃

DC Characteristics 1

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SN74HC190						
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V	1.5	1.2	-	V
		V_{CC}=4.5V	3.15	2.4	-	V
		V_{CC}=6.0V	4.2	3.2	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V	-	0.8	0.5	V
		V_{CC}=4.5V	-	2.1	1.35	V
		V_{CC}=6.0V	-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}; I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
		V_I = V_{IH} or V_{IL}; I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
		V_I = V_{IH} or V_{IL}; I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
		V_I = V_{IH} or V_{IL}; I_O=-4.0mA; V_{CC}=4.5V	3.98	4.32	-	V
		V_I = V_{IH} or V_{IL}; I_O=-5.2mA; V_{CC}=6.0V	5.48	5.81	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}; I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
		V_I = V_{IH} or V_{IL}; I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
		V_I = V_{IH} or V_{IL}; I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
		V_I = V_{IH} or V_{IL}; I_O=4.0mA; V_{CC}=4.5V	-	0.15	0.26	V
		V_I = V_{IH} or V_{IL}; I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.26	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V	-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V	-	-	8.0	uA
input capacitance	C_I	-	-	3.5	-	pF
SN74HCT190						
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V	2.0	1.6	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V	-	1.2	0.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V; I_O=-20uA	4.4	4.5	-	V
		V_I = V_{IH} or V_{IL}; V_{CC}=4.5V; I_O=-4.0mA	3.98	4.32	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V; I_O=20uA	-	0	0.1	V
		V_I = V_{IH} or V_{IL}; V_{CC}=4.5V; I_O=4.0mA	-	0.16	0.26	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=5.5V	-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V	-	-	8.0	uA
additional supply current	ΔI_{CC}	V_I=V_{CC}-2.1V; other inputs at V_{CC} or GND; I_O=0A; V_{CC}=4.5V to 5.5V	-	-	360	uA
input capacitance	C_I	-	-	3.5	-	pF

DC Characteristics 2

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
SN74HC190							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.84	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.34	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	-	0.33	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA
SN74HCT190							
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V		2.0	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	-	-	V
			I_O=-4.0mA	3.84	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=20uA	-	-	0.1	V
			I_O=4.0mA	-	-	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	80	uA
additional supply current	ΔI_{CC}	V_I=V_{CC}-2.1V; other inputs at V_{CC} or GND; I_O=0A; V_{CC}=4.5V to 5.5V		-	-	450	uA

DC Characteristics 3

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
SN74HC190							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.7	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.2	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	-	0.4	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.4	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	160	uA
SN74HCT190							
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V		2.0	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	-	-	V
			I_O=-4.0mA	3.7	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=20uA	-	-	0.1	V
			I_O=4.0mA	-	-	0.4	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	160	uA
additional supply current	ΔI_{CC}	V_I=V_{CC}-2.1V; other inputs at V_{CC} or GND; I_O=0A; V_{CC}=4.5V to 5.5V		-	-	490	uA

AC Characteristics 1

(T_{amb}=25℃, GND=0V; t_r=t_f=6ns; C_L=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
SN74HC190							
propagation delay	t_{pd}	CP to Qn; see Figure 10	V_{CC}=2.0V	-	72	220	ns
			V_{CC}=4.5V	-	26	44	ns
			V_{CC}=5.0V; C_L=15pF	-	22	-	ns
			V_{CC}=6.0V	-	21	37	ns
		CP to TC; see Figure 10	V_{CC}=2.0V	-	83	255	ns
			V_{CC}=4.5V	-	30	51	ns
			V_{CC}=6.0V	-	24	43	ns
		CP to $\overline{RC}$; see Figure 11	V_{CC}=2.0V	-	44	150	ns
			V_{CC}=4.5V	-	16	30	ns
			V_{CC}=6.0V	-	13	26	ns
		$\overline{CE}$ to $\overline{RC}$; see Figure 11	V_{CC}=2.0V	-	33	130	ns
			V_{CC}=4.5V	-	12	26	ns
			V_{CC}=6.0V	-	10	22	ns
		Dn to Qn; see Figure 12	V_{CC}=2.0V	-	63	220	ns
			V_{CC}=4.5V	-	23	44	ns
			V_{CC}=6.0V	-	18	37	ns
		$\overline{PL}$ to Qn; see Figure 13	V_{CC}=2.0V	-	63	220	ns
			V_{CC}=4.5V	-	23	44	ns
			V_{CC}=6.0V	-	18	37	ns
		$U/\overline{D}$ to TC; see Figure 14	V_{CC}=2.0V	-	44	190	ns
			V_{CC}=4.5V	-	16	38	ns
			V_{CC}=6.0V	-	13	32	ns
		$U/\overline{D}$ to $\overline{RC}$; see Figure 14	V_{CC}=2.0V	-	50	210	ns
			V_{CC}=4.5V	-	18	42	ns
			V_{CC}=6.0V	-	14	36	ns
transition time	t_t	see Figure 15	V_{CC}=2.0V	-	19	75	ns
			V_{CC}=4.5V	-	7	15	ns
			V_{CC}=6.0V	-	6	13	ns
pulse width	t_W	CP; HIGH or LOW; see Figure 10	V_{CC}=2.0V	155	28	-	ns
			V_{CC}=4.5V	31	10	-	ns
			V_{CC}=6.0V	26	8	-	ns
		$\overline{PL}$; LOW; see Figure 15	V_{CC}=2.0V	100	25	-	ns
			V_{CC}=4.5V	20	9	-	ns
			V_{CC}=6.0V	17	7	-	ns
recovery time	t_{rec}	$\overline{PL}$ to CP; see Figure 15	V_{CC}=2.0V	35	8	-	ns
			V_{CC}=4.5V	7	3	-	ns
			V_{CC}=6.0V	6	2	-	ns
set-up time	t_{su}	$U/\overline{D}$ to CP;	V_{CC}=2.0V	205	61	-	ns

		see Figure 16	V_{CC}=4.5V	41	22	-	ns
			V_{CC}=6.0V	35	18	-	ns
		Dn to $\overline{PL}$; see Figure 17	V_{CC}=2.0V	100	19	-	ns
			V_{CC}=4.5V	20	7	-	ns
			V_{CC}=6.0V	17	6	-	ns
		$\overline{CE}$ to CP; see Figure 16	V_{CC}=2.0V	140	39	-	ns
			V_{CC}=4.5V	28	14	-	ns
			V_{CC}=6.0V	24	11	-	ns
hold time	t_h	$\overline{U}$/D to CP; see Figure 16	V_{CC}=2.0V	0	-44	-	ns
			V_{CC}=4.5V	0	-16	-	ns
			V_{CC}=6.0V	0	-13	-	ns
		Dn to $\overline{PL}$; see Figure 17	V_{CC}=2.0V	0	-14	-	ns
			V_{CC}=4.5V	0	-5	-	ns
			V_{CC}=6.0V	0	-4	-	ns
		$\overline{CE}$ to CP; see Figure 16	V_{CC}=2.0V	0	-19	-	ns
			V_{CC}=4.5V	0	-7	-	ns
			V_{CC}=6.0V	0	-6	-	ns
maximum frequency	f_{max}	CP; see Figure 10	V_{CC}=2.0V	3.0	8.3	-	MHz
			V_{CC}=4.5V	15	25	-	MHz
			V_{CC}=5.0V; C_L=15pF	-	28	-	MHz
			V_{CC}=6.0V	18	30	-	MHz
power dissipation capacitance	C_{PD}	V_I=GND to V_{CC}		-	36	-	pF
SN74HCT190							
propagation delay	t_{pd}	CP to Qn; see Figure 10	V_{CC}=4.5V	-	28	48	ns
			V_{CC}=5.0V; C_L=15pF	-	24	-	ns
		CP to TC; see Figure 10	V_{CC}=4.5V	-	34	58	ns
		CP to $\overline{RC}$; see Figure 11	V_{CC}=4.5V	-	20	35	ns
		$\overline{CE}$ to $\overline{RC}$; see Figure 11	V_{CC}=4.5V	-	18	33	ns
		Dn to Qn; see Figure 12	V_{CC}=4.5V	-	24	44	ns
		$\overline{PL}$ to Qn; see Figure 13	V_{CC}=4.5V	-	29	49	ns
		$\overline{U}$/D to TC; see Figure 14	V_{CC}=4.5V	-	24	45	ns
		$\overline{U}$/D to $\overline{RC}$; see Figure 14	V_{CC}=4.5V	-	26	45	ns
transition time	t_t	V_{CC}=4.5V; see Figure 15		-	7	15	ns
pulse width	t_W	CP; HIGH or LOW; V_{CC}=4.5V see Figure 10		25	10	-	ns
		$\overline{PL}$; LOW; V_{CC}=4.5V; see Figure 15		22	12	-	ns
recovery time	t_{rec}	$\overline{PL}$ to CP; V_{CC}=4.5V; see Figure 15		7	1	-	ns

set-up time	t_{su}	$\overline{U}$/D to CP; V_{CC}=4.5V; see Figure 16		42	25	-	ns
		Dn to $\overline{PL}$; V_{CC}=4.5V; see Figure 17		20	10	-	ns
		$\overline{CE}$ to CP; V_{CC}=4.5V;see Figure 16		31	18	-	ns
hold time	t_h	$\overline{U}$/D to CP; V_{CC}=4.5V; see Figure 16		0	-18	-	ns
		Dn to $\overline{PL}$; V_{CC}=4.5V; see Figure 17		0	-6	-	ns
		$\overline{CE}$ to CP; V_{CC}=4.5V;see Figure 16		0	-10	-	ns
maximum frequency	f_{max}	CP; see Figure 10	V_{CC}=4.5V	16	27	-	MHz
			V_{CC}=5.0V; C_L=15pF	-	30	-	MHz
power dissipation capacitanc e	C_{PD}	V_I=GND to V_{CC}- 1.5V		-	38	-	pF

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the sameast_{THL} and t_{TLH}.

[3] C_{PD} isused to determine the dynamic power dissipation (P_D in uW).

$P_D=C_{PD}\times V_{CC}^2\times f_i+\Sigma(C_L\times V_{CC}^2\times f_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

$\Sigma(C_L\times V_{CC}^2\times f_o)$=sum of outputs.

AC Characteristics 2

(T_{amb}=-40℃ to +85℃, GND=0V; t_r=t_f=6ns; C_L=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
SN74HC190							
propagation delay	t_{pd}	CP to Qn; see Figure 10	V_{CC}=2.0V	-	-	275	ns
			V_{CC}=4.5V	-	-	55	ns
			V_{CC}=6.0V	-	-	47	ns
		CP to TC; see Figure 10	V_{CC}=2.0V	-	-	320	ns
			V_{CC}=4.5V	-	-	64	ns
			V_{CC}=6.0V	-	-	54	ns
		CP to $\overline{RC}$; see Figure 11	V_{CC}=2.0V	-	-	190	ns
			V_{CC}=4.5V	-	-	38	ns
			V_{CC}=6.0V	-	-	33	ns
		$\overline{CE}$ to $\overline{RC}$; see Figure 11	V_{CC}=2.0V	-	-	165	ns
			V_{CC}=4.5V	-	-	33	ns
			V_{CC}=6.0V	-	-	28	ns
		Dn to Qn; see Figure 12	V_{CC}=2.0V	-	-	275	ns
			V_{CC}=4.5V	-	-	55	ns
			V_{CC}=6.0V	-	-	47	ns
		$\overline{PL}$ to Qn; see Figure 13	V_{CC}=2.0V	-	-	275	ns
			V_{CC}=4.5V	-	-	55	ns
			V_{CC}=6.0V	-	-	47	ns

		U/D to TC; see Figure 14	V_{CC}=2.0V	-	-	240	ns
			V_{CC}=4.5V	-	-	48	ns
			V_{CC}=6.0V	-	-	41	ns
		U/D to RC; see Figure 14	V_{CC}=2.0V	-	-	265	ns
			V_{CC}=4.5V	-	-	53	ns
			V_{CC}=6.0V	-	-	45	ns
transition time	t_t	see Figure 15	V_{CC}=2.0V	-	-	95	ns
			V_{CC}=4.5V	-	-	19	ns
			V_{CC}=6.0V	-	-	16	ns
pulse width	t_W	CP; HIGH or LOW; see Figure 10	V_{CC}=2.0V	195	-	-	ns
			V_{CC}=4.5V	39	-	-	ns
			V_{CC}=6.0V	33	-	-	ns
		PL; LOW; see Figure 15	V_{CC}=2.0V	125	-	-	ns
			V_{CC}=4.5V	25	-	-	ns
			V_{CC}=6.0V	21	-	-	ns
recovery time	t_{rec}	PL to CP; see Figure 15	V_{CC}=2.0V	45	-	-	ns
			V_{CC}=4.5V	9	-	-	ns
			V_{CC}=6.0V	8	-	-	ns
set-up time	t_{su}	U/D to CP; see Figure 16	V_{CC}=2.0V	255	-	-	ns
			V_{CC}=4.5V	51	-	-	ns
			V_{CC}=6.0V	43	-	-	ns
		Dn to PL; see Figure 17	V_{CC}=2.0V	125	-	-	ns
			V_{CC}=4.5V	25	-	-	ns
			V_{CC}=6.0V	21	-	-	ns
		CE to CP; see Figure 16	V_{CC}=2.0V	175	-	-	ns
			V_{CC}=4.5V	35	-	-	ns
			V_{CC}=6.0V	30	-	-	ns
hold time	t_h	U/D to CP; see Figure 16	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
		Dn to PL; see Figure 17	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
		CE to CP; see Figure 16	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
maximum frequency	f_{max}	CP; see Figure 10	V_{CC}=2.0V	2.4	-	-	MHz
			V_{CC}=4.5V	12	-	-	MHz
			V_{CC}=6.0V	14	-	-	MHz
SN74HCT190							
propagation delay	t_{pd}	CP to Qn; see Figure 10	V_{CC}=4.5V	-	-	60	ns
		CP to TC; see Figure 10	V_{CC}=4.5V	-	-	73	ns
		CP to RC; see Figure 11	V_{CC}=4.5V	-	-	44	ns

		$\overline{CE}$ to $\overline{RC}$; see Figure 11	V_{CC}=4.5V	-	-	41	ns
		Dn to Qn; see Figure 12	V_{CC}=4.5V	-	-	55	ns
		$\overline{PL}$ to Qn; see Figure 13	V_{CC}=4.5V	-	-	61	ns
		$\overline{U}$/D to TC; see Figure 14	V_{CC}=4.5V	-	-	56	ns
		$\overline{U}$/D to $\overline{RC}$; see Figure 14	V_{CC}=4.5V	-	-	56	ns
transition time	t_t	V_{CC}=4.5V; see Figure 15		-	-	19	ns
pulse width	t_W	CP; HIGH or LOW; V_{CC}=4.5V see Figure 10		31	-	-	ns
		$\overline{PL}$; LOW; V_{CC}=4.5V; see Figure 15		28	-	-	ns
recovery time	t_{rec}	$\overline{PL}$ to CP; V_{CC}=4.5V; see Figure 15		9	-	-	ns
set-up time	t_{su}	$\overline{U}$/D to CP; V_{CC}=4.5V; see Figure 16		53	-	-	ns
		Dn to $\overline{PL}$; V_{CC}=4.5V; see Figure 17		25	-	-	ns
		$\overline{CE}$ to CP; V_{CC}=4.5V;see Figure 16		39	-	-	ns
hold time	t_h	$\overline{U}$/D to CP; V_{CC}=4.5V; see Figure 16		0	-	-	ns
		Dn to $\overline{PL}$; V_{CC}=4.5V; see Figure 17		0	-	-	ns
		$\overline{CE}$ to CP; V_{CC}=4.5V;see Figure 16		0	-	-	ns
maximum frequency	f_{max}	CP; see Figure 10	V_{CC}=4.5V	13	-	-	MHz

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the sameast_{THL} and t_{TLH}.

AC Characteristics 3

(T_{amb}=-40℃ to +125℃, GND=0V; t_r=t_f=6ns; C_L=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
SN74HC190							
propagation delay	t_{pd}	CP to Qn; see Figure 10	V_{CC}=2.0V	-	-	330	ns
			V_{CC}=4.5V	-	-	66	ns
			V_{CC}=6.0V	-	-	56	ns
		CP to TC; see Figure 10	V_{CC}=2.0V	-	-	384	ns
			V_{CC}=4.5V	-	-	77	ns
			V_{CC}=6.0V	-	-	65	ns
		CP to $\overline{RC}$; see Figure 11	V_{CC}=2.0V	-	-	228	ns
			V_{CC}=4.5V	-	-	46	ns
			V_{CC}=6.0V	-	-	40	ns
		$\overline{CE}$ to $\overline{RC}$; see Figure 11	V_{CC}=2.0V	-	-	198	ns
			V_{CC}=4.5V	-	-	40	ns
			V_{CC}=6.0V	-	-	34	ns
		Dn to Qn; see Figure 12	V_{CC}=2.0V	-	-	330	ns
			V_{CC}=4.5V	-	-	66	ns

			V_{CC}=6.0V	-	-	56	ns
		$\overline{PL}$ to Qn; see Figure 13	V_{CC}=2.0V	-	-	330	ns
			V_{CC}=4.5V	-	-	66	ns
			V_{CC}=6.0V	-	-	56	ns
		$\overline{U}$/D to TC; see Figure 14	V_{CC}=2.0V	-	-	288	ns
			V_{CC}=4.5V	-	-	58	ns
			V_{CC}=6.0V	-	-	49	ns
		$\overline{U}$/D to $\overline{RC}$; see Figure 14	V_{CC}=2.0V	-	-	318	ns
			V_{CC}=4.5V	-	-	64	ns
			V_{CC}=6.0V	-	-	54	ns
transition time	t_t	see Figure 15	V_{CC}=2.0V	-	-	114	ns
			V_{CC}=4.5V	-	-	23	ns
			V_{CC}=6.0V	-	-	19	ns
pulse width	t_W	CP; HIGH or LOW; see Figure 10	V_{CC}=2.0V	234	-	-	ns
			V_{CC}=4.5V	47	-	-	ns
			V_{CC}=6.0V	40	-	-	ns
		$\overline{PL}$; LOW; see Figure 15	V_{CC}=2.0V	150	-	-	ns
			V_{CC}=4.5V	30	-	-	ns
			V_{CC}=6.0V	25	-	-	ns
recovery time	t_{rec}	$\overline{PL}$ to CP; see Figure 15	V_{CC}=2.0V	54	-	-	ns
			V_{CC}=4.5V	11	-	-	ns
			V_{CC}=6.0V	10	-	-	ns
set-up time	t_{su}	$\overline{U}$/D to CP; see Figure 16	V_{CC}=2.0V	306	-	-	ns
			V_{CC}=4.5V	61	-	-	ns
			V_{CC}=6.0V	52	-	-	ns
		Dn to $\overline{PL}$; see Figure 17	V_{CC}=2.0V	150	-	-	ns
			V_{CC}=4.5V	30	-	-	ns
			V_{CC}=6.0V	25	-	-	ns
		$\overline{CE}$ to CP; see Figure 16	V_{CC}=2.0V	210	-	-	ns
			V_{CC}=4.5V	42	-	-	ns
			V_{CC}=6.0V	36	-	-	ns
hold time	t_h	$\overline{U}$/D to CP; see Figure 16	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
		Dn to $\overline{PL}$; see Figure 17	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
		$\overline{CE}$ to CP; see Figure 16	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
maximum frequency	f_{max}	CP; see Figure 10	V_{CC}=2.0V	2	-	-	MHz
			V_{CC}=4.5V	10	-	-	MHz
			V_{CC}=6.0V	12	-	-	MHz
SN74HCT190							
propagation	t_{pd}	CP to Qn;	V_{CC}=4.5V	-	-	72	ns

delay		see Figure 10					
		CP to TC; see Figure 10	V_{CC}=4.5V	-	-	88	ns
		CP to $\overline{RC}$; see Figure 11	V_{CC}=4.5V	-	-	53	ns
		$\overline{CE}$ to $\overline{RC}$; see Figure 11	V_{CC}=4.5V	-	-	49	ns
		Dn to Qn; see Figure 12	V_{CC}=4.5V	-	-	66	ns
		$\overline{PL}$ to Qn; see Figure 13	V_{CC}=4.5V	-	-	73	ns
		$\overline{U}$/D to TC; see Figure 14	V_{CC}=4.5V	-	-	67	ns
		$\overline{U}$/D to $\overline{RC}$; see Figure 14	V_{CC}=4.5V	-	-	67	ns
transition time	t_t	V_{CC}=4.5V; see Figure 15		-	-	23	ns
pulse width	t_W	CP; HIGH or LOW; V_{CC}=4.5V see Figure 10		37	-	-	ns
		$\overline{PL}$; LOW; V_{CC}=4.5V; see Figure 15		34	-	-	ns
recovery time	t_{rec}	$\overline{PL}$ to CP; V_{CC}=4.5V; see Figure 15		11	-	-	ns
set-up time	t_{su}	$\overline{U}$/D to CP; V_{CC}=4.5V; see Figure 16		64	-	-	ns
		Dn to $\overline{PL}$; V_{CC}=4.5V; see Figure 17		30	-	-	ns
		$\overline{CE}$ to CP; V_{CC}=4.5V;see Figure 16		47	-	-	ns
hold time	t_h	$\overline{U}$/D to CP; V_{CC}=4.5V; see Figure 16		0	-	-	ns
		Dn to $\overline{PL}$; V_{CC}=4.5V; see Figure 17		0	-	-	ns
		$\overline{CE}$ to CP; V_{CC}=4.5V;see Figure 16		0	-	-	ns
maximum frequency	f_{max}	CP; see Figure 10	V_{CC}=4.5V	11	-	-	MHz

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the sameast$_{THL}$ and t_{TLH}.

Testing Circuit

AC Testing Circuit

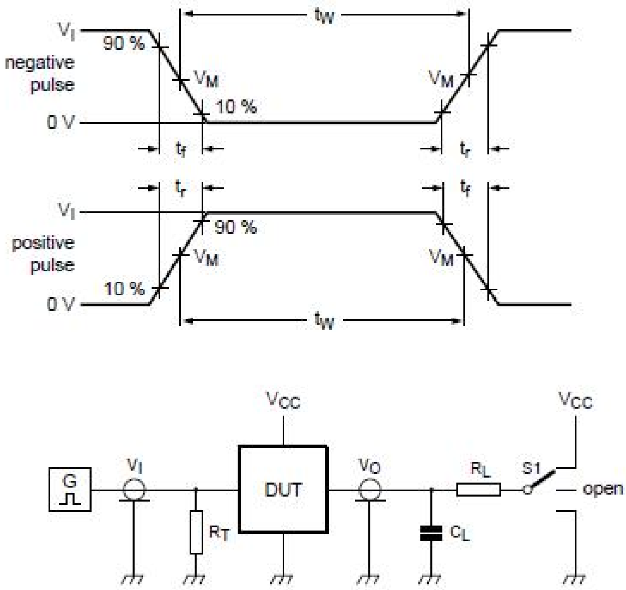


Figure 9. Test circuit for measuring switching times

Definitions for test circuit:

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_L=Load resistance.

S1=Test selection switch

AC Testing Waveforms

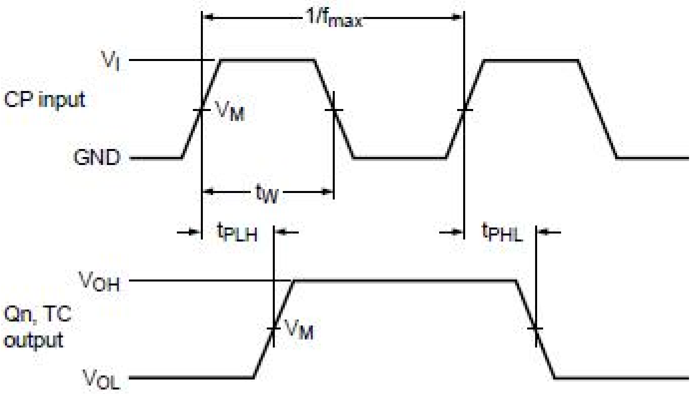


Figure 10. The clock input (CP) to outputs (Qn, TC) propagation delays, clock pulse width and maximum clock frequency

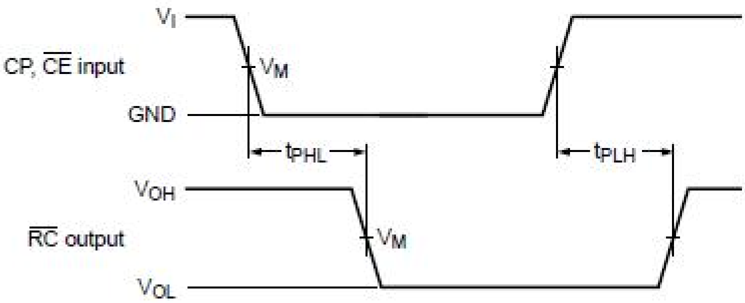


Figure 11. The clock and count enable inputs (CP, CE) to ripple clock output (RC) propagation delays

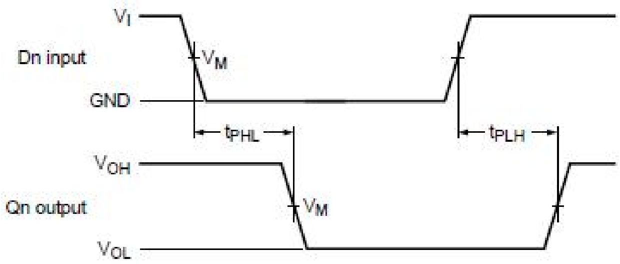


Figure 12. The input (Dn) to output (Qn) propagation delays

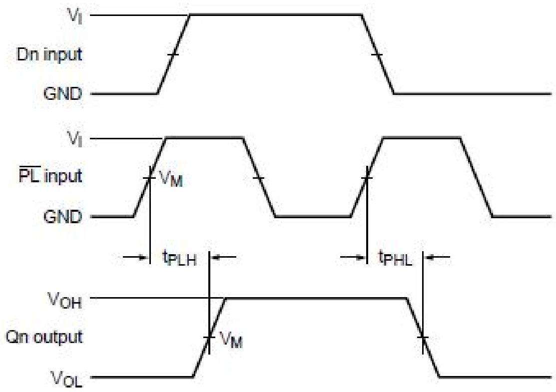


Figure 13. The parallel load input (PL) to output (Qn) propagation delays

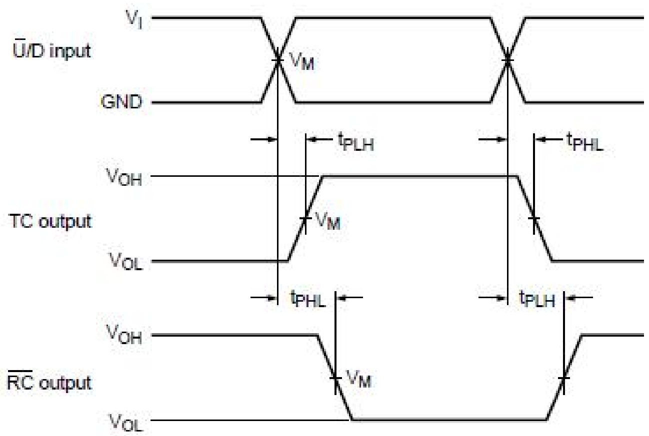


Figure 14. The up/down count input (U/D) to terminal count and ripple clock output (TC, RC) propagation delays

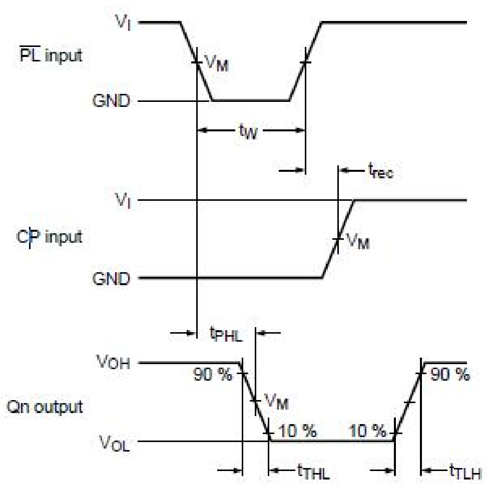


Figure 15. The parallel load input (PL) to clock (CP) recovery times, parallel load pulse width and output (Qn) transition times

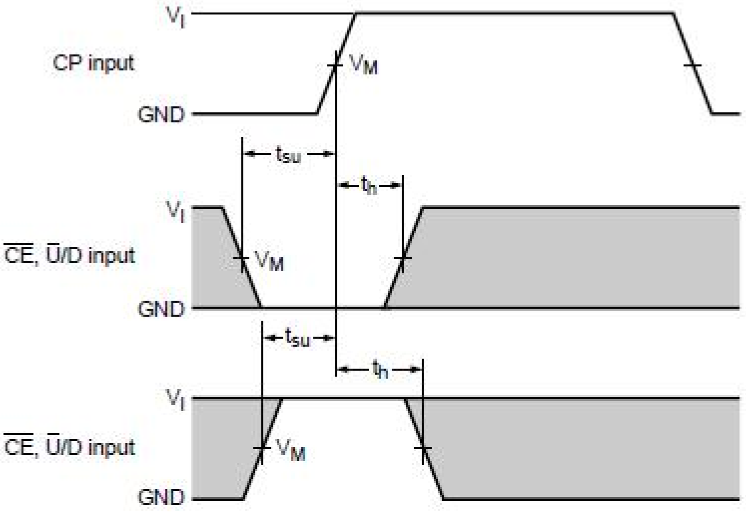


Figure 16. The count enable and up/down count inputs (CE, U/D) to clock input (CP) set-up and hold times

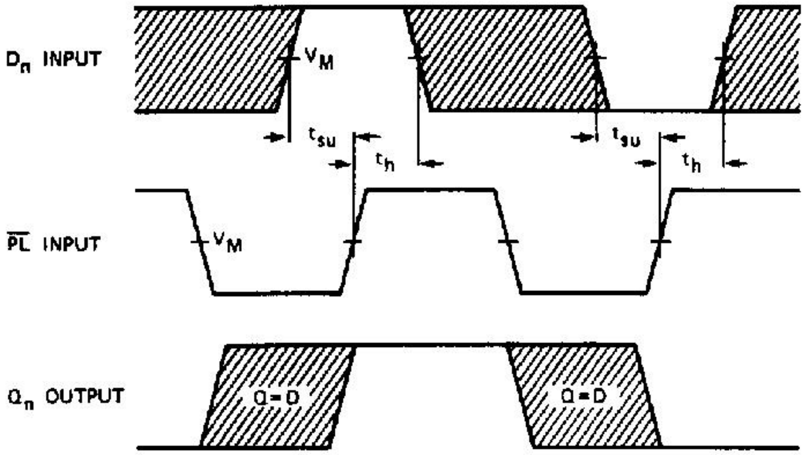


Figure 17. Waveforms showing the set-up and hold times from the parallel load input (PL) to the data input (Dn)

Measurement Points

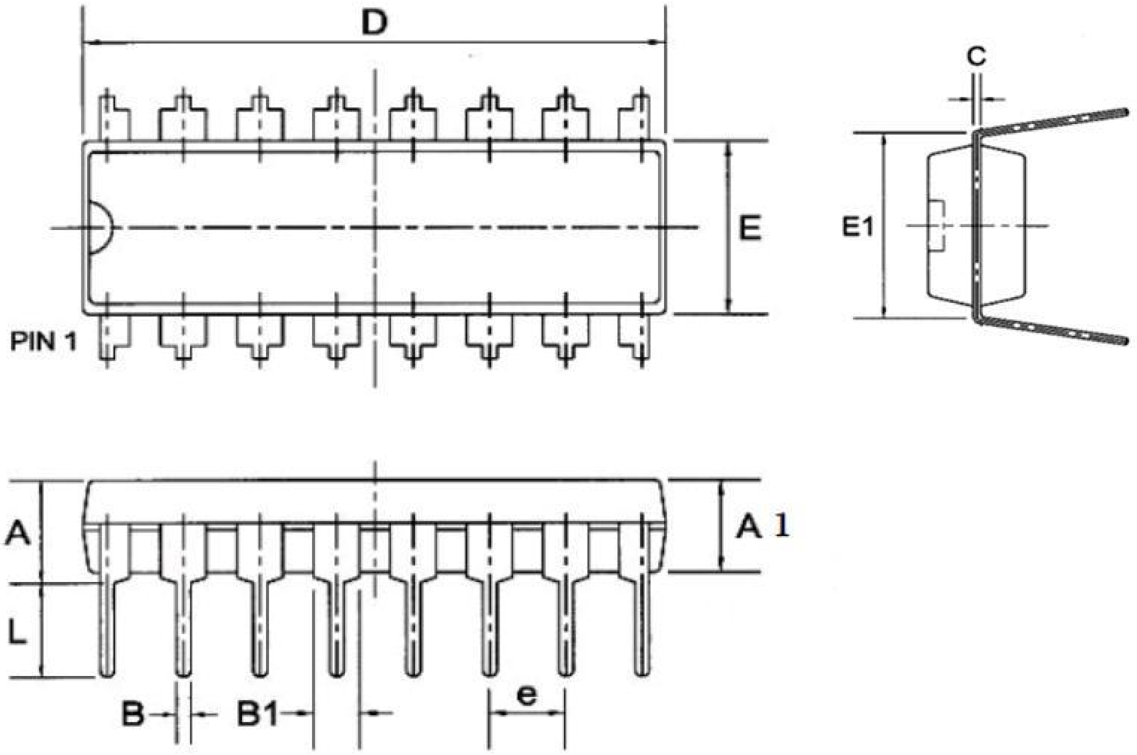
Type	Input	Output
	V_M	V_M
SN74HC190	0.5×V_{CC}	0.5×V_{CC}
SN74HCT190	1.3V	1.3V

Test Data

Type	Input		Load		S1 position
	V_I	t_r ,t_f	C_L	R_L	t_{PLH}, t_{PHL}
SN74HC190	V_{CC}	6ns	15pF, 50pF	1kΩ	open
SN74HCT190	3V	6ns	15pF, 50pF	1kΩ	open

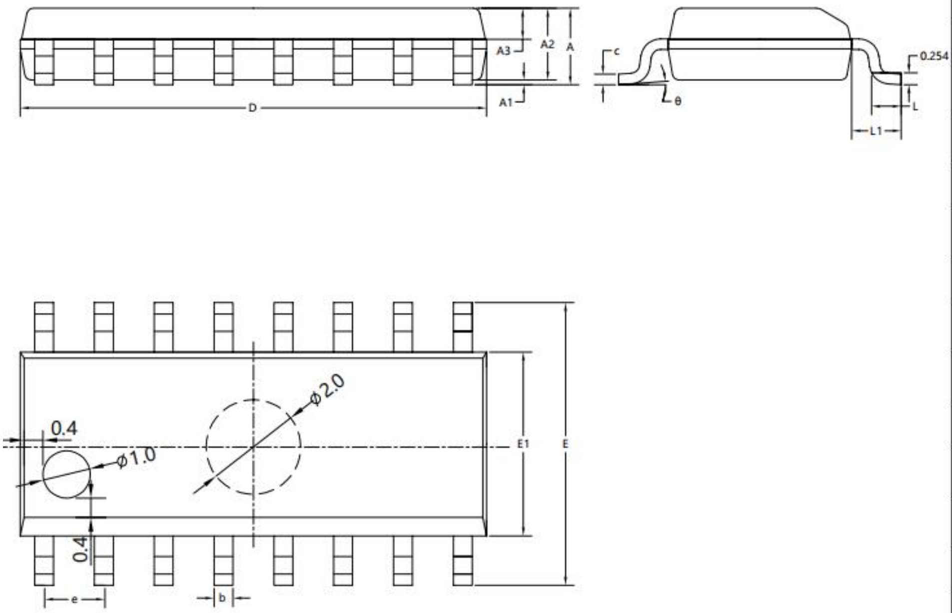
Package Information

DIP16



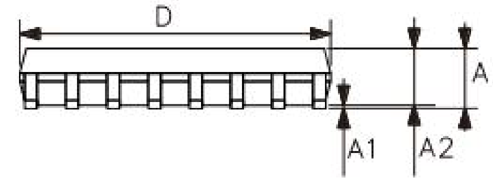
Symbol	Dimensions in Millimeters		
	Min	Nom	Max
A	--	--	4.31
A1	3.15	3.30	3.65
B	--	0.50	--
B1	--	1.6	--
C	--	0.27	--
D	19.00	19.20	19.60
E	6.20	6.50	6.60
E1	--	8.0	--
e	--	2.3	--
L	3.00	3.20	3.60

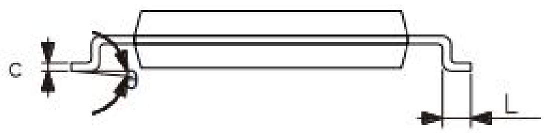
SOP16

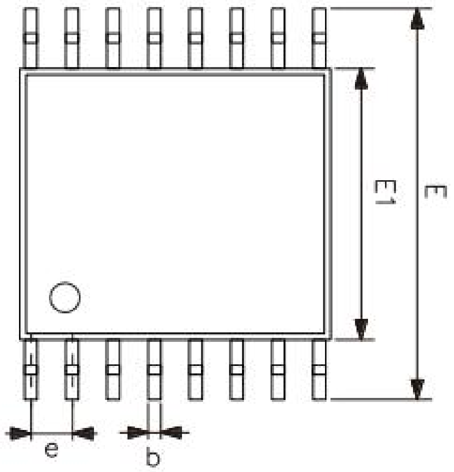


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.50	1.60	1.70
A1	0.10	0.15	0.25
A2	1.40	1.45	1.50
A3	0.60	0.65	0.70
b	0.30	0.40	0.50
c	0.15	0.20	0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.85	3.90	3.95
e	1.27BSC		
L	0.50	0.60	0.70
L1	1.05BSC		
θ	0°	4°	8°

TSSOP16







Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
θ	0°	8°

Statement：

✧ Shenzhen xinbole electronics co., ltd. reserves the right to change the product specifications, without notice! Before placing an order, the customer needs to confirm whether the information obtained is the latest version, and verify the integrity of the relevant information.

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✧ This document is for referenceonly,and the actual use should be based on the application test results.

✧ Product performance is never ending, Shenzhen xinbole electronics co., ltd will be dedicated to provide customers with better performance, better quality of integrated circuit products.

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