



General Description

CD4060 is a 14-stage ripple-carry binary counter/divider and oscillator with three oscillator terminals (RS, REXT and CEXT), ten buffered outputs (Q3 to Q9 and Q11 to Q13) and an overriding asynchronous master reset input (MR).

The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may be replaced by an external clock signal at input RS. The counter advances on the negative -going transition of RS. A HIGH level on MR resets the counter (Q3 to Q9 and Q11 to Q13=LOW), independent of other input conditions.

It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

Features

- Wide supply voltage range from 3V to 15V
- Tolerant of slow clock rise and fall times
- Fully static operation
- 5V, 10V, and 15V parametric ratings
- Standardized symmetrical output characteristics
- Inputs and outputs are protected against electrostatic effects
- Specified from -40°C to +85°C
- Packaging information: DIP16/SOP16/TSSOP16

Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
CD4060BE	DIP-16	CD4060BE	Tube	1000/Box
CD4060BDTR	SOP-16	CD4060B	Tape	2500/Reel
CD4060BDTR	TSSOP-16	CD4060B	Tape	3000/Reel

2、Block Diagram And Pin Description

2.1、Block Diagram

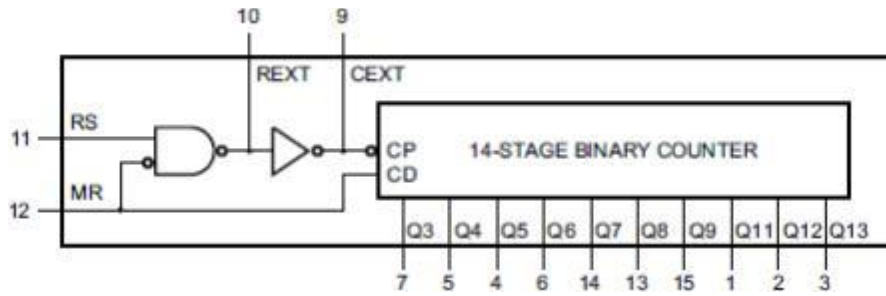


Figure 1. Functional diagram

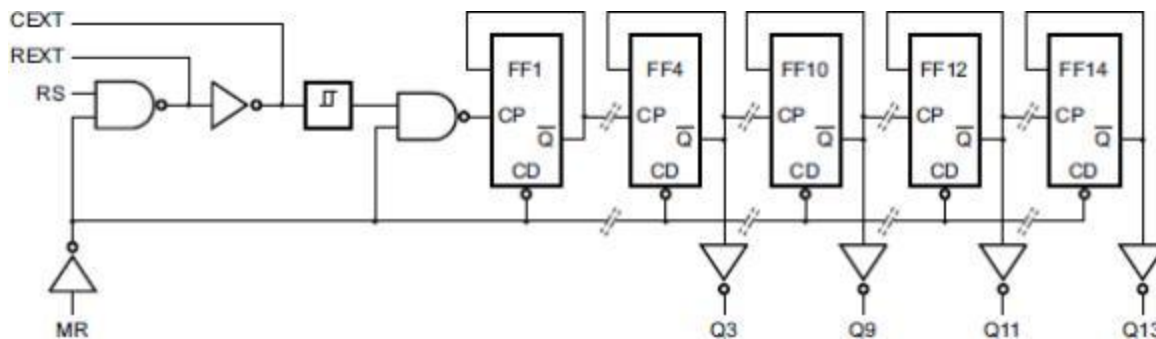
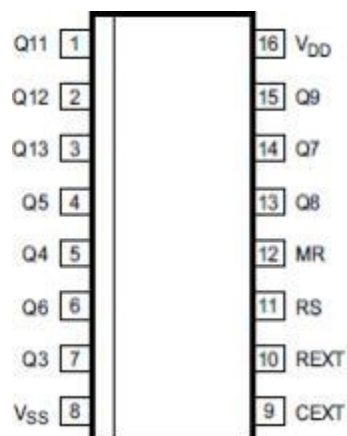


Figure 2. Logic diagram

2.2、Pin Configurations





2.3 、 Pin Description

Pin No.	Pin Name	Description
1	Q11	counter output
2	Q12	counter output
3	Q13	counter output
4	Q5	counter output
5	Q4	counter output
6	Q6	counter output
7	Q3	counter output
8	V _{SS}	ground (0V)
9	CEXT	external capacitor connection
10	REXT	oscillator pin
11	RS	clock input/oscillator pin
12	MR	master reset
13	Q8	counter output
14	Q7	counter output
15	Q9	counter output
16	V _{DD}	supply voltage

2.4 、 Function Table

Input		Output
RS	MR	Q3 to Q9 and Q11 to Q13
t	L	no change
↓	L	count
X	H	L

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care; t=LOW-to-HIGH clock transition.

3 Electrical Parameter

3.1 、 Absolute Maximum Ratings

(Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V _{DD}	-	-0.5	+18	V
DC input current	I _{IK}	any one input	-	±10	mA
input voltage	V _I	all inputs	-0.5	V _{DD} +0.5	V
storage temperature	T _{stg}	-	-65	+150	°C
total power dissipation	P _{tot}	-	-	500	mW
device dissipation	P	per output transistor	-	100	mW
Soldering temperature	T _L	10s	DIP	245	°C
			SOP	250	°C

Note:

[1] For DIP16 packages: above 70°C the value of P_{tot} derates linearly with 12mW/K.

[2] For SOP16 packages: above 70°C the value of P_{tot} derates linearly with 8mW/K.

[3] For (T)SSOP16 packages: above 60°C the value of P_{tot} derates linearly with 5.5mW/K.



3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
supply voltage	V_{DD}	-	3	-	15	V	
ambient temperature	T_{amb}	in free air	-40	-	+85	°C	
input pulse width	t_w	$f=100\text{kHz}$	$V_{DD}=5\text{V}$	100	-	-	ns
			$V_{DD}=10\text{V}$	40	-	-	ns
			$V_{DD}=15\text{V}$	30	-	-	ns
input pulse rise and fall time	t_{rIN}, t_{fIN}	$V_{DD}=5\text{V}$	unlimited			-	
		$V_{DD}=10\text{V}$				-	
		$V_{DD}=15\text{V}$				-	
input pulse frequency	f_{RS}	external pulse source	$V_{DD}=5\text{V}$	-	-	3.5	MHz
			$V_{DD}=10\text{V}$	-	-	8	MHz
			$V_{DD}=15\text{V}$	-	-	12	MHz
reset pulse width	t_{wR}	$V_{DD}=5\text{V}$	120	-	-	ns	
		$V_{DD}=10\text{V}$	60	-	-	ns	
		$V_{DD}=15\text{V}$	40	-	-	ns	

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(Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

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supply voltage	V_{DD}	-	-0.5	+18	V	
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device dissipation	P	per output transistor	-	100	mW	
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			$V_{DD}=10\text{V}$	40	-	-	ns
			$V_{DD}=15\text{V}$	30	-	-	ns
input pulse rise and fall time	t_{rIN}, t_{fIN}	$V_{DD}=5\text{V}$	unlimited			-	
		$V_{DD}=10\text{V}$				-	
		$V_{DD}=15\text{V}$				-	
input pulse frequency	f_{RS}	external pulse source	$V_{DD}=5\text{V}$	-	-	3.5	MHz
			$V_{DD}=10\text{V}$	-	-	8	MHz
			$V_{DD}=15\text{V}$	-	-	12	MHz
reset pulse width	t_{wR}	$V_{DD}=5\text{V}$	120	-	-	ns	
		$V_{DD}=10\text{V}$	60	-	-	ns	
		$V_{DD}=15\text{V}$	40	-	-	ns	



LOW-level output voltage	V _{OL}	-	0, 5	5	-	0.05	-	0.05	V
		-	0, 10	10	-	0.05	-	0.05	V
		-	0, 15	15	-	0.05	-	0.05	V
HIGH-level output voltage	V _{OH}	-	0, 5	5	4.95	-	4.95	-	V
		-	0, 10	10	9.95	-	9.95	-	V
		-	0, 15	15	14.95	-	14.95	-	V
LOW-level input voltage	V _{IL}	0.5, 4.5	-	5	-	1.5	-	1.5	V
		1, 9	-	10	-	3	-	3	V
		1.5, 13.5	-	15	-	4	-	4	V
HIGH-level input voltage	V _{IH}	0.5, 4.5	-	5	3.5	-	3.5	-	V
		1, 9	-	10	7	-	7	-	V
		1.5, 13.5	-	15	11	-	11	-	V
input leakage current	I _I	-	0, 15	15	-	±0.1	-	±1	uA

3.3.3 AC Characteristics 1

(T_{amb}=25°C, V_{SS}=0V, t_r, t_f=20ns, C_L=50pF, R_L=200kΩ, unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
propagation delay time	t _{PHL} , t _{PLH}	RS to Q3 out; see Figure 4	V _{DD} =5V	-	370	740	ns
			V _{DD} =10V	-	150	300	ns
			V _{DD} =15V	-	100	200	ns
		Q _n to Q _{n+1} ; see Figure 4	V _{DD} =5V	-	100	200	ns
			V _{DD} =10V	-	50	100	ns
			V _{DD} =15V	-	40	80	ns
		MR to Q _n ; see Figure 4	V _{DD} =5V	-	180	360	ns
			V _{DD} =10V	-	80	160	ns
			V _{DD} =15V	-	50	100	ns
transition time	t _t	see Figure 4	V _{DD} =5V	-	100	200	ns
			V _{DD} =10V	-	50	100	ns
			V _{DD} =15V	-	40	80	ns
pulse width	t _w	minimum width; f=100kHz; RS HIGH;	V _{DD} =5V	-	50	100	ns
			V _{DD} =10V	-	20	40	ns
			V _{DD} =15V	-	15	30	ns
		minimum width; MR HIGH; see Figure 4	V _{DD} =5V	-	60	120	ns
			V _{DD} =10V	-	30	60	ns
			V _{DD} =15V	-	20	40	ns
input pulse rise and fall time	t _{rIN} , t _{fIN}	-	V _{DD} =5V	unlimited			-
			V _{DD} =10V	unlimited			-
			V _{DD} =15V	unlimited			-
maximum clock frequency	f _{max}	input RS; see Figure 4	V _{DD} =5V	3.5	7	-	MHz
			V _{DD} =10V	8	16	-	MHz
			V _{DD} =15V	12	24	-	MHz
input capacitance	C _I	any input	-	5	7.5	pF	

Note: t_t is the same as t_{TLH} and t_{THL}.

4、Testing Circuit

4.1、AC Testing Circuit

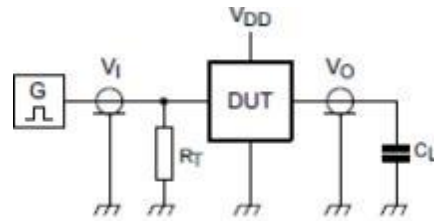


Figure 3. Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

4.2、AC Testing Waveforms

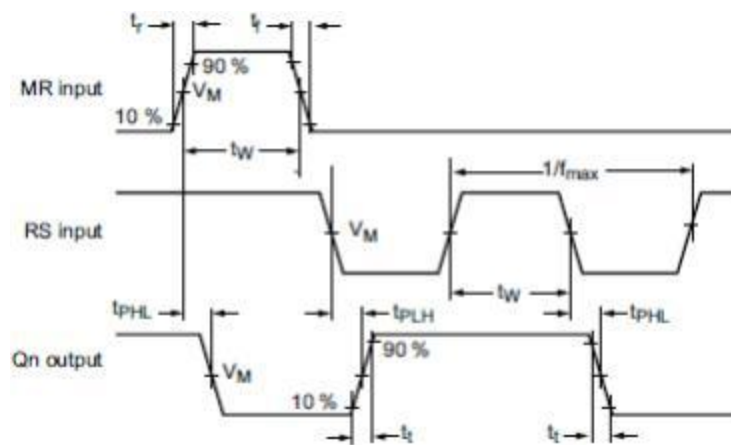


Figure 4. Waveforms showing propagation delays

4.3、Measurement Points

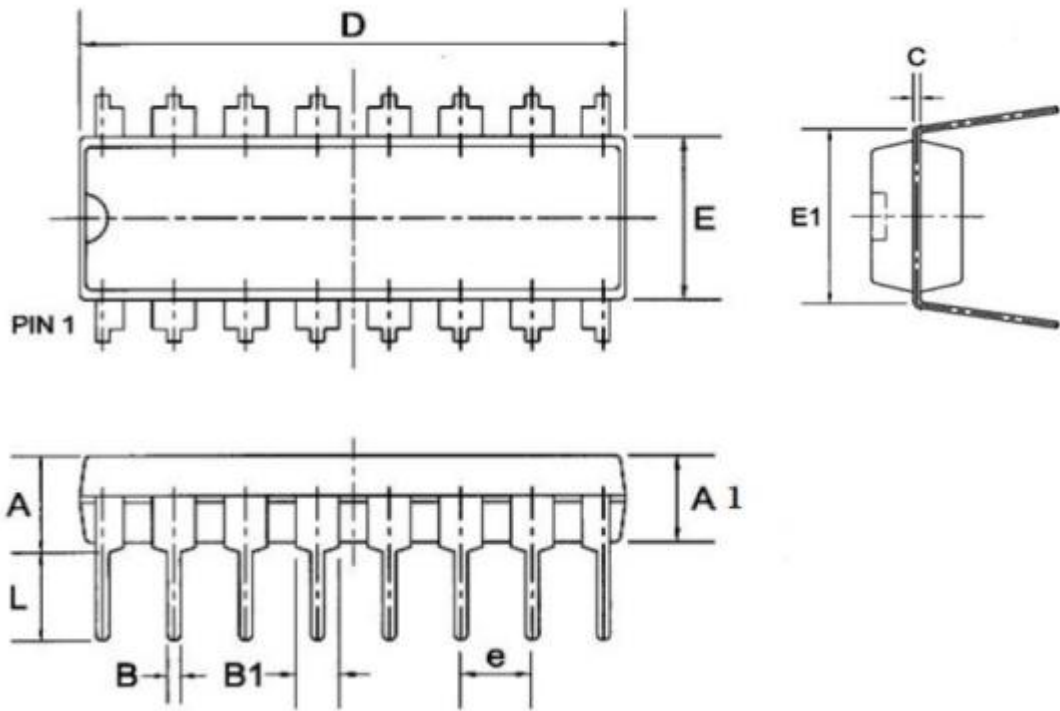
Supply voltage	Input	Output
V_{DD}	V_M	V_M
5V to 15V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$

4.4、Test Data

Supply voltage	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5V to 15V	V_{SS} or V_{DD}	$\leq 20\text{ns}$	50pF

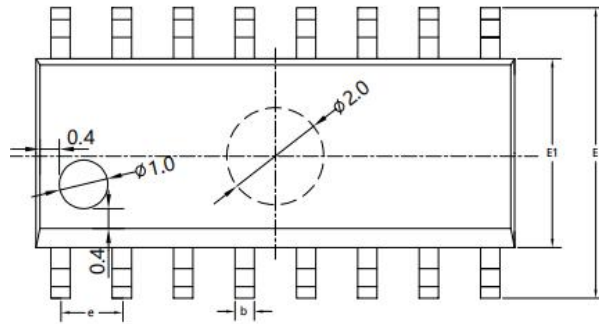
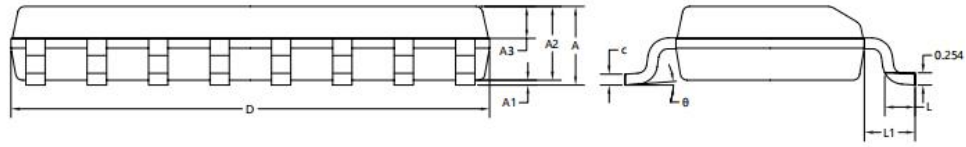
5、Package Information

5.1 DIP16



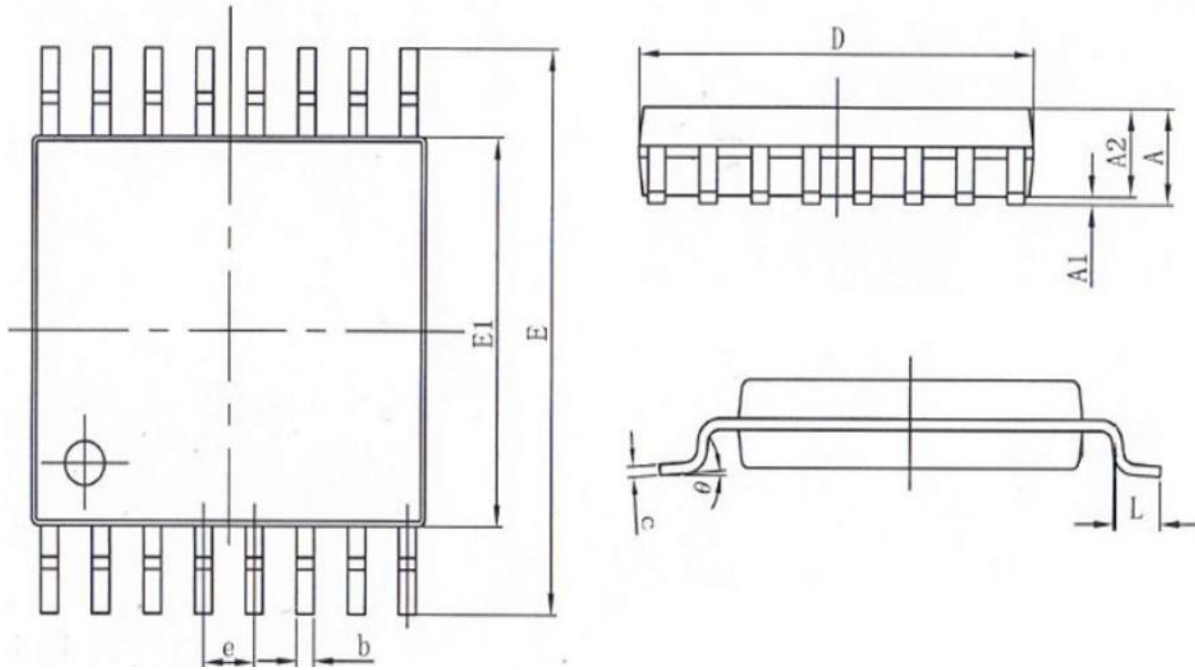
Symbol	Dimensions in Millimeters		
	Min	Nom	Max
A	--	--	4.31
A1	3.15	3.30	3.65
B	--	0.50	--
B1	--	1.6	--
C	--	0.27	--
D	19.00	19.20	19.60
E	6.20	6.50	6.60
E1	--	8.0	--
e	--	2.3	--
L	3.00	3.20	3.60

5.2 SOP16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.50	1.60	1.70
A1	0.10	0.15	0.25
A2	1.40	1.45	1.50
A3	0.60	0.65	0.70
b	0.30	0.40	0.50
c	0.15	0.20	0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.85	3.90	3.95
e	1.27BSC		
L	0.50	0.60	0.70
L1	1.05BSC		
θ	0°	4°	8°

5.3 TSSOP16



SYMBOL	MILLIMETER	
	MIN	MAX
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
θ	0°	8°

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