EMMC 规格书

XC08MAAJ-NTS

EMMC 8GB (x8) 3.3V/1.8V FBGA153Balls

深圳市芯存科技有限公司

Tel: 0755-29708864

Technical support: fae@szxincun.com

Website: www.szxincun.com

产品型号规格列表:

规格型号	FLASH 容量	BUS	工作电压	封装
XC04MAAJ-NTM	4GB	X8	3.3V/1.8V	FBGA153
XC08MAAJ-NTS	8GB	X8	3.3V/1.8V	FBGA153
XC16MAAJ-NTS	16GB	X8	3.3V/1.8V	FBGA153

版本更新记录:

Rev	Changes	Date	Note
Rev1.0	Initial release	2021.3.19	
Rev1.1	ADD 1.8V support	2022.4.26	
Rev1.2	Change LBA Date	2022.12.02	

产品特性：

- MLC Nand Flash: 8GB.
- ●嵌入式 MMC 控制器。
- ●兼容 JEDEC/MMC 标准版本 5.0/5.1(向后兼容 EMMC4.5).
- ● 擦写次数 1 万次。
- ● 可编程总线宽度 1bit(默认),4bit 8bit.

电源输入

- ●VCC: 3.3V / VCCQ:3.3V (适用于 3.3V 平台).
- ●VCC: 3.3V / VCCQ:1.8V (适用于 1.8V 平台)

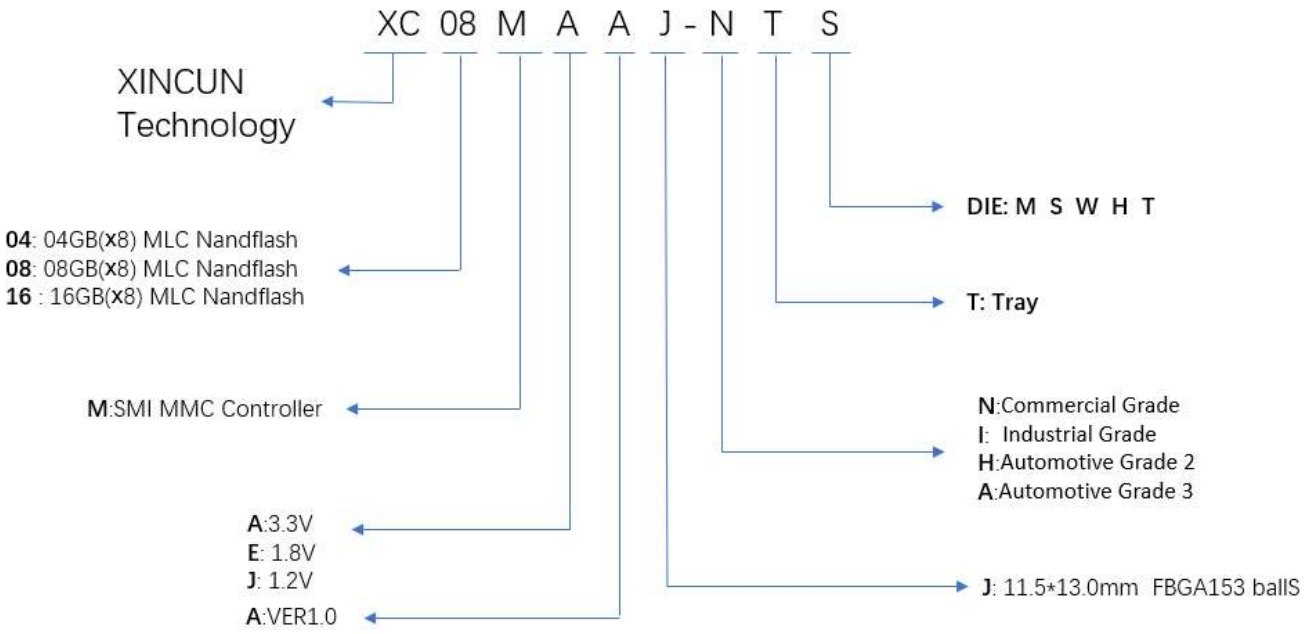
封装尺寸

- ●11.5 x 13.0 x 1.0mm.
- ●FBGA153 Balls.
- ●Ball Pitch: 0.5mm.
- ●**重量** 250mg±5mg

温度

- ●工作温度:-10 to +85 ℃.
- ●储存温度:-55 to +125 ℃.

XINCUN 命 名 规 则 说 明

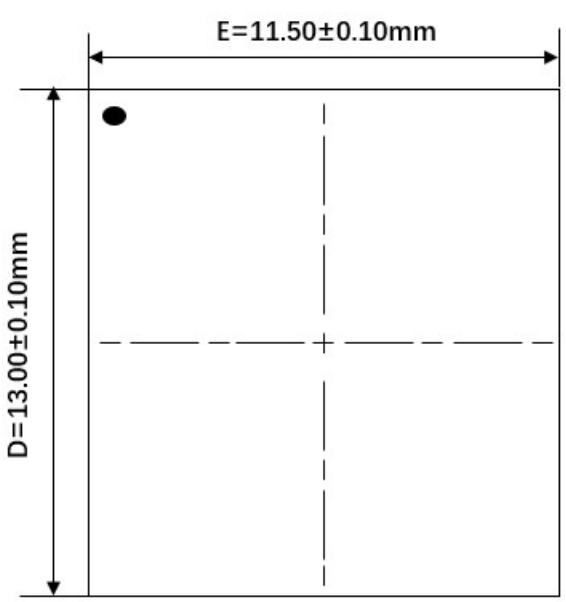


PIN CONFIGURATION

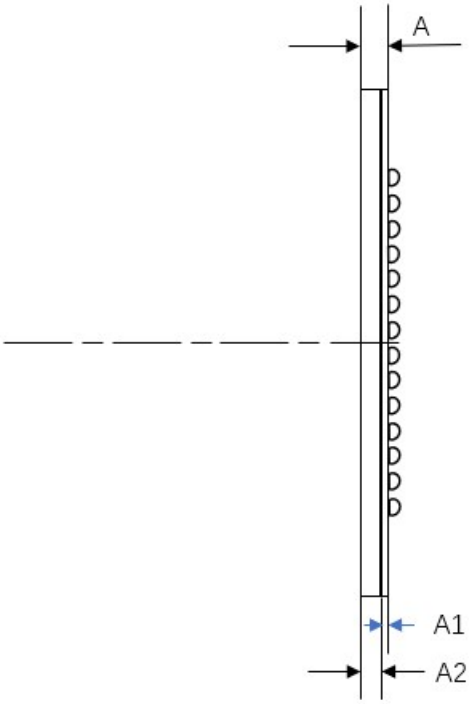
Pin Assignment

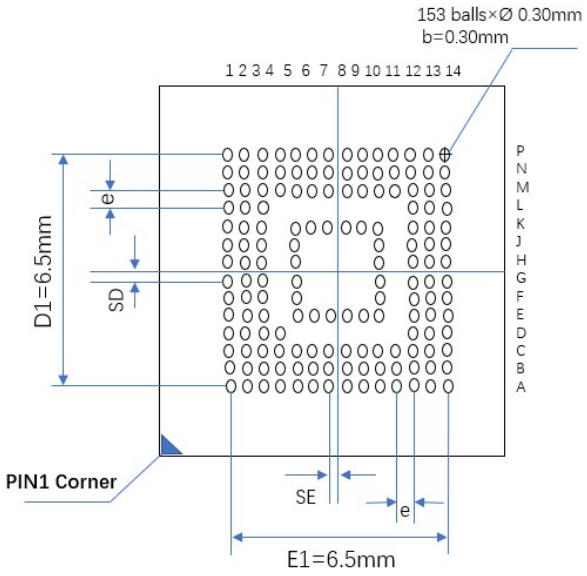
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC	NC	DAT0	DAT1	DAT2	Vss	RFU	NC	NC	NC	NC	NC	NC	NC
B	NC	DAT3	DAT4	DAT5	DAT6	DAT7	NC	NC	NC	NC	NC	NC	NC	NC
C	NC	VDDIM	NC	VssQ	RFU	VccQ	NC	NC	NC	NC	NC	NC	NC	NC
D	NC	NC	NC	NC								NC	NC	NC
E	NC	NC	NC		RFU	Vcc	Vss	RFU	RFU	RFU		NC	NC	NC
F	NC	NC	NC		Vcc					RFU		NC	NC	NC
G	NC	NC	RFU		Vss					RFU		NC	NC	NC
H	NC	NC	NC		DS					Vss		NC	NC	NC
J	NC	NC	NC		Vss					Vcc		NC	NC	NC
K	NC	NC	NC		RST_n	RFU	RFU	Vss	Vcc	RFU		NC	NC	NC
L	NC	NC	NC									NC	NC	NC
M	NC	NC	NC	VccQ	CMD	CLK	NC	NC	NC	NC	NC	NC	NC	NC
N	NC	VssQ	NC	VccQ	VssQ	NC	NC	NC	NC	NC	NC	NC	NC	NC
P	NC	NC	VccQ	VssQ	VccQ	VssQ	RFU	NC	NC	RFU	NC	NC	NC	NC

TOP VIEW

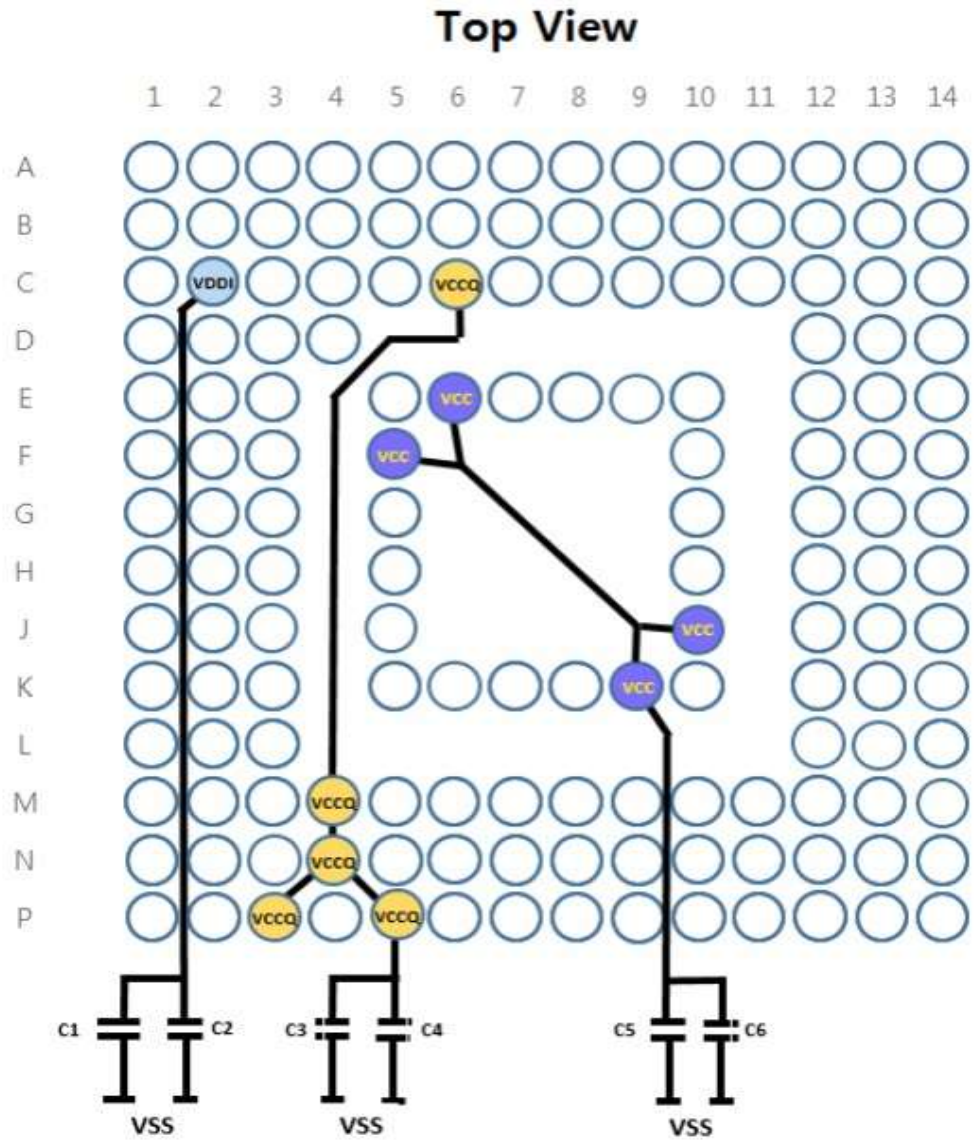


Top View





SYMBOL	DIMENSION IN mm		
	MIN	NOM	MAX
D	12.90	13.00	13.10
E	11.40	11.50	11.60
D1	-------	6.50	--------
E1	-------	6.50	--------
e	-------	0.50	--------
A	-------	--------	1.00
A1	0.15	--------	--------
A2	-------	--------	0.80
b	0.25	0.30	0.35



Paramter	Symbol	Unit	Value
V_{DDI_M}	C1 + C2	uF	4.7 + 0.1
V_{CCQ}	C3 + C4	uF	4.7 + 0.1
V_{CC}	C5 + C6	uF	10 + 0.1

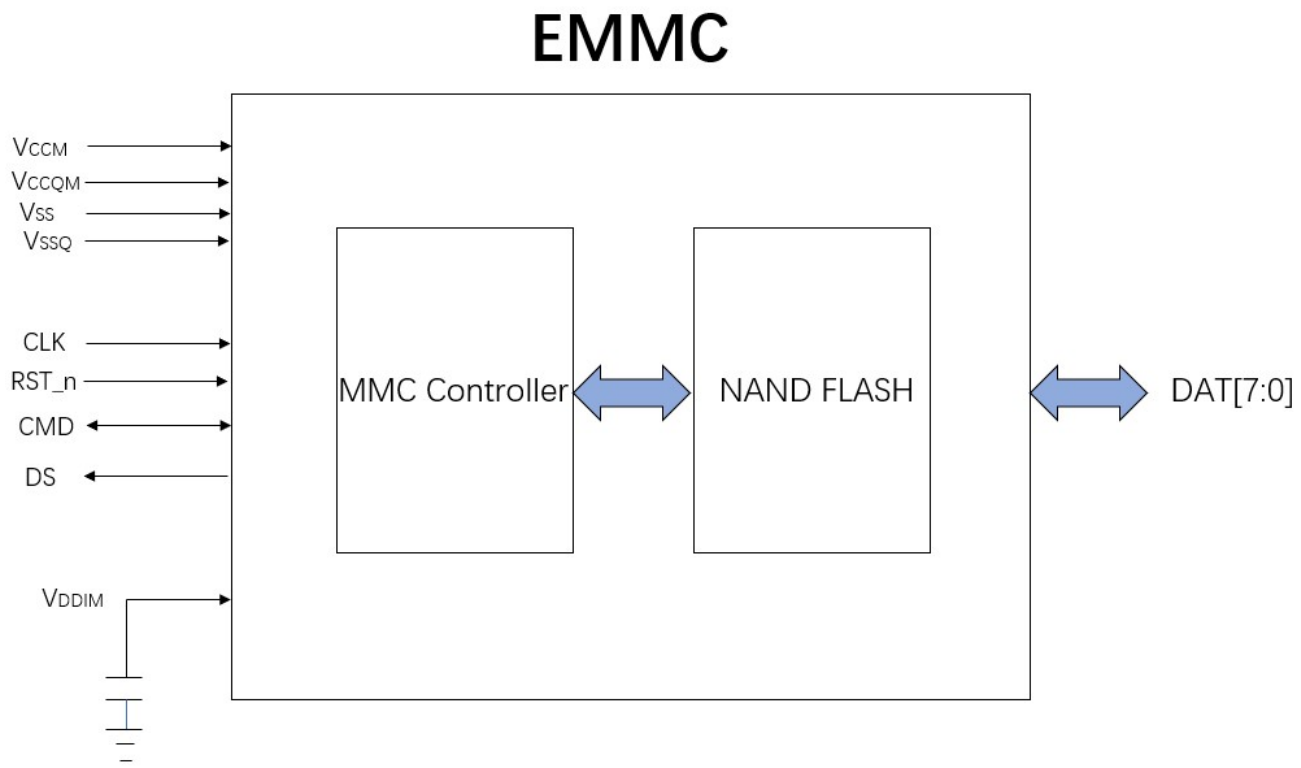
Note:

Coupling capacitor should be connected with V_{DD} and V_{SS} as closely as possible.

MMC-Specific Features

- Supports features of eMMC5.1 which are defined in JEDEC Standard
  - Supported Features : Boot, RPMB, Write Protection, DDR, HS200, Multi-partitioning, Secure Erase/Trim, Trim, HPI, Background operation, Enhance Reliable Write, Discard, Sanitize, Security features, Partition types, Packed commands, Real time clock, Dynamic device capacity, Power off notification, Thermal spec, Cache, HS400, Field Firmware Update, Security Removal type, Device Health Report, Enhanced Strobe, Command Queuing, Secure Write protection
  - Non-supported Features : Large Sector Size (4KB)
- Full backward compatibility with previous eMMC 4.41/4.5/5.0 specification
- Programmable bus width : 1bit (Default), 4bit and 8bit Data bus.
- eMMC I/F Clock Frequency : 0 ~ 200MHz eMMC I/F Boot Frequency : 0 ~ 52MHz

FUNCTION DIAGRAM



Note:

1. VSS and VSSQ are internally connected.

Pin Descriptions

Type Symbol	Description	Type Symbol	Description
I	Input	P	Power
O	Output	G	Ground
I/O	Bi-direction	X	No connect (No function, don't care)

Symbol	Type	Count	Description
DAT[7:0]	I/O	8	**Data I/O:** These are bidirectional data signals. The DAT signals operate in push-pull mode. By default,after power-on or assertion of the RST_n signal, only DAT0 is used for data transfer. TheMMC controller can configure a wider data bus for data transfer either using DAT[3:0] (4-bit mode)or DAT[7:0] (8-bit mode). The device includes internal pull-up resistors for data lines DAT[7:1]. Immediatelyafter entering
CMD	I/O	1	**Command:** This signal is a bidirectional command channel used for command and response transfers.The CMD signal has two bus modes: open-drain mode and push-pull mode. Commands aresent from the MMC host to the device, and
CLK	I	1	**Clock:** Each cycle of the clock directs a transfer on the command line and on the data line(s). Thefrequency can vary between the minimum and the maximum clock frequency.
DS	O	1	**Data strobe:** Generated by the device and used for data output and CRC status response output inHS400 mode. The frequency of this signal follows the frequency of CLK. For data output, each cycleof this signal directs two bits transfer (2x) on the data, one bit for the positive edge and the otherbit for the negative edge. For CRC
RST_n	I	1	**Reset:** The RST_n signal is used by the host for resetting the device, moving the device to the preidlestate. By default, the RST_n signal is temporarily disabled in the device. The host must set ECSDregister byte 162, bits[1:0] to 0x1 to enable this
V_{CC}	P	4	**V_{CC}:** NAND interface (I/F) I/O and NAND Flash power supply.
V_{CCQ}	P	5	**V_{CCQ}:** eMMC controller core and eMMC I/F I/O power supply.
V_{DDIM} (V_{DDI_M})	P	1	Internal voltage node. Do not tie to supply voltage or ground.
V_{SS}	G	6	**V_{SS}:** NAND I/F I/O and NAND Flash ground connection.
V_{SSQ}	G	5	**V_{SSQ}:** eMMC controller core and eMMC I/F ground connection.
RFU	X	14	**Reserved for future use:** No internal connection is present. Leave it floatingexternally.
NC	X	106	**No connect:** No internal connection is present.

EMMC

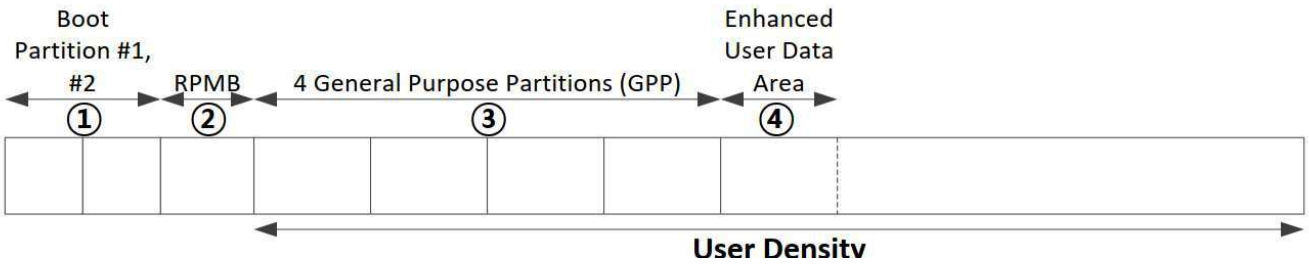
Technical Notes

HS400 Interface

Support HS400 DDR interface timing mode to achieve a bus speed of 400 MB/s at 200MHz clock frequency with 8bit bus width only. At this mode, the host may need to have an adjustable sampling point to reliably receive the incoming data, due to the speed. Please refer to JESD84-B50-1 standard for additional information.

Partition Management

The device initially consists of two Boot partitions, RPMB (Replay Protected Memory Block) partition and User Data Area. Both Boot and RPMB area have fixed size of area and can't be adjusted. Further information for re-partitioning these areas will be provided with additional application note and please contact to us.



Boot Area Partition and RPMB Area Partition

The device has fixed size of Boot and RPMB area.

Boot partition size is calculated as (128KB *BOOT_SIZE_MULT)
The size of Boot Area Partition 1 and 2 cannot be set independently. It is set as same value.
RPMB partition size is calculated as(128KB*RPMB_SIZE_MULT).
In RPMB partition, CMD 0, 6, 8, 12, 13, 15, 18, 23, 25 are admitted.

Access Size of RPMB partition is defined as the below:

Table 4-1 Setting sequence of Boot Area Partition size and RPMB Area Partition size

REL_WR_SEC_C	Description
REL_WR_SEC_C = 1	Access sizes 256B and 512B supported to RPMB partition
REL_WR_SEC_C > 1	Access sizes up to REL_WR_SEC_C * 512B supported to RPMB partition with 256B granularity

Any undefined set of parameters or sequence of commands results in failure access.
If the failure is in data programming case, the data is not programmed. And if the failure occurs in data read case, the read data is '0x00'.

Table 4-2 Capacity according to partition

Device	Boot partition 1 [KB]	Boot partition 2 [KB]	RPMB[KB]
8GB	4,096	4,096	4,096

Enhanced Partition (Area)

Xincun 8GB eMMC applies MLC Mode for Enhanced User Data Area and it leads to occupying double size of original set up size if master set some area of User Data Area as enhanced user area. For example, if master set
1MB as enhanced mode, then, total 2MB of user data area is used for it. Max Enhanced user Data Area follows below formula of JESD84-B50-1.

Max Enhanced User Data Area size is defined as (MAX_ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GRP_SIZE x 512Kbytes).

Table 4-3 Maximum Enhanced Partition Size

Device	LBA [Hex]	LBA [Dec.]	Max. Enhanced Partition Size
8GB	0x1C80	7,296	3,735,552 Bytes

User Density

As mentioned in Enhanced Partition (Area) section, total User Density depends on partition type to be set. Xincun 8GB applies MLC mode for enhanced user area and so, assigning any size for it occupies double of that value assigned. For example, assigning 64MB in the MLC mode takes 128MB of capacity in MLC.

Table 4-4 User Density Size

Device	LBA [Hex]	LBA [Dec.]	User Partition Size
8GB	0xE40048	149,429,280	7,650,410,496 Bytes

Boot operation

Device supports not only boot mode but also alternative boot mode. Device supports high speed timing and dual data rate during boot.

Figure 4-1 embedded MultiMediaCard state diagram (boot mode)

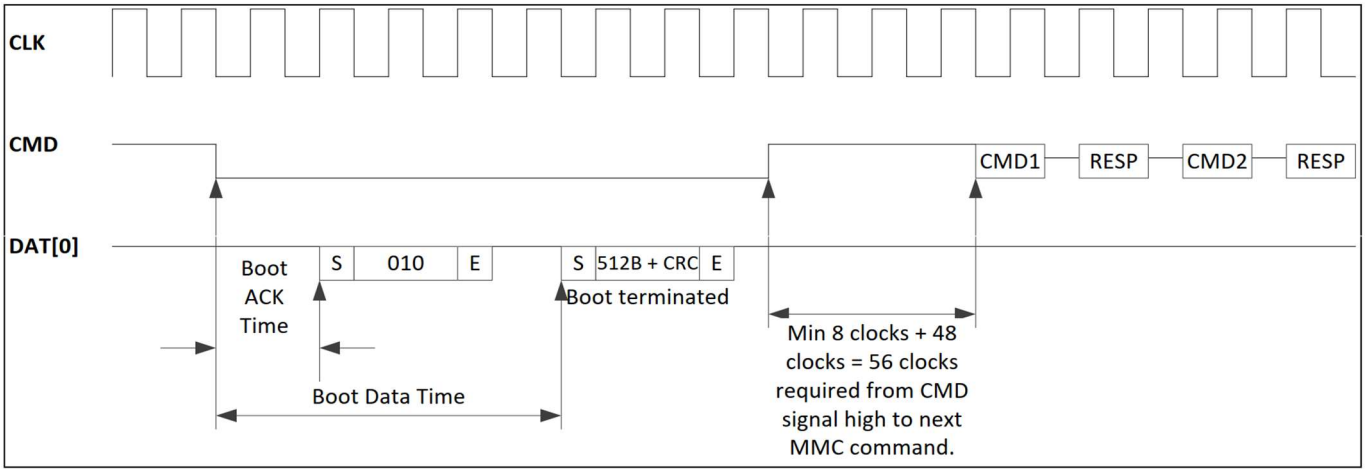


Figure 4-2 embedded MultiMediaCard state diagram (alternative boot mode)

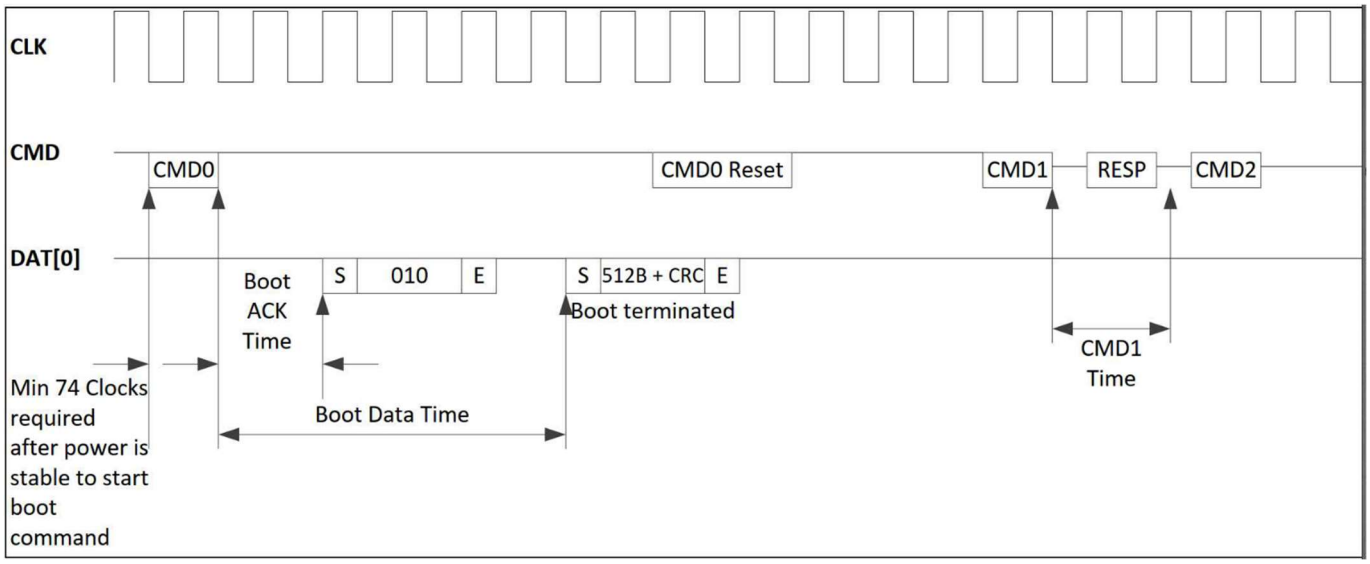


Table 4-5 Boot ack, boot data and initialization Time

Timing Factor	Value
Boot ACK Time	< 50 ms
Boot Data Time	< 1 sec
Initialization Time[1]	< 3 secs

Note:

1. The value for this initialization time is for such case which includes partition setting also. For details, please refer to INI_TIMEOUT_AP in Extended CSD Register of JESD84-B50-1.
   Normal initialization time (without partition setting) is completed within 1sec

Field Firmware Upgrade (FFU)

Field Firmware Updates (FFU) is for customer's FW updating in field for those cases of debugging, enhancing and adding new features of FW itself. The host can download a new version of the firmware into the eMMC device by this mechanism and whole FFU process can happen without affecting any user/OS data, even in parallel with Host's performing other operations.

For additional information refer to JEDEC Standards No.JESD84-B50-1.

Cache

This device supports 128KB of volatile memory as an eMMC cache for performance improvement of both sequentialand random access. For additional information please refer to JESD84-B50 standard.

Packed command

This device supports packed commands feature of eMMC standard version 5.0 and allows the host to pack Read or Write commands into groups (of single type of operation) and transfer these to the device in a single transfer on the bus, which leads reducing overall bus overheads and thus, enables optimal system performance.

Please refer to JESD84-B50 for information details.

Secure Delete Sanit ize

The device supports Sanitize operation for removing data from the unmapped user address space in the device, physically. Device keeps the sanitize operation until one of the following events occurs, with keeping busy asserted.

- Sanitize operation is complete
- HPI is used to abort the operation
- Power failure
- Hardware reset

No data should exist in the unmapped host address space after the sanitize operation is completed.

Secure Erase

This device supports the optional Secure Erase command, which is for backward compatibility reasons, as well as standard erase command. Host will erase provided range of LBAs and ensure no older copies of this data exist in the flash with this command.

Please refer to JEDEC Standards No. JESD84-B50 for more information.

Secure Trim

This device supports Secure Trim command which is similar to the Secure Erase command but different in thatperforms a secure purge operation on write blocks instead of erase groups. This is for backward compatibility reasons.

The secure trim command is performed in two steps:

1) Mark the LBA range as candidate for erase.

2) Do Erase the marked address range and then, ensure no old copies are left within that range. . For additional information refer to JEDEC Standards No. JESD84-B50.

High Priority Interrupt (HPI)

This device supports High Priority Interrupt and prevent problem of Host being stalled due to too much delayed Write operation by new paging request of operating system, by user. It will delay the request for new paging until currently going write operation is completed.

Please refer to JEDEC Standards No. JESD84-B50 for more information.

Device Health

This device supports Device Health Report feature which is featured to others in that separately report MLC type area and other area by each bytes of DEVICE_LIFE_TIME_EST_TYP_A[268] and DEVICE_LIFE_TIME_EST_TYP_A[269], respectively. It can be queried by standard MMC command for getting xtended CSD structure. Please refer to below and JEDEC Standards No. JESD84-B50 for details.

DEVICE_LIFE_TIME_EST_TYP_A[268], The host may use it to query health information of MLC area.
DEVICE_LIFE_TIME_EST_TYP_B[269], The host may use it to query health information of other partition area.

Auto Power Saving Mode

This device supports Auto Power Saving Mode which can save power consumption definitely. Device will enter this mode if host does not issue any command during 1ms, after completion of previously issued command.

Any newly issued commands during this mode will be carried normally.

Table 4-6 Auto Power Saving Mode enter and exit

Mode	Enter Condition	Escape Condition
Auto Power Saving Mode	When previous operation which came from Host is completed and no com-mand is issued during a certain time.	If Host issues any command

Table 4-7 Auto Power Saving Mode and Sleep Mode

Mode	Enter Condition	Escape Condition
NAND Power	ON	ON/OFF
GotoSleep Time	< 100ms	< 1ms

Enhanced Strobe

Supports Enhanced Strobe which is new feature of eMMC version 5.1 standard to synchronize CMD response. Host shall support this feature and it enables faster and more reliable operation.

For more information, please refer to JEDEC Standards No. JESD84-B50.

Performance

Table 4-8 Sustained Sequential Performance

Capacity (GB)	Sequential Read (MB/s)	Sequential Write (MB/s)
8	250	25

Note:

1. Test Condition: Bus width x8, HS400, 512KB data transfer, Packed Off, Cache On, w/o file system overhead.

Register Value

Following sections are for describing all register value of eMMC device at its default. And these values here may be updated in later version without notice.

There are defined total six registers in this section: OCR, CID, CSD, EXT_CSD, RCA and DSR. All of them has its own commands corresponded and for details, please refer JEDEC Standards No. JESD84-B50 for details. The OCR, CID and CSD registers has information of device and content, while the RCA and DSR registers are for configuring parameters of device. For the EXT_CSD register, it contains both device specific information and actual configuration parameters.

OCR Register

The operation conditions register (OCR) contains: V_{CC} voltage profile of the device, access mode indication, status information bit. The status bit is set when the device finished its power up procedure. All eMMC devices shall have this register implemented.

Table 4-9 OCR Register

OCR bit	V_{CCQ} Voltage Window[2]	Register Value
[6:0]	Reserved	00 00000b
[7]	1.70 ~ 1.95	1b
[14:8]	2.0 ~ 2.6	000 0000b
[23:15]	2.7 ~ 3.6	1 1111 1111b
[28:24]	Reserved	0 0000b
[30:29]	Access Mode	00b (byte mode) -[2GB] 10b (sector mode) -[*Higher than 2GB only]
[31]	eMMC power up status bit (busy)[1]	

Notes:

1. This bit is set to LOW if the eMMC has not finished the power up routine.
2. The voltage for internal flash memory (V_{CC}) should be 2.7 ~ 3.6V regardless of OCR register value.

CID Register

The device Identification (CID) register is 128bits wide. It contains the device identification information used during the device identification phase (eMMC protocol). eMMC device shall have a unique identification number.

Users can define their own CID register and the CID contents will be programmed into the eMMC device when firmware fusing process. After the programming is complete, end users cannot change CID, unless the whole foundry production program is re-done. Users can install the new downloaded firmware into the device by using FFU (Field Firmware Update) mode.

Table 4-10 CID Register

Name	Field	Width	CID-slice	CID Value
Manufacturer ID	MID	8	[127:120]	0xAD
Reserved		6	[119:114]	–
Card/BGA	CBX	2	[113:112]	0x01
OEM/Application ID	OID	8	[111:104]	–
Product name	PNM	48	[103:56]	–
Product revision	PRV	8	[55:48]	–
Product serial number	PSN	32	[47:16]	–[3]
Manufacturing date	MDT	8	[15:8]	–[1]
CRC7 checksum	CRC	7	[7:1]	–[1]
not used, always '1'	–	1	[0:0]	–

Notes:

1. Tdescription are same as eMMC JEDEC standard.
2. PRV is composed of the revision count of controller and the revision count of F/W patch.
3. A 32 bits unsigned binary integer. (Random Number).

Product name table (In CID Register)

Table 4-11 Product name table

Part Number	Density (GB)	PKG Type
XC08MAAJ-NTS	8	11.5x13.0x1.0

RCA Register

The writable 16-bit relative device address (RCA) register carries the device address assigned by the host during the device identification. This address is used for the addressed host-device communication after the device identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all devices into the Stand-by State with CMD7.

CSD Register

The device Specific Data (CSD) register provides information on how to access the device contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E) can be changed by CMD27.

The CSD register defines the behavior or of eMMC devices. The eMMC behavior is related to the controller design. The following table shows a typical CSD definition of XC08MAAJ-NTS based eMMC. If users need to add on more features, firmware or hardware modifications may be necessary.

※Note that the register values are preliminary data and may be updated in a later version. And the updated value will be supported by specified application note later.

Table 4-12 Typical CSD Register

Name	Field	Bit	Type	Slice	Value	Note
CSD structure	CSD_STRUCTURE	2	R	[127:126]	0x03	
System specification version	SPEC_VERS	4	R	[125:122]	0x04	
Reserved	–	2	R	[121:120]	–	
Data read access-time	TAAC	8	R	[119:112]	0x27	
Data read access-time in CLK cycles (NSAC x 100)	NSAC	8	R	[111:104]	0x01	
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	0x32	
Device command classes	CCC	12	R	[95:84]	0x8F5	
Max. read data block length	READ_BL_LEN	4	R	[83:80]	0x09	
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0x00	
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0x00	
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0x00	
DSR implemented	DSR_IMP	1	R	[76:76]	0x00	
Reserved	–	2	R	[75:74]	–	
Device size	C_SIZE	12	R	[73:62]	0xFFF	
Max read current@VCCQ min	VCCQ_R_CURR_MIN	3	R	[61:59]	0x07	
Max read current@VCCQ max	VCCQ_R_CURR_MAX	3	R	[58:56]	0x07	
Max write current@VCCQ min	VCCQ_W_CURR_MIN	3	R	[55:53]	0x07	
Max write current@VCCQ max	VCCQ_W_CURR_MAX	3	R	[52:50]	0x07	
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	0x07	
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	0x1F	
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	0x1F	
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0x0F	
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	0x01	
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0x00	
Write speed factor	R2W_FACTOR	3	R	[28:26]	0x02	

Table 4-12 Typical CSD Register (Continued)

Name	Field	Bit	Type	Slice	Value	Note
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	0x09	
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0x00	
Reserved	–	4	R	[20:17]	–	
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0x00	
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0x00	
Copy flag (OTP)	COPY	1	R/W	[14:14]	0x01	
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0x00	
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0x00	
File format	FILE_FORMAT	2	R/W	[11:10]	0x00	
ECC code	ECC	2	R/W/E	[9:8]	0x00	
CRC	CRC	7	R/W/E	[7:1]	–	
Not used, always '1'	–	1		[0:0]	–	

Note:

1.The type of the CSD Registry entries in the Table 4-12 is coded as follows. R: Read only.

W: One time programmable and not readable

R/W: One time programmable and readable

W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.

R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.

R/W/C_P: Writable after value cleared by power failure and HW/rest assertion (the value not cleared by CMD0 reset) and readable.

R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.

W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

Extended CSD Register (EXT_CSD)

The Extended CSD register defines the additional behavior of eMMC devices due to limited CSD information. The following table shows a typical extended CSD definition of XC08MAAJ-NTS based eMMC. If users need to add on more features, firmware or hardware modifications may be necessary.

※Notethat the register values are preliminary data and may be updated in a later version. And the updated value will be supported by specified application note later.

Table 4-13 Typical EXT_CSD Register

Name	Field	Byte	Type	Slice	Value	Note
Properties Segment						
Reserved	–	6	–	[511:506]	–	
Extended security	EXT_SECURITY_ERR	1	R	[505]	0x00	
Supported command sets	S_CMD_SET	1	R	[504]	0x01	
HPI features	HPI_FEATURES	1	R	[503]	0x01	
Background operations support	BKOPS_SUPPORT	1	R	[502]	0x01	
Max packed read commands	MAX_PACKED_READS	1	R	[501]	0x3F	
Max packed write commands	MAX_PACKED_WRITES	1	R	[500]	0x3F	
Data tag support	DATA_TAG_SUPPORT	1	R	[499]	0x01	
Tag unit size	TAG_UNIT_SIZE	1	R	[489]	0x08	
Tag resources size	TAG_RES_SIZE	1	R	[497]	0x00	
Context management capabilities	CONTEXT_CAPABILITIES	1	R	[496]	0x05	
Large unit size	LARGE_UNIT_SIZE_M1	1	R	[495]	0x07	
Extended partitions attribute support	EXT_SUPPORT	2	R	[494]	0x03	
Supported modes	SUPPORTED_MODES	1	R	[493]	0x01	
FFU features	FFU_FEATURES	1	R	[492]	0x00	
Operation codes timeout	OPERATION_CODE_TIMEOUT	1	R	[491]	0x10	
FFU Argument	FFU_ARG	4	R	[490:487]	0x00	
Barrier Support	BARRIER_SUPPORT	1	R	[486]	0x01	
Reserved	–	181	–	[485:309]	–	
CMD Queuing Support	CMDQ_SUPPORT	1	R	[308]	0x01	
CMD Queuing Depth	CMDQ_DEPTH	1	R	[307]	0x1F	
Reserved	–	1	–	[306]	–	
Number of FW sectors correctly programmed	NUMBER_OF_FW_ SECTOR S_CORRECTLY_ PROGRAM MED	4	R	[305:30]	0x00	
Vendor proprietary health report	VENDOR_PROPRIETARY_ HEALTH_REPORT	32	R	[301:270]	0x00	
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP _B	1	R	[269]	0x01	Other area except
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP _A	1	R	[268]	0x01	MLC type area

Table 4-13 Typical EXT_CSD Register (Continued)

Name	Field	Byte	Type	Slice	Value	Note
Properties Segment						
Pre EOL information	PRE_EOL_INFO	1	R	[267]	0x01	
Optimal read size	OPTIMAL_READ_SIZE	1	R	[266]	0x00	
Optimal write size	OPTIMAL_WRITE_SIZE	1	R	[265]	0x04	
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	0x03	
Device version	DEVICE_VERSION	2	R	[263:262]	0x00	
Firmware version	FIRMWARE_VERSION	8	R	[261:254]	→	TBD
Power class for 200MHz, DDR at 3.6V	PWR_CL_DDR_200_360	1	R	[253]	0x77	
Cache size	CACHE_SIZE	4	R	[252:249]	→	0x00000400
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	0x0A	
Power off notification(long) timeout	POWER_OFF_LONG_TIME	1	R	[247]	0x3C	
Background operations status	BKOPS_STATUS	1	R	[246]	0x00	
Number of correctly programmed	CORRECTLY_PRG_SECTORS	4	R	[245:242]	→	0x00000000
1st initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	0x1E	
Cache Flushing Policy	CACHE_FLUSH_POLICY	1	R	[240]	0x01	
Power class for 52MHz, DDR at 3.6V	PWR_CL_DDR_52_360	1	R	[239]	0x77	
Power class for 52 MHz, DDR at 1.95V	PWR_CL_DDR_52_195	1	R	[238]	0x77	
Power class for 200 MHz at 1.95V	PWR_CL_200_195	1	R	[237]	0x77	
Power class for 200 MHz, at 1.3V	PWR_CL_200_130	1	R	[236]	0x00	
Minimum write performance for 8 bit at 52 MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	0x00	
Minimum read performance for 8 bit at 52 MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	0x00	
Reserved	–	1	–	[233]	0x00	
TRIM multiplier	TRIM_MULT	1	R	[232]	0x02	
Secure feature support	SEC_FEATURE_SUPPORT	1	R	[231]	0x55	
Secure erase multiplier	SEC_ERASE_MULT	1	R	[230]	0x0A	
Secure trim multiplier	SEC_TRIM_MULT	1	R	[229]	0x0A	
Boot information	BOOT_INFO	1	R	[228]	0x07	
Reserved	–	1	–	[227]	–	
Boot partition size	BOOT_SIZE_MULTI	1	R	[226]	0x20	

Table 4-13 Typical EXT_CSD Register (Continued)

Name	Field	Byte	Type	Slice	Value	Note
Properties Segment						
Access size	ACC_SIZE	1	R	[225]	0x06	
High-capacity erase unit siz	HC_ERASE_GRP_SIZE	1	R	[224]	0x01	
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	0x02	
Reliable write sector count	REL_WR_SEC_C	1	R	[222]	0x01	
High-capacity write protect	HC_WP_GRP_SIZE	1	R	[221]	0x10	
Sleep current (V_{CC})	S_C_VCC	1	R	[220]	0x07	
Sleep current (V_{CCQ})	S_C_VCCQ	1	R	[219]	0x07	
Product state awareness timeout	PRODUCTION_STATE_ AWARENESS_TIMEOUT	1	R	[218]	0x0A	
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	0x12	
Sleep notification timeout	SLEEP_NOTIFICATION_TIME	1	R	[216]	0x10	
Sector count	SEC_COUNT	4	R	[215:212]	→	8GB
Secure Write Protect Information	SECURE_WP_INFO	1	R	[211]	0x01	
Minimum write performance for 8bit at 52MHz	MIN_PERF_W_8_52	1	R	[210]	0x00	
Minimum read performance	MIN_PERF_R_8_52	1	R	[209]	0x00	
Minimum write performance for 8bit at 26MHz,	MIN_PERF_W_8_26_4_52	1	R	[208]	0x00	
Minimum read performance for 8bit at 26MHz,	MIN_PERF_R_8_26_4_52	1	R	[207]	0x00	
Minimum write performance for 4bit at 26MHz	MIN_PERF_W_4_26	1	R	[206]	0x00	
Minimum read performance for 4bit at 26MHz	MIN_PERFR_4_26	1	R	[205]	0x00	
Reserved	–	1	–	[204]	–	
Power class or 26 MHz at 3.6V 1 R	PWR_CL_26_360	1	R	[203]	0x77	
Power class for 52 MHz at 3.6V 1 R	PWR_CL_52_360	1	R	[202]	0x77	
Power class for 26 MHz at 1.95V 1	PWR_CL_26_195	1	R	[201]	0x77	
Power class for 52 MHz at 1.95V 1 R	PWR_CL_52_195	1	R	[200]	0x77	
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	0x01	
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	0x64	

Table 4-13 Typical EXT_CSD Register (Continued)

Name	Field	Byte	Type	Slice	Value	Note
Properties Segment						
I/O Driver Strength CSD structure version	DRIVER_STRENGTH	1	R	[197]	0x1F	
Device type	DEVICE_TYPE	1	R	[196]	0x57	
Reserved	–	1	–	[195]	–	
CSD structure version	CSD_STRUCTURE	1	R	[194]	0x02	
Reserved	–	1	–	[193]	–	
Extended CSD revision	EXT_CSD_REV	1	R	[192]	0x08	
Modes Segment						
Command set	CMD_SET	1	R/W/E_P	[191]	0x00	
Reserved	–	1	–	[190]	–	
Command set revision	CMD_SET_REV	1	R	[189]	0x00	
Reserved	–	1	–	[188]	–	
Power class	POWER_CLASS	1	R/W/E_P	[187]	0x00	
Reserved	–	1	–	[186]	–	
High speed interface timing	HS_TIMING	1	R/W/E_P	[185]	0x01	
Strobe Support	STROBE_SUPPORT-	1	-R	[184]	0x01	
Bus width mode	BUS_WIDTH	1	W/E_P	[183]	0x00	
Reserved	–	1	–	[182]	–	
Erased memory content	ERASED_MEM_CONT	1	R	[181]	0x00	
Reserved	–	1	–	[180]	–	
Partition configuration	PARTITION_CONFI	1	R/W/E &	[179]	0x00	
Boot config protection	BOOT_CONFIG_PROT	1	R/W &	[178]	0x00	
Boot bus conditions	BOOT_BUS_CONDITIONS	1	R/W/E	[177]	0x00	
Reserved	–	1	–	[176]	–	
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	[175]	0x00	
Boot write protection status registers	BOOT_WP_STATU	1	R	[174]	0x00	
Boot area write protection register	BOOT_WP	1	R/W &	[173]	0x00	
Reserved	–	1	–	[172]	–	
User area write protection register	USER_WP	1	R/W, R/W/C_P &	[171]	0x00	
Reserved	–	1	–	[170]	–	

Table 4-13 Typical EXT_CSD Register (Continued)

Name	Field	Byte	Type	Slice	Value	Note
Modes Segment						
FW configuration	FW_CONFIG	1	R/W	[169]	0x00	
RPMB size	RPMB_SIZE_MULT	1	R	[168]	0x20	
Write reliability setting register	WR_REL_SET	1	R/W	[167]	0x1F	
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	0x14	
Start sanitize operation	SANITIZE_START	1	W/E_P	[165]	0x00	
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0x00	
Enable background	BKOPS_EN	1	R/W	[163]	0x00	
H/W reset function	RST_n_FUNCTION	1	R/W	[162]	0x00	
HPI management	HPI_MGMT	1	R/W/E_P	[161]	0x00	
Partitioning support	PARTITIONING_SUPPORT	1	R	[160]	0x07	
Max enhanced area size	MAX_ENH_SIZE_MULT	3	R	[159:157]	0xEC	8GB
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0x00	
Partitioning setting	PARTITION_SETTING_ COMPLETED	1	R/W	[155]	0x00	
General purpose partition size	GP_SIZE_MULT	12	R/W	[154:143]	0x00	
Enhanced user data area size	ENH_SIZE_MULT	3	R/W	[142:140]	0x00	
Enhanced user data start address	ENH-START_ADDR	4	R/W	[139:136]	0x00	
Reserved	–	1	–	[135]	–	
Bad block management mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	0x00	
Production state awareness	PRODUCTION_ STATE_AWARENESS	1	R/W/E	[133]	0x00	
Package case temperature is controlled	TCASE_SUPPORT	1	W/E_P	[132]	0x00	
Periodic wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	0x00	
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_ DDR_SUPPORT	1	R	[130]	0x01	
Reserved	–	2	–	[129:128]	–	
Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	64		[127:64]	0x00	
Native sector size	NATIVE_SECTOR_SIZE	1	R	[63]	0x00	
Sector size emulation	USE_NATIVE_SECTOR	1	R/W	[62]	0x00	
Sector size	DATA_SECTOR_SIZE	1	R	[61]	0x00	
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	[60]	0x00	

Table 4-13 Typical EXT_CSD Register (Continued)

Name	Field	Byte	Type	Slice	Value	Note
Modes Segment						
Class 6 commands control	CLASS_6_CTRL	1	R/W/E_P	[59]	0x00	
Number of addressed group to be released	DYNCAP_NEEDED	1	R	[58]	0x00	
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	0x00	
Exception events status	EXCEPTION_EVENTS_ STATUS	2	R	[55:54]	0x00	
Extended partitions attribute	EXT_PARTITIONS_ATTRIBUTE	2	R/W	[53:52]	0x00	
Context configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	0x00	
Packed command status	PACKED_COMMAND_STATUS	1	R	[36]	0x00	
Packed command failure index	PACKED_FAILURE_INDEX	1	R	[35]	0x00	
Power off notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	0x00	
Control to turn the cache ON/OF	CACHE_CTRL	1	R/W/E_P	[33]	0x00	
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	0x00	
Reserved	–	1	–	[31]	–	
Mode config	MODE_CONFIG	1	R/W/E_P	[30]		
Mode operation codes	MODE_OPERATION_CODES	1	W/E_P	[29]	0x00	
Reserved	–	2	–	[28:27]	–	
FFU status	FFU_STATUS	1	R	[26]	0x00	
Pre loading data size	PRE_LOADING_ DATA_SIZE	4	R/W/E_P	[25:22]	→	8GB
Max pre loading data size	MAX_PRE_LOADING_ DATA_SIZE	4	R	[21:18]	→	8GB (003B0000)
Product state awareness enablement	PRODUCT_STATE_ AWARENESS_ ENABLEMENT	1	R/W/E & R	[17]	0x03	
Secure removal type	SECURE_REMOVAL_TYPE	1	R/W/E & R	[16]	0x09	
Command Queue Mode Enable	CMDQ_MODE_EN	1	R/W/E_P	[15]	0x00	
Reserved	–	15	–	[14:0]	–	

Notes:

1. The following is for the type of the EXT_CSD Register entries in the Table 4-14. R: Read only.
   W: One time programmable and not readable. R/W: One time programmable and readable.
   W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
   R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
   R/W/C_P: Writable after value cleared by power failure and HW/reset assertion (the value not cleared by CMD0 reset) and readable.
   R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
   W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

AC Parameter

Timing Parameter

Table 4-14 Timing Parameter

Timing Paramter		Max. Value
Initialization Time (tINIT)	Normal [1]	1 sec
	After partition setting [2]	3 sec
Read Timeout		100 ms
Write Timeout		350 ms
Erase Timeout		20 ms
Force Erase Timeout		3 min
Secure Erase Timeout		6 sec
Secure Trim step Timeout		6 sec
Trim Timeout		600 ms
Partition Switching Timeout (after Init)		10 ms
Power Off Notification (Short) Timeout		100 ms
Power Off Notification (Long) Timeout		600 ms

Notes:

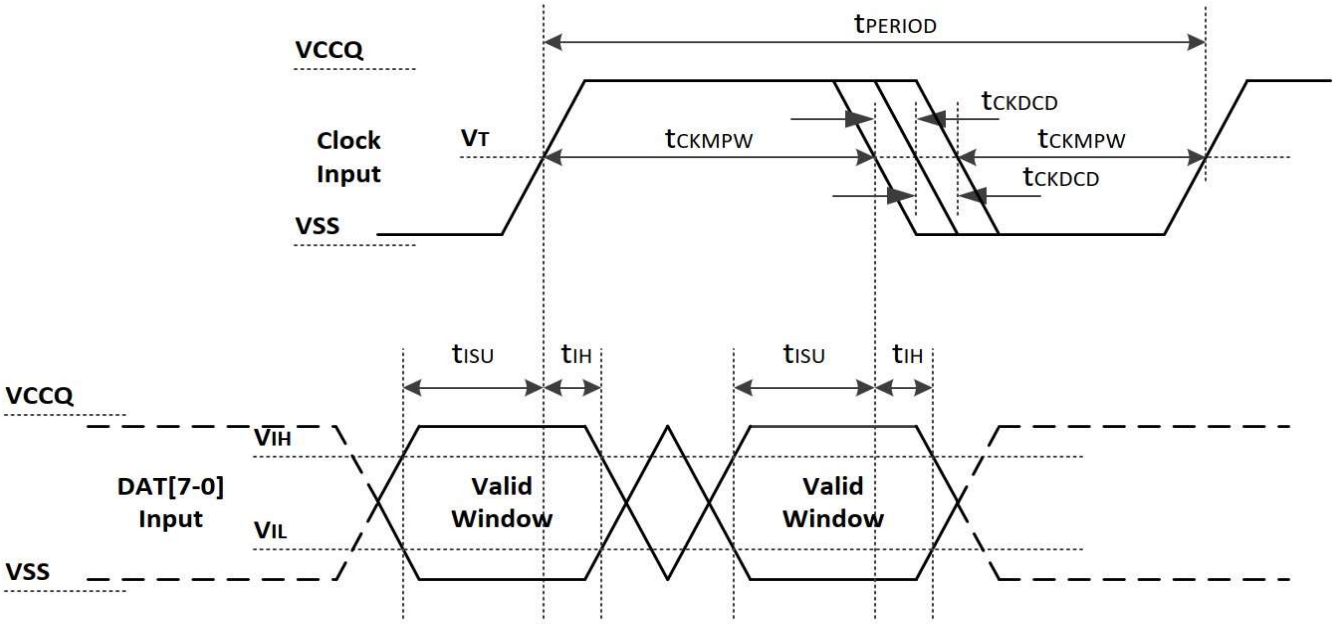
1.Normal Initialization Time without partition setting.

2.For the Initialization Time after partition setting, refer to INI_TIMEOUT_AP in EXT_CSD register.

3.All those Timeout Values specified in the above Table are only for testing purposes under specific test case only and it can vary in real cases. Also, it may be affected may vary due to user environment.

Bus Timing Specification in HS400 mode
HS400 Device Input Timing

Figure 4-3 HS400 Device Input Timing Diagram



Notes:

1.t_{ISU} and t_{IH} are measured at $V_{IL\ (max)}$ and $V_{IH\ (min)}$.

2.V_{IH} denotes $V_{IH\ (min)}$ and V_{IL} denotes $V_{IL\ (max)}$.

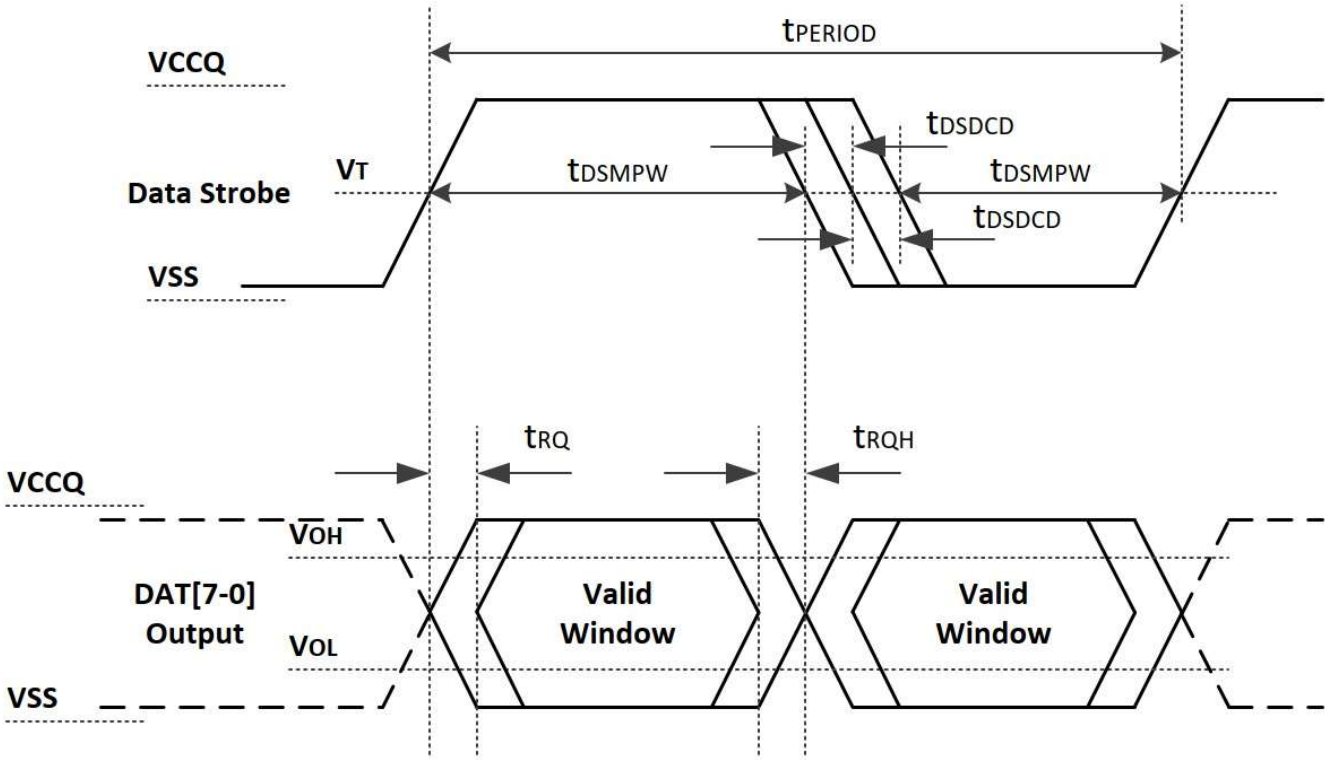
Table 4-15 HS400 Device Input Timing

Paramter	Symbol	Min	Max	Unit	Remark
Input CLK					
Cycle time datatransfer mode	t_{PERIOD}	5	–	ns	200MHz(Max), betweenwith respect to V_T.
Slew rate	SR	1.125	–	V/ns	
Duty cycle distortion	t_{CKDCD}	0.0	0.3	ns	
Minimum pulse width	t_{CKMPW}	2.2	–	ns	
Input DAT (referenced to CLK)					
Input set-up time	t_{ISUddr}	0.4	–	ns	
Input hold time	t_{IHddr}	0.4	–	ns	
Slew rate	SR	1.125	–	V/ns	

HS 400 Device Onput Timing

Data Strobe is used to read data (data read and CRC status response read) in HS400 mode. The device output value of Data Strobe is “High-Z” when the device is not in outputting data (data read, CRC status response). Data Strobe is toggled only during data read period.

Figure 4-4 HS400 Device Output Timing Diagram



Note:

1. VOH denotes VOH (min) and VOL denotes VOL (max).

Table 4-16 HS400 DeviceOutput Timing

Paramter	Symbol	Min	Max	Unit	Remark
Data Strobe					
Cycle time datatransfer mode	t_{PERIOD}	5	–	ns	200MHz(Max), betweenwith respect to V_T.
Slew rate	SR	1.125	–	V/ns	
Duty cycle distortion	t_{CKDCD}	0.0	0.2	ns	
Minimum pulse width	t_{CKMPW}	2.0	–	ns	
Read pre-amble	t_{RPRE}	0.4	–	t_{PERIOD}	
Read post-amble	t_{RPST}	0.4	–	t_{PERIOD}	
Output DAT (referenced to Data Strobe)					
Output skew	t_{RQ}	–	0.4	ns	
Output hold skew	t_{RQH}	–	0.4	ns	
Slew rate	SR	1.125	–	V/ns	

Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

Figure 4-5 Bus Signal Levels

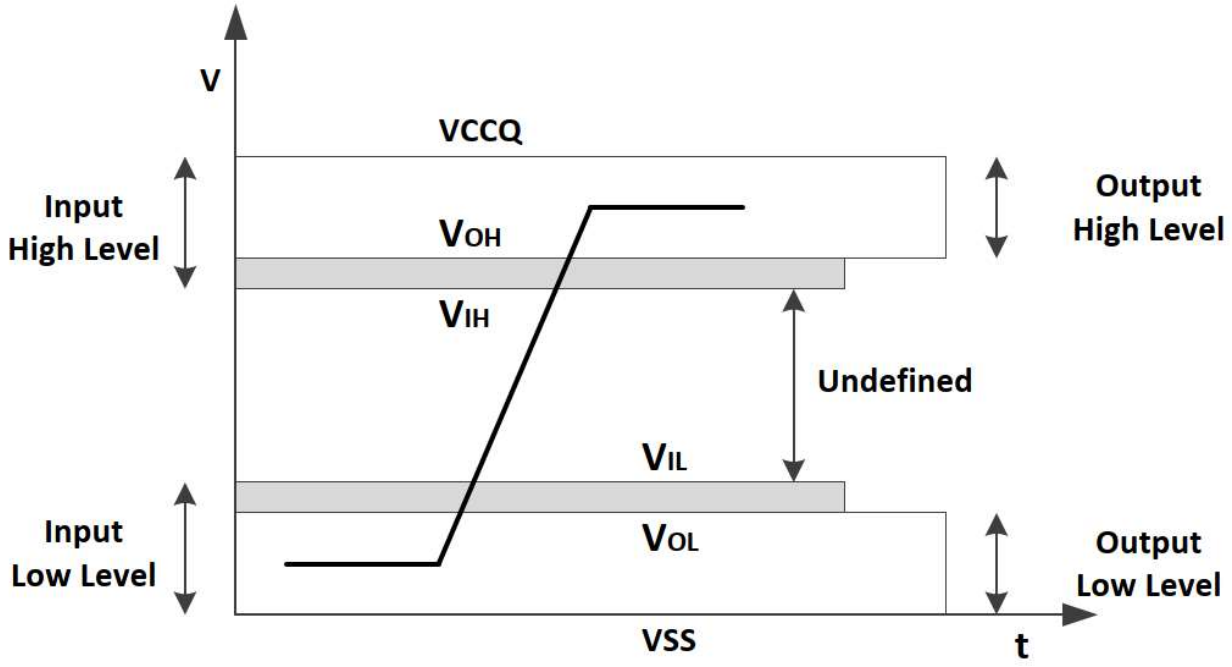


Table 4-17 Bus Signal Levels

Paramter	Symbol	Min	Max	Unit	Remark
Open-drain mode					
Output HIGH voltage	V_{OH}	V_{CCQ} – 0.2	–	V	
Output LOW voltage	V_{OL}	–	0.3	V	I_{OL} = TBD
Push-pull mode (High-voltage eMMC)					
Output HIGH voltage	V_{OH}	0.75 x V_{CCQ}	–	V	I_{OH} = –100uA @ V_{CCQ} min
Output LOW voltage	V_{OL}	–	0.125 x V_{CCQ}	V	I_{OL} = 100uA @ V_{CCQ} min
Input HIGH voltage	V_{IH}	0.625 x V_{CCQ}	V_{CCQ} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} – 0.3	0.25 x V_{CCQ}	V	

DC Parameter

Power Consumption

Table 4-18 Active Power Consumption during operation

Density (GB)	NAND Type (MLC)	CTRL (Max RMSmA)	NAND (Max RMS,mA)
8	64Gb x1	120	120

Notes:

1.Power Measurement conditions: Bus configuration =x8 @200MHz DDR.

2.Typical value is measured at V_{CC}/V_{CCQ}=3.3V, TA=25°C. Not 100% tested.

3.The measurement for max RMS current is the average RMS current consumption over a period of 100ms.

Table 4-19 Standby Power Consumption in auto power saving mode and standby state

Density (GB)	NAND Type (MLC)	CTRL (Ave. RMS, uA)		NAND (Max RMS,mA)	
		25°C (Typ)	85°C	25°C (Typ)	85°C
8	64Gb x1	130	800	40	50

Notes:

1.Power Measurement conditions: Bus configuration =x8, No CLK.

2.Typical value is measured at V_{CC}/V_{CCQ}=3.3V, TA=25°C. Not 100% tested.

Table 4-20 Sleep Power Consumption in Sleep State

Density (GB)	NAND Type (MLC)	CTRL (uA)		NAND (uA)
		25°C (Typ)	85°C	
8	64Gb x1	130	800	TBD [3]

Notes:

1.Power Measurement conditions: Bus configuration =x8, No CLK.

2.Typical value is measured at V_{CC}/V_{CCQ}=3.3V, TA=25°C. Not 100% tested.

3.In auto power saving mode, NAND power can not be turned off, However in sleep mode NAND power can be turned off. If NAND power is alive, NAND power is same with that of the Standby state.

Supply Voltage

Table 4-21-A Supply Voltage Suitable for 3.3V platform

Symbol	Min (V)	Max (V)
V_{CCQ}	2.7	3.6
V_{CC}	2.7	3.6
V_{SS}	-0.5	0.5

Table 4-21-B Supply Voltage Suitable for 1.8V platform

Symbol	Min (V)	Max (V)
V_{CCQ}	1.7	1.9
V_{CC}	2.7	3.6
V_{SS}	-0.5	0.5

Bus Signal Line Load

The total capacitance CL of each line of the eMMC bus is the sum of the bus master capacitance CHOST, the bus capacitance CBUS itself and the capacitance CDEVICE of the eMMC connected to this line:

$$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$$

The sum of the host and bus capacitances should be under 20pF.

Table 4-22 Bus SIgnal Line Load

Paramter	Symbol	Min	Typ	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7		100	KOhm	to prevent bus floating
Pull-up resistance for DAT0-DAT7	R_{DAT}	10		100	KOhm	to prevent bus floating
Internal pull up resistance DAT1-DAT7	R_{int}	10		150	KOhm	to prevent unconnected lines floating
Single Device capacitance	C_{DEVICE}			6	pF	
Maximum signal line inductance				16	nHV	f_{PP}<= 52 MHz

Table 4-23 Capacitance and Resistance for HS400 mode

Paramter	Symbol	Min	Typ	Max	Unit	Remark
Bus signal line capacitance	C_L			13	pF	Single Device
Single Device capacitance	C_{DEVICE}			6	pF	
Pull-down resistance for Data Strobe	$R_{Data\ Strobe}$	10		100	KOhm	

Power Delivery And Capacitor Specifications

Power Domains

Xincun 8GB eMMC has three power domains assigned to V_{CCQ}, V_{CC} and V_{DDI_M}, as shown below.

Table 4-24 Power Domains

Symbol	Power Domain	Comments
V_{CCQ}	Host Interface	
V_{CC}	Memory	
V_{DDI_M}	Internal	V_{DDI_M} is the internal regulator connection to an external decoupling capacitor.

Capacitor Connection Guidelines

It is recommended to place the following capacitors on V_{CC} & V_{CCQ} domains:

- C_1/C_3= 4.7uF

◆ E.g. :

Manufacturer	Manufacturer P/N
MURATA	GRM185R60J475ME15D
TAIYO YUDEN	JMK107BJ475MK-T

● C_2/C_4/C_6= 0.1uF

◆ E.g. :

Manufacturer	Manufacturer P/N
MURATA	GRM155R71A104KA01D
KYOCERA	CM05X5R104K06AH

For V_{CC} (3.3V), it is recommended to place:

● C_5 (V_{CC}) = 10uF

◆ E.g. :

Manufacturer	Manufacturer P/N
TAIYO YUDEN	JMK107ABJ106MAHT
PANASONIC	ECJ-1VB0J106M
SAMSUNG	CL10A106MQ8NNNC

Capacitors Type:

● SMT-Ceramic
● X5R
● 6.3V
● Min height – 0.55mm
● Foot Print: 0402 or above

Suggested capacitors should be located as close to the supply ball as possible and they will eliminate as much trace inductance effects as possible and give cleaner voltage supply to device. Also, they reduce lead length and eliminate noise coupling onto through-hole components, which may have effects of antenna.

Make all of the power (high current) traces as short, direct, and thick as possible and put all capacitors as close to each other as possible, for reducing EMI radiated by the power traces due to the high switching currents through them. Again, it shall also reduce lead inductance and resistance as well and thus, noise spikes, ringings, and resistive losses which cause voltage errors.

For the ground of these capacitors, they should be connected close together directly to a ground plane and it is also recommended to have a ground plane on both sides of the PCB, to reduce noise by eliminating ground loop errors as well.

The loop inductance per capacitor shall not exceed 3nH (both on V_{CC}/V_{CCQ} & V_{SS} loops). Multiple via connections are recommended per each capacitor pad.

Signal Traces:

● Data, CMD, CLK & RCLK bus trace length mismatch should be minimal (up to +/-1mm).
● Traces should be 50ohm controlled impedance.

http//www.szxincun.com