

DATA SHEET

ULTRA LOW CAPACITANCE PROTECTION DEVICE

UE0402

RoHS compliant & Halogen free



YAGEO Phicomp

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UE

SERIES

0402

SCOPE

This specification describes UE0402 has a typical capacitance of only 0.07pF (I/O to GND), and it can be used to meet the ESD immunity requirement of IEC61000-4-2 (15KV air, 8KV contact discharge).

YAGEO Phicomp

<u>APPLICATIONS</u>

- High Definition Multi-Media Interface
- (HDMI)
- Digital Visual Interface (DVI)
- Display Port Interface (DP)
- Unified Display Interface (UDI)
- Mobile Display Digital Interface (MDDI)
- Gigabit Ethernet
- USB2.0 and USB3.0
- IEEE1394 interface

FEATURES

- Halogen Free Epoxy
- ESD protection for high speed data lines to
- IEC61000-4-2
- ESD contact discharge typical 8KV, max I5KV
- ESD air discharge typical I5KV, max 25KV
- Surface mount
- Extremely low capacitance
- Very low leakage current
- Fast response time
- Bi-directional ESD protection
- Lead free solder termination
- The best ESD protection for high frequency,
- low voltage applications

ORDERING INFORMATION - GLOBAL PART NUMBER

Part number is identified by the series name, size, clamping voltage, trigger voltage, packaging type, capacitance, taping reel, working voltage.

GLOBAL PART NUMBER (PREFERRED)

UE0402 X X X - XX XX X

(1) (2) (3) (4) (5) (6) (7)

(I) CLAMPING VOLTAGE

E = 35V

(2) TRIGGER VOLTAGE

C = 350V

(3) PACKAGING TYPE

R = Paper taping reel

(4) CAPACITANCE

- = Base on spec

(5) TAPING REEL

07 = 7 inch dia Reel

7D = 7 inch reel with double quantity

(6) WORKING VOLTAGE

15V = 15V

(7) DEFAUL CODE

Letter L is system default code for ordering only

ORDERING EXAMPLE

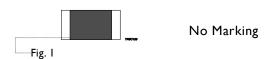
The ordering code for a UE00402 clamping voltage 35V, trigger voltage 350V ESD suppressor working voltage 15V, supplied in 7-inch tape reel with IOKpcs quantify is: UE00402CR-0715VL.



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MARKING

UE0402



CONSTRUCTION

The ESD suppressors are constructed out of a highgrade ceramic body. Internal metal electrode is cut a kerf into two parts which are connected by ESD absorbent paste. The ESD absorbent layer is covered with protective coat. Finally, the two external terminations (matte tin) are added. See Fig. 2.

DIMENSIONS

Table I

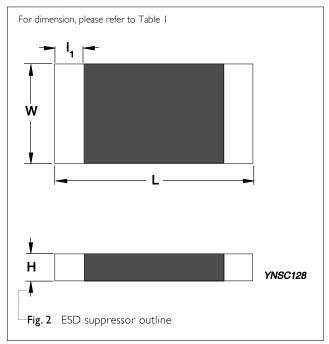
TYPE L (mm) W (mm) H (mm) I₁ (mm) **UE0402** 1.00 ±0.05 0.50 ±0.05 0.35 ±0.05 0.25 ±0.15

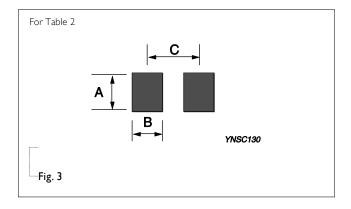
RECOMMENDED FOOTPRINT DIMENSIONS

Table 2

SIZE FOOTPRINT	Dimensions	code	(unit: mm)
UE0402	Α	В	С
000002	0.60	0.50	1.00

OUTLINES







Chin	Da	oiot	OH	CIII	food	IIA/II	Ount
Chip	nt	:919t	Uľ	our	latt		UUIIL

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ABSOLUTE MAXIMUM RATINGS

Table 3

PARAMETER	VALUE
Maximum Contact discharge voltage Per IEC61000-4-2	I5KV
Maximum Air discharge voltage Per IEC61000-4-2	25KV
Maximum Operating temperature(TOPER)	-55°C to +125°C
Maximum temperature for soldering during 10s (TL)	260°C

<u>ELECTRICAL CHARACTERISTICS</u> (TA=25°C)

Table 4

CHARACTERISTICS	UE0402
Rated Voltage (V _R)	I5V (Max)
Trigger Voltage (V₁)	350V (Typical)
Clamping Voltage (Vc)	35V (Typical)
Leakage current (IL)	I 0nA (Typical)
Capacitance (C _P)	0.07pF(typical)

NOTE:

- 1. Trigger and clamping voltage are measured per IEC 61000-4-2, 8KV contact discharge method.
- 2. After reliability tests such as high temp storage, temp cycles, continuous ESD strike etc, the maximum leakage current is less than 10uA.
- 3. Capacitance is measured at VR=0V, f=IMHZ

PACKING STYLE AND PACKAGING QUANTITY

Table 5 Packing style and packaging quantity

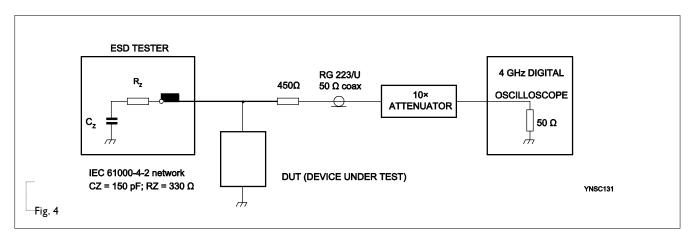
PACKING STYLE	REEL DIMENSION	UE0402	
Paper taping reel (R)	7" (178 mm)	10,000	

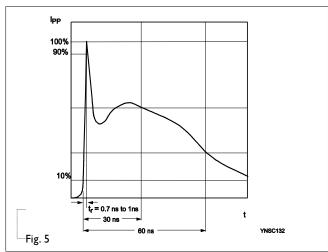


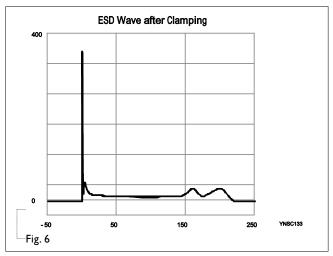
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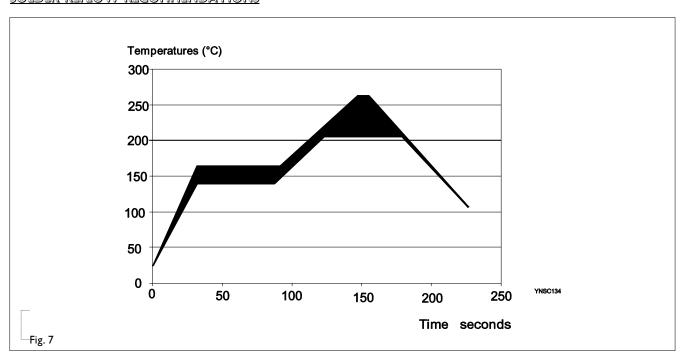
ESD CLAMPING TEST







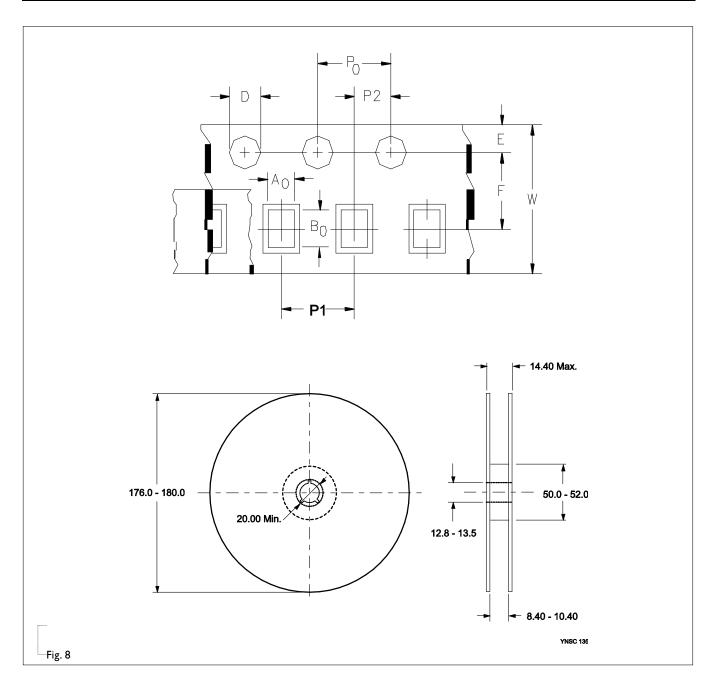
SOLDER REFLOW RECOMMENDATIONS



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PACKAGE INFORMATION

Dimension	A0	В0	D	P0	PI	P2	Е	F	W
Typical (mm)	0.65	1.15	1.50	4.00	2.00	2.00	1.75	3.50	8.00





Chip Resistor Surface Mount

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TESTS AND REQUIREMENTS

Table 6 Test condition, procedure and requirements

TEST	REFERENCE STANDARD	TEST CONDITION	SPECIFICATION
Operating temperature		-55 °C to 125°C	IL =10µ A
Bending	IEC 60068-2-21	3 mm deflection	_
Resistance of solder heat	IEC 60068-2-58	$260 \pm 5^{\circ}$ C for 10 ± 1 sec	_
Thermal shock	MIL-STD-202G Method-107G	-55°C to 125°C, 5 cycles	_
Solderability	IPC/JEDEC J-STD-002B test B	$245 \pm 5^{\circ}\text{C}$ solder, 2 ± 0.5 sec dwell.	95% coverage
		Solder: Sn96.5/Ag3.0/Cu0.5	
Capacitance		VR=0V, f=1MHZ	0.07pF (typical)



Chip Resistor Surface Mount UE SERIES 0402

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Product specification

REVISION HISTORY

REVISION DATE CHANGE NOTIFICATION DESCRIPTION

Nov. 28, 2014-Version 0 - First issue of this specification

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