



DATA SHEET SURFACE-MOUNT CERAMIC MULTILAYER CAPACITORS

Low-Inductance

X5R / X7R 6.3 V TO 50 V 10 nF to 1 uF

RoHS compliant & Halogen Free



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6.3V to 50V

SCOPE

This specification describes LW revised low ESL chips multilayer ceramic capacitors with lead-free terminations

APPLICATIONS

High speed IC packages

Processor package decoupling

AC noise reduction in multi-chip modules.

FEATURES

Supplied in tape on reel Nickel-barrier end termination **RoHS** compliant Halogen Free compliant

ORDERING INFORMATION - GLOBAL PART NUMBER, PHYCOMP CTC

All part numbers are identified by the series, size, tolerance, TC material, packing style, voltage, process code, termination and capacitance value.

YAGEO BRAND ordering code

GLOBAL PART NUMBER (PREFERRED)

CL <u>xxxx x x x xxx x</u> BB <u>xxx</u> (2) (3) (4) (5) (1) (6)

(I) SIZE – INCH BASED (METRIC)

0204(0510) 0306(0816) 0508(1220) 0612(1632)

(2) TOLERANCE

 $K = \pm 10\%$

 $M = \pm 20\%$

(3) PACKING STYLE

- R = Paper/PE taping reel; Reel 7 inch
- K = Blister taping reel; Reel 7 inch
- P = Paper/PE taping reel; Reel 13 inch
- F = Blister taping reel; Reel 13 inch

(4) TC MATERIAL

X5R / X7R

(5) RATED VOLTAGE

- 5 = 6.3 V 6 = 10 V
- 7 = 16 V
- 8 = 25 V
- 9 = 50 V

(6) CAPACITANCE VALUE

2 significant digits+number of zeros

The 3rd digit signifies the multiplying factor, and letter R is decimal point

Example: $121 = 12 \times 10^{1} = 120 \text{ pF}$

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ctrod

CONSTRUCTION

The capacitor consists of a rectangular block of ceramic dielectric in which a number of interleaved metal electrodes are contained. This structure gives rise to a high capacitance per unit volume.

The inner electrodes are connected to the two end terminations and finally covered with a layer of plated tin (NiSn). The terminations are lead-free. A cross section of the structure is shown in Fig. I.

Table I For outlines see fig. 2

DIMENSION

TYPE	l (mm))(/()	T ()	L ₂ / L ₃	L ₄ (mm)	
TYPE	L _I (mm)	W (mm)	T (mm)	min.	max.	min.
0204	0.5 ±0.1	1.0 ±0.1	0.3 ±0.05	0.1	0.3	0.1
0306	0.8 ±0.15	1.6 ±0.2	0.5 ±0.1	0.1	0.3	0.2
0508	1.25 ±0.2	2.0 ±0.2	0.85 ±0.1	0.13	0.46	0.38
0612	1.6 ±0.2	3.2 ±0.2	0.85 ±0.1	0.13	0.46	0.50
0612*	1.6 ±0.2	3.2 ±0.2	1.15 ±0.1	0.13	0.46	0.50

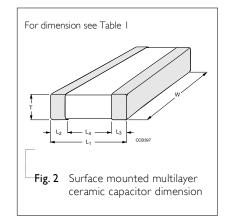
0612*: luF/16V, 470nF~luF/25V, 120nF~470nF/50V



ceramic material

-Fig. I Surface mounted multilayer ceramic capacitor construction

terminations



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CAPACITANCE RANGE & THICKNESS FOR X5R

Table 2	Sizes from 0204
CAP.	0204 6.3 V / 10V
I0 nF	0.3 ±0.05
15 nF	0.3 ±0.05
22 nF	0.3 ±0.05
33 nF	0.3 ±0.05
47 nF	0.3 ±0.05
68 nF	0.3 ±0.05
100 nF	0.3 ±0.05
150 nF	
220 nF	
330 nF	
470 nF	
680 nF	
l uF	

NOTE

I. Values in shaded cells indicate thickness class in mm



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CAPACITANCE RANGE & THICKNESS FOR X7R

Table 3	Sizes from 0306 to 05	08		
CAP.	0306	0508		
	6.3 V / 10V	6.3V/10V	16 V	25 V
I0 nF	0.5 ±0.1	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1
15 nF	0.5 ±0.1	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1
22 nF	0.5 ±0.1	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1
33 nF	0.5 ±0.1	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1
47 nF	0.5 ±0.1	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1
68 nF	0.5 ±0.1	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1
100 nF	0.5 ±0.1	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1
150 nF	0.5 ±0.1	0.85 ±0.1	0.85 ±0.1	
220 nF	0.5 ±0.1	0.85 ±0.1	0.85 ±0.1	
330 nF				
470 nF		0.85 ±0.1		
680 nF				
l uF		0.85 ±0.1		

NOTE

I. Values in shaded cells indicate thickness class in mm



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Product specification $\frac{6}{18}$

CAPACITANCE RANGE & THICKNESS FOR X7R

Table4	Sizes from 0612				
CAP.	0612				
. <u> </u>	6.3 V	10 V	16 V	25 V	50 V
10 nF	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1
I5 nF	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1
22 nF	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1
33 nF	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1
47 nF	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1
68 nF	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1
100 nF	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1
150 nF	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1	1.15 ±0.1	1.15 ±0.1
220 nF	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1	1.15 ±0.1	1.15 ±0.1
330 nF	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1	1.15 ±0.1	1.15 ±0.1
470 nF	0.85 ±0.1	0.85 ±0.1	0.85 ±0.1	1.15 ±0.1	1.15 ±0.1
680 nF	1.15 ±0.1	1.15 ±0.1	1.15 ±0.1	1.15 ±0.1	
l uF	1.15 ±0.1	1.15 ±0.1	1.15 ±0.1	1.15 ±0.1	

ΝΟΤΕ

I. Values in shaded cells indicate thickness class in mm

THICKNESS CLASSES AND PACKING QUANTITY

Table 5

SIZE	THICKNESS	TAPE WIDTH -			Ø330 MN	1 / 13 INCH	QUANTITY
CODE	CLASSIFICATION	QUANTITY PER REEL	Paper	Blister	Paper	Blister	PER BULK CASE
0204	0.3 ±0.05 mm	8 mm	10,000				
0306	0.5 ±0.1 mm	8 mm	4,000		15,000		
0508	0.85 ±0.1 mm	8 mm	4,000		15,000		
0612	0.85 ±0.1 mm	8 mm	4,000		15,000		
0612	1.15 ±0.1 mm	8 mm		3,000			

Surface-Mount Ceramic Multilayer Capacitors Low ASR, X7R 6.3V to 50V

ELECTRICAL CHARACTERISTICS

X7R DIELECTRIC CAPACITORS

Unless otherwise specified, all test and measurements shall be made under standard atmospheric conditions for testing as given in 5.3 of IEC 60068-1:

- Temperature: 15 $\degree\,$ C to 35 $\degree\,$ C
- Relative humidity: 25% to 75%
- Air pressure: 86 kPa to 106 kPa

Before the measurements are made, the capacitor shall be stored at the measuring temperature for a time sufficient to allow the entire capacitor to reach this temperature.

The period as prescribed for recovery at the end of a test is normally sufficient for this purpose.

Table 6	
DESCRIPTION	VALUE
Capacitance range	I0 nF to I uF
Capacitance tolerance	
X5R / X7R	±10%, ±20%
Dissipation factor (D.F.)	
X5R / X7R	≤ 5 %
Insulation resistance after 1 minute at U _r (DC)	$R_{ins} \ge 10 \text{ G}\Omega \text{ or } R_{ins} \times C \ge 500 \Omega \cdot F$ whichever is less
Maximum capacitance change as a function of temperature (temperature characteristic/coefficient):	
X5R / X7R	±15%
Operating temperature range:	
X5R	–55 °C to +85 °C
X7R	–55 °C to +125 °C

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SOLDERING RECOMMENDATION

Table 7				
SOLDERING	SIZE			
METHOD	0204	0306	0508	0612
Reflow				
Reflow/Wave	0	0	0	0

TESTS AND REQUIREMENTS

 Table 8
 Test procedures and requirements

TEST	TEST METHOD		PROCEDURE	REQUIREMENTS		
Mounting	IEC 4.3 60384- 21/22		The capacitors may be mounted on printed-circuit boards or ceramic substrates	No visible damage		
Visual Inspection and Dimension Check		4.4	Any applicable method using × 10 magnification	In accordance with specification		
Capacitance		4.5.1	f = 1 KHz, measuring at voltage 1 Vrms at 20 °C	Within specified tolerance		
Dissipation Factor (D.F.)		4.5.2	f = 1 KHz, measuring at voltage 1 Vrms at 20 °C	In accordance with specification		
Insulation Resistance		4.5.3	At Ur (DC) for I minute	In accordance with specification		

TEST	TEST METHC	D	PROCEDURE	REQUIREMENTS	
Temperature coefficient			Capacitance shall be measured by the steps shown in the following table. The capacitance change should be measured after 5 min at each specified temperature stage. $\boxed{\begin{array}{c c} Step & Temperature(^{\circ}C) \\ a & 25\pm2 \\ \hline b & Lower temperature\pm3^{\circ}C \\ \hline c & 25\pm2 \\ \hline d & Upper Temperature\pm2^{\circ}C \\ \hline e & 25\pm2 \\ \hline \end{array}}$ Capacitance Change shall be calculated from the formula as below $\Delta C = \frac{C2 - C1}{C1} \times 100\%$ C1: Capacitance at step c C2: Capacitance at step b or d	X7R/X5R : Δ C/C : ±15% In case of applying voltage, the capacitance change should be measured after 1 more min with applying voltage in equilibration of each temp. stage.	
Adhesion	IEC 60384- 21/22	4.7	A force applied for 10 seconds to the line joining the terminations and in a plane parallel to the substrate	Force size ≥ 0306: 5N size = 0204: 2.5N	
Bending Strength	4.8		Mounting in accordance with IEC 60384-22 paragraph 4.3	No visible damage	
Strength			=		

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TEST	test Method		PROCEDURE	REQUIREMENTS
Resistance to Soldering Heat	2	4.9	Precondition: 150 +0/–10 °C for 1 hour, then keep for 24 ±1 hours at room	Dissolution of the end face plating shall not exceed 25% of the length of the edge concerned
			temperature Preheating: I20 °C to I50 °C for I minute and I70 °C to 200 °C for I minute.	ΔC/C X7R/X5R : ±10%
			Solder bath temperature: 260 ±5 °C Dipping time: 10 ±0.5 seconds Recovery time: 24 ±2 hours	D.F. within initial specified value R _{ins} within initial specified value
Solderability	2	4.10	Preheated the temperature of 80 °C to 140 °C and maintained for 30 seconds to 60 seconds.	The solder should cover over 95% of the critical area of each termination
			Test conditions for leadfree containing solder alloy Temperature: 245 ±5 °C Dipping time: 3 ±0.3 seconds Depth of immersion: 10 mm	
Rapid Change of Temperature	IEC 4	4.11	Preconditioning; 150 +0/–10 °C for 1 hour, then keep for _	No visual damage
	21/22		24 \pm 1 hours at room temperature	∆C/C X7R/X5R : ±15%
			5 cycles with following detail: 30 minutes at lower category temperature 30 minutes at upper category temperature	X W X X X X X X X X X X X X X X X X X X
			Recovery time 24 ±2 hours	D.F. meet initial specified value R _{ins} meet initial specified value

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Surface-Mount Ceramic Multilayer Capacitors Low Inductance X5R, X7R 6.3V to 50V

TEST	TEST METH	IOD	PROCEDURE	REQUIREMENTS
Damp Heat with Ur Ioad		4.13	 Preconditioning, class 2 only: 150 +0/-10 °C /1 hour, then keep for 24 ±1 hour at room temp Initial measure: Spec: refer initial spec C, D, IR Damp heat test: 500 ±12 hours at 40 ±2 °C; 90 to 95% R.H; 1.0 Ur applied. Recovery: 24 ±2 hours Final measure: C, D, IR P.S. If the capacitance value is less than the minimum value permitted, then after the other measurements have been made the capacitor shall be precondition according to <i>"IEC 60384 4.1"</i> and then the requirement shall be met. 	No visual damage after recovery $\Delta C/C$ $< 1 \mu F : \pm 15\%$ $\ge 1 \mu F : \pm 20\%$ D.F. $\le 2 \times \text{specified value}$ R_{ins} $\ge 500 \text{ M}\Omega \text{ or } R_{\text{ins}} \times C_r \ge 25\Omega \cdot \text{F}$ whichever is less
Endurance	IEC 60384- 21/22	4.14	 Preconditioning, 150 +0/-10 °C /1 hour, then keep for 24 ±1 hour at room temp Initial measure: Spec: refer initial spec C, D, IR Endurance test: Temperature: Specified stress voltage applied for 1,000 hours: Applied 2.0 × U_r for general product Recovery time: 24 ±2 hours Final measure: C, D, IR P.S. If the capacitance value is less than the minimum value permitted, then after the other measurements have been made the capacitor shall be precondition according to "IEC 60384 4.1" and then the requirement shall be met. 	No visual damage $\Delta C/C$ $< 1 \text{ uF} : \pm 15\%$ $\geq 1 \text{ uF} : \pm 20\%$ D.F. $\leq 2 \times \text{ initial value max}$ R_{ins} $\geq 1,000 \text{ M}\Omega \text{ or}$ $R_{\text{ins}} \times Cr \geq 50\Omega \cdot \text{F whichever is less}$
Voltage Proof	IEC 60384-1	4.5.4	Specified stress voltage applied for 1 to 5 seconds $U_r \le 100$ V: series applied 2.5 U_r Charge/Discharge current less than 50mA	No breakdown or flashover

Surface-Mount Ceramic Multilayer Capacitors X5R, X7R 6.3V to 50V

PAPER/PE TAPE SPECIFICATION

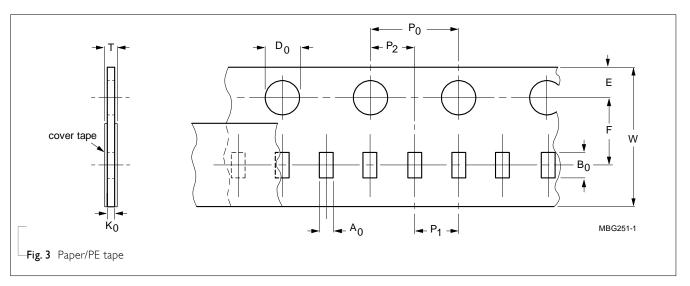


Table 9 Dimensions of paper/PE tape for relevant chip size; see Fig.3

SIZE	SYMBOL Unit										Unit: mm
CODE	A ₀	B ₀	W	E	F	$P_0^{(1)}$	PI	P ₂	ØD ₀	K ₀	Т
0204	0.70 ± 0.15	1.21 ± 0.12	8.0 ± 0.20	1.75 ± 0.1	3.50 ± 0.05	4.0 ± 0.05	2.0 ± 0.05	2.0 ± 0.05	1.50 +0.1 /-0	(0.75 / 0.60)±0.10	(0.85 / 0.70)±0.10
0306	1.05 ± 0.14	1.86 ± 0.13	8.0 ± 0.20	1.75 ± 0.1	3.50 ± 0.05	4.0 ± 0.10	4.0 ± 0.10	2.0 ± 0.05	1.50 +0.1 /-0	(1.05 / 0.95 / 0.75)±0.10	(1.15 / 1.05 / 0.85)±0.10
0508	1.50 ± 0.15	2.26 ± 0.20	8.0 ± 0.20	1.75 ± 0.1	3.50 ± 0.05	4.0 ± 0.10	4.0 ± 0.10	2.0 ± 0.05	1.50 +0.1 /-0	(1.05 / 0.95 / 0.75)±0.10	(1.15 / 1.05 / 0.85)±0.10
0612	1.90 ± 0.15	3.50 ± 0.20	8.0 ± 0.20	1.75 ± 0.1	3.50 ± 0.05	4.0 ± 0.10	4.0 ± 0.10	2.0 ± 0.05	1.50 +0.1 /-0	(0.95 / 0.75)±0.10	(1.05 / 0.85)±0.10

NOTE

1. P_0 pitch tolerance over any 10 pitches is $\pm 0.2 \mbox{ mm}$

REEL SPECIFICATION

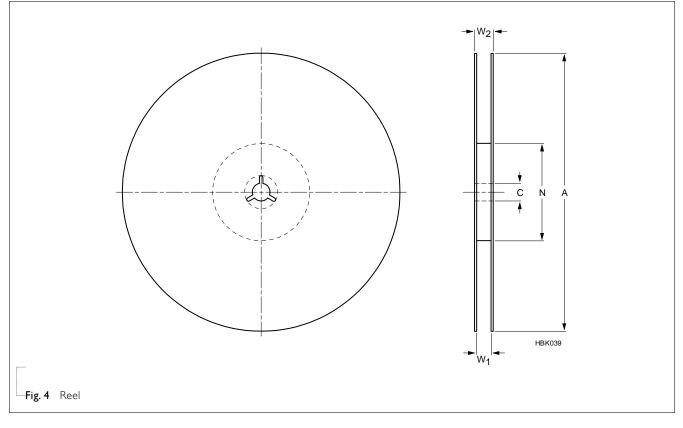


Table 10 Reel dimensions; see Fig.5

TAPE WIDTH	SYMBOL						
	A	N	С	WI	W _{2max.}		
8 (Ø178 mm/7")	178 ±1.0	60 ±1.0	3 +0.50/-0.20	9.4 ±1.5	14.4		
8 (Ø330 mm/13")	330 ±1.0	100 ±1.0	13 +0.50/-0.20	9.0 ±0.2	14.4		
12 (Ø178 mm/7")	178 ±1.0	60 ±1.0	3 +0.50/-0.20	3.4 ± .5	18.4		

PROPERTIES OF REEL

Material: polystyrene Surface resistance: <10¹⁰ X/sq.

<u>MOUNTING</u>

SOLDER REPAIRS

Conventional solder repairs are carried out with a soldering iron as shown as Tab. 11 The tip of the soldering iron should not directly touch the chip component to avoid thermal shock on the interface between termination and body during mounting, repairing or de-mounting processes. Ensure the termination solder has melted before removing the chip component.

Table II Recommended soldering iron condition

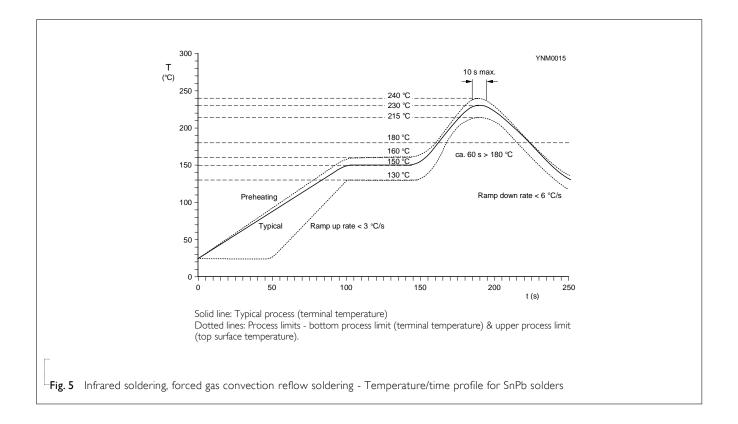
ТҮРЕ	Temp(°C)	DURATION (SEC.)	PREHEATING TEMP(°C)	ATMOSPHERE
CL0204/CL0306/CL0508/CL0612	350 max.	3 max.	150 min.	air

SOLDERING CONDITIONS

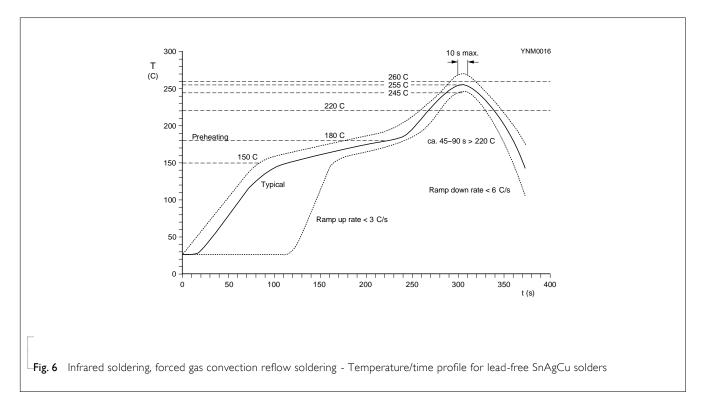
For normal use the capacitors may be mounted on printed-circuit boards or ceramic substrates by applying wave soldering, reflow soldering or conductive adhesive in accordance with *IEC 61760-1* (Standard method for the specification of surface mounting components). For advised soldering profiles see Figs 5, 6, 7.

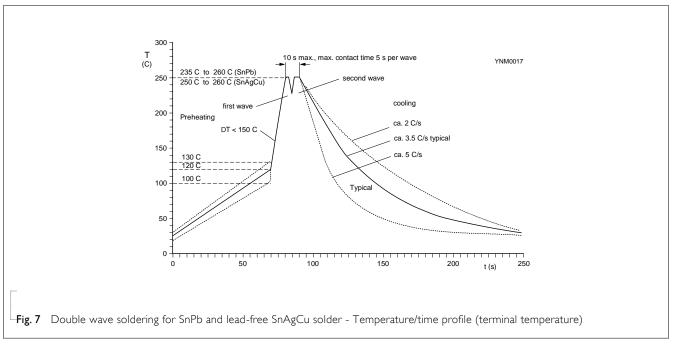
An improper combination of soldering, substrate and chip size can lead to a damaging of the component. The risk increases with the chip size and with temperature fluctuations (>100 $^{\circ}$ C).

Therefore, it is advised to use the smallest possible size and follow the dimensional recommendations given in Tables 12 for reflow and wave soldering. More detailed information is available on request.



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FOOTPRINT DIMENSIONS

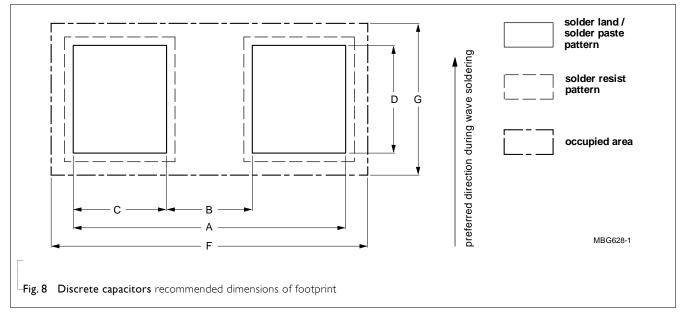


Table	12	Reflow	soldering [.]	for	footprint	dimensions	500	Fig 8
Table	12	I (CHOW	solucing,	101	lootprint	unnensions	SCC	i ig.u

SIZE	FOOTPRIN	Unit: mm					
CODE	A	В	С	D	F	G	Processing remarks
0204	0.55~0.65	0.15~0.20	0.2~0.25	0.7~1.0	0.95 ±0.15	1.75 ±0.15	
0306	0.7~1.0	0.2~0.3	0.3~0.4	1.4~1.6	1.5 ±0.15	2.7±0.15	
0508	1.2~1.5	0.4~0.5	0.4~0.5	1.4~1.8	2.1 ±0.25	3.2 ±0.25	 Ceramic substrate only
0612	1.8~2.3	0.6~0.8	0.6~0.7	2.6~2.8	2.5 ±0.25	4.4 ±0.25	

REVISION HISTORY

REVISION	DATE	CHANGE NOTIFICATION	DESCRIPTION
Version 2	May. 9, 2022	-	- Add 0306/X7R /6.3V and 10V/10nF to 68nF
Version I	Nov. 7, 2016	-	- Add 13" packing
Version 0	Jun. 26, 2015	-	- New

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