13N50

13A N-Channel Power MOSFET

Features

New technology for high voltage device
Low on-resistance and low conduction losses
Small package
Ultra Low Gate Charge cause lower driving requirements
100% Avalanche Tested
ROHS compliant

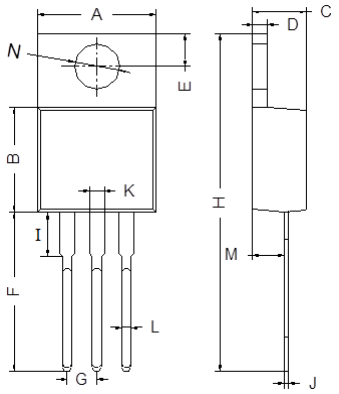
Mechanical Data

Case : TO-220AB
Terminals : Solder plated, solderable per MIL-STD-750, Method 2026
Polarity : As marked
Mounting Position : Any

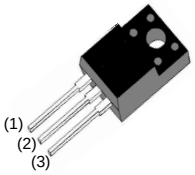
Application

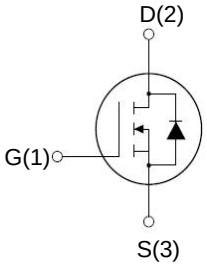
Power factor correction（PFC）
Switched mode power supplies(SMPS)
Uninterruptible Power Supply（UPS）

TO-220AB



TO-220AB		
Dim	Min	Max
A	9.80	10.30
B	8.30	8.90
C	4.37	4.77
D	1.10	1.45
E	2.62	2.87
F	13.14	13.74
G	2.41	2.67
H	28.40	29.16
I	3.55	4.05
J	0.35	0.58
K	1.20	1.32
L	0.68	0.94
M	2.40	2.60
N	3.71	3.91
All Dimensions in mm		





Maximum Ratings And Electrical Characteristics

Ratings at 25℃ ambient temperature unless otherwise specified. Single phase half-wave 60Hz,resistive or inductive load, for capacitive load current derate by 20%.

Table 1. Absolute Maximum Ratings (T_C=25℃)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	500	V
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	13	A
	T_C = 100°C		7.8	A
Pulsed Drain Current (Note 2)		I_{DM}	52	A
Total Power Dissipation @ T_C = 25°C		P_{DTOT}	50	W
Single Pulsed Avalanche Energy (Note 3)		E_{AS}	600	mJ
Single Pulsed Avalanche Current (Note 3)		I_{AR}	10	A
Operating Junction and Storage Temperature Range		T_J, T_{STG}	150，-55～+150	°C

THERMAL PERFORMANCE			
PARAMETER	**SYMBOL**	**LIMIT**	**UNIT**
Junction to Case Thermal Resistance	$R_{\Theta JC}$	2.5	°C/W
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	62.5	°C/W

Notes: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB with minimum recommended footprint in still air.

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Static (Note 4)						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	BV_{DSS}	500	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	$V_{GS(TH)}$	2.0	--	4.0	V
Gate Body Leakage	V_{GS} = ±30V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V_{DS} = 500V, V_{GS} = 0V	I_{DSS}	--	--	1	μA
Drain-Source On-State Resistance	V_{GS} = 10V, I_D = 6.5A	$R_{DS(on)}$	--	0.42	0.50	Ω
Dynamic (Note 5)						
Total Gate Charge	V_{DS} = 400V, I_D = 12A, V_{GS} = 10V	Q_g	--	55	70	nC
Gate-Source Charge		Q_{gs}	--	10	--	
Gate-Drain Charge		Q_{gd}	--	25	--	
Input Capacitance	V_{DS} = 25 V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	1860	2507	pF
Output Capacitance		C_{oss}	--	188	243	
Reverse transfer capacitance		C_{rss}	--	30	48	
Switching (Note 6)						
Turn-On Delay Time	V_{DD} = 250V, R_{GEN} = 25Ω,	$t_{d(on)}$	--	78	102	ns
Turn-On Rise Time		t_r	--	133	175	
Turn-Off Delay Time		$t_{d(off)}$	--	233	310	
Turn-Off Fall Time		t_f	--	105	180	
Source-Drain Diode (Note 4)						
Forward On Voltage	I_S = 13A, V_{GS} = 0V	V_{SD}	--	--	1.4	V
Reverse Recovery Time	V_{GS} = 0V, I_S = 13A dI$_F$/dt = 100A/μs	t_{rr}	--	450	--	ns
Reverse Recovery Charge		Q_{rr}	--	4.9	--	μC

Notes:

1. Current limited by package.
2. Pulse width limited by the maximum junction temperature.
3. L = 11mH, I_{AS} = 13A , V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
4. Pulse test: PW ≤ 300μs, duty cycle ≤ 2%.
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

CHARACTERISTICS CURVES

(T_C = 25°C unless otherwise noted)

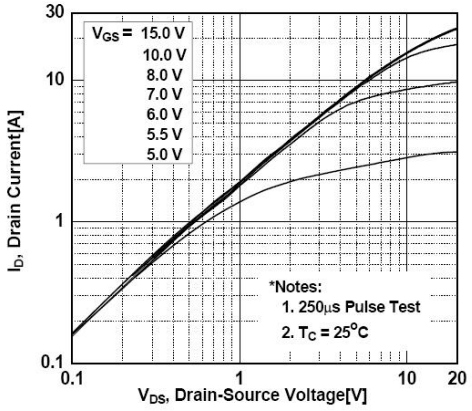


图1. 输出特性曲线

Fig. 1 On-State Characteristics

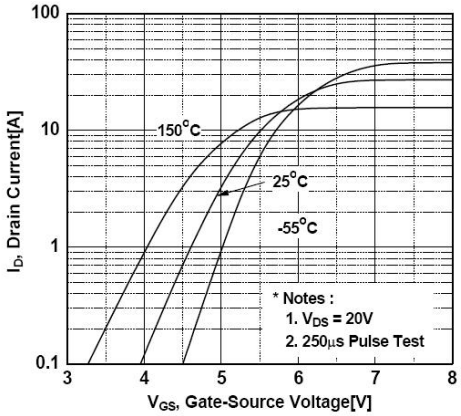


图2. 传输特性曲线

Fig. 2 Transfer Characteristics

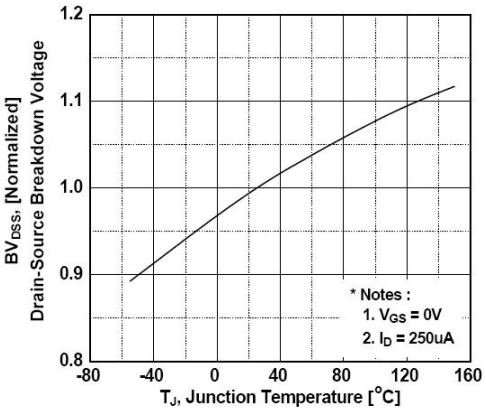


图3. 击穿电压随温度变化曲线

Fig. 3 Breakdown Voltage Variation vs Temperature

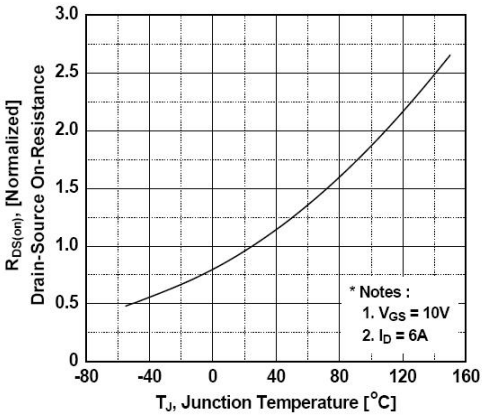


图4. 导通电阻随温度变化曲线

Fig. 4 On-Resistance Variation vs Temperature

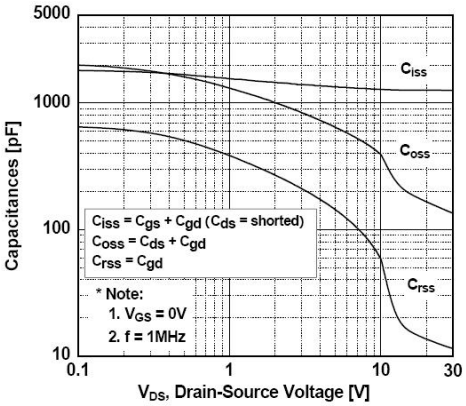


图5. 电容特性曲线

Fig. 5 Capacitance Characteristics

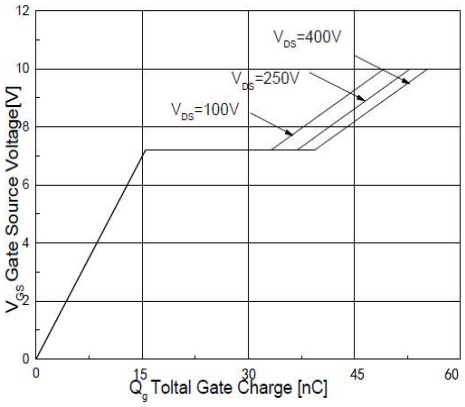


图6. 栅电荷特性曲线

Fig. 6 Gate Charge Characteristics

单击下面可查看定价，库存，交付和生命周期等信息

>>ZG(中鑫半导体)