International
IOR Rectifier

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IRS233(0,2)(D)(S & J)PbF

3-PHASE-BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation Fully operational to +600 V
- Tolerant to negative transient voltage – dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent half-bridge drivers
- Matched propagation delay for all channels
- 3.3 V logic compatible
- Outputs out of phase with inputs
- Cross-conduction prevention logic
- Integrated Operational Amplifier
- Integrated Bootstrap Diode function (IRS233(0,2)D)
- RoHS Compliant

Product Summary

V_{OFFSET}	600V max.
$I_{O+/-}$	200 mA / 420 mA
V_{OUT}	10 V – 20 V (233(0,2)(D))
$t_{on/off}$ (typ.)	500 ns
Deadtime (typ.)	2.0 us (IRS2330(D)) 0.7 us (IRS2332(D))

Applications:

*Motor Control
*Air Conditioners/ Washing Machines
*General Purpose Inverters
*Micro/Mini Inverter Drives

Description

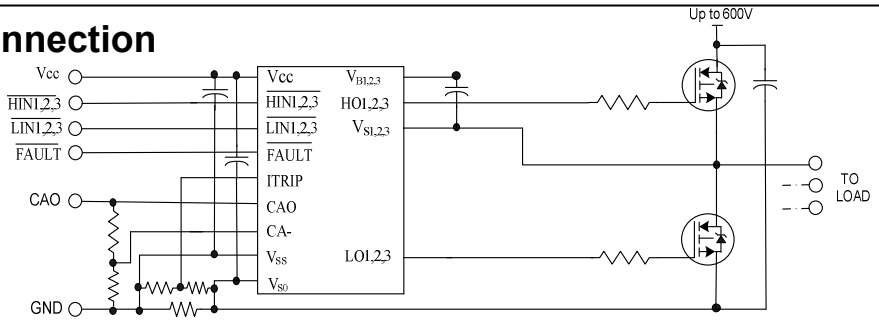
The IRS233(0,2)(D)(S & J) is a high voltage, high speed power MOSFET and IGBT driver with three independent high and low side referenced output channels. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 3.3 V logic. A ground-referenced operational amplifier provides analog feedback of bridge current via an external current sense resistor. A current trip function which terminates all six outputs is also derived from this resistor. An open drain $\overline{\text{FAULT}}$ signal indicates if an over-current or undervoltage shutdown has occurred. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use at high frequencies. The floating channel can be used to drive N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Packages

28-Lead SOIC

44-Lead PLCC w/o 12 Leads

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout.

Qualification Information†

Qualification Level		Industrial††	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		SOIC28W	MSL3††† , 260°C (per IPC/JEDEC J-STD-020)
		PLCC44	MSL3††† , 245°C (per IPC/JEDEC J-STD-020)
ESD	Human Body Model	Class 2 (per JEDEC standard JESD22-A114)	
	Machine Model	Class B (per EIA/JEDEC standard EIA/JESD22-A115)	
IC Latch-Up Test		Class I, Level A (per JESD78)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to V_{SO}. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
$V_{B1,2,3}$	High-side floating supply voltage		-0.3	620	V
$V_{S1,2,3}$	High-side floating offset voltage		$V_{B1,2,3}$ - 20	$V_{B1,2,3}$ + 0.3	
$V_{HO1,2,3}$	High-side floating output Voltage		$V_{S1,2,3}$ - 0.3	$V_{B1,2,3}$ + 0.3	
V_{CC}	Low-side and logic fixed supply voltage		-0.3	20	
V_{SS}	Logic ground		V_{CC} - 20	V_{CC} + 0.3	
$V_{LO1,2,3}$	Low-side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage ($\overline{\text{HIN1,2,3}}$, $\overline{\text{LIN1,2,3}}$ & ITRIP)		V_{SS} -0.3	(V_{SS} + 15) or (V_{CC} + 0.3) Whichever is lower	
V_{FLT}	$\overline{\text{FAULT}}$ output voltage		V_{SS} -0.3	V_{CC} +0.3	
V_{CAO}	Operational amplifier output voltage		V_{SS} -0.3	V_{CC} +0.3	
V_{CA-}	Operational amplifier inverting input voltage		V_{SS} -0.3	V_{CC} +0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ TA ≤ +25 °C	(28 lead SOIC)	—	1.6	W
		(44 lead PLCC)	—	2.0	
Rth_{JA}	Thermal resistance, junction to ambient	(28 lead SOIC)	—	78	°C/W
		(44 lead PLCC)	—	63	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltage referenced to V_{SO}. The V_S offset rating is tested with all supplies biased at 15 V differential.

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High-side floating supply voltage	$V_{S1,2,3}$ +10	$V_{S1,2,3}$ +20	V
$V_{S1,2,3}$	Static high-side floating offset voltage	V_{SO}-8 (Note1)	600	
$V_{St1,2,3}$	Transient high-side floating offset voltage	-50 (Note2)	600	
$V_{HO1,2,3}$	High-side floating output voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
V_{CC}	Low-side and Logic fixed supply voltage	10	20	
V_{SS}	Logic ground	-5	5	
$V_{LO1,2,3}$	Low-side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN1,2,3, LIN1,2,3 & ITRIP)	V_{SS}	V_{SS} + 5	
V_{FLT}	FAULT output voltage	V_{SS}	V_{CC}	
V_{CAO}	Operational amplifier output voltage	V_{SS}	V_{SS} + 5	
V_{CA-}	Operational amplifier inverting input voltage	V_{SS}	V_{SS} + 5	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of (V_{SO} -8 V) to (V_{SO} +600 V). Logic state held for V_S of (V_{SO} -8 V) to (V_{SO} – V_{BS}).
Note 2: Operational for transient negative VS of VSS - 50 V with a 50 ns pulse width. Guaranteed by design. Refer to the Application Information section of this datasheet for more details.
Note 3: CAO input pin is internally clamped with a 5.2 V zener diode.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15 V, $V_{SO1,2,3}$ = V_{SS} , C_L = 1000 pF, T_A = 25 °C unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{on}	Turn-on propagation delay	400	500	700	ns	$V_{S1,2,3}$ = 0 V to 600 V
t_{off}	Turn-off propagation delay	400	500	700		
t_r	Turn-on rise time	—	80	125		$V_{S1,2,3}$ = 0 V
t_f	Turn-off fall time	—	35	55		
t_{itrip}	ITRIP to output shutdown propagation delay	400	660	920		
t_{bl}	ITRIP blanking time	—	400	—		
t_{flt}	ITRIP to $\overline{\text{FAULT}}$ indication delay	350	550	870		
$t_{flt,\ in}$	Input filter time (all six inputs)	—	325	—		
t_{fltclr}	$\overline{\text{LIN}}$1,2,3 to $\overline{\text{FAULT}}$ clear time (2330/2)	5300	8500	13700		
DT	Deadtime: (IRS2330(D))	1300	2000	3100		V_{IN} = 0 V & 5 V without external deadtime
	(IRS2332(D))	500	700	1100		
MDT	Deadtime matching: : (IRS2330(D))	—	—	400		
	(IRS2332(D))	—	—	140		
MT	Delay matching time (t_{ON} , t_{OFF})	—	—	50		V_{IN} = 0 V & 5 V without external deadtime larger than DT
PM	Pulse width distortion	—	—	75		PM input 10 µs

NOTE: For high side PWM, HIN pulse width must be ≥ 1.5 usec

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15 V, $V_{SO1,2,3}$ = V_{SS} , C_L = 1000 pF, T_A = 25 °C unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
SR+	Operational amplifier slew rate (+)	5	10	—	V/µs	1 V input step
SR-	Operational amplifier slew rate (-)	2.4	3.2	—		

Static Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15 V, $V_{SO1,2,3}$ = V_{SS} and T_A = 25 °C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six logic input leads: HIN1,2,3 & LIN1,2,3. The V_O and I_O parameters are referenced to $V_{SO1,2,3}$ and are applicable to the respective output leads: HO1,2,3 or LO1,2,3.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{IH}	Logic "0" input voltage (OUT = LO)	—	—	2.2	V	
V_{IL}	Logic "1" input voltage (OUT = HI)	0.8	—	—		
$V_{IT,TH+}$	ITRIP input positive going threshold	400	490	580	mV	
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	1000		V_{IN} = 0 V, I_O = 20 mA
V_{OL}	Low level output voltage, V_O	—	—	400		V_{IN} = 5 V, I_O = 20 mA
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600 V
I_{QBS}	Quiescent V_{BS} supply current	—	30	50		V_{IN} = 0 V or 4 V
I_{QCC}	Quiescent V_{CC} supply current	—	4.0	6.2	mA	V_{IN} = 4 V
I_{IN+}	Logic "1" input bias current (OUT =HI)	-400	-300	-100	µA	V_{IN} = 0 V
I_{IN-}	Logic "0" input bias current (OUT = LO)	-300	-220	-100		V_{IN} = 4 V
I_{ITRIP+}	"High" ITRIP bias current	—	5	10		ITRIP = 4 V
I_{ITRIP-}	"LOW" ITRIP bias current	—	—	30	nA	ITRIP = 0 V
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	7.5	8.35	9.2	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	7.1	7.95	8.8		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	8.3	9	9.7		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	8	8.7	9.4		
V_{CCUVH}	Hysteresis	—	0.3	—		
V_{BSUVH}	Hysteresis	—	0.4	—		
$R_{on, FLT}$	$\overline{FAULT}$ low on-resistance	—	55	75	Ω	
I_{O+}	Output high short circuit pulsed current	—	-250	-180	mA	V_O = 0 V, V_{IN} = 0 V PW ≤ 10 us
I_{O-}	Output low short circuit pulsed current	420	500	—		V_O = 15 V, V_{IN} = 5 V PW ≤ 10 us
R_{BS}	Integrated bootstrap diode resistance	—	200	—	Ω	
V_{OS}	Operational amplifier input offset voltage	—	—	20	mV	V_{SO} = 0.2 V
I_{CA-}	CA- input bias current	—	—	100	nA	V_{CA-} = 1 V
CMRR	Operational amplifier common mode rejection ratio	—	80	—	dB	V_{SO} = 0.1 V & 5 V
PSRR	Operational amplifier power supply rejection ratio	—	75	—		V_{SO} = 0.2 V V_{CC} = 9.7 V & 20 V
$V_{OH,AMP}$	Operational amplifier high level output voltage	4.8	5.2	5.6	V	V_{CA-} = 0 V, V_{SO} =1 V
$V_{OL,AMP}$	Operational amplifier low level output voltage	—	—	40	mV	V_{CA-} = 1 V, V_{SO} =0 V

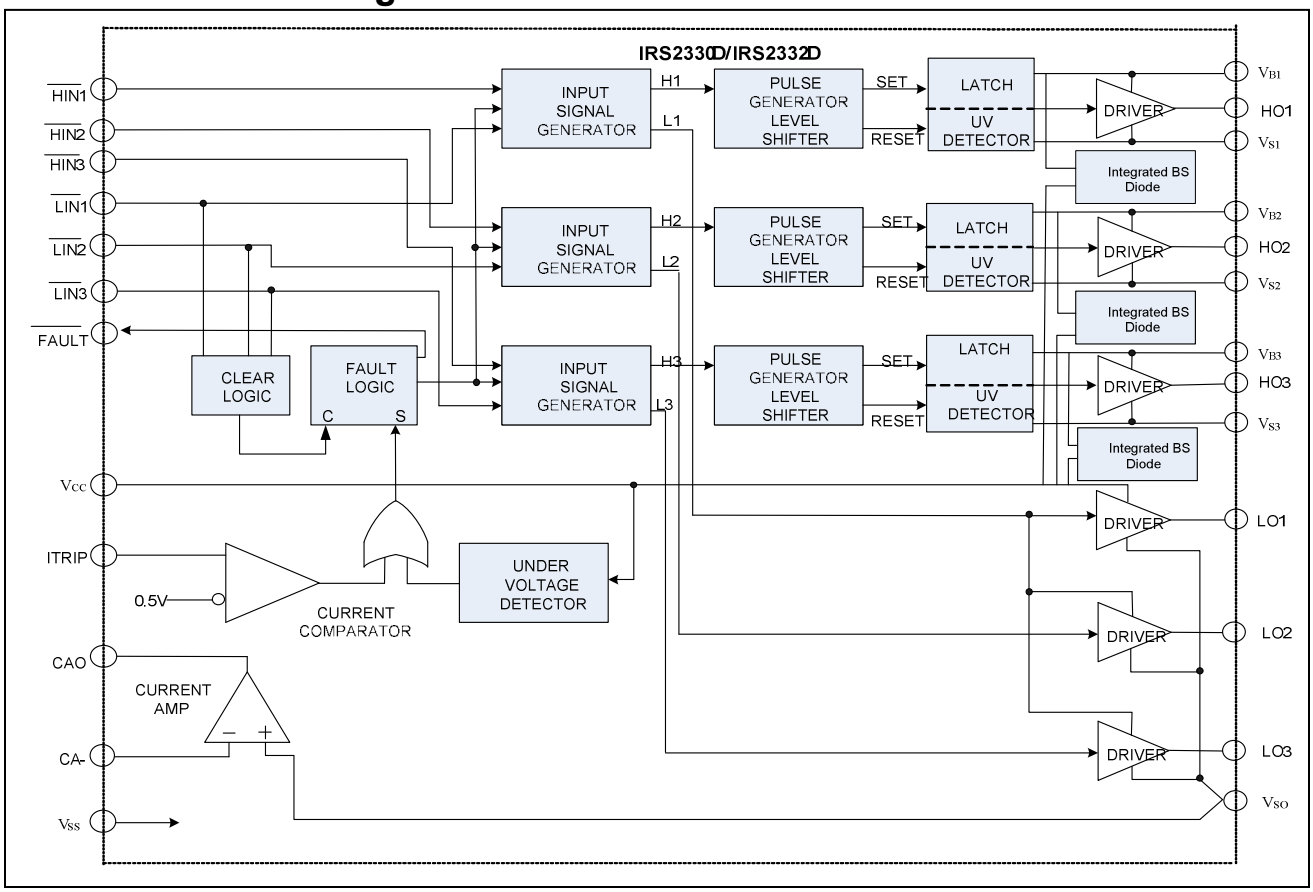
Note: The integrated bootstrap diode does not work well with the trapezoidal control.

Static Electrical Characteristics- Continued

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15 V, $V_{SO1,2,3}$ = V_{SS} and T_A = 25 °C unless otherwise specified. The $V_{IN,}$ V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six logic input leads: $\overline{HIN}$1,2,3 & $\overline{LIN}$1,2,3. The V_O and I_O parameters are referenced to $V_{SO1,2,3}$ and are applicable to the respective output leads: HO1,2,3 or LO1,2,3.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
$I_{SRC,AMP}$	Operational amplifier output source current	—	-7	-4	mA	V_{CA-} = 0 V, V_{SO} =1 V V_{CAO} = 4 V
$I_{SNK,AMP}$	Operational amplifier output sink current	1	2.1	—		V_{CA-} = 1 V, V_{SO} =0 V V_{CAO} = 2 V
$I_{O+,AMP}$	Operational amplifier output high short circuit current	-30	-10	—		V_{CA-} = 0 V, V_{SO} =5 V V_{CAO} = 0 V
$I_{O-,AMP}$	Operational amplifier output low short circuit current	—	4	—		V_{CA-} = 5 V, V_{SO} =0 V V_{CAO} = 5 V

Functional Block Diagram

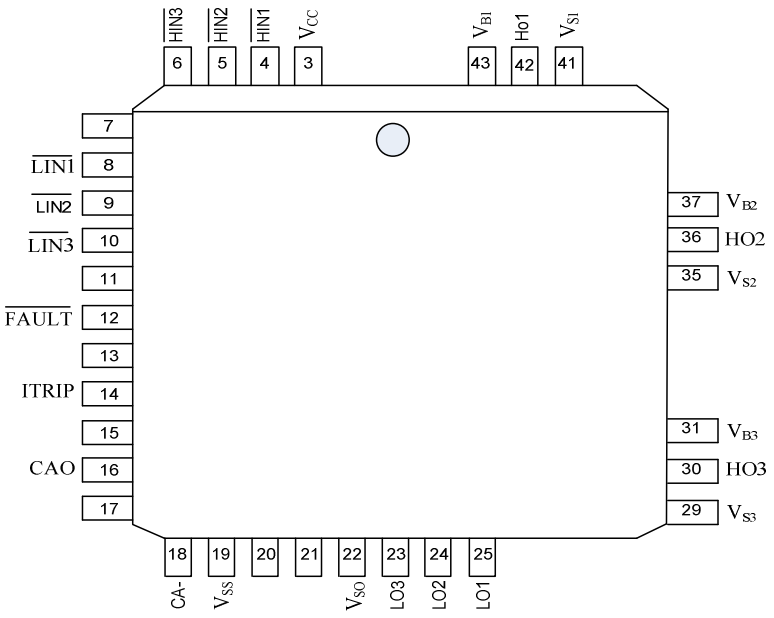


Note: IRS2330 & IRS2332 are without integrated bootstrap diode.

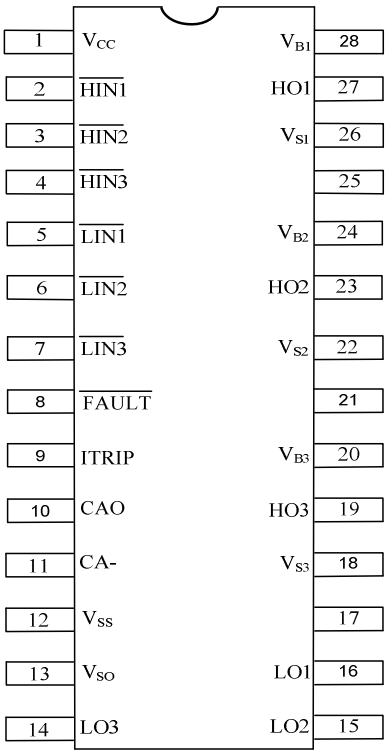
Lead Definitions

Symbol	Description
$\overline{HIN1,2,3}$	Logic input for high-side gate driver outputs (HO1,2,3), out of phase
$\overline{LIN1,2,3}$	Logic input for low-side gate driver output (LO1,2,3), out of phase
$\overline{FAULT}$	Indicates over-current or undervoltage lockout (low-side) has occurred, negative logic
V_{CC}	Low-side and logic fixed supply
ITRIP	Input for over-current shutdown
CAO	Output of current amplifier
CA-	Negative input of current amplifier
V_{SS}	Logic Ground
$V_{B1,2,3}$	High-side floating supply
HO1,2,3	High-side gate drive output
$V_{S1,2,3}$	High-side floating supply return
LO1,2,3	Low-side gate drive output
V_{SO}	Low-side return and positive input of current amplifier

Lead Assignments



44 Lead PLCC w/o 12 Leads



28 Lead SOIC (Wide Body)

Part Number	IRS233(0,2)DJ	IRS233(0,2)DS

Application Information and Additional Details

Information regarding the following topics are included as subsections within this section of the datasheet.

- IGBT/MOSFET Gate Drive
- Switching and Timing Relationships
- Deadtime
- Matched Propagation Delays
- Input Logic Compatibility
- Undervoltage Lockout Protection
- Shoot-Through Protection
- Fault Reporting
- Over-Current Protection
- Over-Temperature Shutdown Protection
- Truth Table: Undervoltage lockout, ITRIP
- Advanced Input Filter
- Short-Pulse / Noise Rejection
- Integrated Bootstrap Functionality
- Bootstrap Power Supply Design
- Separate Logic and Power Grounds
- Negative V_S Transient SOA
- DC- bus Current Sensing
- PCB Layout Tips
- Integrated Bootstrap FET limitation
- Additional Documentation

IGBT/MOSFET Gate Drive

The IRS233(2,0)(D) HVICs are designed to drive up to six MOSFET or IGBT power devices. Figures 1 and 2 illustrate several parameters associated with the gate drive functionality of the HVIC. The output current of the HVIC, used to drive the gate of the power switch, is defined as I_O. The voltage that drives the gate of the external power switch is defined as V_{HO} for the high-side power switch and V_{LO} for the low-side power switch; this parameter is sometimes generically called V_{OUT} and in this case does not differentiate between the high-side or low-side output voltage.

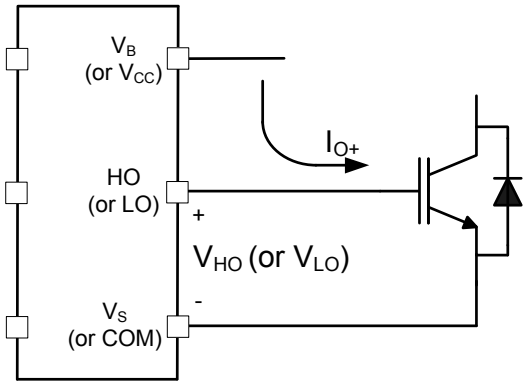


Figure 1: HVIC sourcing current

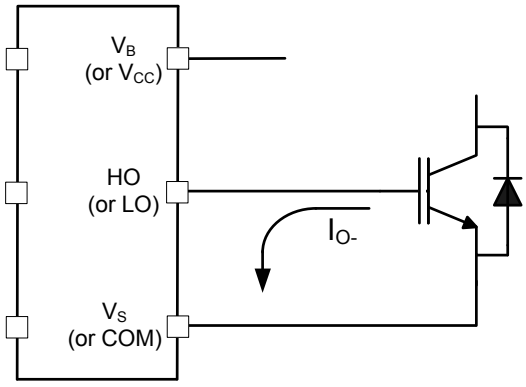


Figure 2: HVIC sinking current

Switching and Timing Relationships

The relationship between the input and output signals of the IRS233(0,2)(D) are illustrated below in Figures 3. From these figures, we can see the definitions of several timing parameters (i.e., PW_{IN}, PW_{OUT}, t_{ON}, t_{OFF}, t_R, and t_F) associated with this device.

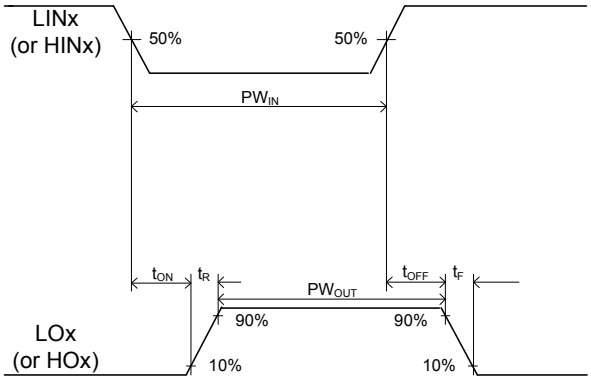


Figure 3: Switching time waveforms

The following two figures illustrate the timing relationships of some of the functionality of the IRS233(0,2)(D); this functionality is described in further detail later in this document.

During interval A of Figure 4, the HVIC has received the command to turn-on both the high- and low-side switches at the same time; as a result, the shoot-through protection of the HVIC has prevented this condition and both the high- and low-side output are held in the off state.

Interval B of Figures 4 shows that the signal on the ITRIP input pin has gone from a low to a high state; as a result, all of the gate drive outputs have been disabled (i.e., see that HOx has returned to the low state; LOx is also held low) and a fault is reported by the FAULT output transitioning to the low state. Once the ITRIP input has returned to the low state, the fault condition is latched until the all LINx become high.

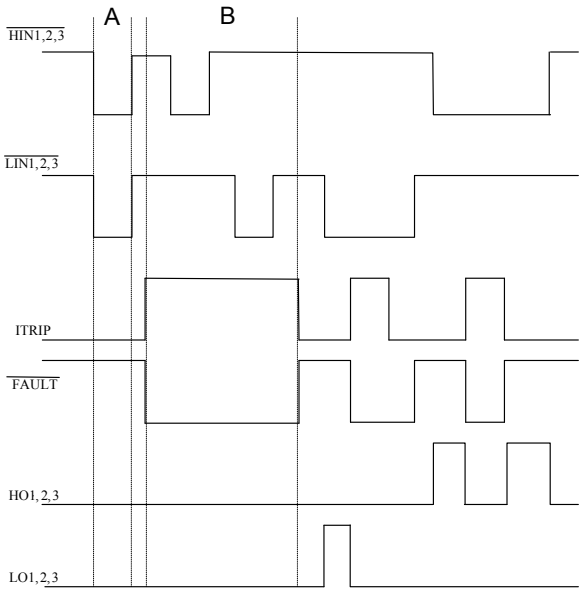


Figure 4: Input/output timing diagram

Deadtime

This family of HVICs features integrated deadtime protection circuitry. The deadtime for these ICs is fixed; other ICs within IR's HVIC portfolio feature programmable deadtime for greater design flexibility. The deadtime feature inserts a time period (a minimum deadtime) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch being turned off has fully turned off before the second power switch is turned on. This minimum deadtime is automatically inserted whenever the external deadtime is shorter than DT; external deadtimes larger than DT are not modified by the gate driver. Figure 5 illustrates the deadtime period and the relationship between the output gate signals.

The deadtime circuitry of the IRS233(0,2)(D) is matched with respect to the high- and low-side outputs of a given channel; additionally, the deadtimes of each of the three channels are matched.

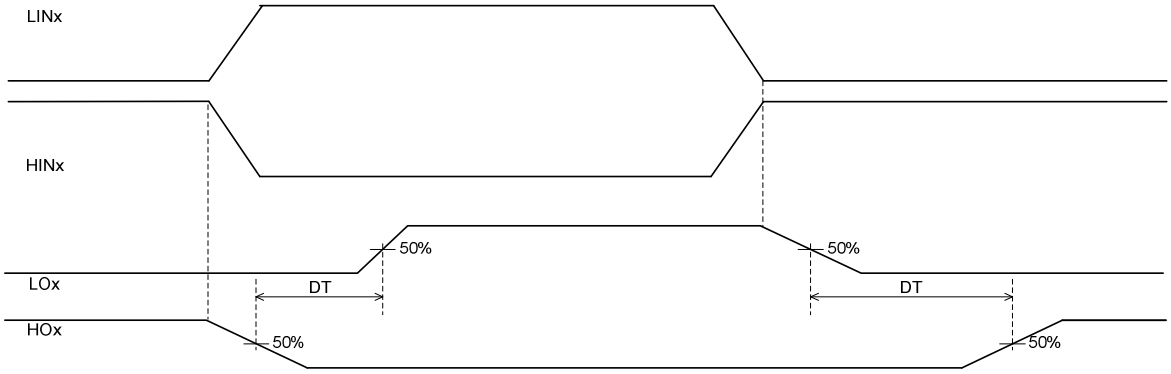


Figure 5: Illustration of deadtime

Matched Propagation Delays

The IRS233(0,2)(D) family of HVICs is designed with propagation delay matching circuitry. With this feature, the IC's response at the output to a signal at the input requires approximately the same time duration (i.e., t_{ON}, t_{OFF}) for both the low-side channels and the high-side channels. Additionally, the propagation delay for each low-side channel is matched when compared to the other low-side channels and the propagation delays of the high-side channels are matched with each other. The propagation turn-on delay (t_{ON}) of the IRS233(0,2)(D) is matched to the propagation turn-on delay (t_{OFF}).

Input Logic Compatibility

The inputs of this IC are compatible with standard CMOS and TTL outputs. The IRS233(0,2)(D) family has been designed to be compatible with 3.3 V and 5 V logic-level signals. The IRS233(0,2)(D) features an integrated 5.2 V Zener clamp on the HIN, LIN, and ITRIP pins. Figure 6 illustrates an input signal to the IRS233(0,2)(D), its input threshold values, and the logic state of the IC as a result of the input signal.

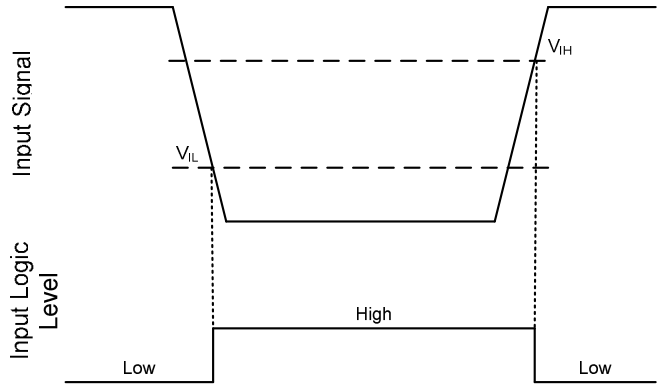


Figure 6: HIN & LIN input thresholds

Undervoltage Lockout Protection

This family of ICs provides undervoltage lockout protection on both the V_{CC} (logic and low-side circuitry) power supply and the V_{BS} (high-side circuitry) power supply. Figure 7 is used to illustrate this concept; V_{CC} (or V_{BS}) is plotted over time and as the waveform crosses the UVLO threshold ($V_{CCUV+/-}$ or $V_{BSUV+/-}$) the undervoltage protection is enabled or disabled.

Upon power-up, should the V_{CC} voltage fail to reach the V_{CCUV+} threshold, the IC will not turn-on. Additionally, if the V_{CC} voltage decreases below the V_{CCUV-} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition and shutdown the high- and low-side gate drive outputs, and the FAULT pin will transition to the low state to inform the controller of the fault condition.

Upon power-up, should the V_{BS} voltage fail to reach the V_{BSUV} threshold, the IC will not turn-on. Additionally, if the V_{BS} voltage decreases below the V_{BSUV} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition, and shutdown the high-side gate drive outputs of the IC.

The UVLO protection ensures that the IC drives the external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power switch could be driven with a low voltage, resulting in the power switch conducting current while the channel impedance is high; this could result in very high conduction losses within the power device and could lead to power device failure.

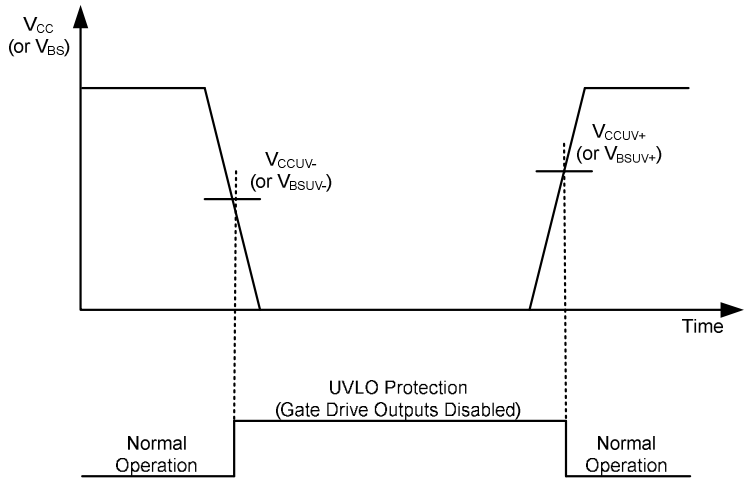


Figure 7: UVLO protection

Shoot-Through Protection

The IRS233(0,2)(D) family of high-voltage ICs is equipped with shoot-through protection circuitry (also known as cross-conduction prevention circuitry). Figure 8 shows how this protection circuitry prevents both the high- and low-side switches from conducting at the same time. Table 1 illustrates the input/output relationship of the devices in the form of a truth table. Note that the IRS233(0,2)(D) has inverting inputs (the output is out-of-phase with its respective input).

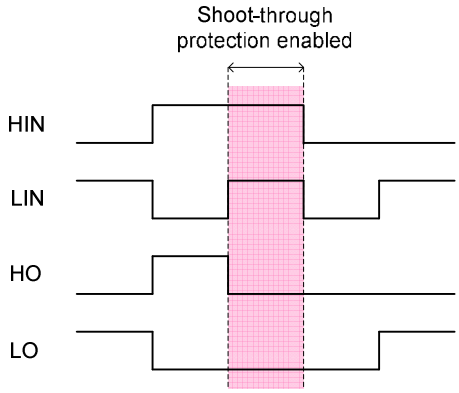


Figure 8: Illustration of shoot-through protection circuitry

IRS233(0,2)(D)			
HIN	**LIN**	**HO**	**LO**
0	0	0	0
0	1	1	0
1	0	0	1
1	1	0	0

Table 1: Input/output truth table

Fault Reporting

The IRS233(0,2)(D) family provides an integrated fault reporting output. There are two situations that would cause the HVIC to report a fault via the FAULT pin. The first is an undervoltage condition of V_{CC} and the second is if the ITRIP pin recognizes a fault. Once the fault condition occurs, the FAULT pin is internally pulled to V_{SS} and the fault condition is latched. The fault output stays in the low state until the fault condition has been removed by all LINx set to high state. Once the fault is removed, the voltage on the FAULT pin will return to V_{CC}.

Over-Current Protection

The IRS233(0,2)(D) HVICs are equipped with an ITRIP input pin. This functionality can be used to detect over-current events in the DC- bus. Once the HVIC detects an over-current event through the ITRIP pin, the outputs are shutdown, a fault is reported through the FAULT pin.

The level of current at which the over-current protection is initiated is determined by the resistor network (i.e., R_0, R_1, and R_2) connected to ITRIP as shown in Figure 9, and the ITRIP threshold ($V_{IT,TH+}$). The circuit designer will need to determine the maximum allowable level of current in the DC- bus and select R_0, R_1, and R_2 such that the voltage at node V_X reaches the over-current threshold ($V_{IT,TH+}$) at that current level.

$$V_{IT,TH+} = R_0 I_{DC-}(R_1/(R_1+R_2))$$

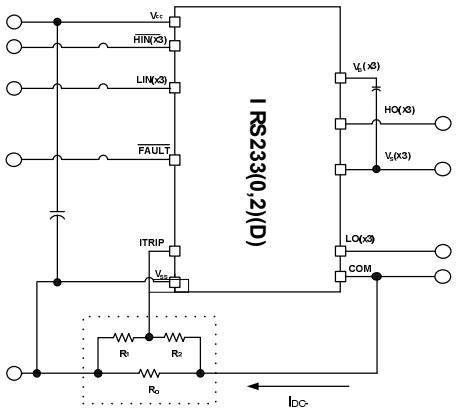


Figure 9: Programming the over-current protection

For example, a typical value for resistor R_0 could be 50 mΩ. The voltage of the ITRIP pin should not be allowed to exceed 5 V; if necessary, an external voltage clamp may be used.

Over-Temperature Shutdown Protection

The ITRIP input of the IRS233(0,2)(D) can also be used to detect over-temperature events in the system and initiate a shutdown of the HVIC (and power switches) at that time. In order to use this functionality, the circuit designer will need to design the resistor network as shown in Figure 10 and select the maximum allowable temperature.

This network consists of a thermistor and two standard resistors R_3 and R_4. As the temperature changes, the resistance of the thermistor will change; this will result in a change of voltage at node V_X. The resistor values should be selected such the voltage V_X should reach the threshold voltage ($V_{IT,TH+}$) of the ITRIP functionality by the time that the maximum allowable temperature is reached. The voltage of the ITRIP pin should not be allowed to exceed 5 V.
When using both the over-current protection and over-temperature protection with the ITRIP input, OR-ing diodes (e.g., DL4148) can be used. This network is shown in Figure 11; the OR-ing diodes have been labeled D_1 and D_2.

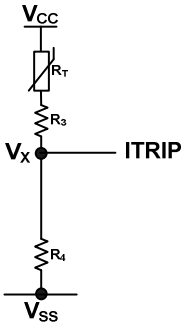


Figure 10: Programming over-temperature protection

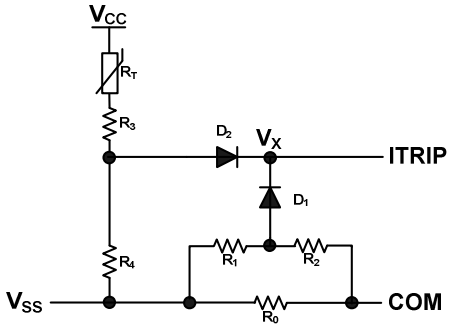


Figure 11: Using over-current protection and over-temperature protection

Truth Table: Undervoltage lockout and ITRIP

Table 2 provides the truth table for the IRS233(0,2)(D). The first line shows that the UVLO for V_{CC} has been tripped; the FAULT output has gone low and the gate drive outputs have been disabled. V_{CCUV} is not latched in this case and when V_{CC} is greater than V_{CCUV}, the FAULT output returns to the high impedance state.

The second case shows that the UVLO for V_{BS} has been tripped and that the high-side gate drive outputs have been disabled. After V_{BS} exceeds the V_{BSUV} threshold, HO will stay low until the HVIC input receives a new falling transition of HIN. The third case shows the normal operation of the HVIC. The fourth case illustrates that the ITRIP trip threshold has been reached and that the gate drive outputs have been disabled and a fault has been reported through the fault pin. The fault output stays in the low state until the fault condition has been removed by all LINx set to high state. Once the fault is removed, the voltage on the FAULT pin will return to V_{CC}.

	VCC	VBS	ITRIP	FAULT	LO	HO
UVLO V_{CC}	$<V_{CCUV}$	---	---	0	0	0
UVLO V_{BS}	15 V	$<V_{BSUV}$	0 V	High impedance	LIN	0
Normal operation	15 V	15 V	0 V	High impedance	LIN	HIN
ITRIP fault	15 V	15 V	$>V_{ITRIP}$	0	0	0

Table 2: IRS233(0,2)(D) UVLO, ITRIP & FAULT truth table

Advanced Input Filter

The advanced input filter allows an improvement in the input/output pulse symmetry of the HVIC and helps to reject noise spikes and short pulses. This input filter has been applied to the HIN and LIN. The working principle of the new filter is shown in Figures 12 and 13.

Figure 12 shows a typical input filter and the asymmetry of the input and output. The upper pair of waveforms (Example 1) show an input signal with a duration much longer then $t_{FIL,IN}$; the resulting output is approximately the difference between the input signal and $t_{FIL,IN}$. The lower pair of waveforms (Example 2) show an input signal with a duration slightly longer then $t_{FIL,IN}$; the resulting output is approximately the difference between the input signal and $t_{FIL,IN}$.

Figure 13 shows the advanced input filter and the symmetry between the input and output. The upper pair of waveforms (Example 1) show an input signal with a duration much longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal. The lower pair of waveforms (Example 2) show an input signal with a duration slightly longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal.

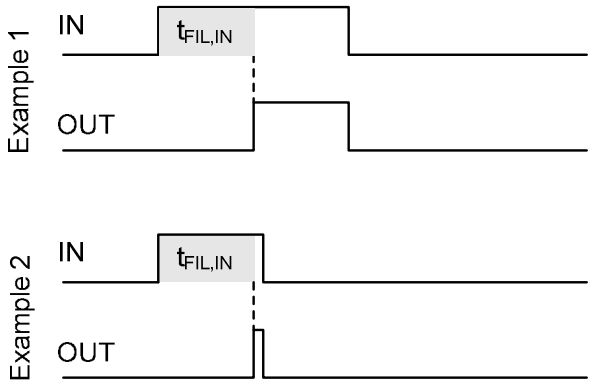


Figure 12: Typical input filter

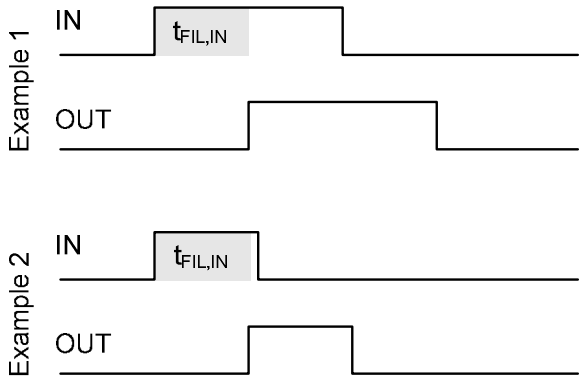


Figure 13: Advanced input filter

Short-Pulse / Noise Rejection

This device's input filter provides protection against short-pulses (e.g., noise) on the input lines. If the duration of the input signal is less than $t_{FIL,IN}$, the output will not change states. Example 1 of Figure 14 shows the input and output in the low state with positive noise spikes of durations less than $t_{FIL,IN}$; the output does not change states. Example 2 of Figure 19 shows the input and output in the high state with negative noise spikes of durations less than $t_{FIL,IN}$; the output does not change states.

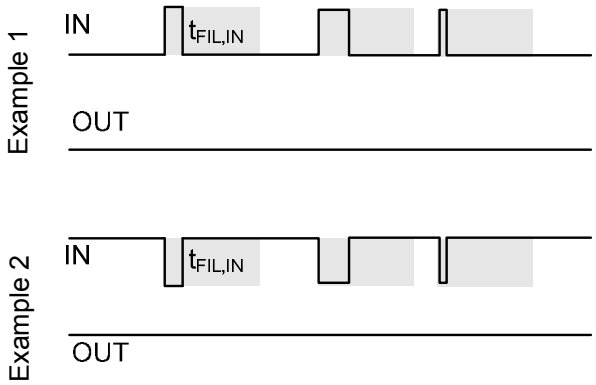


Figure 14: Noise rejecting input filters

Figures 15 and 16 present lab data that illustrates the characteristics of the input filters while receiving ON and OFF pulses.

The input filter characteristic is shown in Figure 15; the left side illustrates the narrow pulse ON (short positive pulse) characteristic while the left shows the narrow pulse OFF (short negative pulse) characteristic. The x-axis of Figure 20 shows the duration of PW_{IN}, while the y-axis shows the resulting PW_{OUT} duration. It can be seen that for a PW_{IN} duration less than $t_{FIL,IN}$, that the resulting PW_{OUT} duration is zero (e.g., the filter rejects the input signal/noise). We also see that once the PW_{IN} duration exceed $t_{FIL,IN}$, that the PW_{OUT} durations mimic the PW_{IN} durations very well over this interval with the symmetry improving as the duration increases. To ensure proper operation of the HVIC, it is suggested that the input pulse width for the high-side inputs be ≥ 500 ns.

The difference between the PW_{OUT} and PW_{IN} signals of both the narrow ON and narrow OFF cases is shown in Figure 16; the careful reader will note the scale of the y-axis. The x-axis of Figure 21 shows the duration of PW_{IN}, while the y-axis shows the resulting PW_{OUT}–PW_{IN} duration. This data illustrates the performance and near symmetry of this input filter.

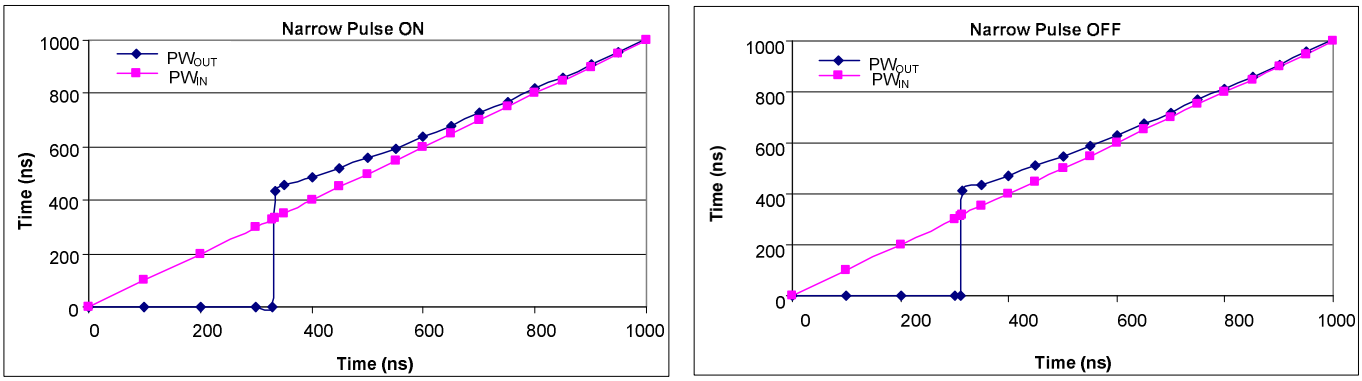


Figure 15: IRS233(0,2)(D) input filter characteristic

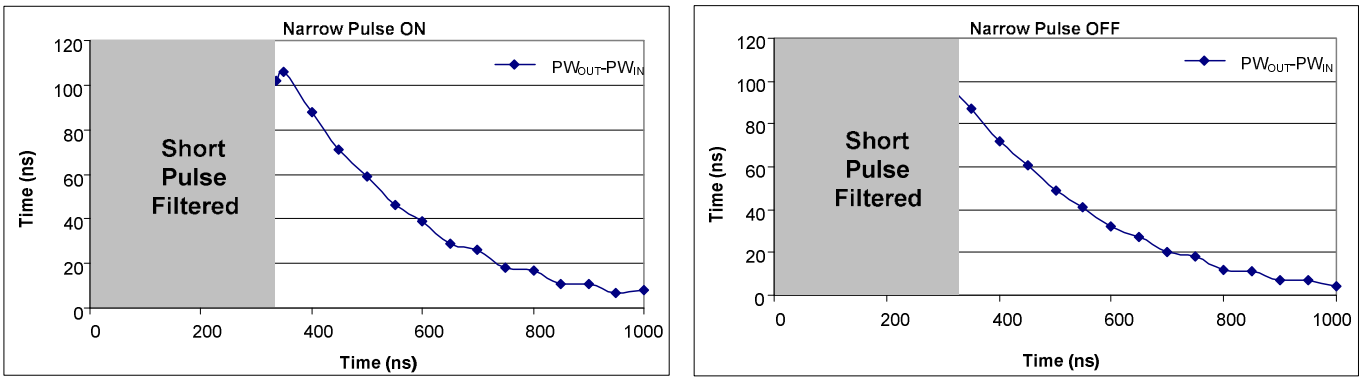


Figure 16: Difference between the input pulse and the output pulse

Integrated Bootstrap Functionality

The new IRS233(0,2)D family features integrated high-voltage bootstrap MOSFETs that eliminate the need of the external bootstrap diodes and resistors in many applications.

There is one bootstrap MOSFET for each high-side output channel and it is connected between the V_{CC} supply and its respective floating supply (i.e., V_{B1}, V_{B2}, V_{B3}); see Figure 17 for an illustration of this internal connection.

The integrated bootstrap MOSFET is turned on only during the time when LO is 'high', and it has a limited source current due to R_{BS}. The V_{BS} voltage will be charged each cycle depending on the on-time of LO and the value of the C_{BS} capacitor, the drain-source (collector-emitter) drop of the external IGBT (or MOSFET), and the low-side free-wheeling diode drop.

The bootstrap MOSFET of each channel follows the state of the respective low-side output stage (i.e., the bootstrap MOSFET is ON when LO is high, it is OFF when LO is low), unless the V_B voltage is higher than approximately 110% of V_{CC}. In that case, the bootstrap MOSFET is designed to remain off until V_B returns below that threshold; this concept is illustrated in Figure 18.

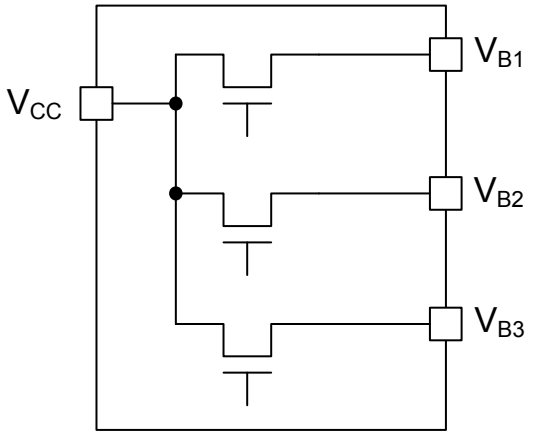


Figure 17: Internal bootstrap MOSFET connection

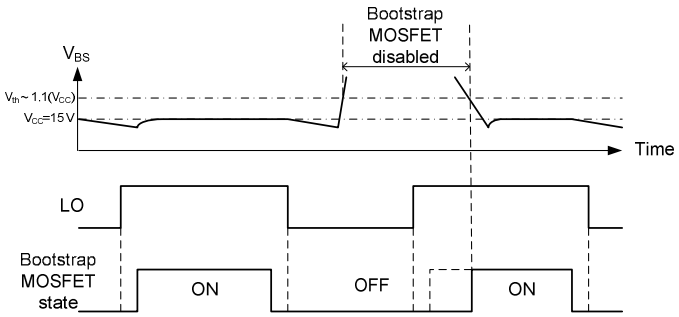


Figure 18: Bootstrap MOSFET state diagram

A bootstrap MOSFET is suitable for most of the PWM modulation schemes and can be used either in parallel with the external bootstrap network (i.e., diode and resistor) or as a replacement of it. The use of the integrated bootstrap as a replacement of the external bootstrap network may have some limitations. An example of this limitation may arise when this functionality is used in non-complementary PWM schemes (typically 6-step modulations) and at very high PWM duty cycle. In these cases, superior performances can be achieved by using an external bootstrap diode in parallel with the internal bootstrap network.

Bootstrap Power Supply Design

For information related to the design of the bootstrap power supply while using the integrated bootstrap functionality of the IRS233(0,2)D family, please refer to Application Note 1123 (AN-1123) entitled "Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality." This application note is available at www.irf.com.

For information related to the design of a standard bootstrap power supply (i.e., using an external discrete diode) please refer to Design Tip 04-4 (DT04-4) entitled "Using Monolithic High Voltage Gate Drivers." This design tip is available at www.irf.com.

Separate Logic and Power Grounds

The IRS233(0,2)(D) has separate logic and power ground pin (V_{SS} and VSO respectively) to eliminate some of the noise problems that can occur in power conversion applications. Current sensing shunts are commonly used in many applications for power inverter protection (i.e., over-current protection), and in the case of motor drive applications, for motor current measurements. In these situations, it is often beneficial to separate the logic and power grounds.

Figure 19 shows a HVIC with separate V_{SS} and VSO pins and how these two grounds are used in the system. The V_{SS} is used as the reference point for the logic and over-current circuitry; V_X in the figure is the voltage between the ITRIP pin and the V_{SS} pin. Alternatively, the VSO pin is the reference point for the low-side gate drive circuitry. The output voltage used to drive the low-side gate is V_{LO}-VSO; the gate-emitter voltage (V_{GE}) of the low-side switch is the output voltage of the driver minus the drop across $R_{G,LO}$.

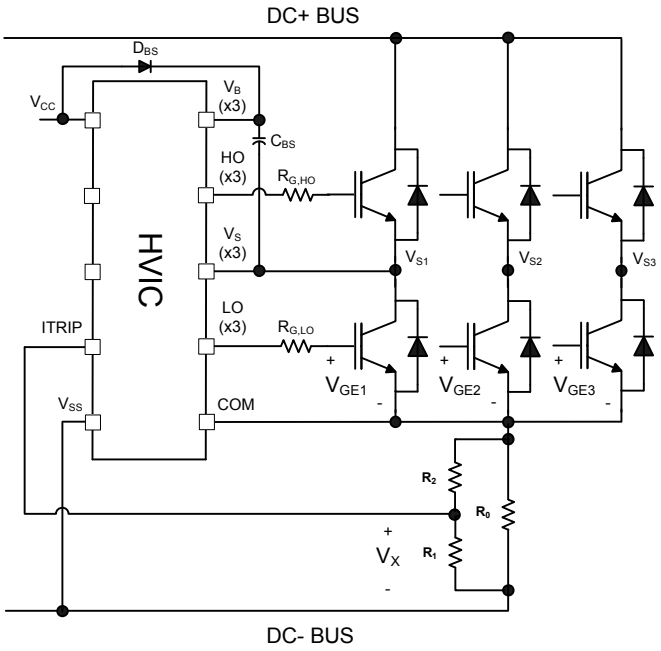


Figure 19: Separate V_{SS} and VSO pins

Negative V_S Transient SOA

A common problem in today's high-power switching converters is the transient response of the switch node's voltage as the power switches transition on and off quickly while carrying a large current. A typical 3-phase inverter circuit is shown in Figure 20; here we define the power switches and diodes of the inverter.

If the high-side switch (e.g., the IGBT Q1 in Figures 21 and 22) switches off, while the U phase current is flowing to an inductive load, a current commutation occurs from high-side switch (Q1) to the diode (D2) in parallel with the low-side switch of the same inverter leg. At the same instance, the voltage node V_{S1}, swings from the positive DC bus voltage to the negative DC bus voltage.

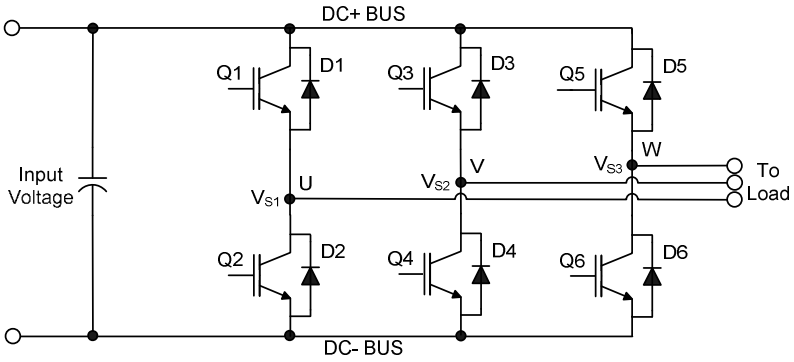


Figure 20: Three phase inverter

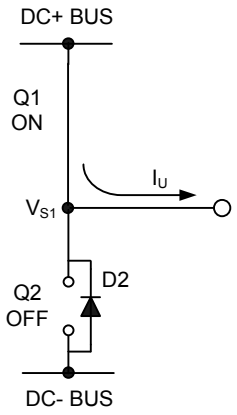


Figure 21: Q1 conducting

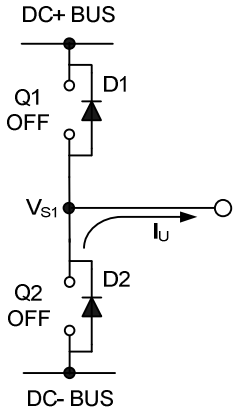


Figure 22: D2 conducting

Also when the V phase current flows from the inductive load back to the inverter (see Figures 23 and 24), and Q4 IGBT switches on, the current commutation occurs from D3 to Q4. At the same instance, the voltage node, V_{S2}, swings from the positive DC bus voltage to the negative DC bus voltage.

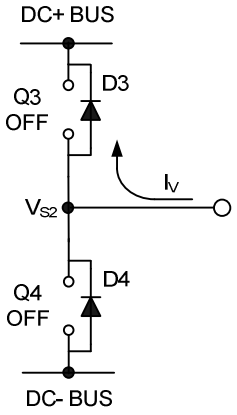


Figure 23: D3 conducting

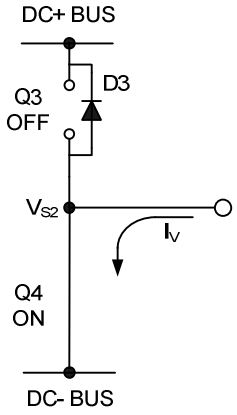


Figure 24: Q4 conducting

However, in a real inverter circuit, the V_S voltage swing does not stop at the level of the negative DC bus, rather it swings below the level of the negative DC bus. This undershoot voltage is called “negative V_S transient”.

The circuit shown in Figure 25 depicts one leg of the three phase inverter; Figures 26 and 27 show a simplified illustration of the commutation of the current between Q1 and D2. The parasitic inductances in the power circuit from the die bonding to the PCB tracks are lumped together in L_C and L_E for each IGBT. When the high-side switch is on, V_{S1} is below the DC+ voltage by the voltage drops associated with the power switch and the parasitic elements of the circuit. When the high-side power switch turns off, the load current momentarily flows in the low-side freewheeling diode due to the inductive load connected to V_{S1} (the load is not shown in these figures). This current flows from the DC- bus (which is connected to the VSO pin of the HVIC) to the load and a negative voltage between V_{S1} and the DC- Bus is induced (i.e., the VSO pin of the HVIC is at a higher potential than the V_S pin).

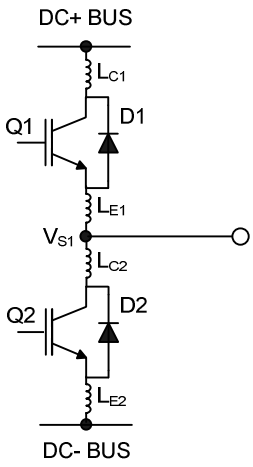


Figure 25: Parasitic Elements

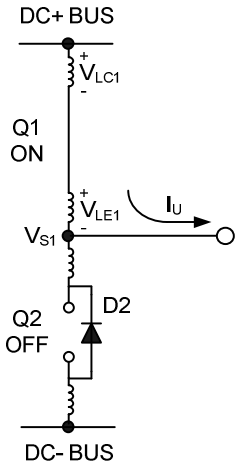


Figure 26: V_S positive

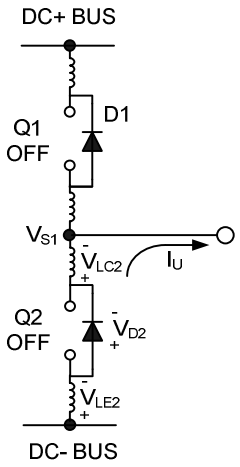


Figure 27: V_S negative

In a typical motor drive system, dV/dt is typically designed to be in the range of 3-5 V/ns. The negative V_S transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when di/dt is greater than in normal operation.

International Rectifier's HVICs have been designed for the robustness required in many of today's demanding applications. An indication of the IRS233(0,2)(D)'s robustness can be seen in Figure 28, where there is represented the IRS233(0,2)(D) Safe Operating Area at V_{BS}=15V based on repetitive negative V_S spikes. A negative V_S transient voltage falling in the grey area (outside SOA) may lead to IC permanent damage; viceversa unwanted functional anomalies or permanent damage to the IC do not appear if negative Vs transients fall inside SOA.
At V_{BS}=15V in case of -V_S transients greater than -16.5 V for a period of time greater than 50 ns; the HVIC will hold by design the high-side outputs in the off state for 4.5 µs.

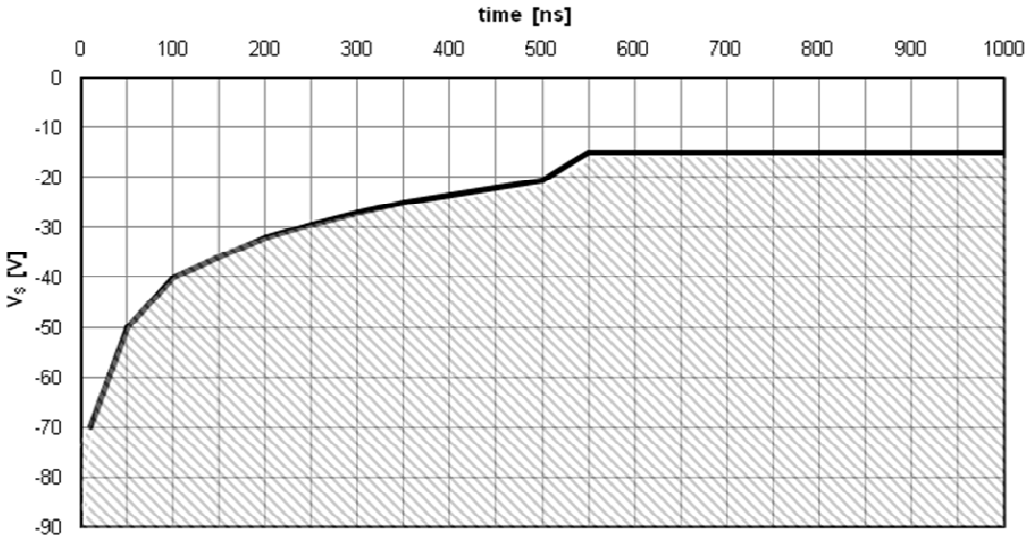


Figure 28: Negative V_S transient SOA for IRS233(0,2)(D)

Even though the IRS233(0,2)(D) has been shown able to handle these large negative V_S transient conditions, it is highly recommended that the circuit designer always limit the negative V_S transients as much as possible by careful PCB layout and component use.

DC- bus Current Sensing

A ground referenced current signal amplifier has been included so that the current in the return leg of the DC bus may be monitored. A typical circuit configuration is provided in Fig.29. The signal coming from the shunt resistor is amplified by the ratio (R1+R2)/R2. Additional details can be found on Design Tip DT 92-6. This design tip is available at www.irf.com.

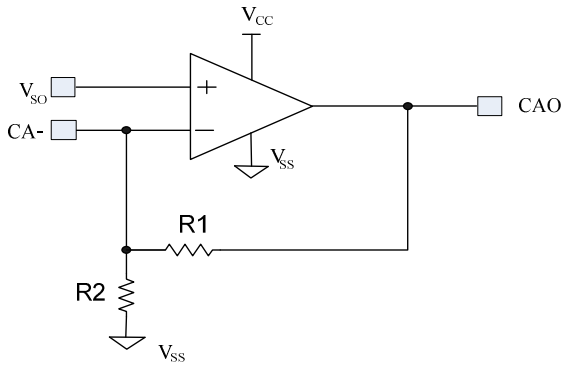


Figure 29: Current amplifier typical configuration

In the following Figures 30, 31, 32, 33 the configurations used to measure the operational amplifier characteristics are shown.

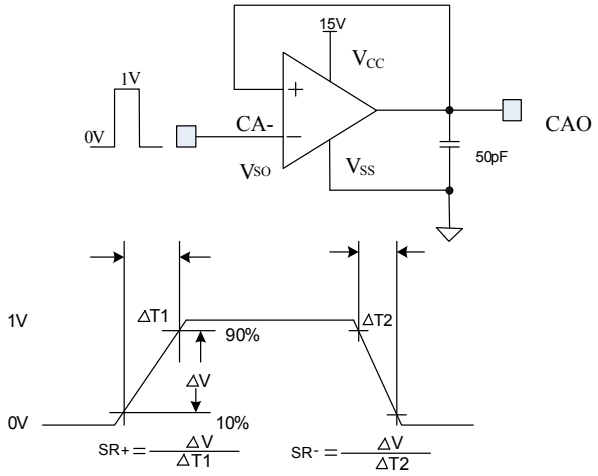


Figure 30: Operational Amplifier Slew rate measurement

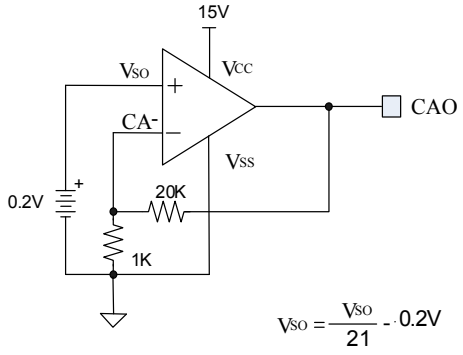
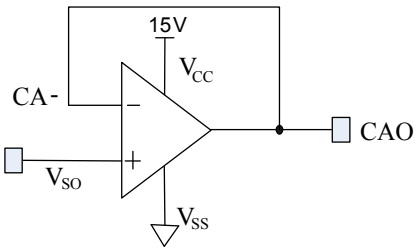


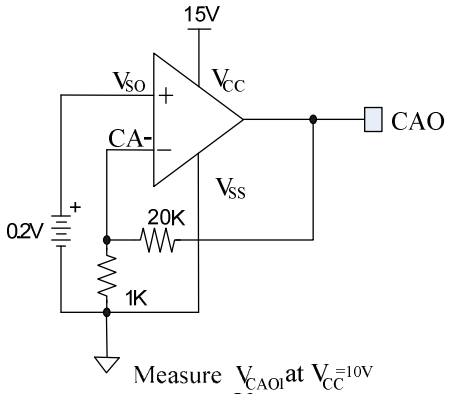
Figure 31: Operational Amplifier Input Offset Voltage measurement



Measure V_{CAO1} at V_{SO}= 0.1V
V_{CAO2} at V_{SO}=1.1V

$$CMRR=-20*LOG\left|\frac{(V_{CAO1}-0.1V)-(V_{CAO2}-1.1V)}{1V}\right| (dB)$$

Figure 32: Operational Amplifier Common mode rejection measurement



Measure V_{CAO1} at V_{CC}=10V
V_{CAO2} at V_{CC}=20V

$$PSRR=-20*LOG\left|\frac{V_{CAO1}-V_{CAO2}}{(10V)\ (21)}\right| (dB)$$

Figure 33: Operational Amplifier Power supply rejection measurement

PCB Layout Tips

Distance between high and low voltage components: It's strongly recommended to place the components tied to the floating voltage pins (V_B and V_S) near the respective high voltage portions of the device. The IRS233(0,2)(D) in the PLCC44 package has had some unused pins removed in order to maximize the distance between the high voltage and low voltage pins. Please see the Case Outline PLCC44 information in this datasheet for the details.

Ground Plane: In order to minimize noise coupling, the ground plane should not be placed under or near the high voltage floating side.

Gate Drive Loops: Current loops behave like antennas and are able to receive and transmit EM noise (see Figure 34). In order to reduce the EM coupling and improve the power switch turn on/off performance, the gate drive loops must be reduced as much as possible. Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to developing a voltage across the gate-emitter, thus increasing the possibility of a self turn-on effect.

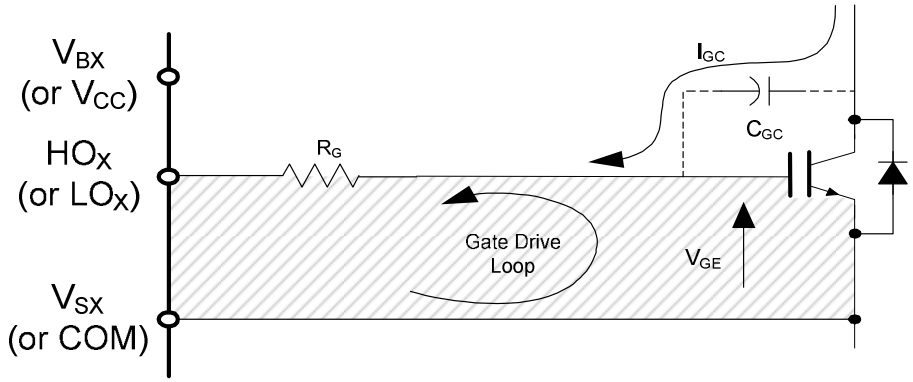


Figure 34: Antenna Loops

Supply Capacitor: It is recommended to place a bypass capacitor (C_{IN}) between the V_{CC} and V_{SS} pins. This connection is shown in Figure 35. A ceramic 1 µF ceramic capacitor is suitable for most applications. This component should be placed as close as possible to the pins in order to reduce parasitic elements.

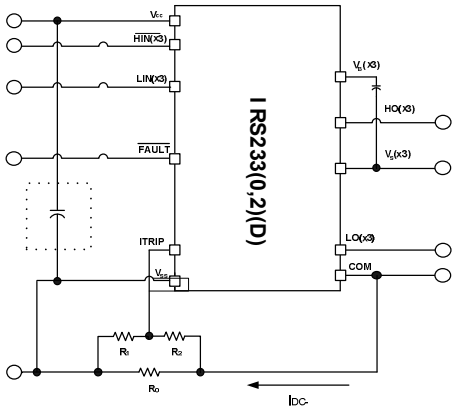


Figure 35: Supply capacitor

Routing and Placement: Power stage PCB parasitic elements can contribute to large negative voltage transients at the switch node; it is recommended to limit the phase voltage negative transients. In order to avoid such conditions, it is recommended to 1) minimize the high-side emitter to low-side collector distance, and 2) minimize the low-side emitter to negative bus rail stray inductance. However, where negative V_S spikes remain excessive, further steps may be taken to reduce the spike. This includes placing a resistor (5 Ω or less) between the V_S pin and the switch node (see Figure 36), and in some cases using a clamping diode between V_{SS} and V_S (see Figure 37). See DT04-4 at www.irf.com for more detailed information.

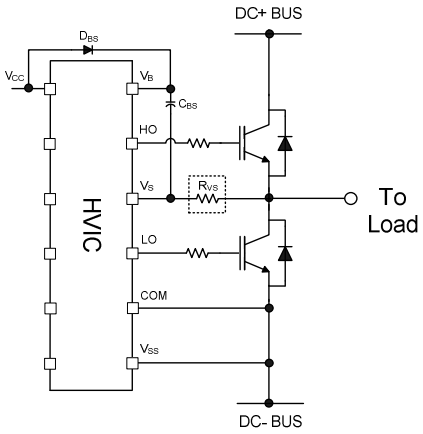


Figure 36: V_S resistor

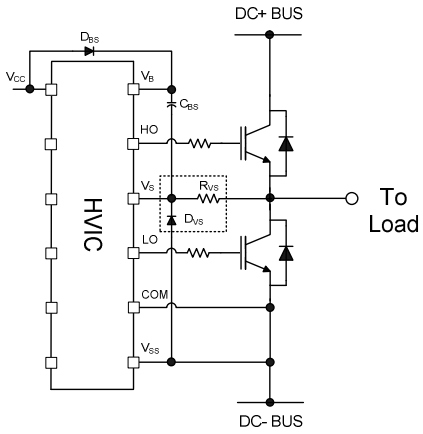


Figure 37: V_S clamping diode

Integrated Bootstrap FET limitation

The integrated Bootstrap FET functionality has an operational limitation under the following bias conditions applied to the HVIC:

- **VCC pin voltage = 0V AND**
- **VS or VB pin voltage > 0**

In the absence of a VCC bias, the integrated bootstrap FET voltage blocking capability is compromised and a current conduction path is created between VCC & VB pins, as illustrated in Fig.38 below, resulting in power loss and possible damage to the HVIC.

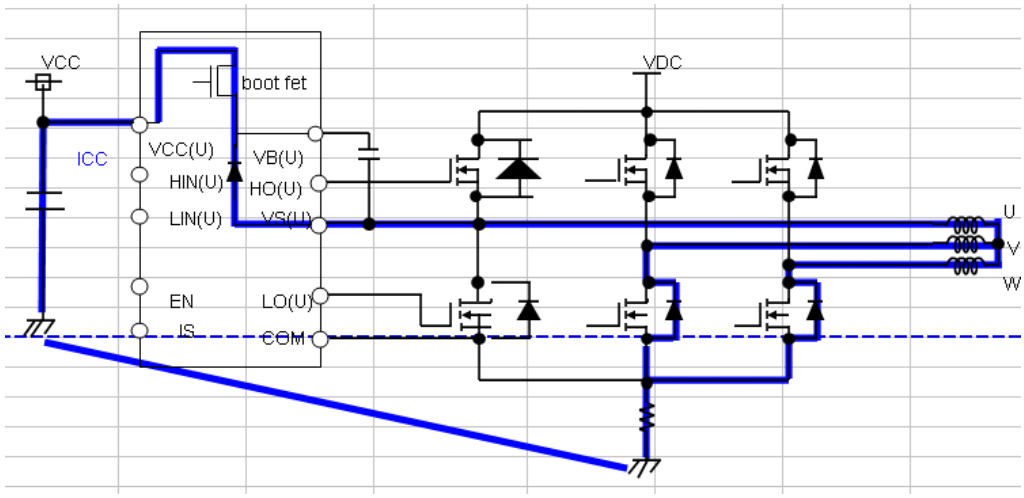


Figure 38: Current conduction path between VCC and VB pin

Relevant Application Situations:

The above mentioned bias condition may be encountered under the following situations:

- In a motor control application, a permanent magnet motor naturally rotating while VCC power is OFF. In this condition, Back EMF is generated at a motor terminal which causes high voltage bias on VS nodes resulting unwanted current flow to VCC.
- Potential situations in other applications where VS/VB node voltage potential increases before the VCC voltage is available (for example due to sequencing delays in SMPS supplying VCC bias)

Application Workaround:

Insertion of a standard p-n junction diode between VCC pin of IC and positive terminal of VCC capacitors (as illustrated in Fig.39) prevents current conduction “out-of” VCC pin of gate driver IC. It is important not to connect the VCC capacitor directly to pin of IC. Diode selection is based on 25V rating or above & current capability aligned to ICC consumption of IC - 100mA should cover most application situations. As an example, Part number # LL4154 from Diodes Inc (25V/150mA standard diode) can be used.

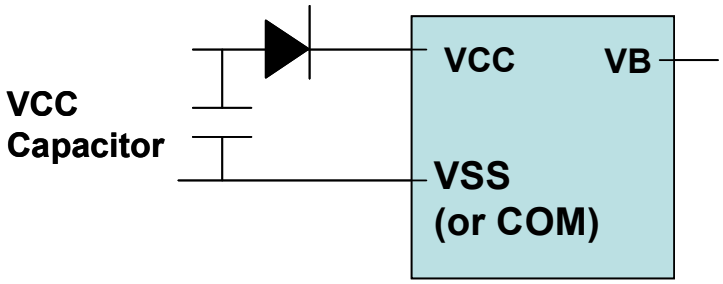


Figure 39: Diode insertion between VCC pin and VCC capacitor

Note that the forward voltage drop on the diode (V_F) must be taken into account when biasing the VCC pin of the IC to meet UVLO requirements. *VCC pin Bias = VCC Supply Voltage – V_F of Diode*.

Additional Documentation

Several technical documents related to the use of HVICs are available at www.irf.com; use the Site Search function and the document number to quickly locate them. Below is a short list of some of these documents.

DT97-3: Managing Transients in Control IC Driven Power Stages
AN-1123: Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality
DT04-4: Using Monolithic High Voltage Gate Drivers
AN-978: HV Floating MOS-Gate Driver ICs

Parameter Temperature Trends

Figures 40-78 provide information on the experimental performance of the IRS233(0,2)(D)(S&J) HVIC. The line plotted in each figure is generated from actual lab data. A small number of individual samples were tested at three temperatures (-40 ºC, 25 ºC, and 125 ºC) in order to generate the experimental (Exp.) curve. The line labeled Exp. consist of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood temperature trend. The individual data points on the curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

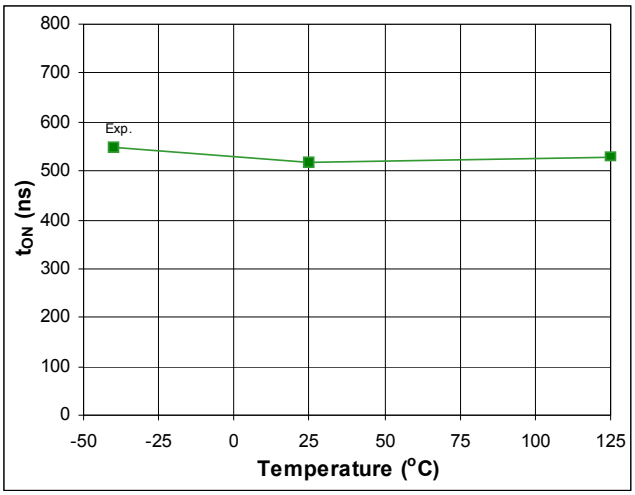


Fig. 40. Turn-on Propagation Delay vs. Temperature

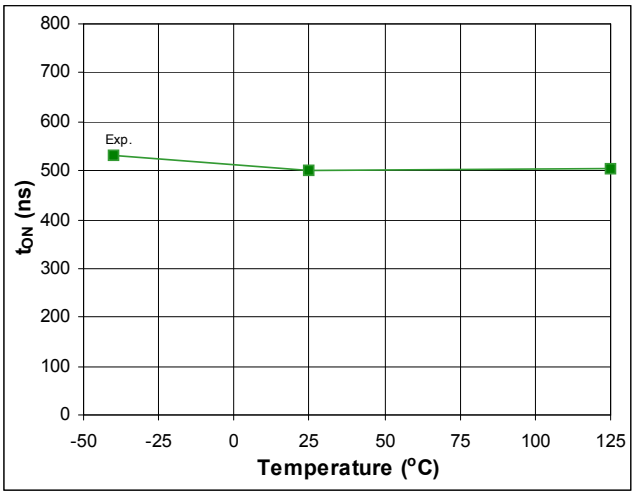


Fig. 41. Turn-on Propagation Delay vs. Temperature

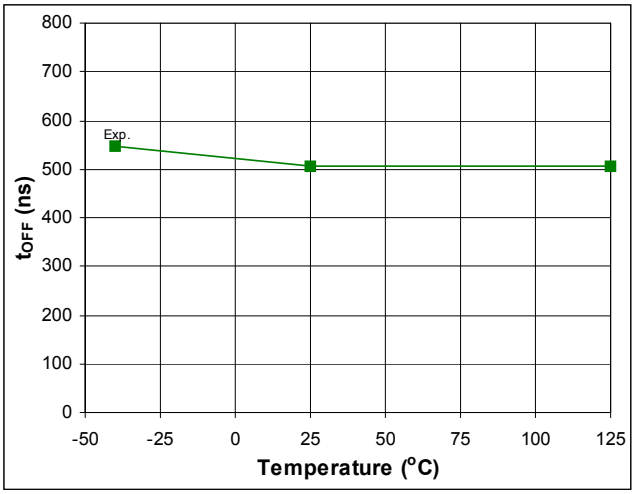


Fig. 42. Turn-off Propagation Delay vs. Temperature

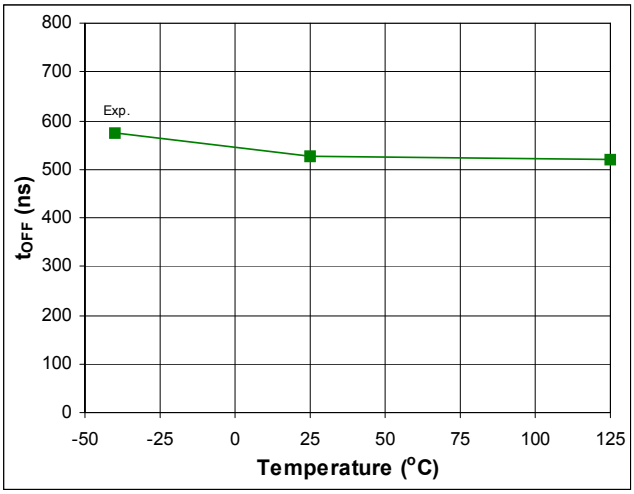


Fig. 43. Turn-off Propagation Delay vs. Temperature

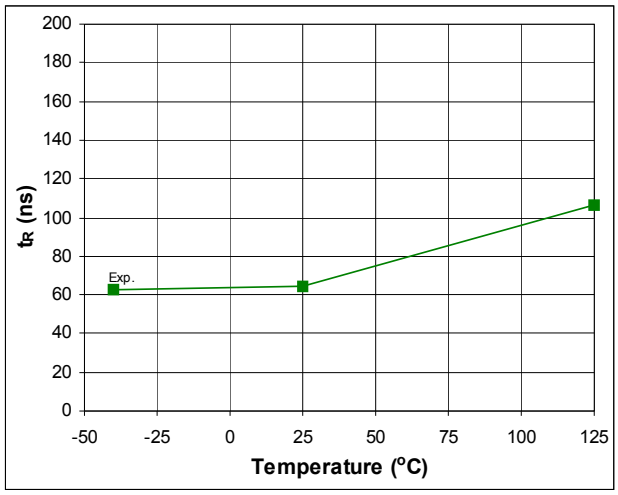


Fig. 44. Turn-on Rise Time vs. Temperature

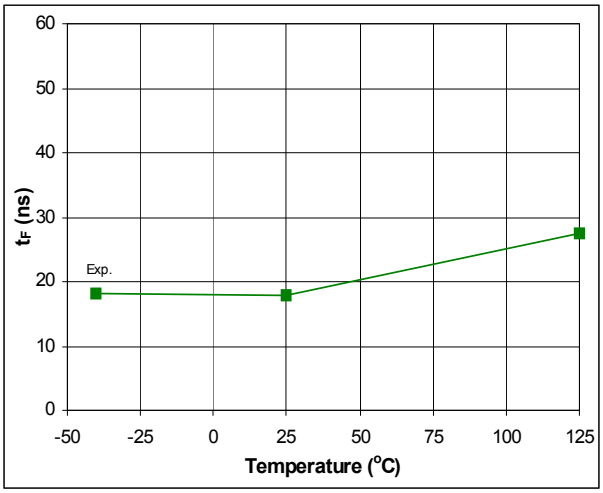


Fig.45. Turn-off Fall Time vs. Temperature

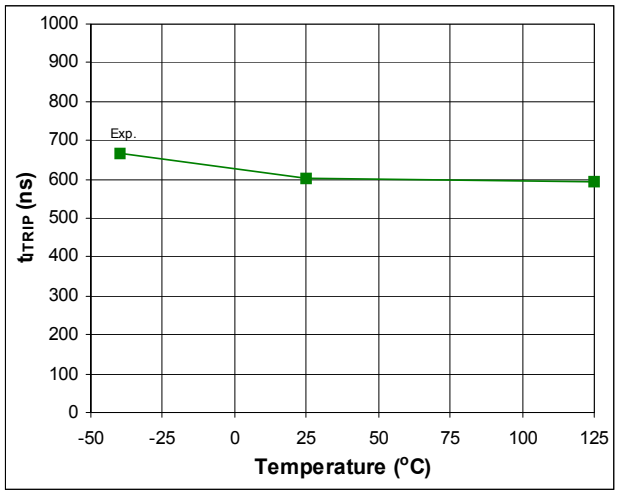


Fig. 46. ITRIP to Output Shutdown Propagation Delay vs. Temperature

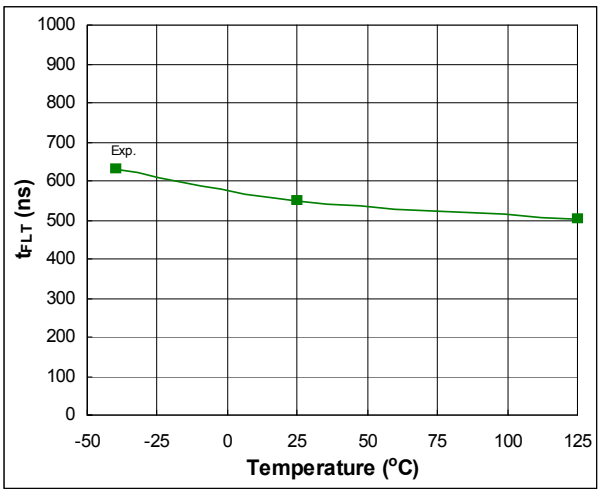


Fig. 47. ITRIP to FAULT Indication Delay vs. Temperature

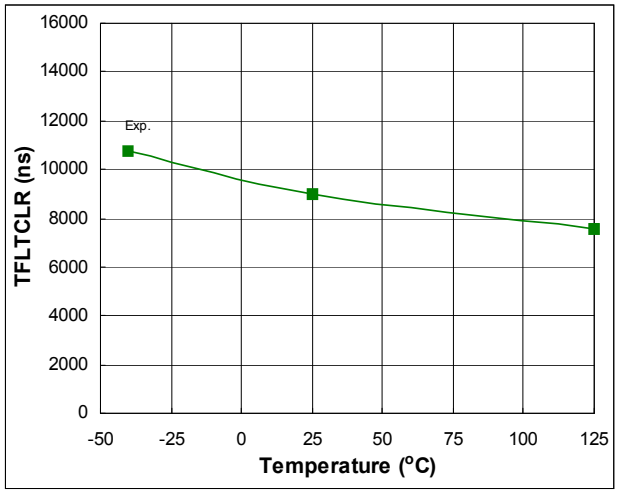


Fig.48. FAULT Clear Time vs. Temperature

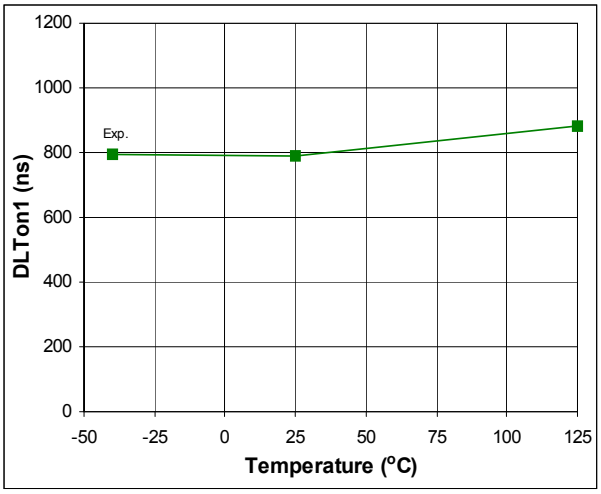


Fig. 49. Dead Time vs. Temperature

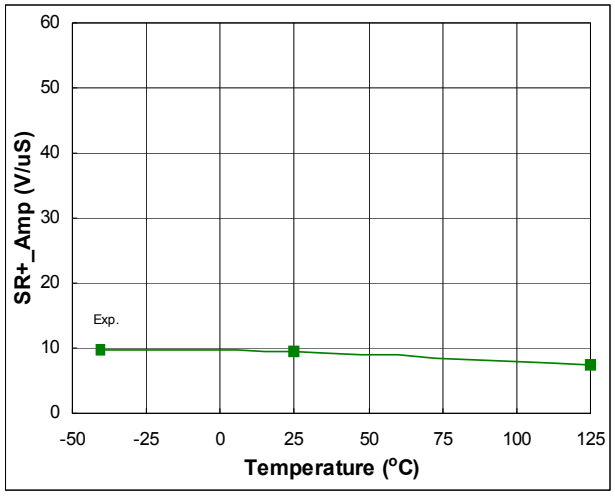


Fig. 50. Operational Amplifier Slew Rate (+) vs. Temperature

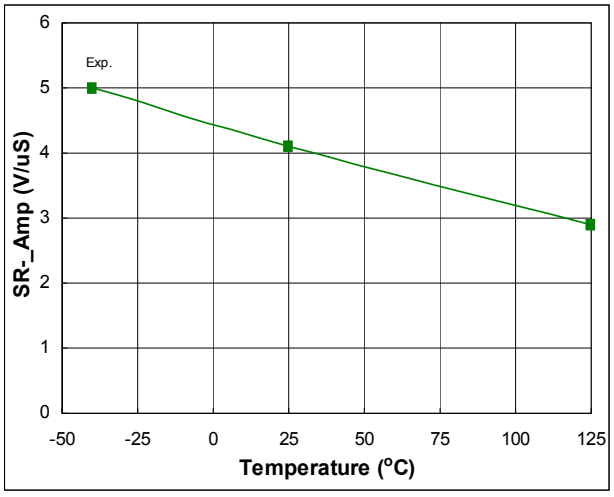


Fig. 51. Operational Amplifier Slew Rate (-) vs. Temperature

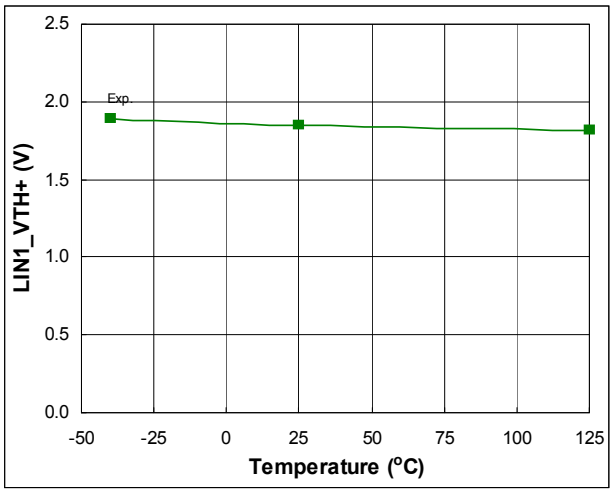


Fig. 52. Input Positive Going Threshold vs. Temperature

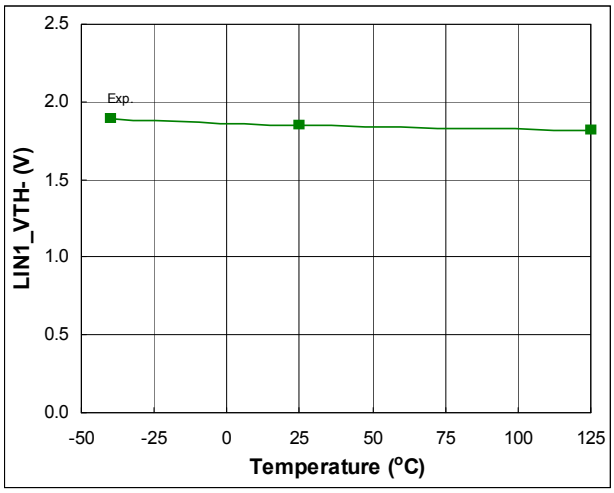


Fig. 53. Input Negative Going Threshold vs. Temperature

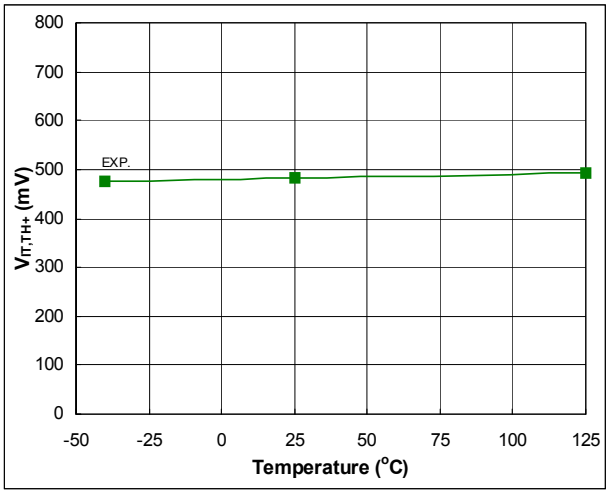


Fig. 54. ITRIP Input Positive Going Threshold vs. Temperature

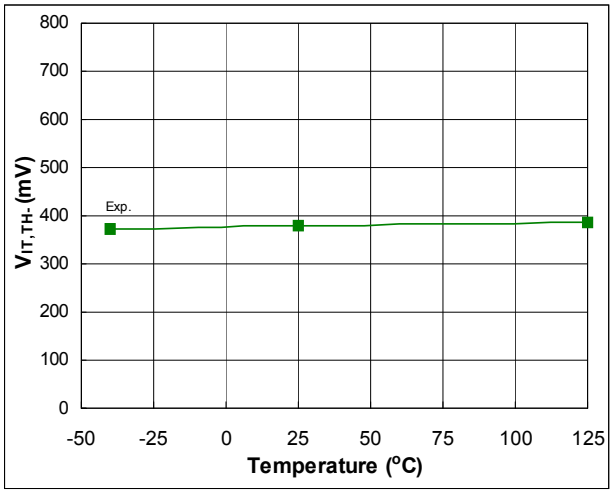


Fig. 55. ITRIP Input Negative Going Threshold vs. Temperature

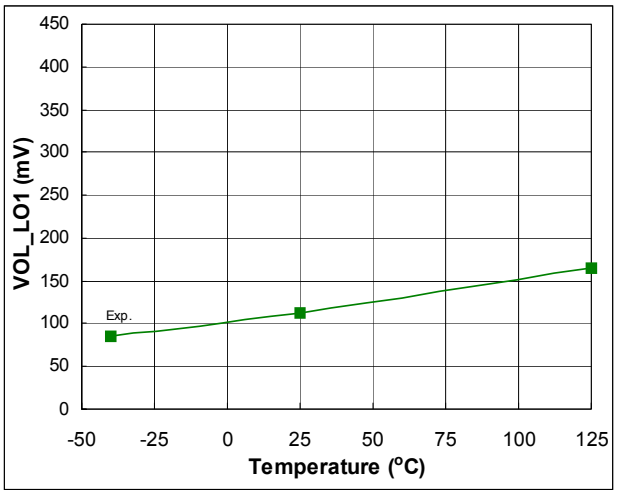


Fig. 56. Low Level Output Voltage vs. Temperature

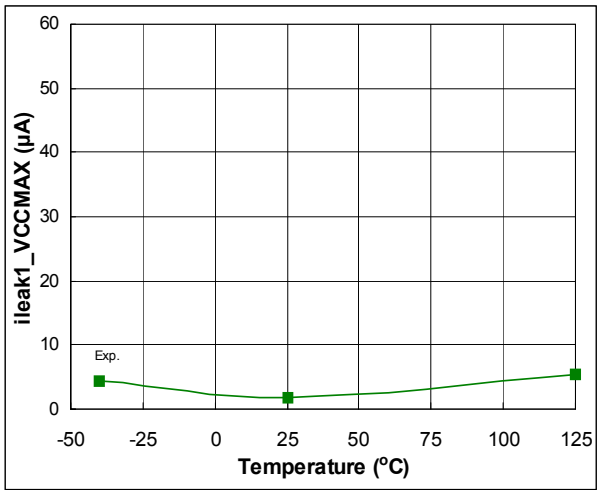


Fig. 57. Offset Supply Leakage Current vs. Temperature

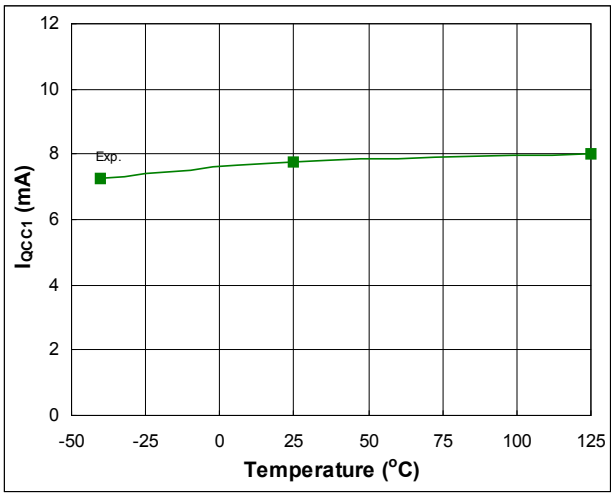


Fig. 58. Quiescent V_{CC} Supply Current vs. Temperature

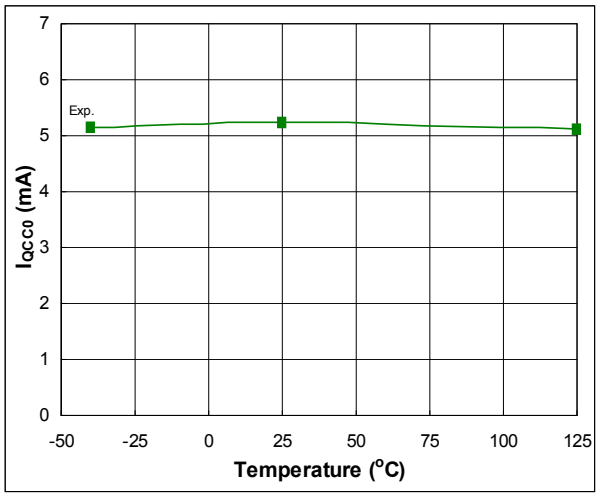


Fig. 59. Quiescent V_{CC} Supply Current vs. Temperature

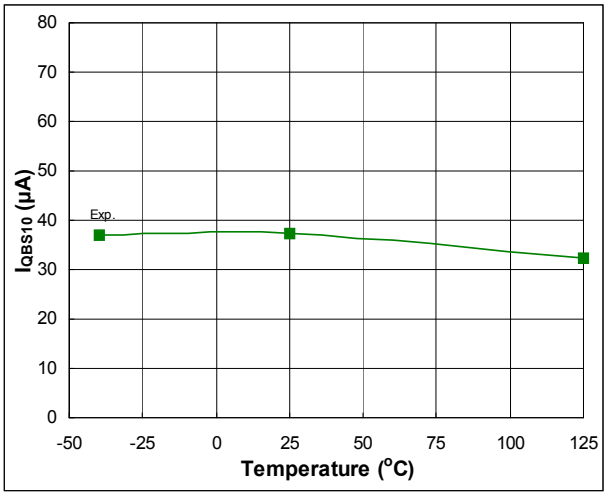


Fig. 60. Quiescent V_{BS} Supply Current vs. Temperature

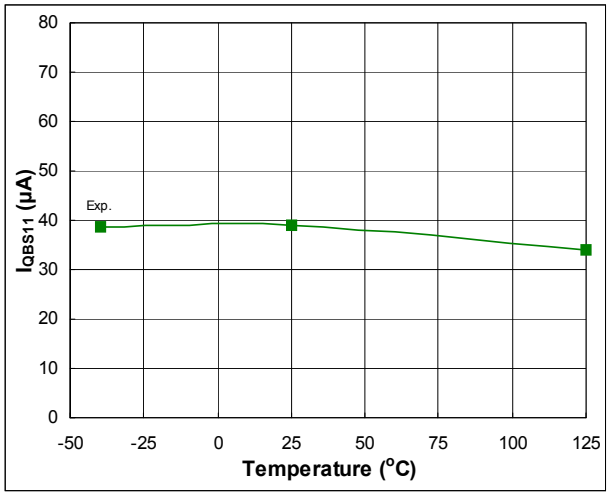


Fig. 61. Quiescent V_{BS} Supply Current vs. Temperature

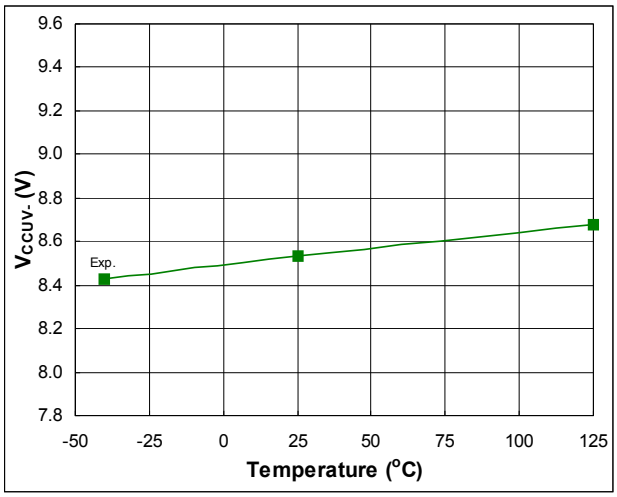


Fig. 62. V_{CC} Supply Undervoltage Negative Going Threshold vs. Temperature

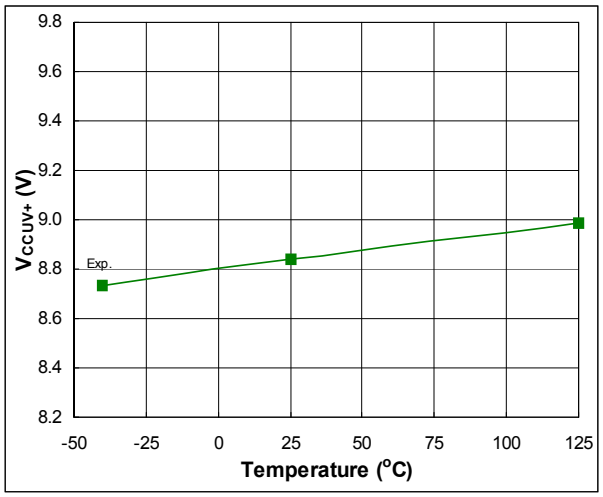


Fig. 63. V_{CC} Supply Undervoltage Positive Going Threshold vs. Temperature

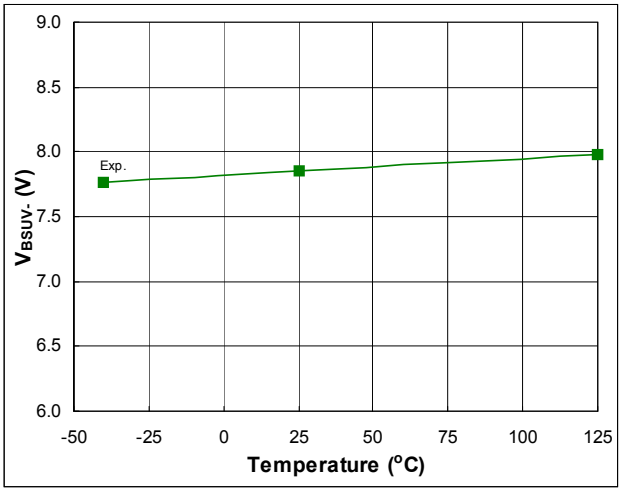


Fig. 64. V_{BS} Supply Undervoltage Negative Going Threshold vs. Temperature

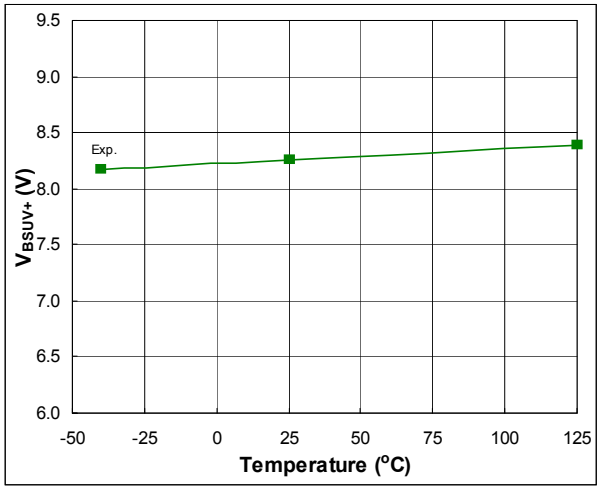


Fig. 65. V_{BS} Supply Undervoltage Positive Going Threshold vs. Temperature

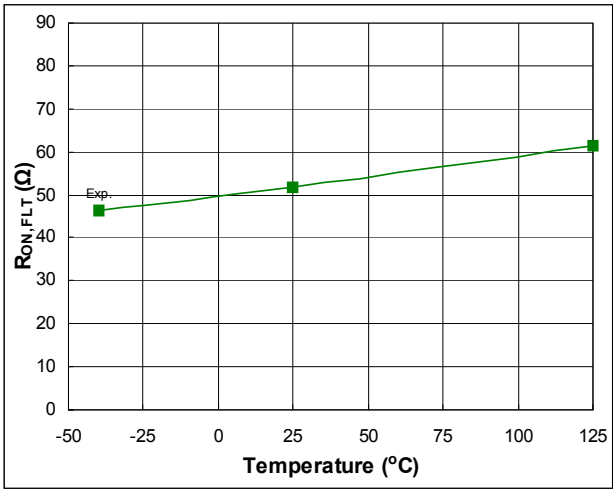


Fig. 66. FAULT Low On-Resistance vs. Temperature

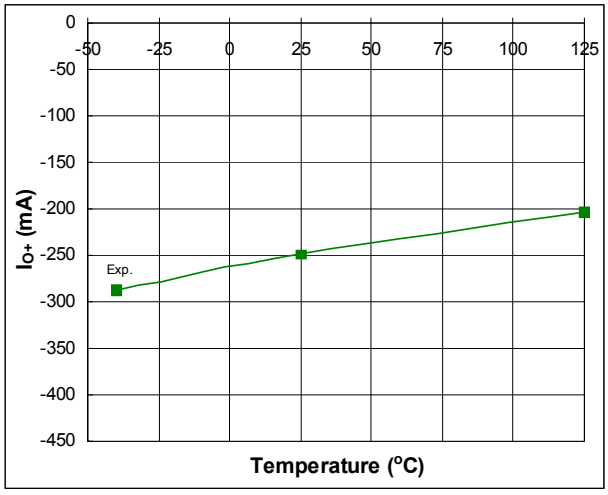


Fig. 67. Output High Short Circuit Pulsed Current vs. Temperature

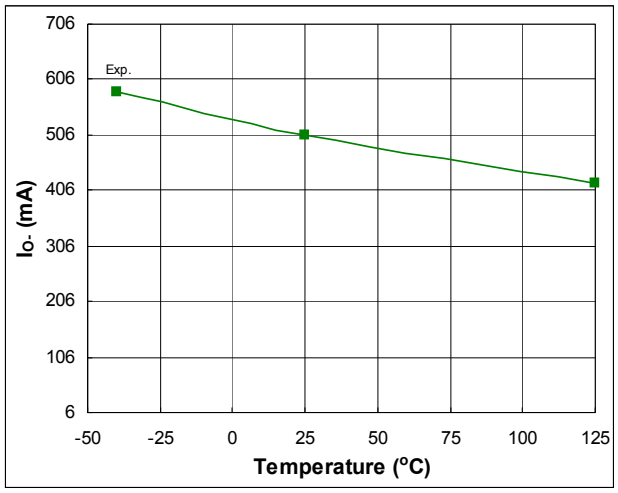


Fig. 68. Output Low Short Circuit Pulsed Current vs. Temperature

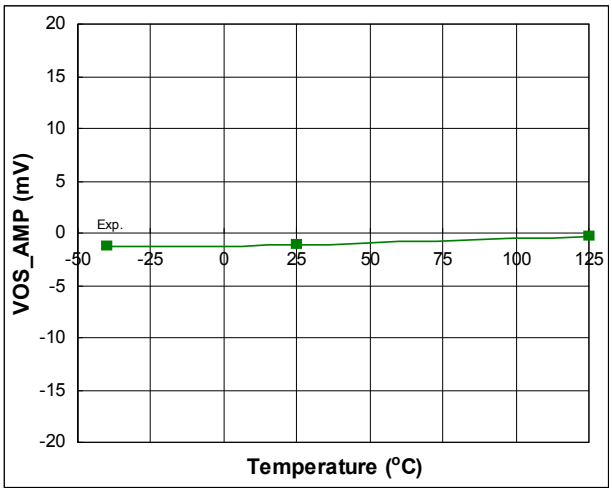


Fig. 69. Offset Opamp vs. Temperature

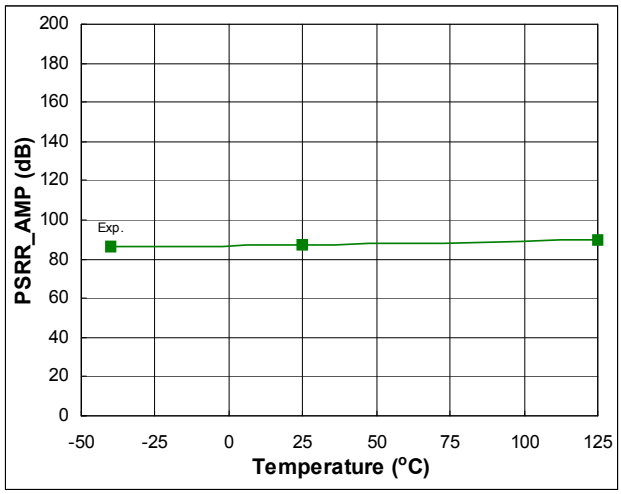


Fig. 70. Operational Amplifier Power Supply Rejection Ratio vs. Temperature

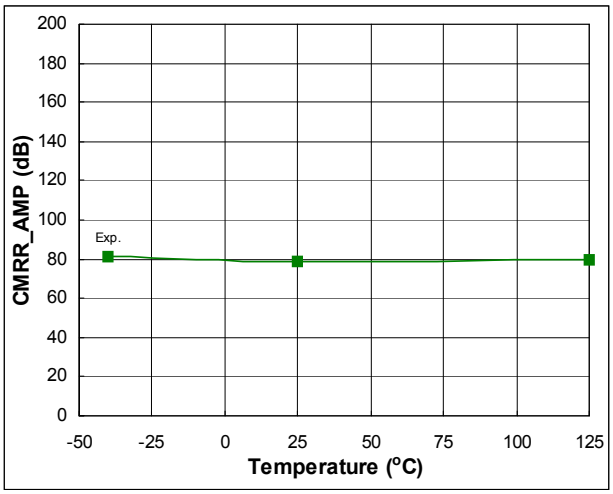


Fig. 71. Operational Amplifier Common Mode Rejection Ratio vs. Temperature

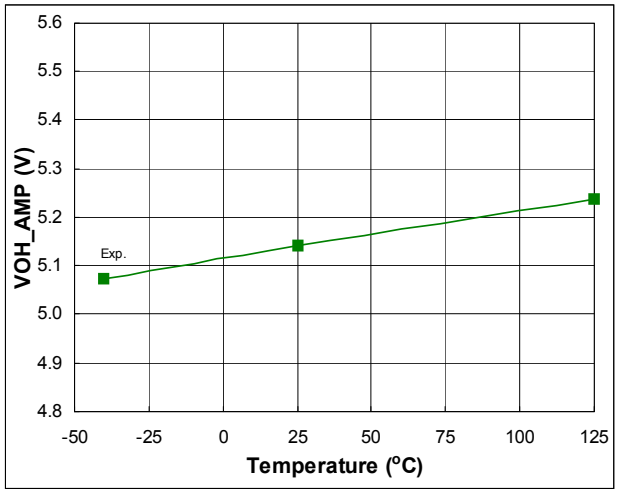


Fig. 72. Operational Amplifier High Level Output Voltage vs. Temperature

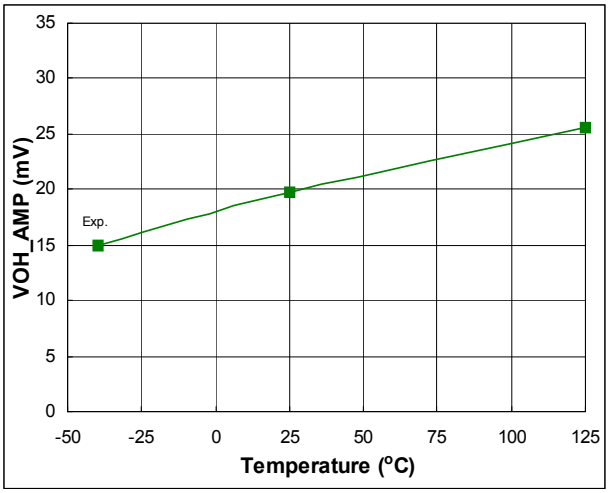


Fig. 73. Operational Amplifier Low Level Output Voltage vs. Temperature

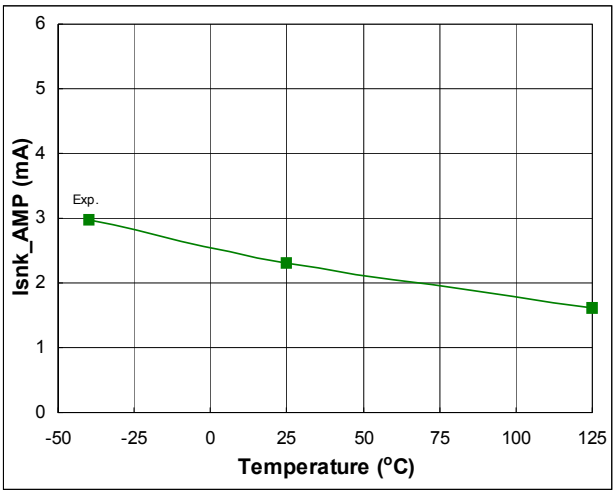


Fig. 74. Operational Amplifier Output Sink Current vs. Temperature

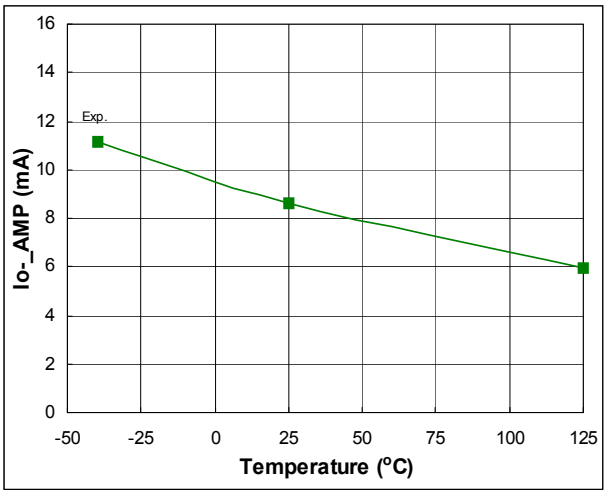


Fig. 75. Operational Amplifier Output Low Short Circuit Current vs. Temperature

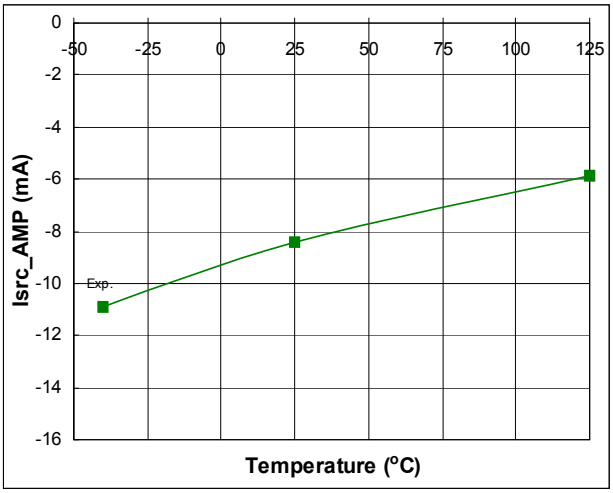


Fig. 76. Operational Amplifier Output Source Current vs. Temperature

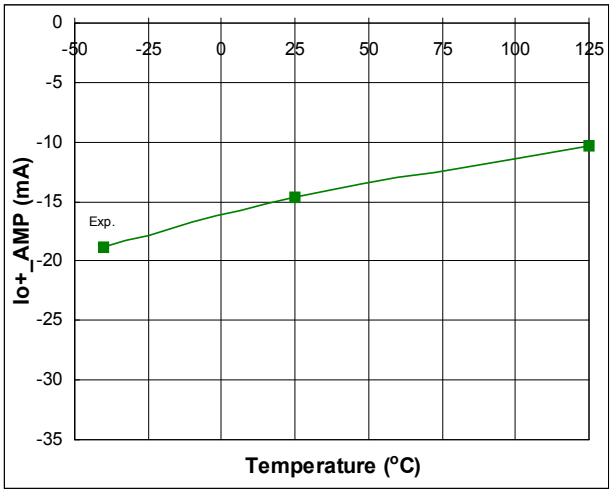


Fig. 77. Operational Amplifier Output High Short Circuit Current vs. Temperature

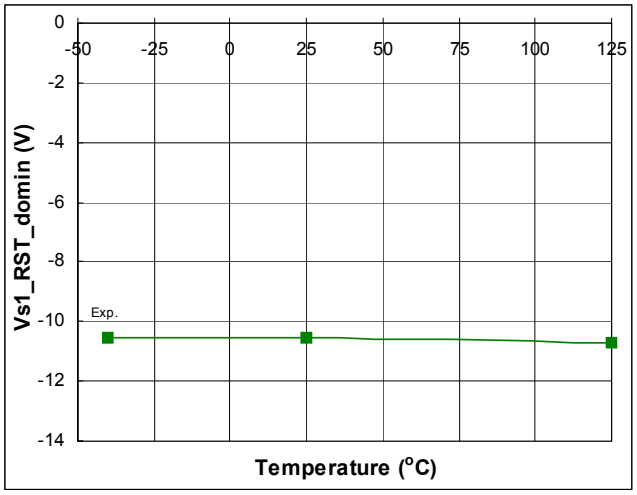
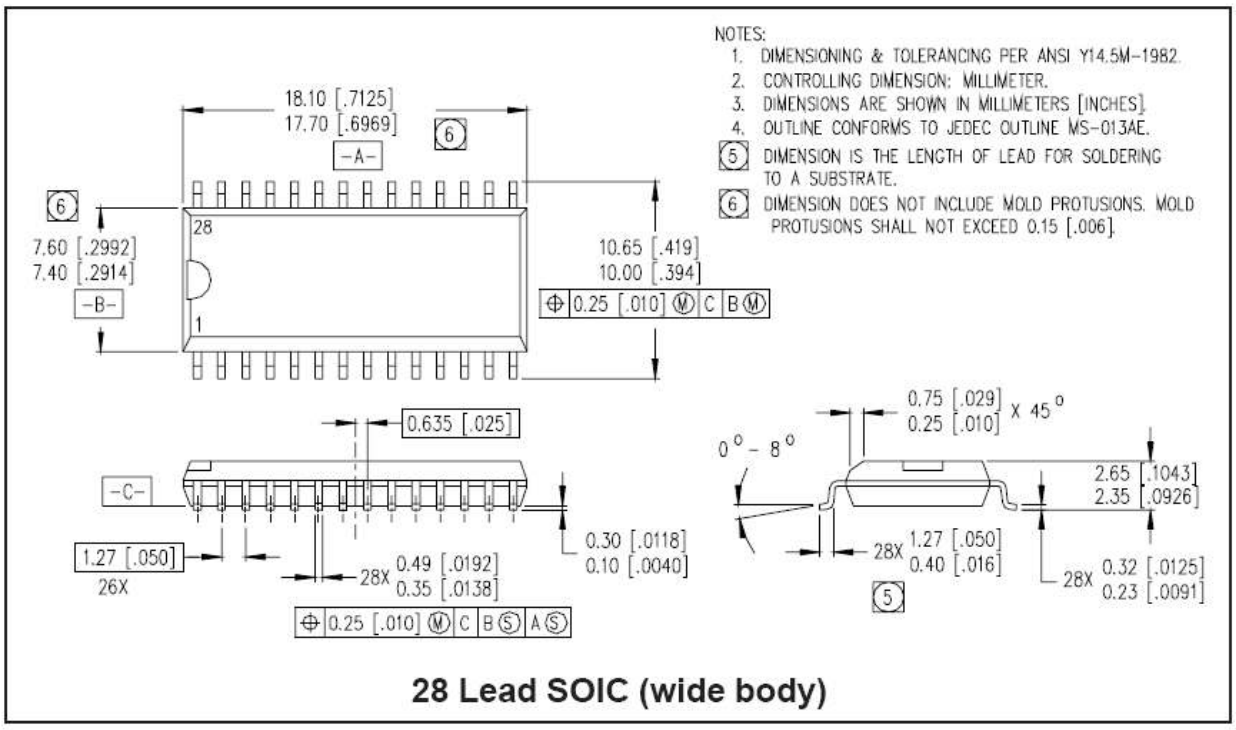


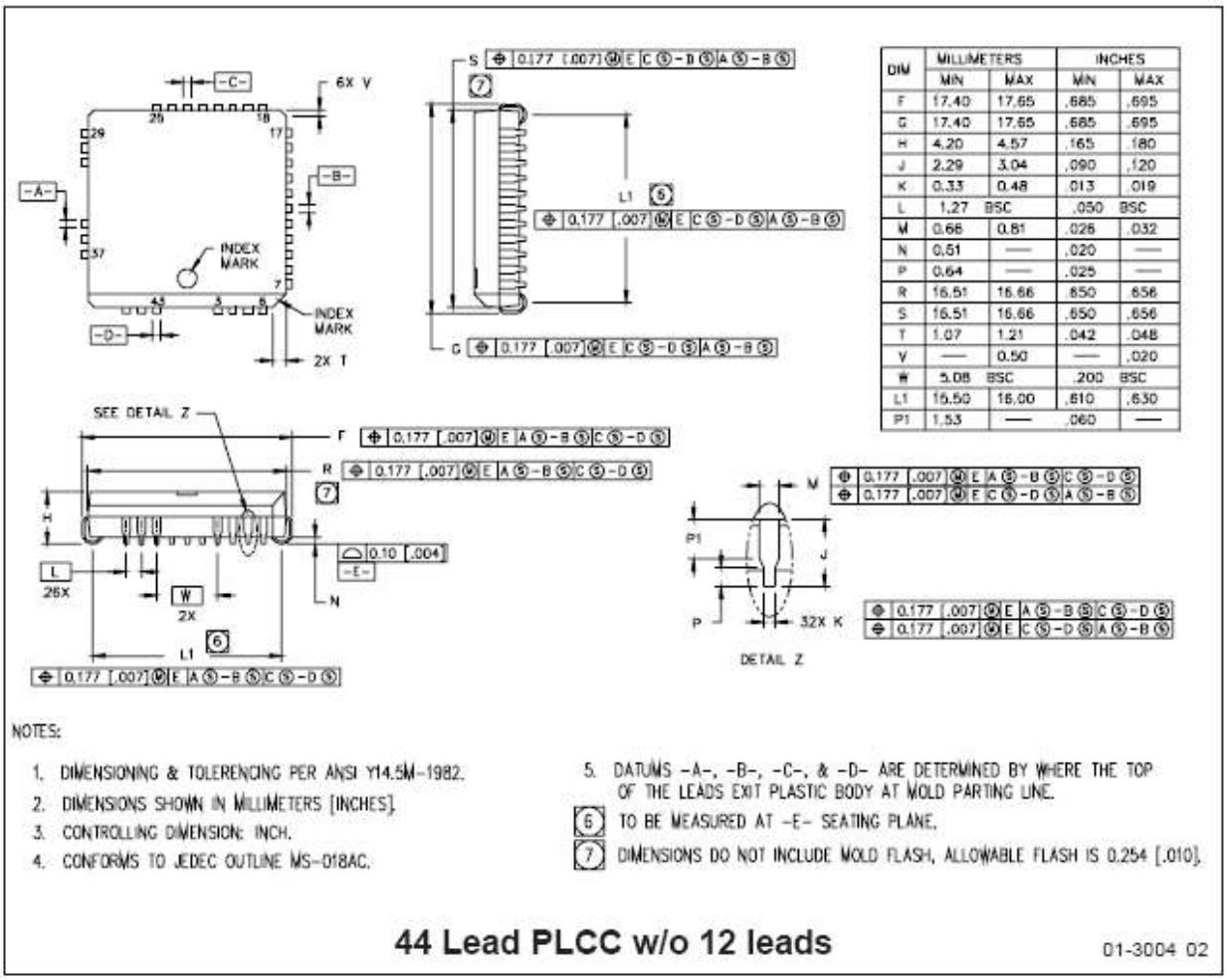
Fig. 78. Max –Vs vs. Temperature

Case Outlines



28 Lead SOIC (wide body)

Case Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F	17.40	17.65	.685	.695
G	17.40	17.65	.685	.695
H	4.20	4.57	.165	.180
J	2.29	3.04	.090	.120
K	0.33	0.48	.013	.019
L	1.27	BSC	.050	BSC
M	0.66	0.81	.026	.032
N	0.51	—	.020	—
P	0.64	—	.025	—
R	16.51	16.66	.650	.656
S	16.51	16.66	.650	.656
T	1.07	1.21	.042	.048
V	—	0.50	—	.020
W	5.08	BSC	.200	BSC
L1	15.50	16.00	.610	.630
P1	1.53	—	.060	—

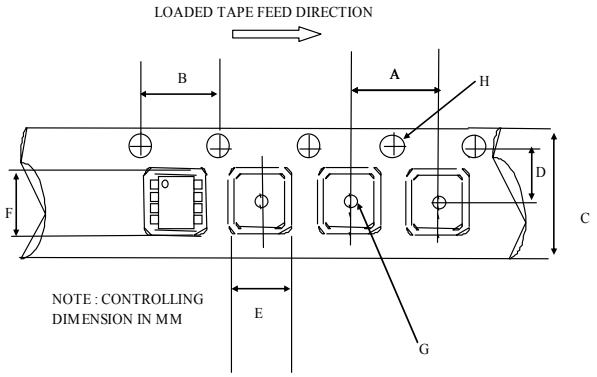
NOTES:

1. DIMENSIONING & TOLERENCING PER ANSI Y14.5M-1982.
2. DIMENSIONS SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE MS-018AC.
5. DATUMS -A-, -B-, -C-, & -D- ARE DETERMINED BY WHERE THE TOP OF THE LEADS EXIT PLASTIC BODY AT MOLD PARTING LINE.
6. TO BE MEASURED AT -E- SEATING PLANE.
7. DIMENSIONS DO NOT INCLUDE MOLD FLASH, ALLOWABLE FLASH IS 0.254 [.010].

44 Lead PLCC w/o 12 leads

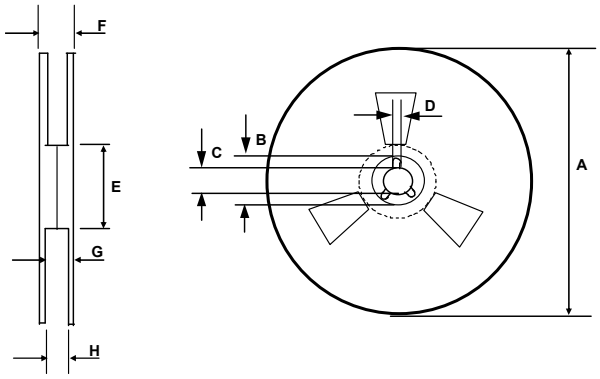
01-3004 02

Tape and Reel Details: SOIC28W



CARRIER TAPE DIMENSION FOR 28SOICW

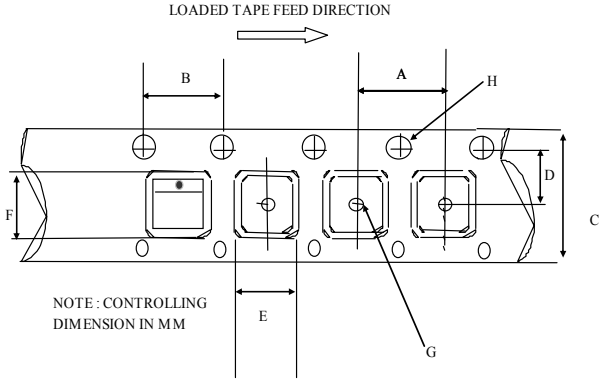
Code	Metric		Imperial	
	Min	Max	Min	Max
A	11.90	12.10	0.468	0.476
B	3.90	4.10	0.153	0.161
C	23.70	24.30	0.933	0.956
D	11.40	11.60	0.448	0.456
E	10.80	11.00	0.425	0.433
F	18.20	18.40	0.716	0.724
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 28SOICW

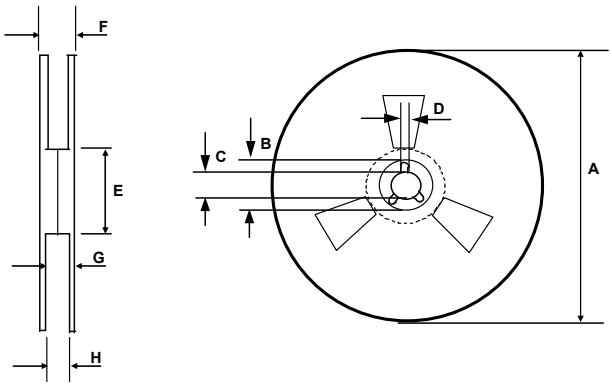
Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	30.40	n/a	1.196
G	26.50	29.10	1.04	1.145
H	24.40	26.40	0.96	1.039

Tape and Reel Details: PLCC44



CARRIER TAPE DIMENSION FOR 44PLCC

	Metric		Imperial	
Code	Min	Max	Min	Max
A	23.90	24.10	0.94	0.948
B	3.90	4.10	0.153	0.161
C	31.70	32.30	1.248	1.271
D	14.10	14.30	0.555	0.562
E	17.90	18.10	0.704	0.712
F	17.90	18.10	0.704	0.712
G	2.00	n/a	0.078	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 44PLCC

	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	38.4	n/a	1.511
G	34.7	35.8	1.366	1.409
H	32.6	33.1	1.283	1.303

Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRS233(0,2)(D)	SOIC28W	Tube/Bulk	25	IRS233(0,2)(D)SPbF
		Tape and Reel	1000	IRS233(0,2)(D)STRPbF
	PLCC44	Tube/Bulk	27	IRS233(0,2)(D)JPbF
		Tape and Reel	500	IRS233(0,2)(D)JTRPbF

For technical support, please contact IR's Technical Assistance Center
http://www.irf.com/technical-info/

WORLD HEADQUARTERS:
233 Kansas St., El Segundo, California 90245
Tel: (310) 252-7105

Change History

Revision	Date	Change comments
0.0	10/17/07	Initial data sheet converted from IRS2130xD data sheet
0.1	03/05/08	Initial Review
0.2	03/18/08	Included tri-temp plots
0.3	03/18/08	Updated test conditions
0.4	03/26/08	Updated limits using DR3 Limits table
0.5	03/27/08	Included application notes
0.6	03/27/08	Updated minor errors and completed review for DR3
0.7	03/28/08	Corrected reflow temperature for PLCC44 to 245°C
0.8	04/02/08	Added Integrated Operational Amplifier feature on front page and RoHS compliant.
0.9	04/11/08	Corrected logic level compatible on Page1 from 2.5V to 3.3V
1.0	04/15/08	Added MDT parameter
1.1	04/16/08	Updated MDT spec. and changed latch-up level to A
1.2	04/28/08	Removed typical MDT spec.; MDT expected to be zero and cannot be more than maximum spec.
	May 8, 08	Changed file format from “rev1.2” to May 8, 2008. Corrected part number in Fig. 15
	July 8, 08	changed Iqcc test condition to Vin=4V from 0V.
	June 1, 11	Add bootstrap fet limitation

单击下面可查看定价，库存，交付和生命周期等信息

>>Infineon Technologies(英飞凌)