IRPLLNR5

IRPLLNR5 Wide Range Input Linear Fluorescent Ballast Reference Design Using the IRS2168D

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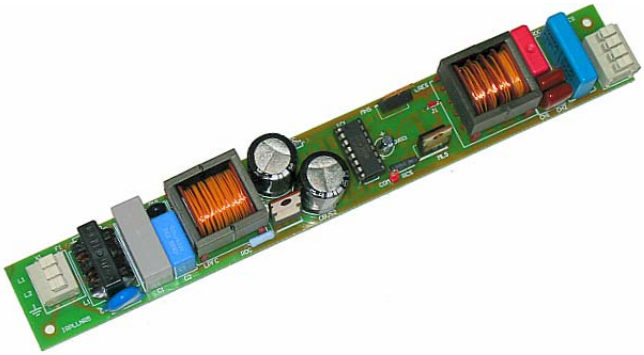


1. Features

- Drives 1 x 54 W TL5 Lamp
- Input Voltage: 90-305 VAC
- High Power Factor/Low Total Harmonic Distortion
- High Frequency Operation
- Lamp Filament Preheating
- Lamp Fault Protection with Auto-Restart After Lamp Replacement
- Low AC Line Protection
- Lamp End-of-Life Shutdown
- **IRS2168D** HVIC Ballast Controller

2. Description

The IRPLLNR5 reference design is a high efficiency, high power factor, fixed output, electronic ballast designed for driving rapid-start fluorescent lamp types. The design contains an EMI filter, active power factor correction, and a ballast control circuit using the IRS2168D(S)PbF Ballast Control IC. This reference design is intended to ease the evaluation of the IRS2168D, demonstrate PCB layout techniques, and serve as an aid in the development of a production-ready ballast using the IRS2168D.

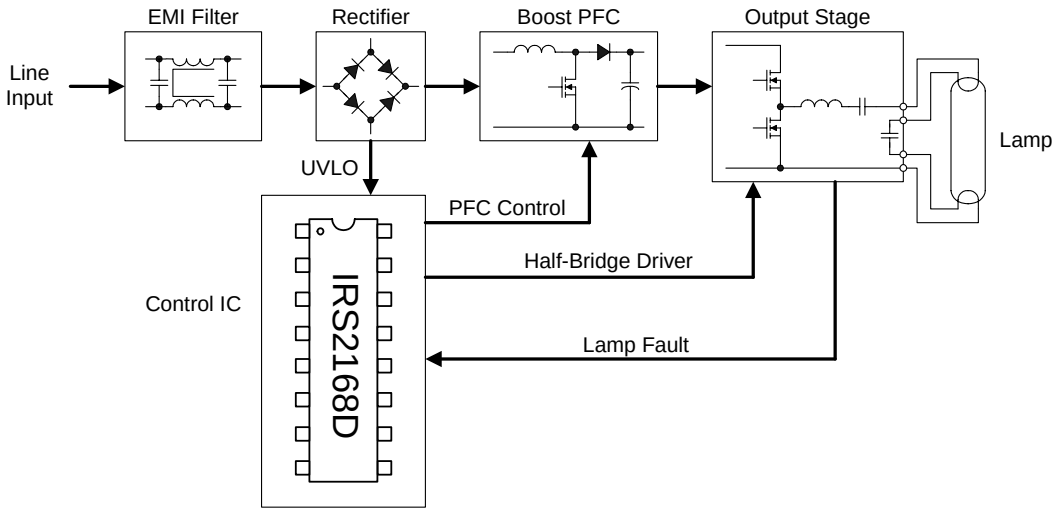


Fig. 1: Ballast Block Diagram

3. Electrical Characteristics

Parameter	Units	Value
Lamp Type		54 W TL5
Input Power	[W]	54
Lamp Running Voltage	[Vpp]	400
Run Mode Frequency	[kHz]	50
Preheat Mode Frequency	[kHz]	85
Preheat Time	[s]	1.0
Lamp Preheat Voltage	[Vpp]	500
Lamp Ignition Voltage	[kVpp]	2.0
Input AC Voltage Range	[VAC]	90-305 VAC
Power Factor		0.995 at 120 VAC 0.98 at 220 VAC
Total Harmonic Distortion	[%]	10 at 120 VAC 14 at 220 VAC

Table 3.1: Ballast Parameters

Vin	Pin (W)	PF	THD (%)	DCBUS (V)
90	55.5	0.997	9.15	495
110	52.8	0.996	9.85	495
130	51.8	0.994	11	495
150	51.1	0.992	11.25	495
170	50.8	0.99	12.2	495
190	50.7	0.987	12.8	495
210	50.6	0.983	13.9	495
230	50.5	0.978	14.9	495
250	50.5	0.972	16.1	495
270	50.5	0.964	17.7	495

Table 3.2: PFC Data

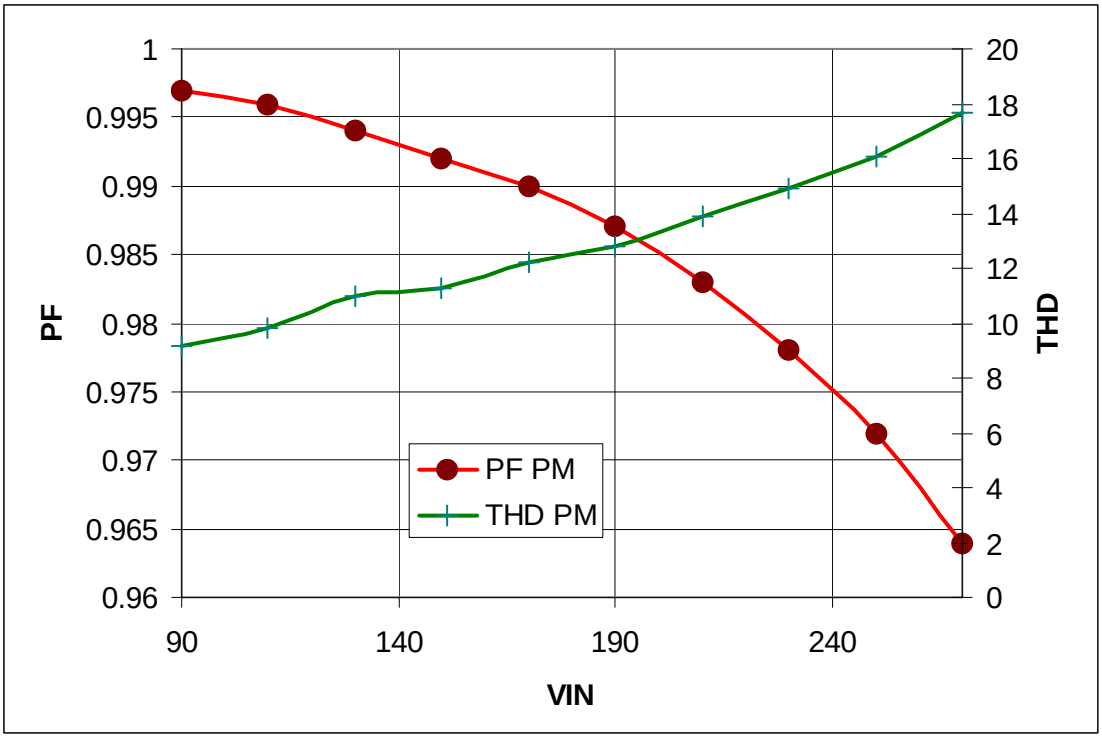


Fig. 2: PFC and THD Performances versus Input Voltage

4. Fault Protection Characteristics

Fault	Ballast	Restart Operation
Line Voltage Low	Deactivates	Increase line voltage
Upper Filament Broken	Deactivates	Lamp exchange
Lower Filament Broken	Deactivates	Lamp exchange
Failure to Ignite	Deactivates	Lamp exchange
Open Circuit (no lamp)	Deactivates	Lamp exchange
End of Life	Deactivates	Lamp exchange

5. IRPLLNR5 Schematics

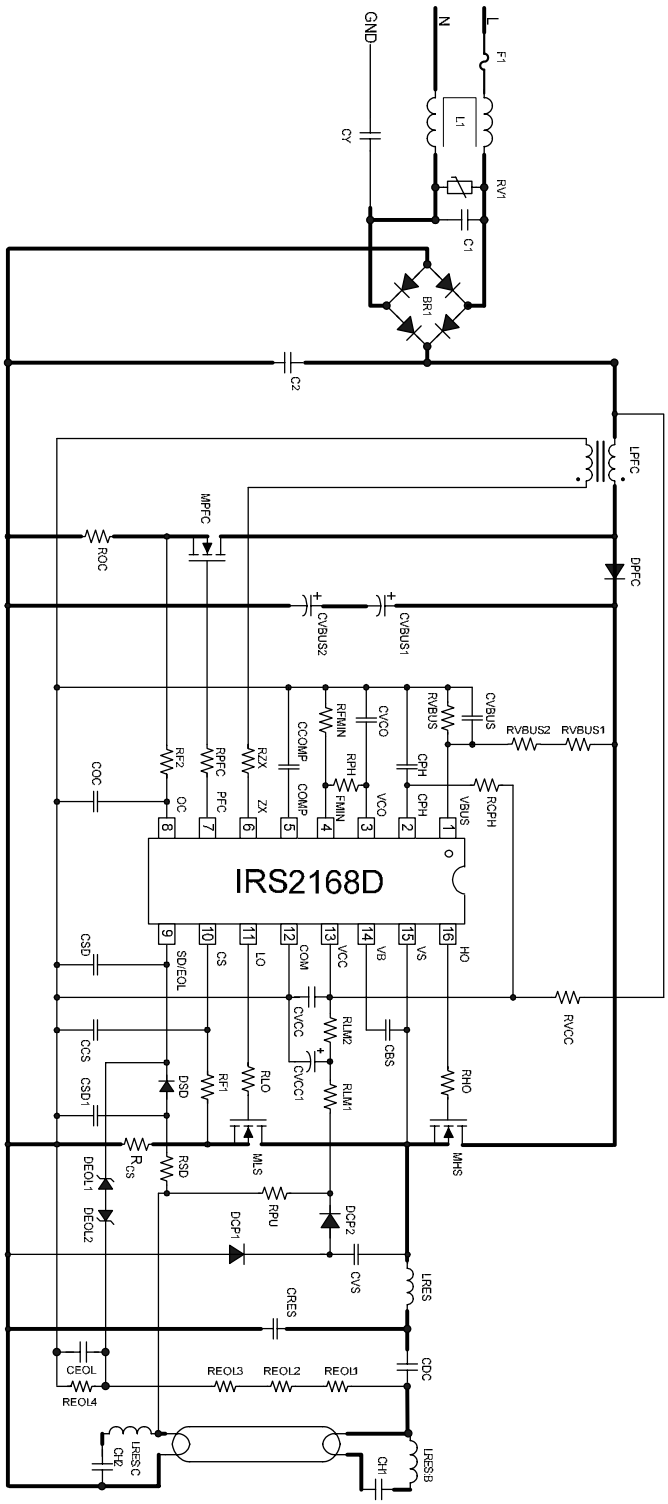


Fig. 3: Schematic Diagram, IRS2168D, Single Lamp, Voltage Mode Heating

6. PCB Component Placement Diagram and Board Fabrication

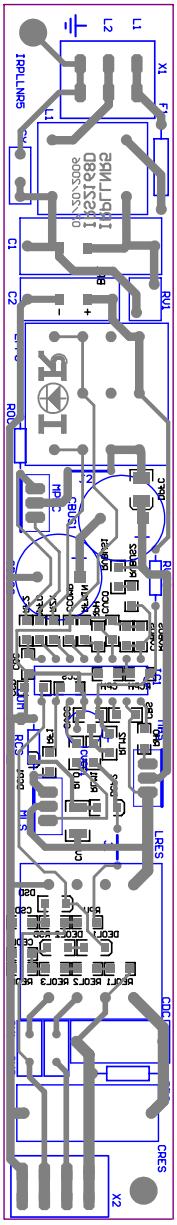


Fig. 4: PCB Component Placement Diagram

Board Fabrication

1) Board size: L = 8.59 inch, W = 1.195 inch
2) No. of copper layers: 1 (bottom layer)
3) Copper: 2 oz.
4) Board material: FR-4
5) Through hole plating: No
6) Solder plating on pads: Yes
7) Solder mask: Green LP1 (bottom layer only)
8) Silk screen layers: Top and bottom
9) Silk screen ink: White epoxy, non-conductive
10) Gerber file: IRPLLNR5.ZIP
11) Gerber file description:
    a) IRPLLNR5.apr Apertures
    b) IRPLLNR5.DRL NC drill
    c) IRPLLNR5.DRR NC drill
    d) IRPLLNR5.GBL Bottom layer
    e) IRPLLNR5.GBO Silk screen bottom
    f) IRPLLNR5.GBS Solder mask bottom
    g) IRPLLNR5.GD1 Drill drawing
    h) IRPLLNR5.GG1 Drill guide
    i) IRPLLNR5.GM1 Mechanical layer
    j) IRPLLNR5.GTO Silk-screen top

7. Bill of Material and Inductor Specification

Item	Qty	Manufacturer	Part Number	Description	Reference
1	1	Diodes Inc.	DF10S	Bridge Rectifier, 1 A, 1000 V	BR1
2	1	Roederstein	WKP222MCPEJ0K	Capacitor, 2.2 nF, 305 VAC Y Cap	CY
3	1	Dale	CW-1/2	Resistor, 0.5 Ω, 1/2 W	F1
4	1	Roederstein	F1772433-2200	Capacitor, 0.33 µF, 275 VAC	C1
5	1	Panasonic	ELF-15N007A	EMI Inductor, 10 mH, 0.7 A peak	L1
6	1	Vishay Dale	MKP1841410634	Capacitor, 0.1 µF, 630 VDC	C2
7	1	Wima	MKP10-.1/400/10	Capacitor, 0.1 µF, 400 VDC	CDC
8	1	Panasonic	ERZ-V05D471	Transient Suppressor	RV1
9	1	VOGT	IL 060 320 41 02	PFC Inductor, 2 mH, 2.5 A peak	LPFC
10	2	Panasonic	EEU-EB2V330S	Capacitor, 33 µF, 350 VDC, 105 °C	CBUS1, CBUS2
11	2	Panasonic	ECJ-3VB1E104K	Capacitor, 0.1 µF, SMT 1206	CBS, CVCC
12	2	Panasonic	ECU-V1H102JCH	Capacitor, 1 nF, SMT 1206	CSD, CEOL (see Note 2)
13	3	Panasonic	ECJ-3YB1E105K	Capacitor, 1 µF, SMT 1206	CCOMP, CPH, CVCO
14	1	Panasonic	ECU-V1H103KBM	Capacitor, 0.01 µF, SMT 1206	CVBUS
15	1	Panasonic	ECJ-3VB1E334K	Capacitor, 0.33 µF, SMT 1206	CSD1
16	1	Panasonic	ECE-A1EKG100	Capacitor, 10 µF, 25 VDC, 105 °C	CVCC1
17	1	Johanson Dielectrics	102R29W102KV4E	Capacitor, 1 nF, 1 kV, SMT 1808	CBS
18	1	WIMA	FKP1-3300/2000/5	Capacitor, 3.3 nF, 2 kV	CRES
19	2	Panasonic	ECU-V1H471KBM	Capacitor, 470 pF, SMT 1206	CCS, COC
20	2	Panasonic	ECQB1104JFW	Capacitor, 0.1 µF, 100 V	CH1, CH2
21	1	Diodes Inc.	ZMM5240B-7	Zener diode, 10 V, Minimelf, 0.5 W	DEOL1
22	1	Diodes Inc.	ZMM5232B-7	Zener diode, 5.6 V, Minimelf, 0.5 W	DEOL2
23	1	Digi-key	MURS160DICT-ND	Diode, 1 A, 600 V, SMT SMB	DPFC
24	3	Diodes	LL4148DICT-ND	Diode, 1N4148, SMT DL35	DCP1, DCP2, DSD
25	1	Tyco Electronics/Amp	2-641262-1	DIP 16 IC Socket Through-Hole	IC1
26	1	International Rectifier	IRS2168D	IC, Ballast Driver / PFC	IC1
27	1	VOGT	IL 060 320 51 01	Resonant Inductor, 2 mH, 2 A peak	LRES
28	3	International Rectifier	IRFB9N60A	Transistor, MOSFET	MPFC, MHS, MLS
29	2		> = 22 A.W.G	Jumpers	J1, J2
30	5	Panasonic	ERJ-8GEYJ120V	Resistor, 12 Ω, SMT 1206	RPFC, RLO, RHO, RLM1, RLM2
31	1	Panasonic	ERJ-8GEYJ474V	Resistor, 470 kΩ, SMT1206	RCPH
32	1	Phoenix Passive Components	5033ED220K0F12AF5	Resistor, 220 kΩ, 1/2 W	RVCC
33	2	Panasonic	ERJ-8GEYJ684V	Resistor, 680 kΩ, SMT 1206	RVBUS1, RVBUS2
34	1	Panasonic	ERJ-8GEYJ333V	Resistor, 33 kΩ, SMT 1206	RZX
35	2	Panasonic	ERJ-8GEYJ102V	Resistor, 1 kΩ, SMT 1206	RF1, RF2
36	1	Vishay/Dale	RS01A1R500FS70	Resistor, 1.5 Ω, 1%, 1 W	RCS
37	1	Digi-Key	P0.62W-1BK-ND	Resistor, 0.62 Ω, 1 W	ROC
38	1	Panasonic	ERJ-8ENF1132V	Resistor, 11.3 kΩ, 1%, SMT 1206	RVBUS
39	1	Panasonic	ERJ-8GEYJ104V	Resistor, 100 kΩ, SMT 1206	RSD
40	4	Panasonic	ERJ-8GEYJ224V	Resistor, 220 kΩ, SMT 1206	REOL1, REOL2, REOL3, RPU
41	1	Panasonic	ERJ-8GEYJ203V	Resistor, 20 kΩ, 5%, SMT 1206	REOL4 (see Note 3)
42	1	Digi-key	36.0KFRCT-ND	Resistor, 36 kΩ, 1%, SMT 1206	RFMIN
43	1	Panasonic	ERJ-8GEYJ563V	Resistor, 56 kΩ, 1%, SMT 1206	RPH
44	1	WAGO	235-203	Connector, 3 terminal	X1
45	1	WAGO	235-207	Connector, 4 terminal	X2

Table 1: Bill of Material
Lamp type: 54 W TL5; Line Input Voltage: 80-305 VAC

Note 1: Different lamp types require different frequency programming components.
Note 2: CEOL and CSD values can be increased up to 470 nF to increase noise immunity.
Note 3: REOL4 value can be increased to 33 kΩ for a more sensitive lamp end-of-life detection

International IOR Rectifier

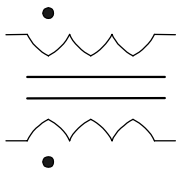
INDUCTOR SPECIFICATION

PART NO.: IL 060 320 41 02 REF DES:LPFC

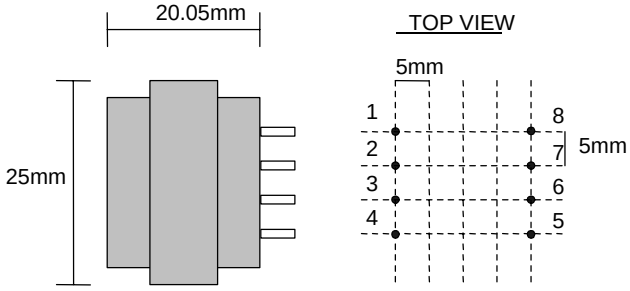
CORE SIZE	EVD25	GAP LENGTH	3.5	mm
BOBBIN	HORIZONTAL	PINS	8	
CORE MATERIAL	Fi 324 or equivalent			
NOMINAL INDUCTANCE	2	mH		
MAXIMUM CURRENT	2.5	Apk		
MAXIMUM CORE TEMPERATURE	115	ºC		

WINDING	START PIN	FINISH PIN	TURNS	WIRE DIAMETER (mm)
MAIN	1	7	TBD	4 strands of AWG 32
ZX	3	5	26	AWG 32

ELECTRICAL LAYOUT



PHYSICAL LAYOUT



TEST (TEST FREQUENCY = 50kHz)

MAIN WINDING INDUCTANCE INDUCTANCE TOLERANCES: +/- 5%

MAIN WINDING INDUCTANCE INDUCTANCE RESISTANCE MAX 3.2 OHM

NOTE : Inductor must not saturate at maximum current and maximum core temperature at given test frequency

Fig. 5: Power Factor Inductor Specification

International
IOR Rectifier

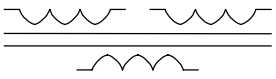
INDUCTOR SPECIFICATION

PART NO.: IL 060 320 51 01 REF DES: LRES

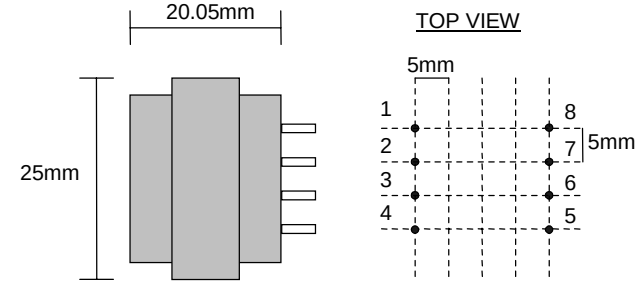
CORE SIZE	EVD25	GAP LENGTH	2.82	mm
BOBBIN	HORIZONTAL	PINS	8	
CORE MATERIAL	Fi 324 or equivalent			
NOMINAL INDUCTANCE	2	mH		
MAXIMUM CURRENT	2	Apk		
MAXIMUM CORE TEMPERATURE	115	ºC		

WINDING	START PIN	FINISH PIN	TURNS	WIRE DIAMETER (mm)
MAIN	1	8	185	4 strands of AWG 32
CATHODE (1)	6	7	8	4 strands of AWG 32
CATHODE (2)	4	5	8	4 strands of AWG 32

ELECTRICAL



PHYSICAL LAYOUT



TEST (TEST FREQUENCY = 50kHz)

MAIN WINDING	MIN 1.9	mH	MAX 2.1	mH
MAIN WINDING	MAX 1.8	Ohms		

NOTE : Inductor must not saturate at maximum current and maximum core temperature at given test frequency.

Fig. 6: Resonant Inductor Specification

8. Functional Description

The IRPLLNR5 reference design consists of an EMI filter, an active power factor correction section, a ballast control section, and a resonant lamp output stage. The active power factor correction section is a boost converter operating in critical conduction, free-running frequency mode. The ballast control section provides frequency modulation control of a traditional RCL lamp resonant output circuit and is easily adaptable to a wide variety of lamp types. The ballast control section also provides the necessary circuitry to perform lamp fault detection, shutdown, and auto-restart.

Reference Design Overview

This demo-board is designed for a single 54 W TL5 lamp with voltage mode heating. TL5 lamps are popular due to their low profile and high lumen/watt output. These lamps, however, can be more difficult to control due to their higher ignition and running voltages. A typical ballast output stage using current-mode filament heating (filament placed inside L-C tank) will result in excessive filament current during running. The output stage has therefore been configured for voltage-mode filament heating using secondary windings off of the resonant inductor LRES. The lamp has been placed outside the under-damped resonant circuit loop, which consist of LRES and CRES. The filament heating during preheat can be adjusted with the capacitors CH1 and CH2. The result is a more flexible ballast output stage necessary for fulfilling the lamp requirements. The DC blocking capacitor, CDC, is also placed outside the under-damped resonant circuit loop such that it does not influence the natural resonance frequency of LRES and CRES. The snubber capacitor, CSNUB, serves as EMI reduction and a charge pump for supplying the IRS2168D.

The IRS2168D ballast control IC is used to program the ballast operating points and protect the ballast against conditions such as lamp strike failures, low DC bus or lamp failure during normal operations. It is also used to regulate the DC bus and for power factor correction to give high power factor and low harmonic distortion of the ballast AC input current.

Power Factor Correction Section

The power factor correction section contained in the IRS2168D controls a boost topology circuit operating in critical conduction mode. This topology is designed to step-up and regulate the output DC bus voltage while drawing sinusoidal current from the line (low THD) which is “in phase” with the AC input line voltage. The power factor correction section also includes over-current protection of the boost MOSFET to prevent damage that can occur during boost inductor saturation.

Ballast Control Section

The ballast control section of the IRS2168D ballast control IC contains an oscillator, a high-voltage half-bridge gate driver, and lamp fault protection circuitry. Please refer to the datasheet of this IC for the block diagram and the state diagram. The following is a breakdown of the different modes of operation for the ballast.

Startup Mode

When power is initially applied to the ballast, the voltage on the VCC pin of the IRS2168D begins to increase. The voltage for the IRS2168D is derived from the current supplied from the rectified AC line through the startup resistor RSUPPLY. During this initial startup when the VCC voltage of the IRS2168D is below the rising under-voltage lock-out threshold (UVLO+), the IC is in UVLO Mode and draws micro-power current at VCC. The micro-power current of the IRS2168D allows for the use of a

large value, low-wattage startup resistor (RSUPPLY). When the voltage on the IRS2168D reaches the rising under-voltage lockout threshold (12.5 V), the gate driver oscillator is enabled (this assumes that there are no fault conditions) and drives the half-bridge output MOSFETs (MHS and MLS). When the half-bridge is oscillating, capacitor CSNUB, diodes DCP1 and DCP2 form a snubber/charge pump circuit which limits the rise and fall time at the half-bridge output and also supplies the current to charge capacitor CVCC2 to the VCC clamp voltage (approx. 15.6 V). When the rising under-voltage lockout threshold of the IRS2168D is reached, the power factor control output also starts to oscillate and drives MOSFET MPFC to boost and regulate the bus voltage to 500 V DC.

Preheat Mode

When the ballast reaches the end of the UVLO mode, the Preheat Mode is entered. At this point, the ballast control oscillator of the IRS2168D has begun to operate and the half-bridge output is driving the resonant load (lamp) circuit.

There is an initial startup frequency that is higher than the preheat frequency that lasts for only a short duration. This is done to ensure that the initial voltage appearing across the lamp at the startup of oscillation does not exceed the minimum lamp ignition voltage. If, at the initiation of oscillation of the half-bridge, the voltage across the lamp is large enough, a visible undesired flash of the lamp can occur. This in effect is a cold strike of the lamp and can shorten the life of the lamp.

The ballast control section oscillator of the IRS2168D consists of an internal timing capacitor and an external timing resistor (RFMIN). Resistors RFMIN and RPH program a current that determines the ramp up time of the internal timing capacitor. The preheat frequency is determined by the equivalent resistance formed by the parallel combination of RFMIN and RPH. The preheat frequency is selected such that the voltage appearing across the lamp is below the minimum lamp ignition voltage while supplying enough current to preheat the lamp filaments to their correct emission temperature within the Preheat Mode time period. The preheating of the lamp filaments is performed using voltage mode heating that consists of a constant voltage across the lamp filaments. The waveform in Figure 7 shows the CPH voltage and lamp voltage during normal Preheat, Ignition, and Run Modes. Figure 8 shows the half-bridge voltage (VS pin) during Preheat Mode.

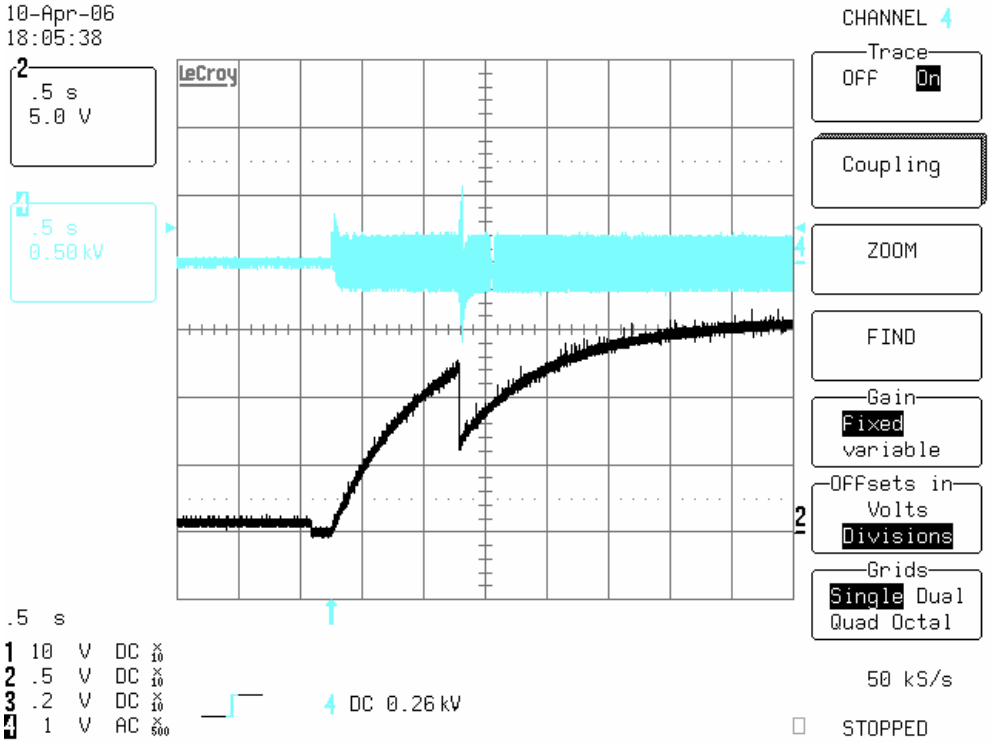


Fig. 7: CPH Pin Voltage (Black) and Lamp Voltage (Blue) During Normal Preheat, Ignition and Run Modes

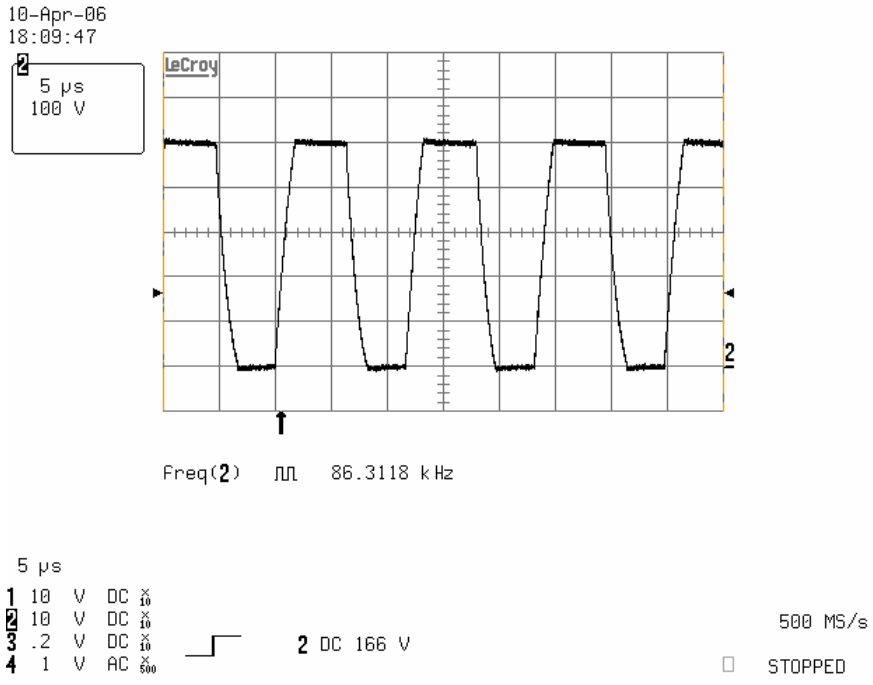


Fig. 8: Half-Bridge Mid-Point Voltage (VS Pin) During Preheat Mode

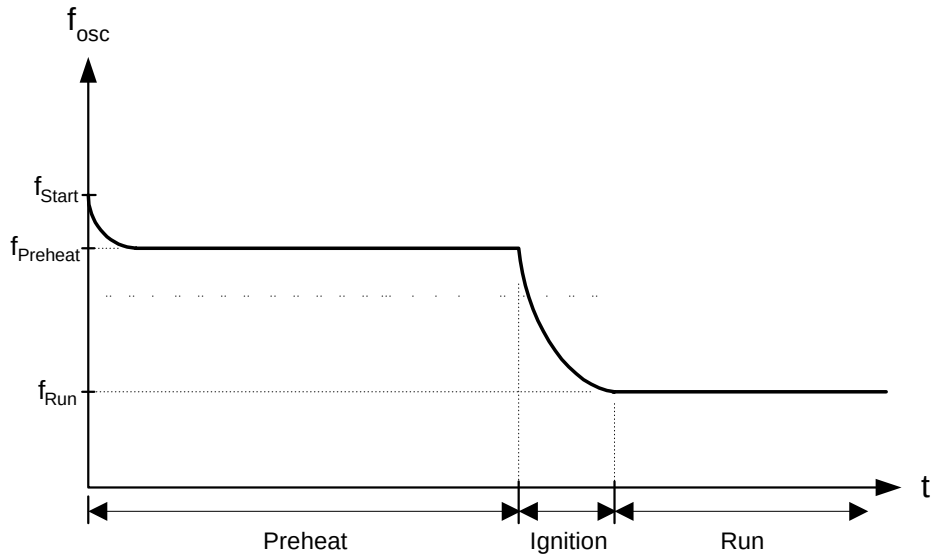


Fig. 9: Oscillator Frequency versus Time During Normal Operating Conditions

Figure 9 shows a plot of the half-bridge oscillation frequency as a function of time for normal Preheat, Ignition and Run ballast operating modes. The duration of the Preheat Mode, as well as all ballast operating modes, are determined by the voltage on the CPH pin of the IRS2168D. At the end of UVLO Mode, Preheat Mode is entered and the external capacitor at the CPH pin of the IRS2168D begins to charge through the external resistor (RCPH) from CPH to VCC. The ballast remains in Preheat Mode until the voltage on the CPH pin exceeds the End-of-Preheat Mode threshold of 0.67(V_{CC}), at which time the ballast then enters Ignition Mode.

Ignition Mode

When the IC enters Ignition Mode, CPH is discharged quickly to 0.33(V_{CC}) and RPH is disconnected from COM via an internal MOSFET at the RPH pin. CPH begins to charge up again from 0.33(V_{CC}) and the frequency begins to ramp down to the run frequency at a rate determined by the time constant RPH(CVCO). During this ramping downward of the frequency, the voltage across the lamp increases in magnitude as the frequency approaches the resonant frequency of the LC load circuit until the lamp ignition voltage is exceeded and the lamp ignites. The maximum ignition voltage that can be generated is determined from the value of RCS, and the ignition frequency must be higher than the run frequency so that the frequency sweeps through the resonance frequency to ensure lamp ignition. If the lamp does not ignite, then the ignition regulation feature of the IRS2168D will regulate the ballast output voltage to a constant level (programmed by RCS) for the duration of Ignition Mode. Figure 10 shows the lamp voltage during ignition ramp and ignition regulation during a lamp non-strike condition.

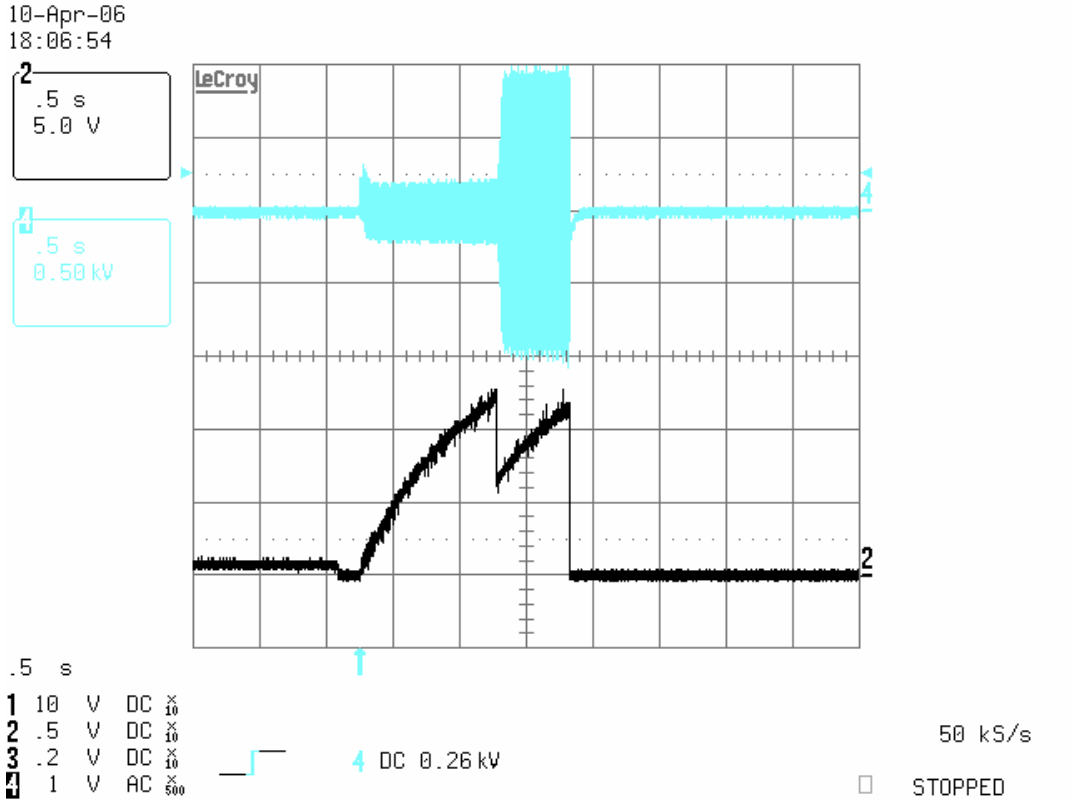


Fig. 10: CPH Pin Voltage (Black) and Lamp Voltage (Blue) During Lamp Non-Strike Fault Condition

During Ignition Mode, the voltage on the CPH pin of the IRS2168D continues to ramp up until the voltage at the CPH pin exceeds 0.67(V_{CC}) a second time and the IC enters Run Mode. The over-current fault counter is disabled during Ignition Mode due to the ignition regulation feature and enabled again at the start of Run Mode. During a lamp non-strike condition, the ignition voltage will be regulated for the duration of Ignition Mode and then unregulated during Run Mode. This means that the ignition voltage will increase slightly after Ignition Mode (as the frequency decreases towards the run frequency) until the fault counter times out, after 65 cycles above the over-current threshold, and the ballast shuts off. The amount of frequency shift and resulting voltage increase is determined by the value of CVCO. The 5 V shutdown threshold at the SD pin is also disabled during Ignition Mode and enabled again at the start of Run Mode. A full explanation of the functionality of the over-current sensing and shutdown functions are in the Fault Mode section.

Run Mode

During Run Mode and after a successful lamp ignition, the frequency is at the final run frequency and is determined by RFMIN. The 1 V and 3 V end-of-life (EOL) window comparator at the SD/EOL pin, the 5 V unlatched shutdown threshold at the SD/EOL pin, and the fault counter at the CS pin, are all enabled in Run Mode. A functional description of the over-current sensing and end-of-life sensing is given in the Fault Mode section.

The Run Mode frequency (Figure 11) is that at which the lamp is driven to the lamp manufacturer's recommended lamp power rating. The running frequency of the lamp resonant output stage for selected component values is defined as,

$$f_{run} = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - 2\left(\frac{P_{Lamp}}{CV^2_{Lamp}}\right)^2 + \sqrt{\left[\frac{1}{LC} - 2\left(\frac{P_{Lamp}}{CV^2_{Lamp}}\right)^2\right]^2 - 4\frac{1-\left(\frac{2V_{DCbus}}{V_{Lamp}\pi}\right)^2}{L^2C^2}}}$$

where,

L	=	Lamp resonant circuit inductor (LRES)	(H)
C	=	Lamp resonant circuit capacitor (CRES)	(F)
P_{Lamp}	=	Lamp running power	(W)
V_{Lamp}	=	Lamp running voltage amplitude	(V)

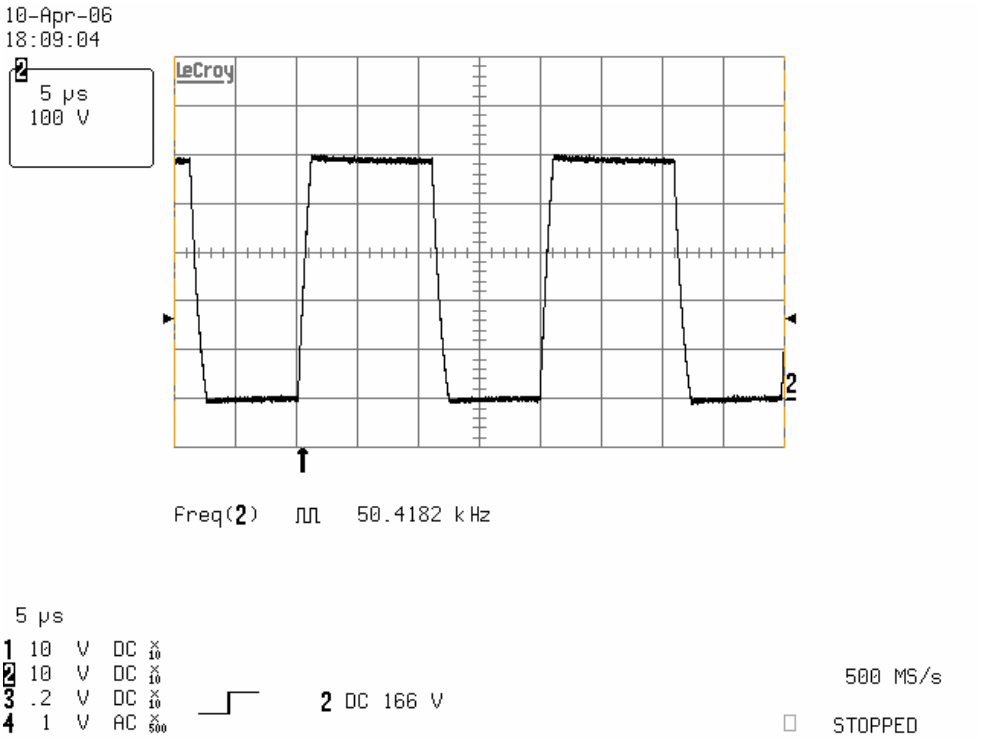


Fig. 11: Half-Bridge Mid-Point Voltage (VS Pin) During Run Mode

Normal Power Down

A normal power down occurs when the AC line voltage is disconnected from the ballast. When this occurs, the voltage on the VBUS pin of the IRS2168D drops below the VBUS pin under-voltage reset threshold of 3 V. This will cause VCC to be discharged internally to UVLO- (10.5 V). The IC enters

UVLO Mode and the PFC and ballast oscillators are disabled, the PFC and half-bridge driver outputs (PFC, LO, and HO) are turned off, and the IRS2168D consumes micro-power current at VCC.

Lamp Removal and Auto-Restart

Resistors RPU, RSD and capacitor CSD1 form a divider/filter network used to detect an open lower lamp filament and/or lamp replacement. Under normal conditions, the voltage across CSD1 is close to zero. If the lower filament becomes open or the lamp is removed, however, the voltage at the SD pin increases above the 5 V threshold and causes the IC to shutdown (Figure 12). The ballast remains shutdown until a lamp replacement is performed. If the lamp is replaced with a lamp with a good lower filament, the voltage on the SD pin of the IRS2168D drops back below the 3 V threshold and the ballast will restart in Preheat Mode. The ballast will go through the Preheat, Ignition, and Run Mode sequences each time a restart is performed. Note that the SD pin of the IRS2168D is active during Preheat and Run Modes and is disabled during Ignition Mode.

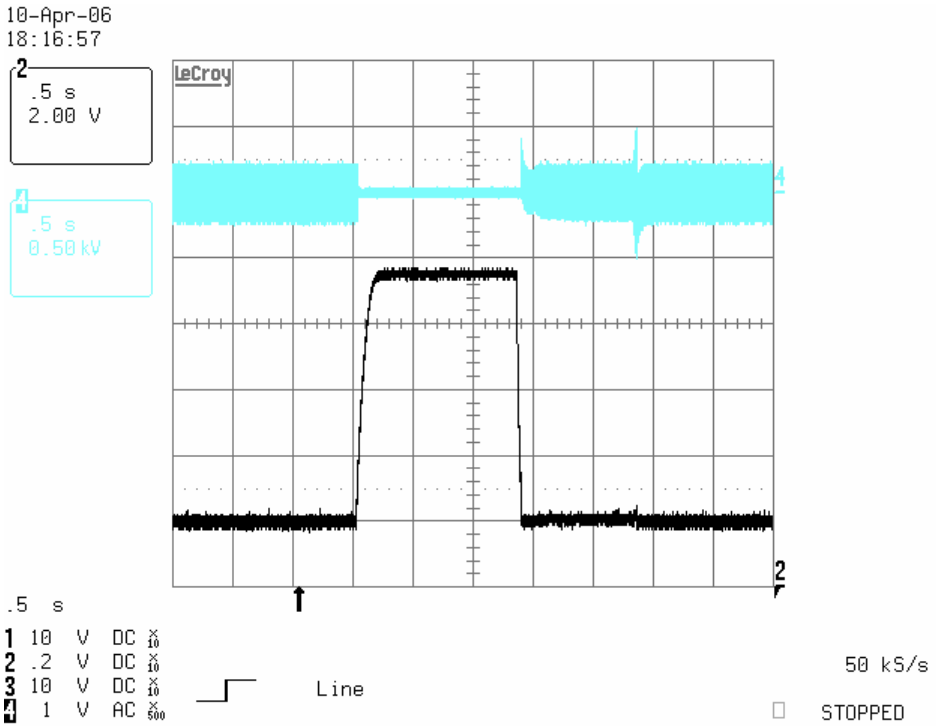


Fig. 12: SD Pin Voltage (Black) and Lamp Voltage (Blue) during Lamp Removal/Auto-Restart Condition

Fault Mode

When a fault is detected at the CS pin or SD/EOL pin, the IC will enter Fault Mode. During Fault Mode, the ballast section and PFC section are both shutdown. The DC bus voltage will drop to the non-boosted peak AC line voltage level. There are several lamp fault conditions that can cause the IC to enter into Fault Mode. These include: hard-switching at the half-bridge mid-point (open load), over-current (non-strike), lamp voltage shift (end-of-life), and lamp removal (SD/EOL pin). Resistor RCS in the source lead of the low-side MOSFET (MLS) serves as the current-sensing point for the half-bridge, and is used to detect hard-switching or over-current. During normal operation when the half-bridge is oscillating, a voltage appears across RCS when the low-side MOSFET, MLS, is turned on. The magnitude of this voltage directly relates to the current in the lamp resonant circuit.

If at any time during Preheat Mode or Run Mode the voltage across resistor RCS rises above the over-current threshold (1.25 V) for 65 events, the PFC and half-bridge MOSFETs, (MPFC, MHS and MLS) are turned off and the ballast goes into Fault Mode. During the Ignition Mode, the over-current is disabled and the ignition regulation feature limits the maximum current flowing in the resonant tank and half-bridge. An over-current condition can occur if the lamp fails to ignite or the lamp is broken (an open circuit cathode or broken lamp). If a cathode is broken (open circuit), the half-bridge output hard-switches. Each time the low-side MOSFET (MLS) is turned on, a large current pulse occurs and thus a large voltage pulse occurs across resistor RCS signaling a fault. The ballast will remain in Fault Mode until the AC line voltage is reset or a lamp replacement is performed.

During an end-of-life lamp fault condition, the lamp voltage can increase or decrease asymmetrically. The resulting excessive voltage across the lamp filaments can cause the lamp ends to reach temperatures high enough to melt the tube glass. The lamp can then fall out of the fixture and cause harm or damage. To protect against this condition, resistors REOL1, REOL2, REOL3, REOL4, and zener diodes DEOL1 and DEOL2, are used for end-of-life protection. The end-of-life window comparator at the SD/EOL pin is enabled in Run Mode. If the voltage on SD/EOL pin falls outside the range of the internal 1 V – 3 V window comparator, the IC will enter Fault Mode. The SD/EOL pin is internally biased at 2 V with an internal +/-10 μA OTA. The value of REOL4, DEOL1 and DEOL2 are selected such that the SD/EOL pin remains at 2 V during normal operation, but increases above 3 V or decreases below 1 V during an end-of-life fault condition. The lamp voltage end-of-life threshold can be adjusted by changing the value of resistor REOL4 and/or zener diodes DEOL1 and DEOL2. A threshold of 30% higher than the nominal running lamp voltage is typical.

PFC Control Section

The IRS2168D contains control circuitry for driving a boost-type power factor correction (PFC) circuit. This is necessary for producing sinusoidal input current at the mains input that is “in phase” with the mains voltage and contains minimal total harmonic distortion (THD). It is also convenient to use the boost converter to regulate the DC bus voltage to a constant DC level. The PFC control is achieved using five control pins. The DC bus voltage is sensed with a resistor divider at the VBUS pin. The loop compensation speed is programmed with an external capacitor at the COMP pin. The cycle-by-cycle zero-crossing of the boost inductor current is detected at the ZX pin. The gate drive for the boost MOSFET is provided by the PFC pin. The cycle-by-cycle over-current protection is performed by the OC pin. The following waveforms show the operation of the PFC at 120 VAC (Figure 13) and 290 V AC (Figure 14) input line conditions.

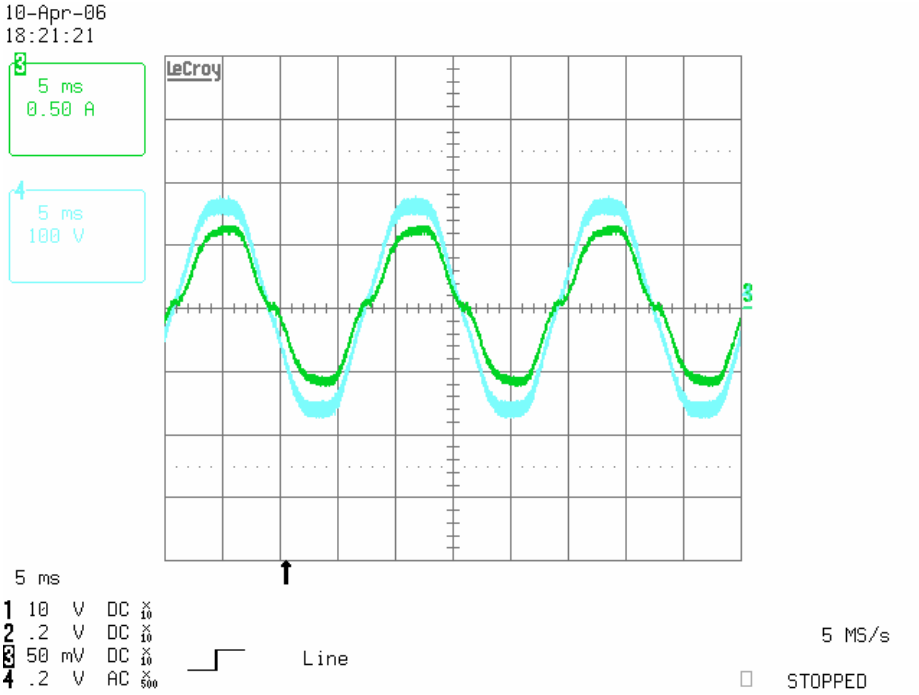


Fig. 13: AC Input Current (Green) and AC Input Voltage (Blue) at 120 VAC

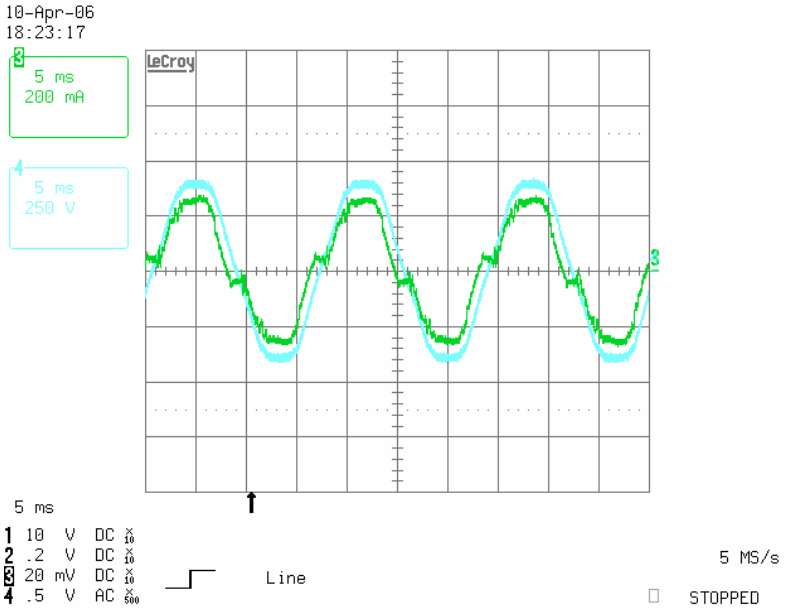


Fig. 14: AC Input Current (Green) and AC Input Voltage (Blue) at 290 VAC

PFC Over-Current Protection

The PFC section includes cycle-by-cycle over-current protection. The OC pin senses the current in the PFC MOSFET via an external sense resistor (ROC). Should the voltage across this resistor exceed the internal threshold (1.25 V typical), the PFC MOSFET will turn off to limit the instantaneous current

and will turn on again at the next zero-crossing of the inductor current as detected by the ZX pin. This over-current condition can occur, for example, during a low-line condition (Figure 15). As the AC line decreases, the PFC inductor and MOSFET current will increase to keep the DC bus constant for a given power level. When the peak current reaches the over-current threshold, the cycle-by-cycle current limit will cause the peak of the MOSFET current to flatten and the DC bus to start to drop. This current limit is necessary to prevent saturation of the PFC inductor current and to protect the PFC MOSFET from being damaged.

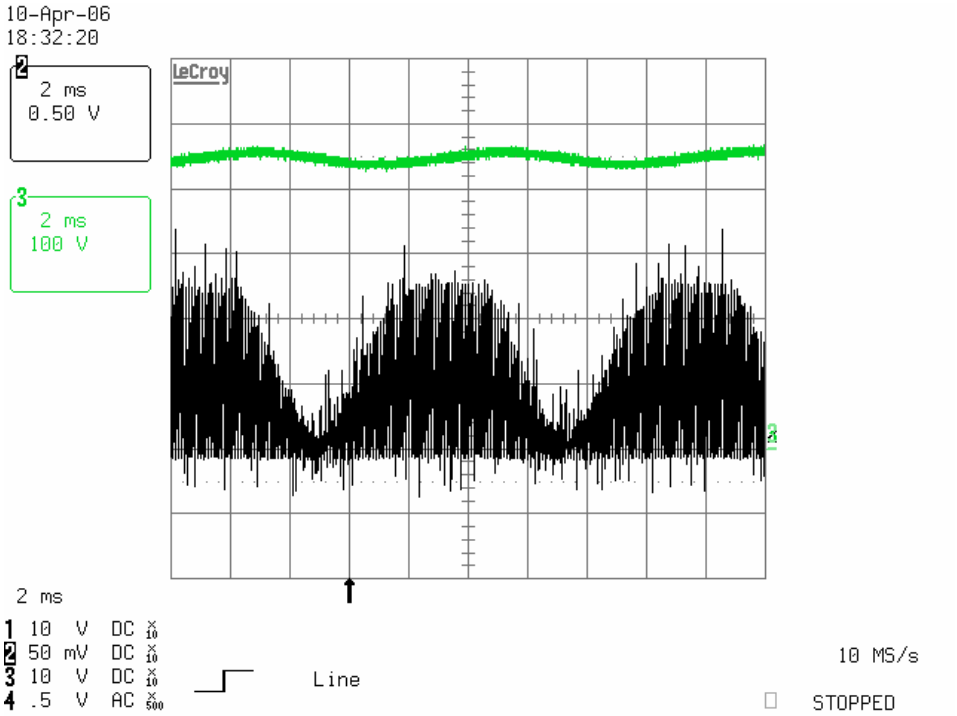


Fig. 15: OC Pin Voltage (Black) and DC Bus Voltage (Green) During Low-Line Condition

Brown-Out Protection

The IRS2168D includes an under-voltage reset (UVR) function at the VBUS pin. Should the DC bus decrease too far during a momentary interrupt of the mains input voltage, the ballast should be properly shutdown and restarted. This will prevent the lamp from extinguishing and will properly preheat and restart the lamp when the mains voltage returns. If the VBUS pin voltage decreases below 3 V, the PFC and half-bridge gate drivers will be turned off and VCC will be discharged to UVLO-. The ballast will then be restarted via the RSUPPLY resistor when the mains voltage reaches a high enough level again (Figure 16).

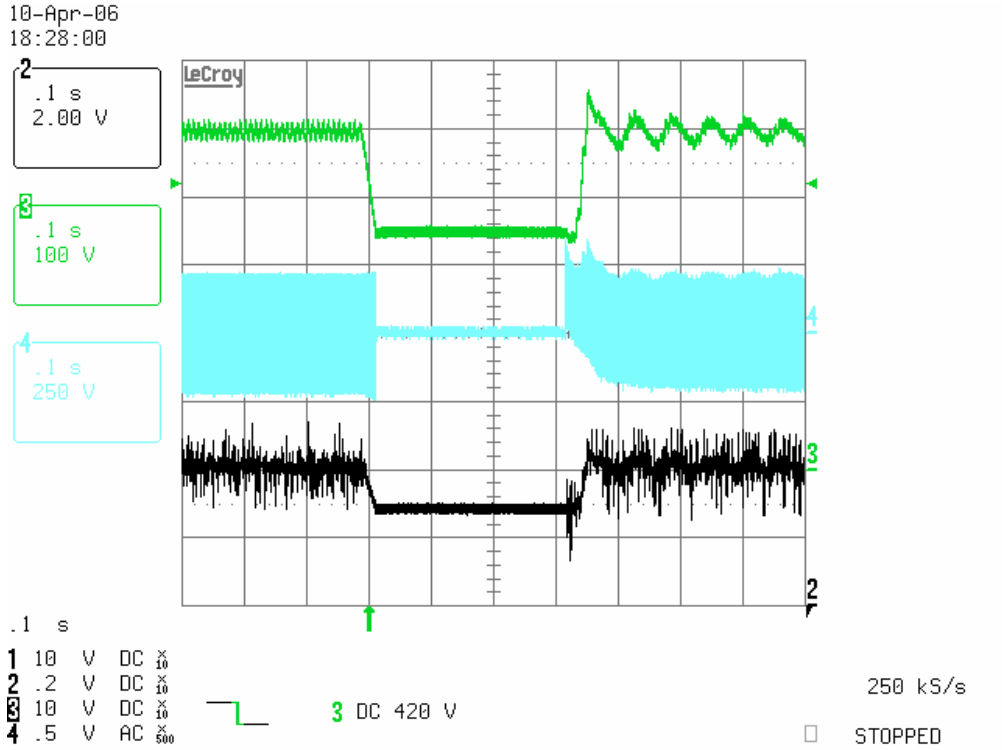


Fig. 16: VBUS Pin (Black), Lamp Voltage (Blue) and DC Bus Voltage (Green) During Momentary Interruption of the Mains

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