TEXAS INSTRUMENTS

DRV8800, DRV8801
SLVS855K – JULY 2008 – REVISED MARCH 2021

DRV880x DMOS Full-Bridge Motor Drivers

1 Features

- H-Bridge Motor Driver
- Low $R_{DS(on)}$ MOSFETs (0.4-Ω Typical)
- Low-Power Sleep Mode
- 100% PWM Duty Cycle Supported
- 8-V to 36-V Operating Supply Voltage Range
- Thermally Enhanced Surface-Mount Package
- Protection Features:
  - VBB Undervoltage Lockout (UVLO)
  - Charge Pump Undervoltage (CPUV)
  - Overcurrent Protection (OCP)
  - Short-to-Supply Protection
  - Short-to-Ground Protection
  - Overtemperature Warning (OTW)
  - Overtemperature Shutdown (OTS)
  - Fault Condition Indication Pin (nFAULT)

2 Applications

- Printers
- Industrial Automation
- Robotics

3 Description

The DRV880x provides a versatile motor driver solution with a variety of capabilities. The device contains a full H-bridge which can be used to drive a brushed DC motor, one winding of a stepper motor, or other devices such as solenoids. A simple PHASE-ENABLE interface allows easy interfacing to controller circuits.

The output stages use N-channel power MOSFETs configured as an H-bridge. The DRV880x is capable of peak output currents up to ±2.8 A and operating voltages up to 36 V. An internal charge pump generates the needed gate drive voltages.

A low-power sleep mode is provided which shuts down internal circuitry to achieve a very low quiescent current draw. This sleep mode can be set using a dedicated nSLEEP pin.

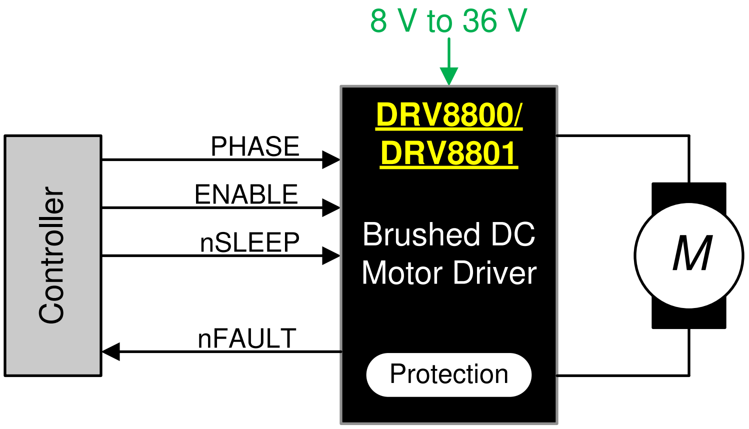
Internal protection functions are provided for undervoltage, charge pump fault, overcurrent, short-to-supply, short-to-ground, and overtemperature. Fault conditions are indicated through the nFAULT pin.

The DRV880x is packaged in a 16-pin WQFN package with PowerPAD™ (Eco-friendly: RoHS & no Sb/Br).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8800	HTSSOP (16)	5.00 mm × 4.40 mm
	WQFN (16)	4.00 mm × 4.00 mm
DRV8801	HTSSOP (16)	5.00 mm × 4.40 mm
	WQFN (16)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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• Added missing GND pin reference to *Pin Functions* Table	3
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• Improved description for pins nFAULT, nSLEEP, VBB and VCP in *Pin Functions* Table	3
• Added entries for VCP and CP2 pins in *Absolute Maximum Ratings* table	5
• Added VDD pin voltage limits and device's PWM frequency limits to *Recommended Operation Conditions* table	5
• Changed SLEEP to nSLEEP in PWM Control Timing Figure	8
• Added equation for VPROPI to help when connecting pin's output to ADC in *Feature Description*	12
• Provide additional information on SENSE pin behavior	13
• Added device specific details to *Control Logic* Table	13
• Added die temperature estimation equation utilizing junction to ambient thermal impedance in Application and Implementation section	18
• Added information on using motor driver's pulse width modulating modes in Application and Implementation section	18

Changes from Revision I (January 2014) to Revision J (July 2014)	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	5

Changes from Revision H (November 2013) to Revision I (January 2014)	Page
• Added I_{OCP} to ELECTRICAL CHARACTERISTICS	6
• Changed *Parameter Measurement Information*	8

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• Changed maximum junction temperature from 190°C to 150°C	5
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• Changed Protection Circuitry section	6
• Changed Note in SENSE section	13

5 Pin Configuration and Functions

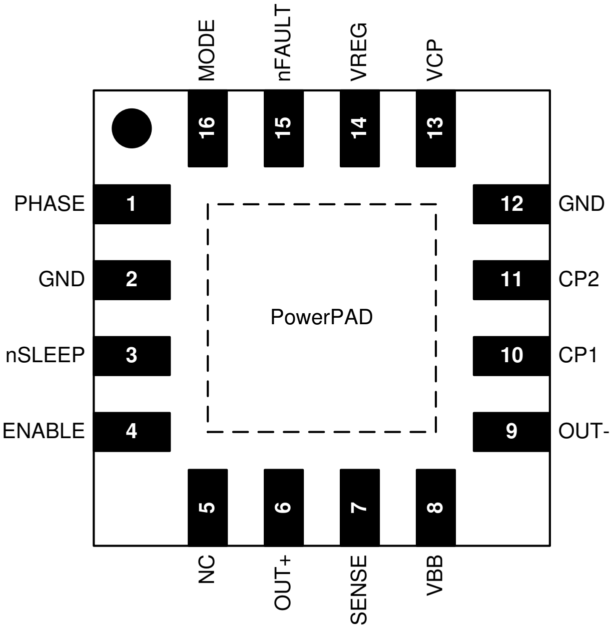


Figure 5-1. DRV8800 RTY Package 16-Pin WQFN Top View

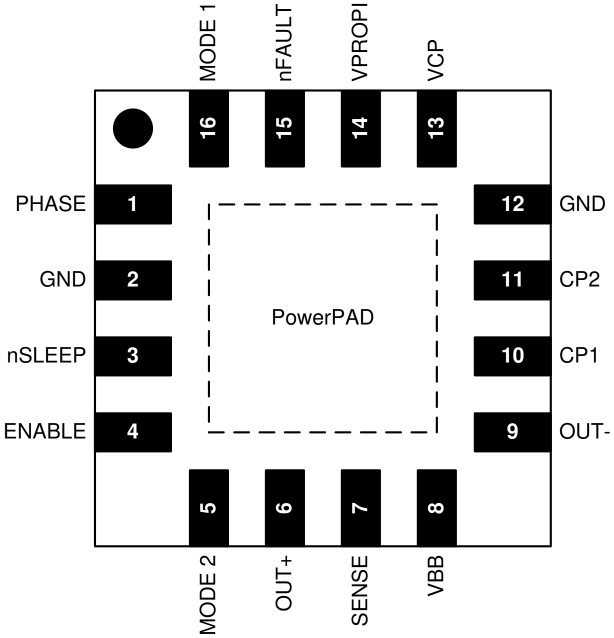


Figure 5-2. DRV8801 RTY Package 16-Pin WQFN Top View

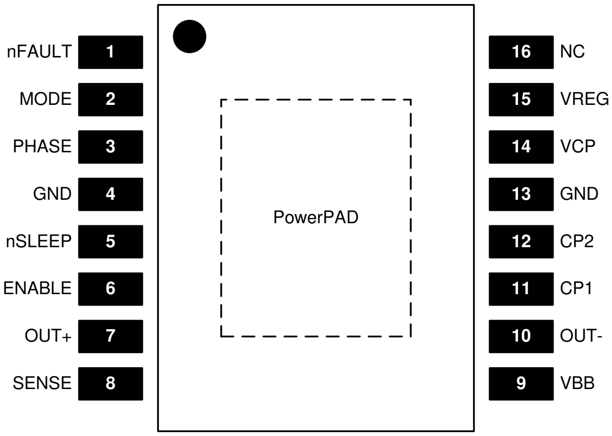


Figure 5-3. DRV8800 PWP Package 16-Pin HTSSOP Top View

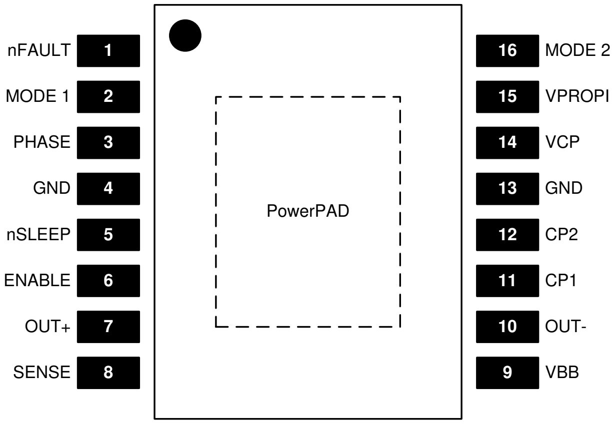


Figure 5-4. DRV8801 PWP Package 16-Pin HTSSOP Top View

Table 5-1. Pin Functions

PIN					I/O	DESCRIPTION
NAME	DRV8800		DRV8801			
	WQFN	HTSSOP	WQFN	HTSSOP		
CP1	10	11	10	11	P	Charge pump switching node. Connect a 0.1-µF X7R ceramic capacitor rated for VBB between CP1 and CP2.
CP2	11	12	11	12	P	Charge pump switching node. Connect a 0.1-µF X7R ceramic capacitor rated for VBB between CP1 and CP2.

Table 5-1. Pin Functions (continued)

PIN					I/O	DESCRIPTION
NAME	DRV8800		DRV8801			
	WQFN	HTSSOP	WQFN	HTSSOP		
ENABLE	4	6	4	6	I	Enable logic input. Set high to enable the H-bridge.
GND	2,12	4, 13	2, 12	4, 13	P	Device ground
MODE	16	2	—	—	I	Mode logic input
MODE 1	—	—	16	2	I	Mode logic input
MODE 2	—	—	5	16	I	Mode 2 logic input
NC	5	16	—	—	NC	No connect
nFAULT	15	1	15	1	OD	Fault indication. Pulled logic low with fault condition; open-drain output requires an external pullup resistor.
nSLEEP	3	5	3	5	I	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown resistor.
OUT+	6	7	6	7	O	DMOS H-bridge output. Connect to motor terminal.
OUT-	9	10	9	10	O	DMOS H-bridge output. Connect to motor terminal.
PHASE	1	3	1	3	I	WQFN Package: Phase logic input for direction control. HTSSOP Package: Phase logic input. Controls the direction of the H-bridge.
SENSE	7	8	7	8	O (DRV8800) IO (DRV8801)	Sense Power Return
VBB	8	9	8	9	P	Driver supply voltage. Bypass to GND with 0.1-μF ceramic capacitors plus a bulk capacitor rated for VBB.
VCP	13	14	13	14	P	Charge pump reservoir capacitor pin. Connect a X7R, 0.1-μF, 16-V ceramic capacitor to VBB.
VREG	14	15	—	—	P	Regulated voltage.
VPROPI	—	—	14	15	O	Voltage output proportional to winding current.
PowerPAD	—	—	—	—	—	Exposed pad for thermal dissipation. Connect to ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VBB	Load supply voltage(2)	–0.3	40	V
VCP and CP2	Charge Pump Voltage	–0.3	VBB+17V	V
	Output current	–2.8	2.8	A
V_{Sense}	Sense voltage	–500	500	mV
	VBB to OUTx		36	V
	OUTx to SENSE		36	V
VDD	PHASE, ENABLE, MODE, MODE1, MODE2, nSLEEP and nFAULT(2)	–0.3	7	V
	Continuous total power dissipation	See *Section 6.4*		
T_A	Operating free-air temperature	–40	85	°C
T_J	Maximum junction temperature		150	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage, VBB	8	32	38	V
VDD	Logic Supply Voltage	0		5.5	V
f(PWM)	Applied PMW signal (PHASE and ENABLE)	0		100	kHz
T_A	Operating free-air temperature	–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		DRV880x		UNIT
		RTY (WQFN)	PWP (HTSSOP)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.1	43.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.7	30.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	16.1	25.3	
ψ_{JT}	Junction-to-top characterization parameter	0.3	1.1	
ψ_{JB}	Junction-to-board characterization parameter	16.2	25	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.1	5.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IBB	Motor supply current	f_{PWM} < 50 kHz		6		mA
		Charge pump on, Outputs disabled		3.2		
		Sleep mode			10	µA
V_{IH}	PHASE, ENABLE, MODE input voltage		2			V
V_{IL}					0.8	
V_{IH}	nSLEEP input voltage		2.7			V
V_{IL}					0.8	
I_{IH}	PHASE, MODE input current	V_{IN} = 2 V		<1.0	20	µA
I_{IL}		V_{IN} = 0.8 V	–20	≤–2.0	20	
I_{IH}	ENABLE input current	V_{IN} = 2 V		40	100	µA
I_{IL}		V_{IN} = 0.8 V		16	40	
I_{IH}	nSLEEP input current	V_{IN} = 2.7 V		27	50	µA
I_{IL}		V_{IN} = 0.8 V		<1	10	
V_{OL}	nFAULT output voltage	I_{sink} = 1 mA			0.4	V
VBBNFR	VBB nFAULT release	8 V < VBB < 40 V		12	13.8	V
V_{IHys}	Input hysteresis, except nSLEEP		100	500	800	mV
$r_{DS(on)}$	Output ON-resistance	Source driver, I_{OUT} = –2.8 A, T_J = 25°C		0.48		Ω
		Source driver, I_{OUT} = –2.8 A, T_J = 125°C		0.74	0.85	
		Sink driver, I_{OUT} = 2.8 A, T_J = 25°C		0.35		
		Sink driver, I_{OUT} = 2.8 A, T_J = 125°C		0.52	0.7	
VTRP	RSENSE voltage trip	SENSE connected to ground through a 0.2-Ω resistor		500		mV
V_f	Body diode forward voltage	Source diode, I_f = –2.8 A			1.4	V
		Sink diode, I_f = 2.8 A			1.4	
t_{pd}	Propagation delay time	PWM, Change to source or sink ON		600		ns
		PWM, Change to source or sink OFF		100		
t_{COD}	Crossover delay			500		ns
DAGain	Differential AMP gain	Sense = 0.1 V to 0.4 V		5		V/V
PROTECTION CIRCUITRY						
VUV	UVLO threshold	VBB increasing		6.5	7.5	V
I_{OCP}	Overcurrent threshold		3			A
t_{DEG}	Overcurrent deglitch time			3		µs
t_{OCP}	Overcurrent retry time			1.2		ms
TJW	Thermal warning temperature	Temperature increasing(1)		160		°C
TJTSD	Thermal shutdown temperature	Temperature increasing(2)		175		°C

(1) After the device reaches the thermal warning temperature of 160°C, the device will remain in thermal warning until the device cools to 145°C. This is known as the device's thermal warning hysteresis.

(2) After the device reaches the thermal shutdown temperature of 175°C, the device will remain in thermal shutdown until the device cools to 160°C. This is known as the device's thermal shutdown hysteresis.

6.6 Typical Characteristics

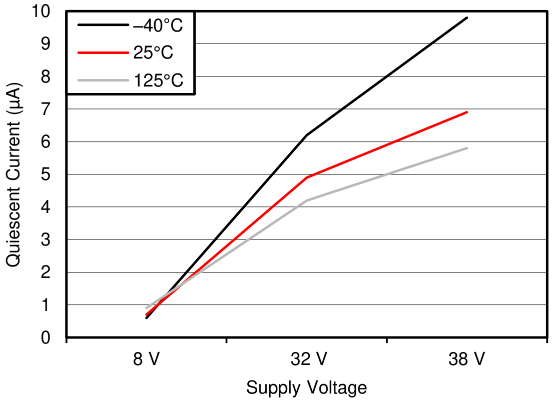


Figure 6-1. I_{VBBQ} vs VBB

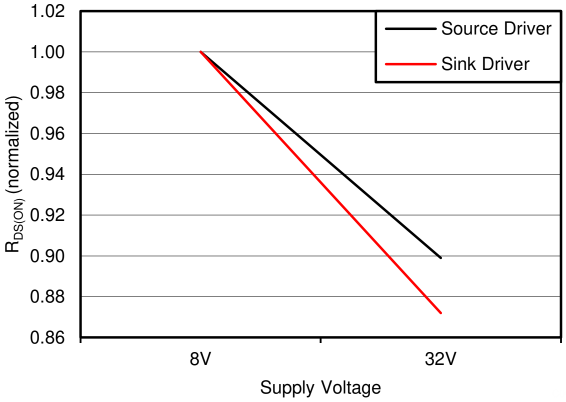


Figure 6-2. $R_{DS(ON)}$ vs VBB (Normalized to VBB = 8 V)

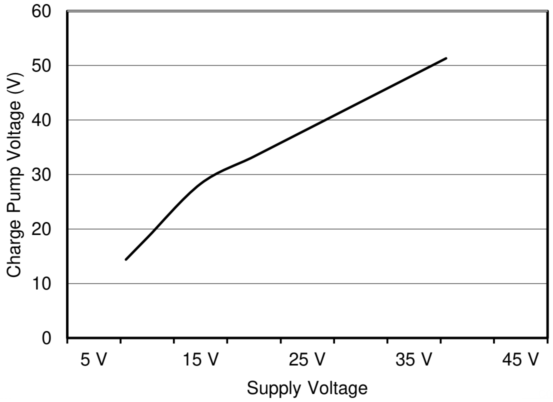
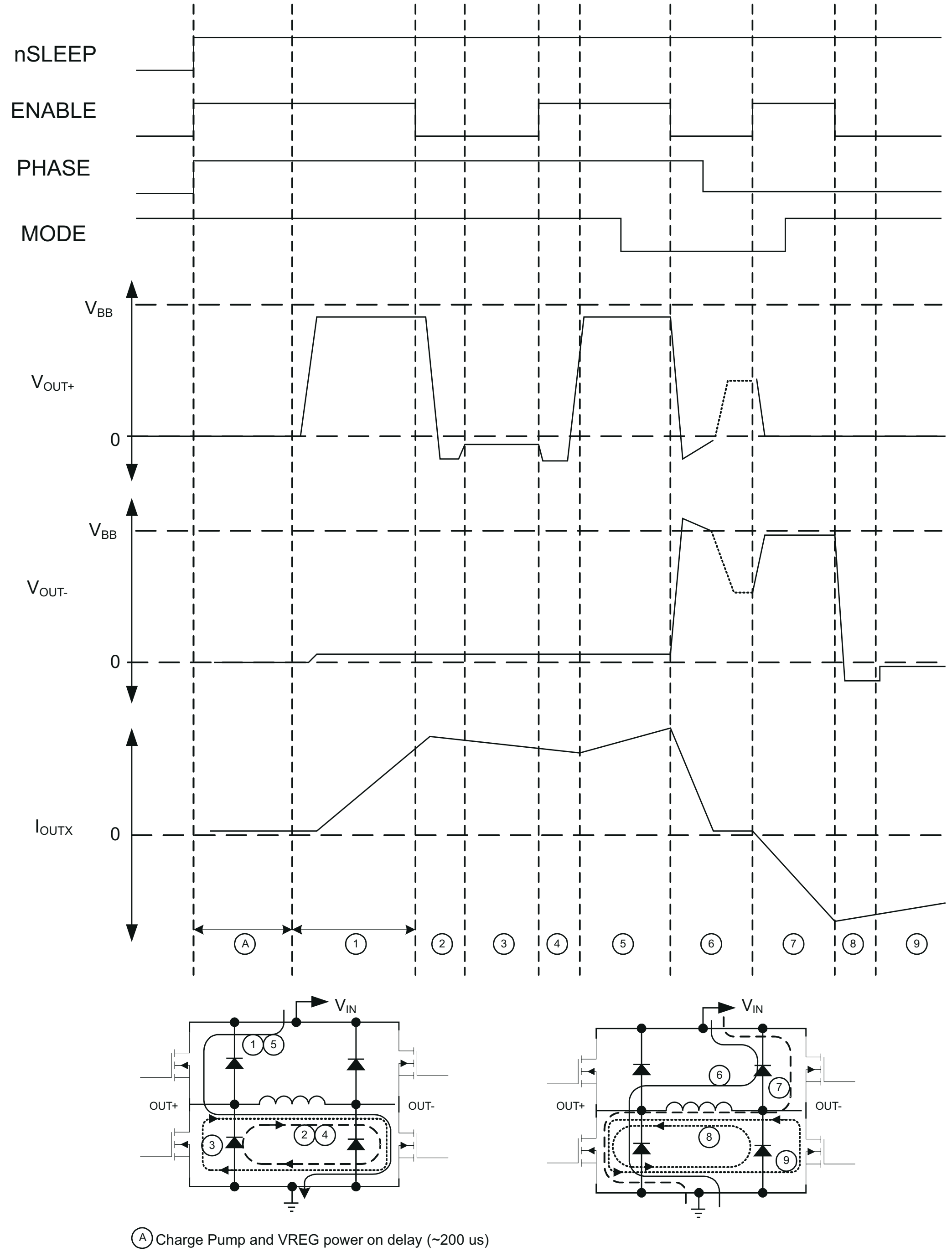


Figure 6-3. VCP vs VBB

7 Parameter Measurement Information



Ⓐ Charge Pump and VREG power on delay (~200 us)

Figure 7-1. PWM Control Timing

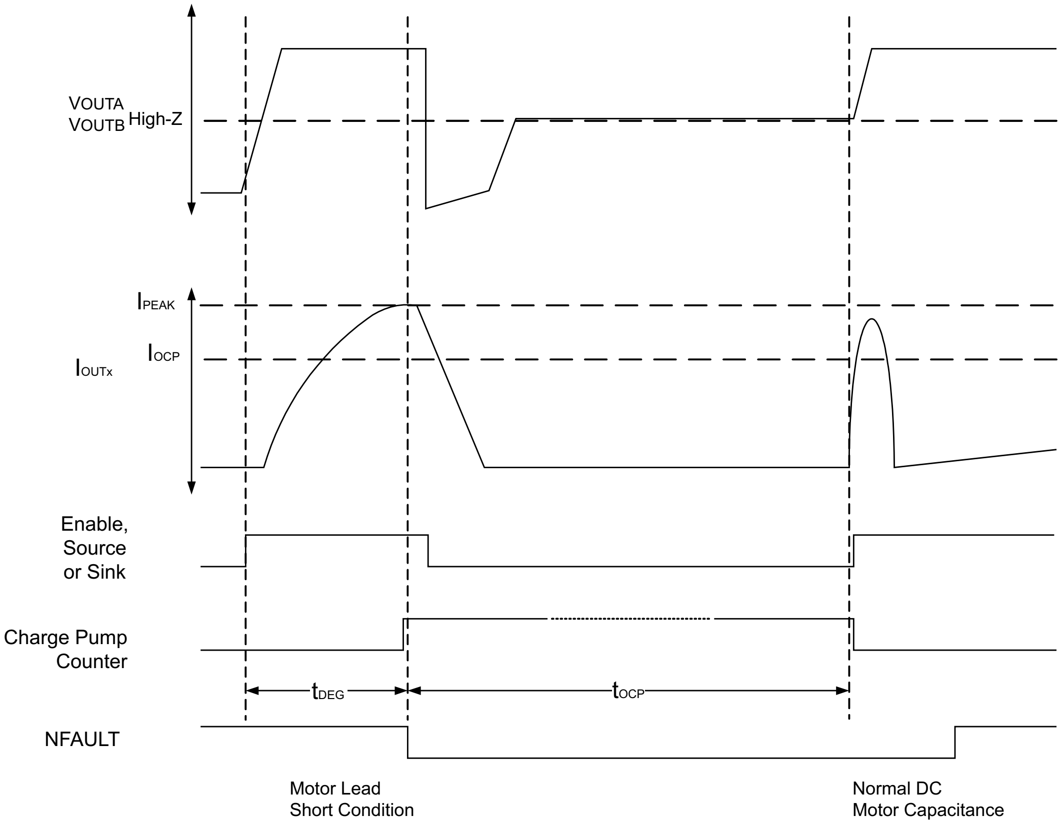


Figure 7-2. Overcurrent Control Timing

8 Detailed Description

8.1 Overview

The DRV880x devices are integrated motor driver solutions for brushed DC motors. The devices integrate a DMOS H-bridge, protection circuitry, and simple digital interface. The devices can be powered with a supply voltage between 8 and 36 V and are capable of providing an output current up to 2.8 A.

A PHASE-ENABLE interface allows for easy interfacing to the controller circuit. The PHASE input controls the direction of the H-bridge and the ENABLE input specifies whether the H-bridge is enabled or not.

Two MODE pins allow for specifying which current decay method the device utilizes. MODE1 specifies between fast decay or slow decay and MODE2 specifies between high side or low side slow decay.

The DRV8801 provides the option to monitor the motor winding current through a proportional voltage output.

8.2 Functional Block Diagrams

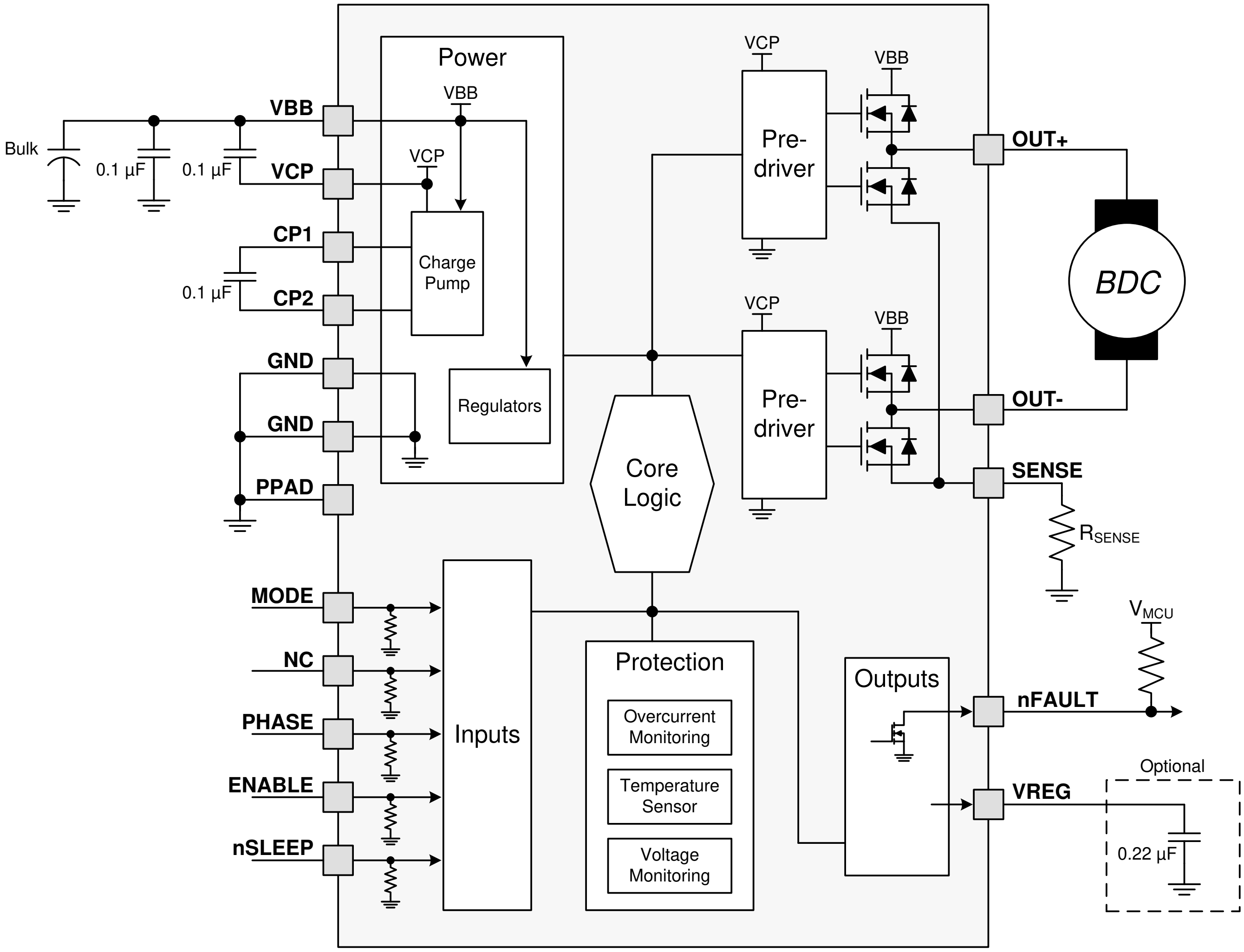


Figure 8-1. DRV8800 Functional Block Diagram

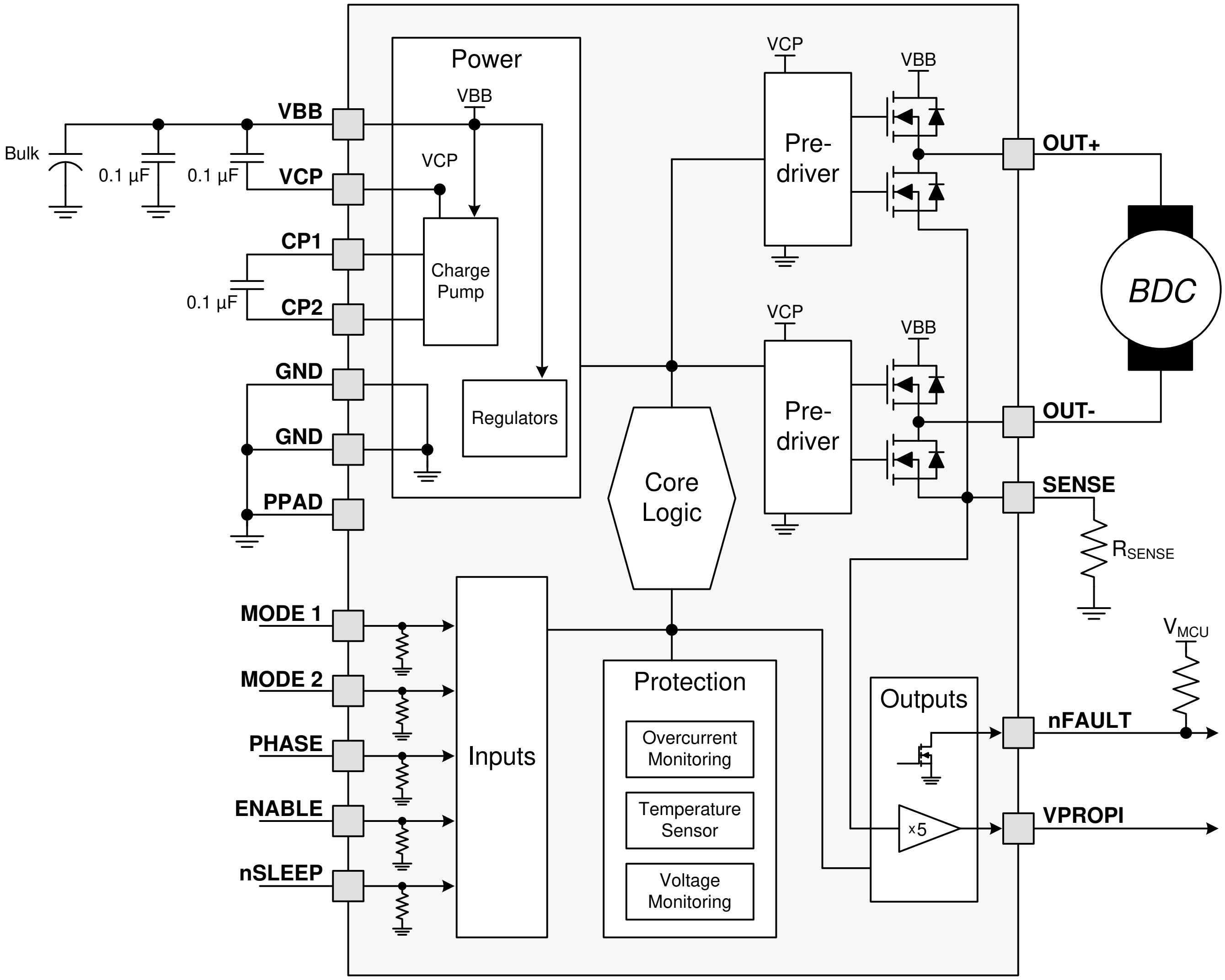


Figure 8-2. DRV8801 Functional Block Diagram

8.3 Feature Description

8.3.1 Logic Inputs

TI recommends using a high-value pullup resistor when logic inputs are pulled up to V_{DD}. This resistor limits the current to the input in case an overvoltage event occurs. Logic inputs are nSLEEP, MODE, PHASE, and ENABLE. Voltages higher than 7 V on any logic input can cause damage to the input structure.

8.3.2 VREG (DRV8800 Only)

This output represents a measurement of the internal regulator voltage. This pin should be left disconnected. A voltage of approximately 7.5 V can be measured at this pin.

8.3.3 VPROPI (DRV8801 Only)

The analog output VPROPI offers SENSE current information as an analog voltage proportional to the current flowing through the DC motor winding. This voltage can be used by an analog to digital converter and microcontroller to accurately determine how much current is flowing through the controlled DC motor. See Section 8.3.11 for guidance on selecting a SENSE resistor value.

8.3.3.1 Connecting VPROPI Output to ADC

The analog output VPROPI varies proportionally with the SENSE voltage according to Equation 1. It's important to note even if V_{SENSE} is negative VPROPI will remain at 0 V.

$$\mathrm{VPROPI} = 5 \times V_{\mathrm{SENSE}} \tag{1}$$

An RC network in series with the VPROPI output is recommended, if this voltage is to be sampled by an analog to digital converter.

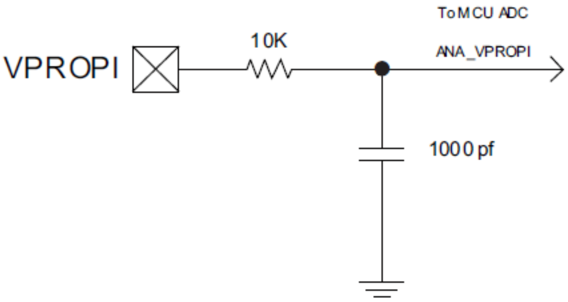


Figure 8-3. RC Network in Series With the VPROPI Output

It is imperative to realize that VPROPI will decrease to 0 V while the H-Bridge enters slow decay recirculation.

8.3.4 Charge Pump

The charge pump is used to generate a supply above VBB to drive the source-side DMOS gates. A 0.1-µF ceramic monolithic capacitor should be connected between CP1 and CP2 for pumping purposes. A 0.1-µF ceramic monolithic capacitor, CStorage, should be connected between VCP and VBB to act as a reservoir to run the high-side DMOS devices. The VCP voltage level is internally monitored and, in the case of a fault condition, the outputs of the device are disabled.

8.3.5 Shutdown

As a measure to protect the device, faults caused by very high junction temperatures or low voltage on VCP disable the outputs of the device until the fault condition is removed. At power on, the UVLO circuit disables the drivers.

8.3.6 Low-Power Mode

Control input nSLEEP is used to minimize power consumption when the DRV880x is not in use. A logic low on the nSLEEP input disables much of the internal circuitry, including the internal voltage rails and charge pump. A logic high on this input pin results in normal operation. When switching from low to high, the user should allow a 1-ms delay before applying PWM signals. This time is needed for the charge pump to stabilize.

8.3.7 Braking

The braking function is implemented by driving the device in slow-decay mode (MODE 1 pin is high) and deasserting the enable to low. Because it is possible to drive current in both directions through the DMOS switches, this configuration effectively shorts out the motor-generated BEMF as long as the ENABLE chop mode is asserted. The maximum current can be approximated by VBEMF/RL. Care should be taken to ensure that the maximum ratings of the device are not exceeded in worse-case braking situations – high-speed and high-inertia loads.

8.3.8 Diagnostic Output

The nFAULT pin signals a problem with the chip via an open-drain output. A motor fault, undervoltage condition, or T_J > 160°C drives the pin low. This output is not valid when nSLEEP puts the device into minimum power dissipation mode (that is, nSLEEP is low). nFAULT stays asserted (nFAULT = L) until VBB reaches VBBNFR to give the charge pump headroom to reach its undervoltage threshold. nFAULT is a status-only signal and does not affect any device functionality. The H-bridge portion still operates normally down to VBB = 8 V with nFAULT asserted.

8.3.9 Thermal Shutdown (TSD)

Two die-temperature monitors are integrated on the chip. As die temperature increases toward the maximum, a thermal warning signal is triggered at 160°C. This fault drives the nFAULT low, but does not disable the operation of the chip. If the die temperature increases further, to approximately 175°C, the full-bridge outputs are disabled until the internal temperature falls below a hysteresis of 15°C.

8.3.10 Overcurrent Protection

The current flowing through the high-side and low-side drivers is monitored to ensure that the motor lead is not shorted to supply or ground. If a short is detected, the full-bridge outputs are turned off, flag nFAULT is driven low, and a 1.2-ms fault timer is started. After this 1.2-ms period, t_{OCP} , the device is then allowed to follow the input commands and another turnon is attempted (nFAULT becomes high again during this attempt). If there is still a fault condition, the cycle repeats. If after t_{OCP} expires it is determined the short condition is not present, normal operation resumes and nFAULT is deasserted.

8.3.11 SENSE

A low-value SENSE resistor is used to set an overcurrent threshold lower than the default maximum value of 2.8 A and to provide a voltage for VPROPI (DRV8801 Only). This SENSE resistor must be connected between the SENSE pin and ground. To minimize ground-trace IR drops in sensing the output current level, the current-sensing resistor should have an independent ground return to the star ground point. This trace should be as short as possible. For low-value sense resistors, the IR drops in the PCB can be significant, and should be taken into account.

A direct connection to ground yields a SENSE voltage equal to zero. In that case, maximum current is 2.8 A and VPROPI outputs 0 V. A resistor connected as explained before, will yield a VPROPI output as detailed in Section 8.3.3. Size the sense resistor such that voltage drop across the sense resistor is less than 500mV under normal loading conditions. Any voltage equal or larger to 500 mV will signal the device to hi-Z the H-bridge output as overcurrent trip threshold has been reached. In this case, device will enter recirculation as stipulated by the MODE input pin. The device automatically retries with a period of $t_{(OCP)}$.

Equation 2 shows the value of the resistor to a particular current setting.

$$R_{sense} = \frac{500\text{ mV}}{I_{trip}} \tag{2}$$

8.4 Device Functional Modes

8.4.1 Device Operation

The DRV880x supports a low power sleep mode through the nSLEEP pin. In this mode the device shuts down a majority of the internal circuitry including the internal voltage rails and charge pump. Bringing the nSLEEP pin HIGH will put the device back into its active state.

During normal operation the DRV880x is designed to operate a single brushed DC motor. The outputs are connected to each side on the motor coil, allowing for full bidirectional control.

Table 8-1. Control Logic Table(1)

PINS							OPERATION
PHASE	ENABLE	MODE 1	MODE 2	nSLEEP	OUT+	OUT-	
1	1	X	X	1	H	L	Forward
0	1	X	X	1	L	H	Reverse
X	0	1	0	1	L	L	Brake (slow decay)
X	0	1	1	1	H	H	Brake (slow decay)
1	0	0	X	1	L	H	Fast-decay synchronous rectification(2)

Table 8-1. Control Logic Table[1] (continued)

PINS							OPERATION
PHASE	ENABLE	MODE 1	MODE 2	nSLEEP	OUT+	OUT-	
0	0	0	X	1	H	L	Fast-decay synchronous rectification[2]
X	X	X	X	0	Z	Z	Sleep mode

(1) X = Don't care, Z = high impedance

(2) To prevent reversal of current during fast-decay synchronous rectification, outputs go to the high-impedance state as the current approaches 0 A.

- MODE 1 (MODE on the DRV8800)

  Input MODE 1 is used to toggle between fast-decay mode and slow-decay mode. A logic high puts the device in slow-decay mode.

- MODE 2 (DRV8801 only)

  MODE 2 is used to select which set of drivers (high side versus low side) is used during the slow-decay recirculation. MODE 2 is meaningful only when MODE 1 is asserted high. A logic high on MODE 2 has current recirculation through the high-side drivers. A logic low has current recirculation through the low-side drivers.

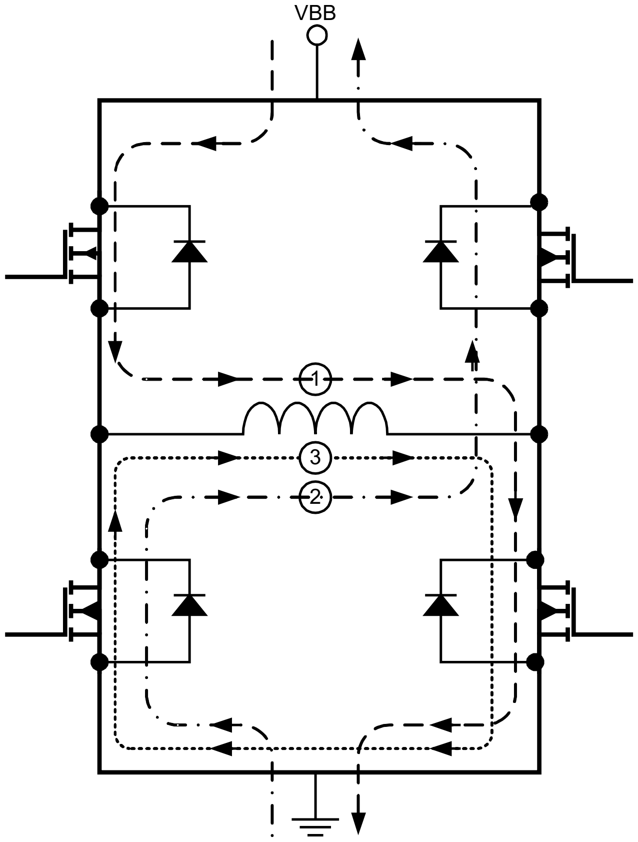
8.4.1.1 Slow-Decay SR (Brake Mode)

In slow-decay mode, both low-side sinking drivers turn on, allowing the current to circulate through the H-bridge's low side (two sink drivers) and the load. Power dissipation I^2R losses in one source and one sink DMOS driver, as shown in Equation 7

8.4.1.2 Fast Decay With Synchronous Rectification

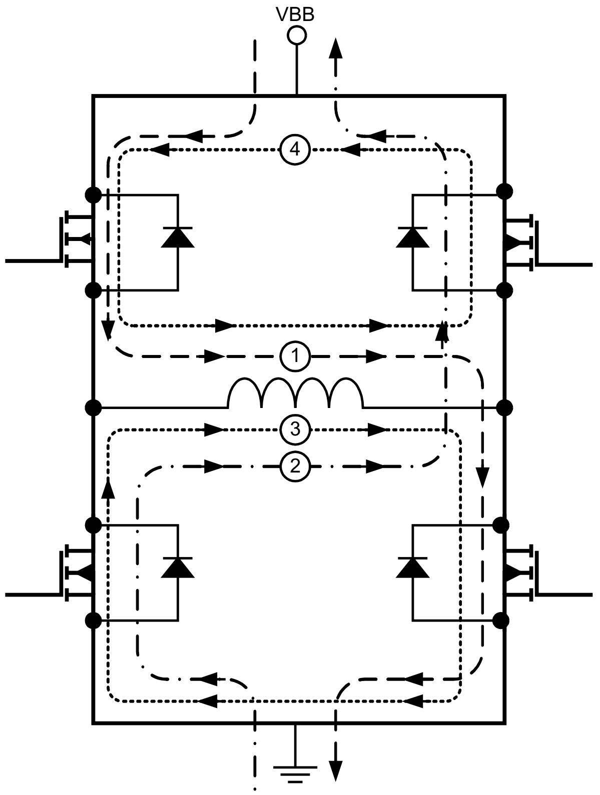
This decay mode is equivalent to a phase change where the opposite drivers are switched on. When in fast decay, the motor current is not allowed to go negative (direction change). Instead, as the current approaches zero, the drivers turn off. The power calculation is the same as the drive current calculation (see Equation 7).

8.4.1.2.1



① Drive Current
② Fast decay with synchronous rectification (reverse)
③ Slow decay with synchronous rectification (brake)

Figure 8-4. Current Path DRV8800



① Drive Current
② Fast decay with synchronous rectification (reverse)
③ Slow decay with synchronous rectification (brake) Low Side
④ Slow decay with synchronous rectification (brake) High Side

Figure 8-5. Current Path DRV8801

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

DRV880x device is used in medium voltage brushed DC motor control applications.

9.2 Typical Application

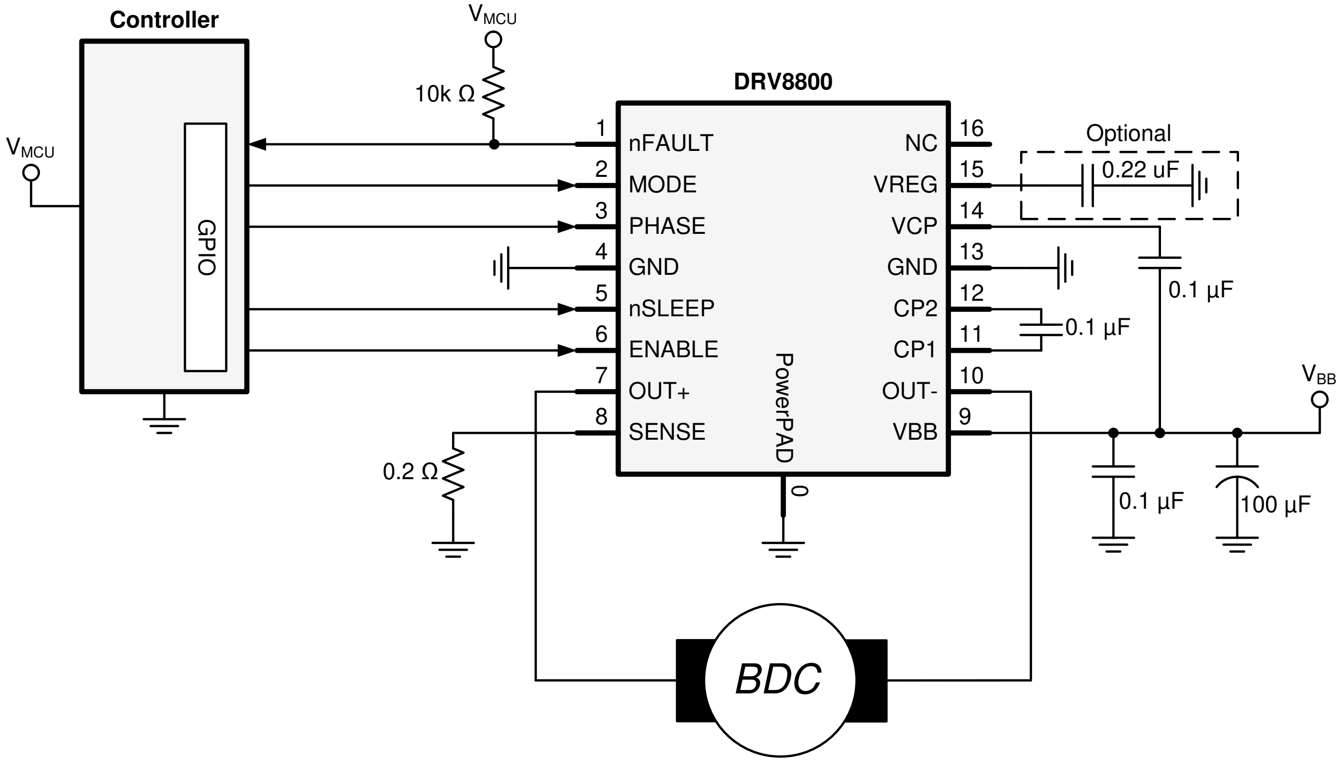


Figure 9-1. DRV8800 Typical Application Schematic

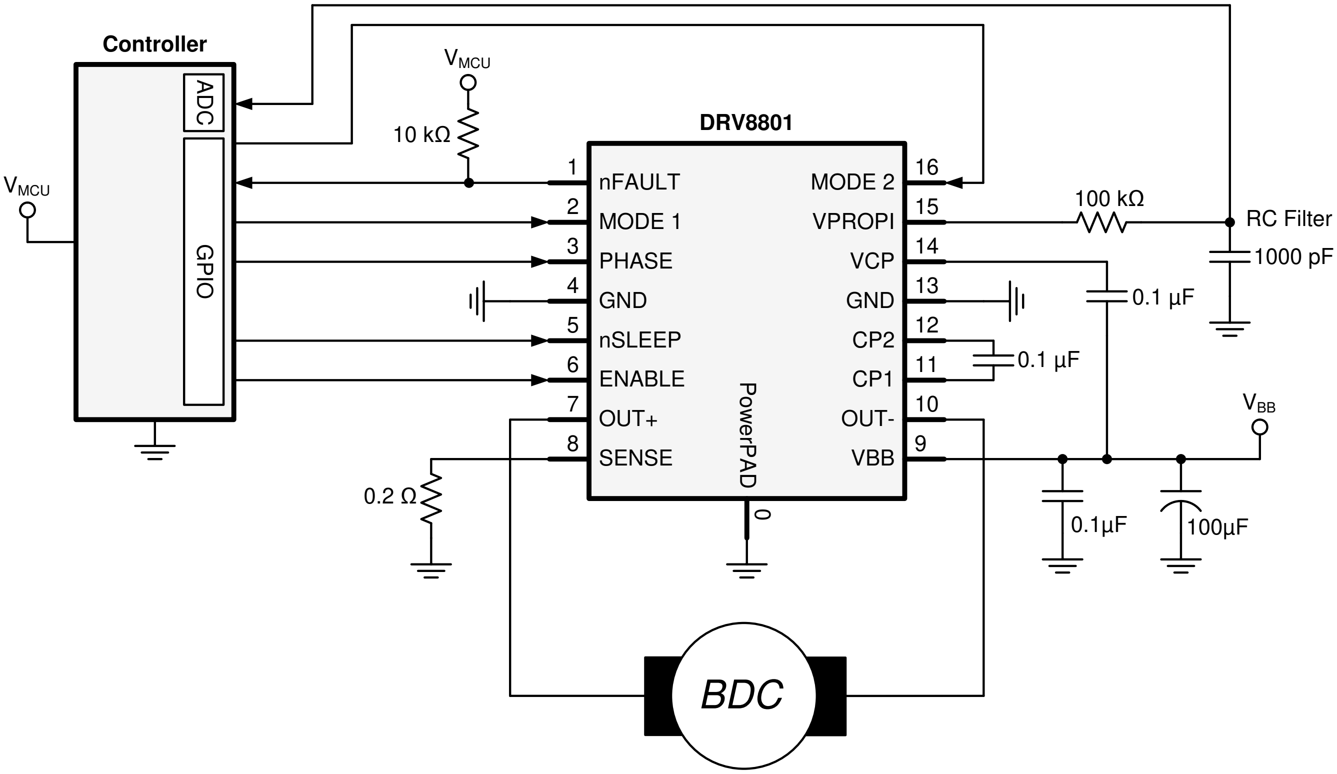


Figure 9-2. DRV8801 Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 9-1 as the input parameters.

Table 9-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor Voltage	VBB	24 V
Motor RMS Current	IRMS	0.8 A
Motor Startup Current	ISTART	2 A
Motor Current Trip Point	ITRIP	2.5 A

9.2.2 Detailed Design Procedure

9.2.2.1 Motor Voltage

The motor voltage to use will depend on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

9.2.2.2 Power Dissipation

The power dissipation of the DRV880x is a function of the RMS motor current and the each output's FET resistance ($R_{DS(ON)}$).

$$\text{Power} \approx I_{RMS}{}^{2} \times (\text{High-Side } R_{DS(ON)} + \text{Low-Side } R_{DS(ON)}) \quad (3)$$

For this example, the ambient temperature is 35°C, and the junction temperature reaches 65°C. At 65°C, the sum of RDS(ON) is about 1Ω. With an example motor current of 0.8A, the dissipated power in the form of heat will be 0.8 A^2x 1 Ω = 0.64 W.

The temperature that the DRV880x reaches will depend on the thermal resistance to the air and PCB. It is important to solder the device PowerPAD to the PCB ground plane, with vias to the top and bottom board layers, to dissipate heat into the PCB and reduce the device temperature. In the example used here, the DRV880x had an effective thermal resistance $R_{θJA}$ of 47°C/W, and:

$$T_J = T_A + (P_D \times R_{θJA}) = 35°C + (0.64\ W \times 47°C/W) = 65°C \quad (4)$$

9.2.2.3 Thermal Considerations

Although the DRV8800 and DRV8801 are rated at 2.8-A of current handling, the previous only holds true as long as the internal temperature does not exceeds 170°C. In order to operate at this rate, the following measures must be taken under consideration.

9.2.2.3.1 Junction-to-Ambiant Thermal Impedance (ΘJA)

At any given time during the steady state portion of the cycle, two FETs are enabled: A high side sourcing FET and a low side sinking FET. The increase in die temperature above ambient can be estimated by Equation 5

$$T_{die} = θ_{JA} \frac{°C}{W} \times I_{winding}{}^{2} \times RDS_{ON} + T_A \quad (5)$$

9.2.2.4 Motor Current Trip Point

When the voltage on pin SENSE exceeds V_{TRP} (0.5 V), overcurrent is detected. The R_{SENSE} resistor should be sized to set the desired I_{TRIP} level.

$$R_{SENSE} = 0.5\ V / I_{TRIP} \quad (6)$$

To set I_{TRIP} to 2.5 A, R_{SENSE} = 0.5 V / 2.5 A = 0.2 Ω.

To prevent false trips, I_{TRIP} must be higher than regular operating current. Motor current during startup is typically much higher than steady-state spinning, because the initial load torque is higher, and the absence of back-EMF causes a higher voltage and extra current across the motor windings.

It can be beneficial to limit startup current by using series inductors on the DRV880x output, as that allows I_{TRIP} to be lower, and it may decrease the system's required bulk capacitance. Startup current can also be limited by ramping the forward drive duty cycle.

9.2.2.5 Sense Resistor Selection

For optimal performance, it is important for the sense resistor to be:

- Surface-mount
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

9.2.2.6 Drive Current

This current path is through the high-side sourcing DMOS driver, motor winding, and low-side sinking DMOS driver. Power dissipation I^2R losses in one source and one sink DMOS driver, as shown in Equation 7.

$$P_D = I^2 (r_{DS(on)} Source + r_{DS(on)} Sink) \quad (7)$$

9.2.3 Pulse-Width Modulating

9.2.3.1 Pulse-Width Modulating ENABLE

The most common H-Bridge direction/speed control scheme is to use a conventional GPIO output for the PHASE (selects direction) and pulse-width modulate ENABLE for speed control.

9.2.3.2 Pulse-Width Modulating PHASE

Another technique is to use a speed/direction control scheme where ENABLE is connected to a GPIO output and the PHASE is pulse-width modulated. In this case, both direction and speed are controlled with a single signal. ENABLE is only used to disable the motor and stop all current flow.

When pulse-width modulating PHASE, a 50% duty cycle will stop the motor. Duty cycles above 50% will have the motor moving on the clockwise direction with proportional control; 100% duty cycle represents full speed.

Duty cycles below 50% will have the motor rotating with a counter clockwise direction; 0% duty cycle represents full speed.

9.2.4 Application Curves

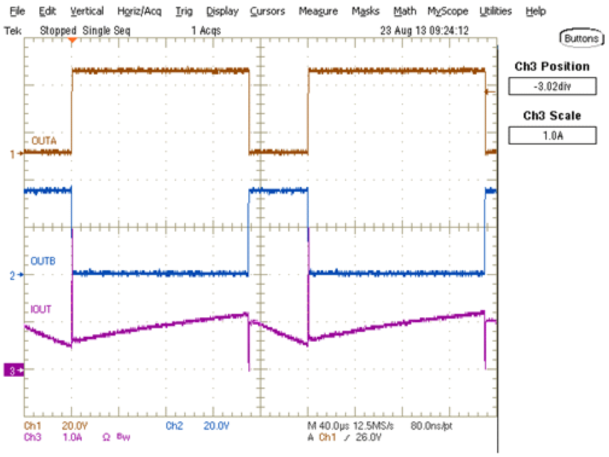


Figure 9-3. Forward Drive, Fast Decay

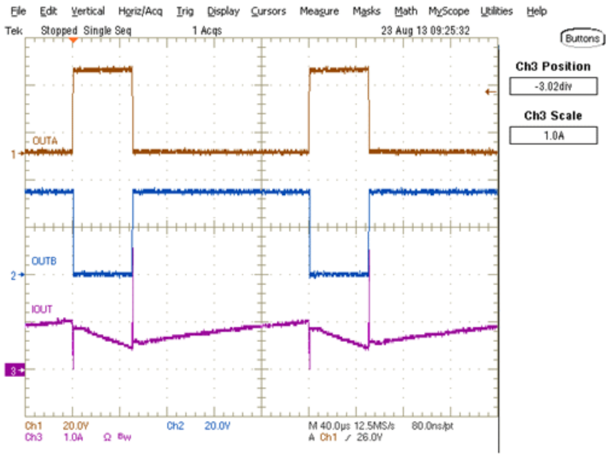


Figure 9-4. Reverse Drive, Fast Decay

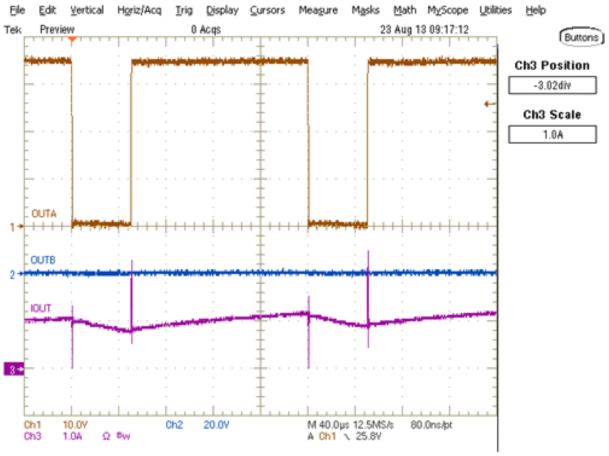


Figure 9-5. Forward Drive, Slow Decay

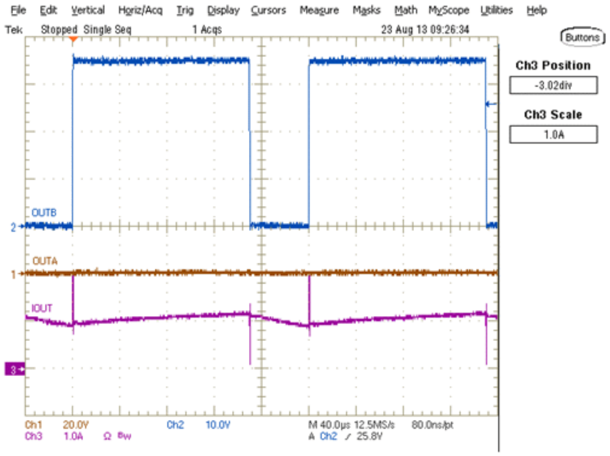


Figure 9-6. Reverse Drive, Slow Decay

9.3 Parallel Configuration

It is possible to drive higher than the 2.8 A of current by connecting more than one DRV8800 or DRV8801 in parallel. To properly use this option the guidelines documented below must be followed.

Note

It is not recommended that one connect a DRV8800 in parallel with a DRV8801. Only place like devices in the configuration outlined in this document

---

9.3.1 Parallel Connections

Figure 9-7 shows the signals that need to be connected together.

For DRV8801, ENABLE, PHASE, MODE 1, MODE 2, nSLEEP, OUT+, OUT-, SENSE, VBB and GND.

For DRV8800, ENABLE, PHASE, MODE, nSLEEP, OUT+, OUT-, SENSE, VBB and GND.

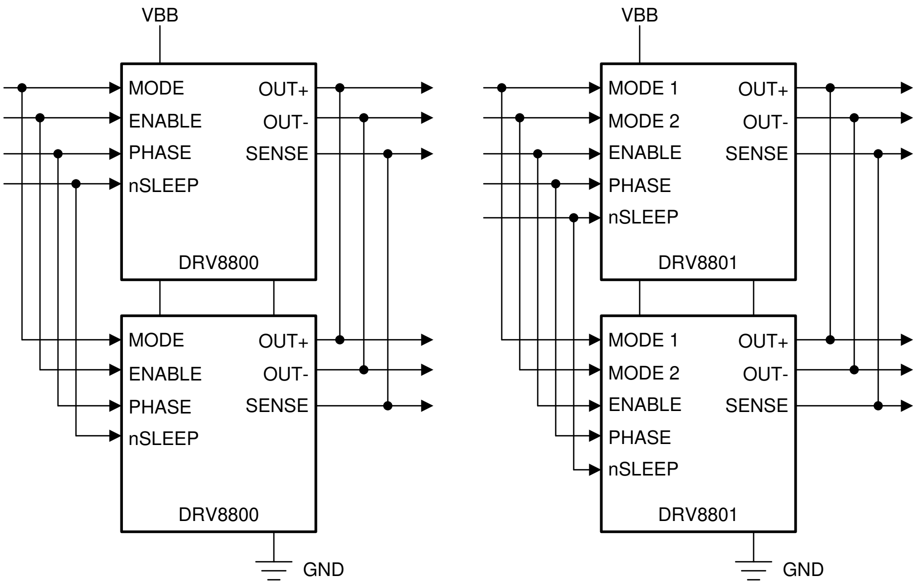


Figure 9-7. Functional Block Diagram (Connected Signals)

9.3.2 Non – Parallel Connections

Figure 9-8 shows the signals that should not be connected together and will be driven on an individual basis. These are: VCP, CP1, CP2, and VPROPI (on the DRV8801)

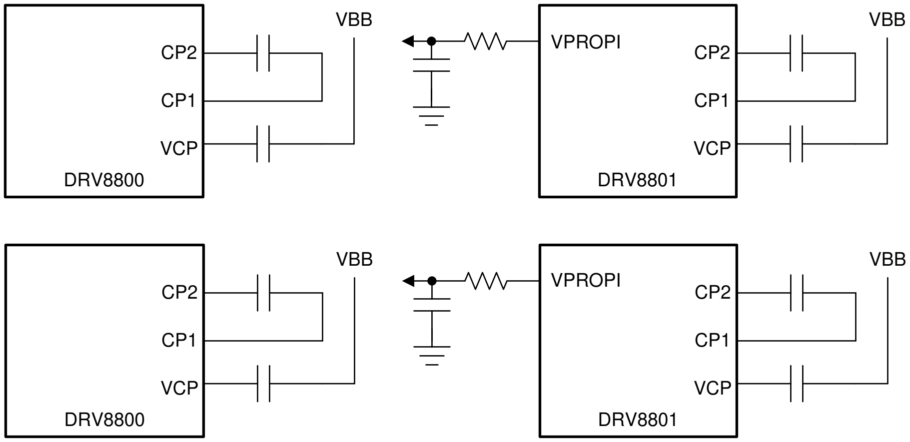


Figure 9-8. Functional Block Diagram (Individual Signals)

9.3.3 Wiring nFAULT as Wired OR

Since nFAULT is an open drain output, multiple nFAULT outputs can be paralleled with a single resistor. The end result is a wired OR configuration. When any individual nFAULT output goes to a logic low, the wired OR output will go to the same logic low. There is no need to determine which device signaled the fault condition, as once they are connected in parallel they function as a single device.

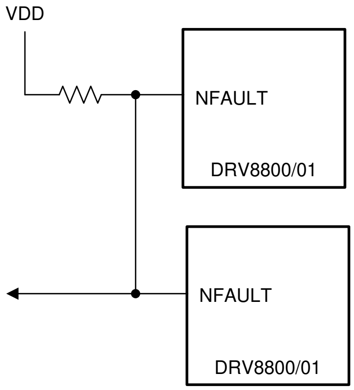


Figure 9-9. nFAULT as Wired OR

9.3.4 Electrical Considerations

9.3.4.1 Device Spacing

It is recommended that devices be connected as close as possible and with trace lengths as short as possible. Doing this minimizes the potential of generating timing differences between devices. Although it may seem like a harmful situation for the power stage, the DRV8800 and DRV8801 devices contain enough protection to effectively deal with enable time skews from device to device. This consideration focuses on motion quality, as total current needed for acceleration and proper speed control will only be available when all power stages are brought online.

9.3.4.2 Recirculation Current Handling

During recirculation, it is not possible to synchronize all devices connected in parallel so that the current is equally distributed. Also, during the asynchronous portion of the current decay, the body diode with the lowest forward voltage will start conducting and sink all of the current. Said body diode is not meant to handle the new increased current capacity and will be severely affected if allowed to sink current of said magnitude.

In order to assure proper operation when devices are connected in parallel, it is imperative that external schottky diodes be used. These schottky diodes will conduct during the asynchronous portion of the recirculation mode and will sink the inductive load current until the respective FET switches are brought online.

Schottky diodes should be connected as shown in Figure 9-10.

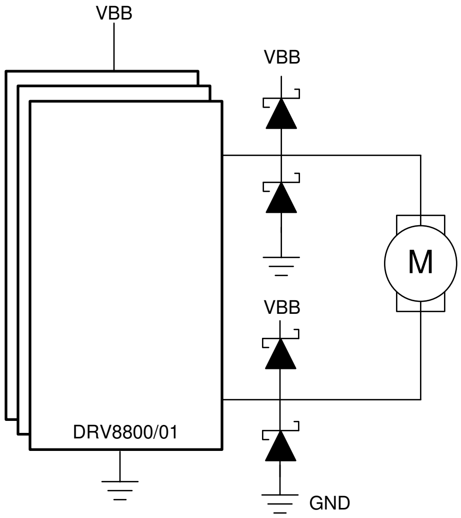


Figure 9-10. Schottky Diodes Connection

9.3.4.3 Sense Resistor Selection

The guideline for the SENSE resistor chosen doesn't change in parallel mode. As the goal of this configuration is to evenly distribute the current load across multiple devices, each device should be configured with the same I_{TRIP} setting. Therefore, the same SENSE resistor should be used for all devices connected in parallel.

Connection of the SENSE resistors should be as shown in Figure 9-11.

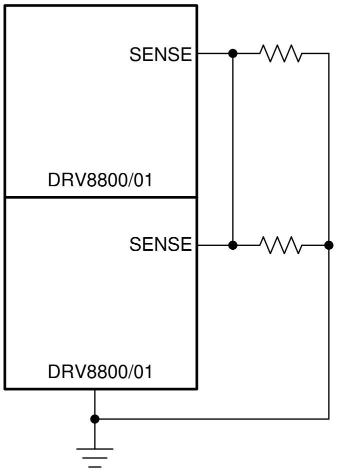


Figure 9-11. SENSE Resistors Connection

9.3.4.4 Maximum System Current

The idea behind placing multiple DRV8800/01 devices in parallel is to increase maximum drive current. At first glance, it may seem that the new increased I_{TRIP} setting is given by Equation 8.

$$\text{System}I_{TRIP} = \left(I_{TRIP} \times N\right) \tag{8}$$

Where:

N is the number of DRV8800/01 devices connected in parallel.

I_{TRIP} is the individual I_{TRIP} value per device.

However, although in theory accurate, due to tolerances in internal SENSE amplifier/comparator circuitry, the system I_{TRIP} should be expected to be less than the addition of all the individual I_{TRIP}. The reason for this is that as soon as one of the devices senses a current for which the H Bridge should be disabled, the remaining devices will end up having to conduct the same current but with less capacity. Therefore, remaining devices are expected to get disabled shortly after.

A good rule of thumb is to expect 90% of the theoretical maximum.

By way of example, if the system level requirements indicate that 6 A of current are required to meet the motion control requirements, then:

6 A = (2.8 A x 0.9)N

N = (6 A) / (2.8 A x 0.9)

N = 2.38

In this example, three DRV8800/01 devices would be required to meet the safety needs of the system.

10 Power Supply Recommendations

10.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system.
- The capacitance of the power supply and its ability to source current.
- The amount of parasitic inductance between the power supply and motor systems.
- The acceptable voltage ripple.
- The type of motor used (Brushed DC, Brushless DC, Stepper).
- The motor braking method.

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

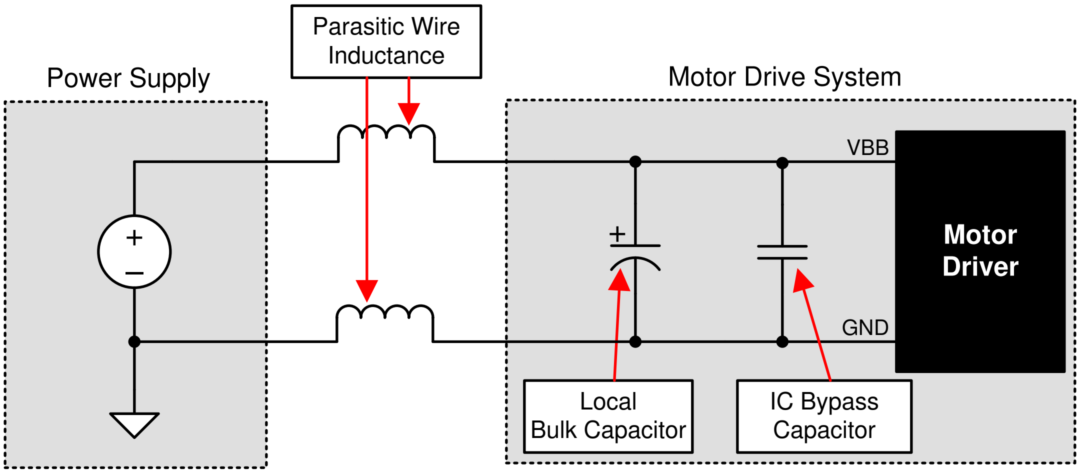


Figure 10-1. Example Setup of Motor Drive System With External Power Supply

11 Layout

11.1 Layout Guidelines

- The printed-circuit-board (PCB) should use a heavy ground plane. For optimal electrical and thermal performance, the DRV880x must be soldered directly onto the board. On the underside of the DRV880x is a thermal pad, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to an exposed surface on the PCB. Thermal vias are used to transfer heat to other layers of the PCB.
- The load supply pin VBB, should be decoupled with an electrolytic capacitor (typically 100 μF) in parallel with a ceramic capacitor (0.1 μF) placed as close as possible to the device.
- The ceramic capacitors (0.1 μF) between VCP and VBB and between CP1 and CP2 should be placed as close as possible to the device.
- The SENSE resistor should be close as possible to the SENSE pin and ground return to minimize parasitic inductance.

11.2 Layout Example

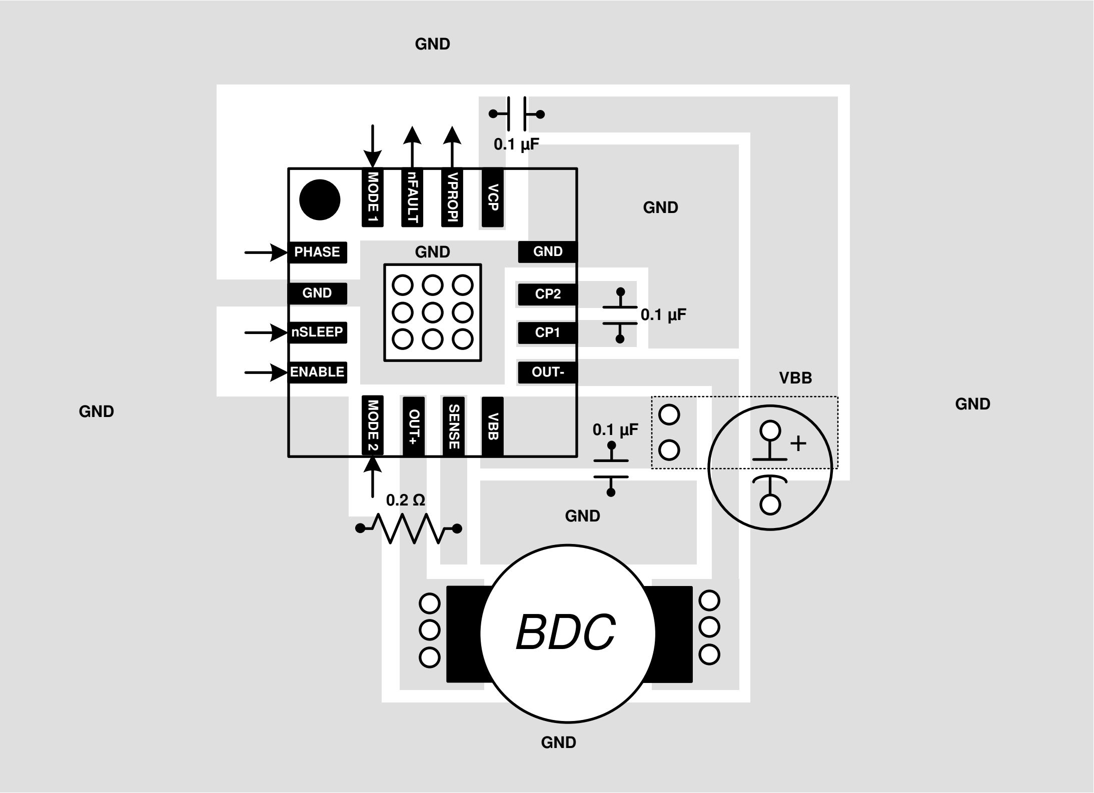


Figure 11-1. RTY Layout Example

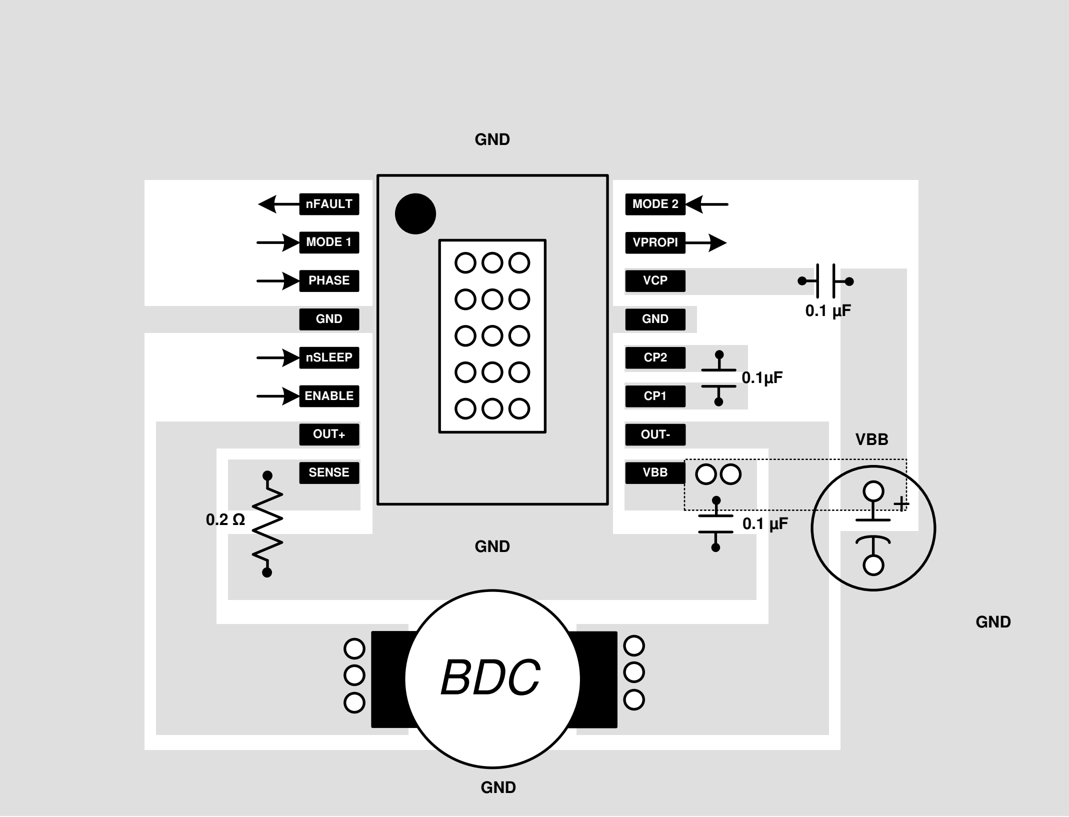


Figure 11-2. PWP Layout Example

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 12-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DRV8800	Click here	Click here	Click here	Click here	Click here
DRV8801	Click here	Click here	Click here	Click here	Click here

12.2 Trademarks

PowerPAD™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.4 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8800PWP	ACTIVE	HTSSOP	PWP	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV8800	Samples
DRV8800PWPR	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV8800	Samples
DRV8800RTYR	ACTIVE	QFN	RTY	16	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV 8800	Samples
DRV8800RTYT	ACTIVE	QFN	RTY	16	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV 8800	Samples
DRV8801PWP	ACTIVE	HTSSOP	PWP	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV8801	Samples
DRV8801PWPR	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV8801	Samples
DRV8801RTYR	ACTIVE	QFN	RTY	16	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV 8801	Samples
DRV8801RTYT	ACTIVE	QFN	RTY	16	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV 8801	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

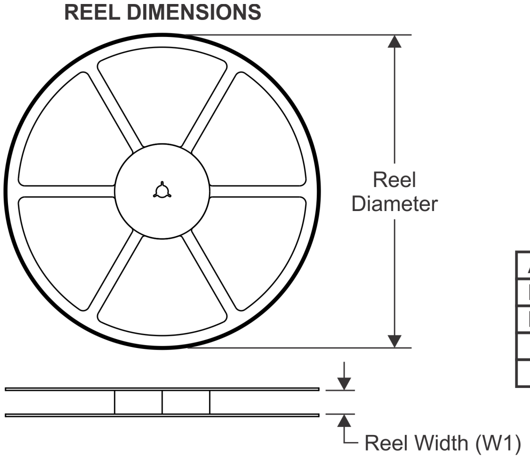
OTHER QUALIFIED VERSIONS OF DRV8801 :

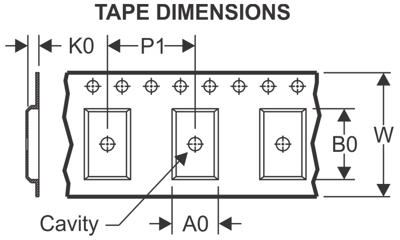
- Automotive: DRV8801-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

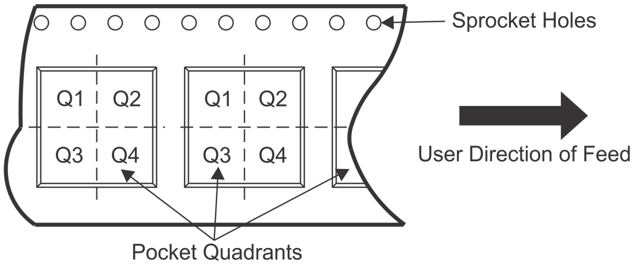
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

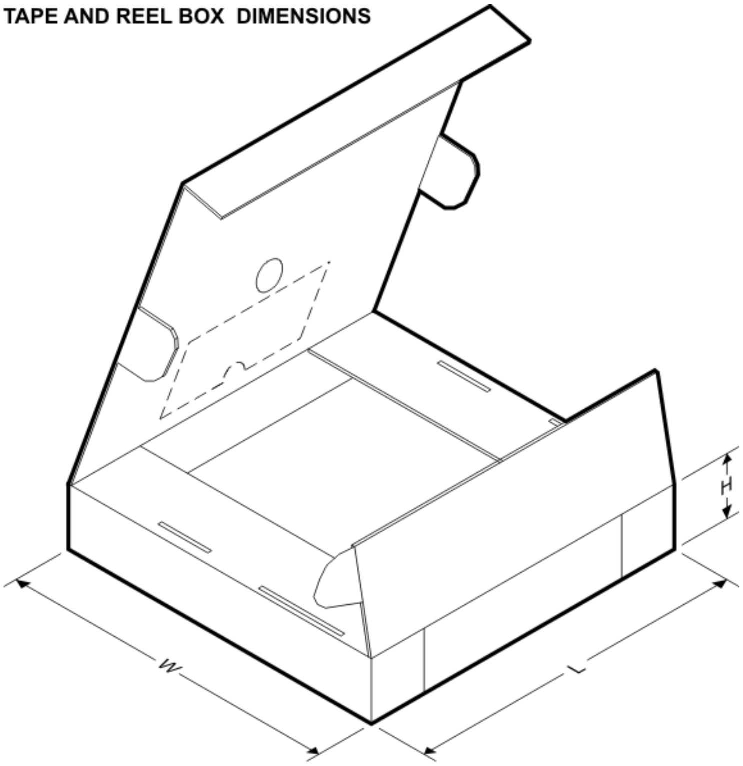
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8800PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DRV8800RTYR	QFN	RTY	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
DRV8800RTYT	QFN	RTY	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
DRV8801PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DRV8801RTYR	QFN	RTY	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
DRV8801RTYT	QFN	RTY	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

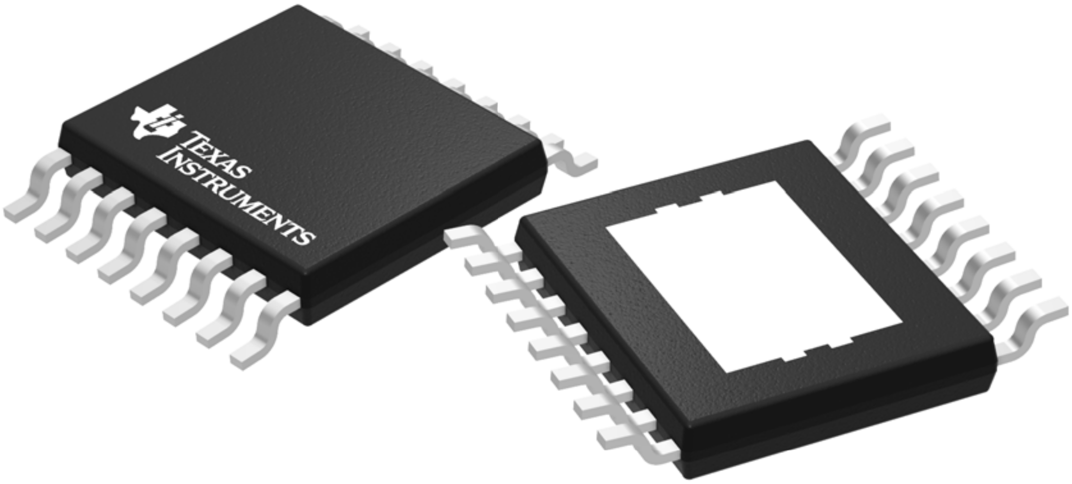
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8800PWPR	HTSSOP	PWP	16	2000	350.0	350.0	43.0
DRV8800RTYR	QFN	RTY	16	3000	853.0	449.0	35.0
DRV8800RTYT	QFN	RTY	16	250	210.0	185.0	35.0
DRV8801PWPR	HTSSOP	PWP	16	2000	350.0	350.0	43.0
DRV8801RTYR	QFN	RTY	16	3000	853.0	449.0	35.0
DRV8801RTYT	QFN	RTY	16	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

PWP 16

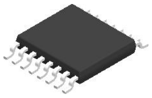
PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4073225-3/J

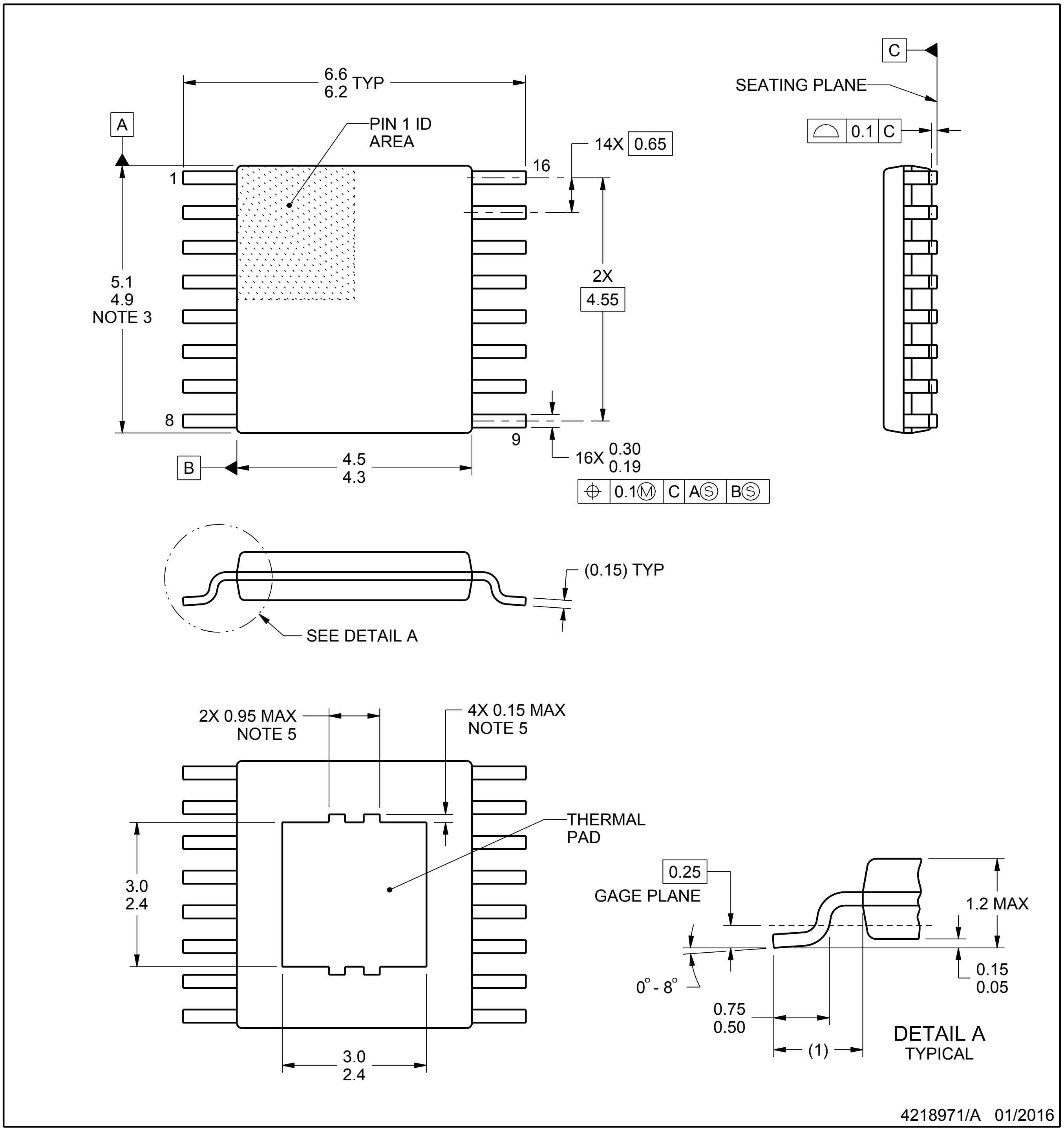


PACKAGE OUTLINE

PWP0016B

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



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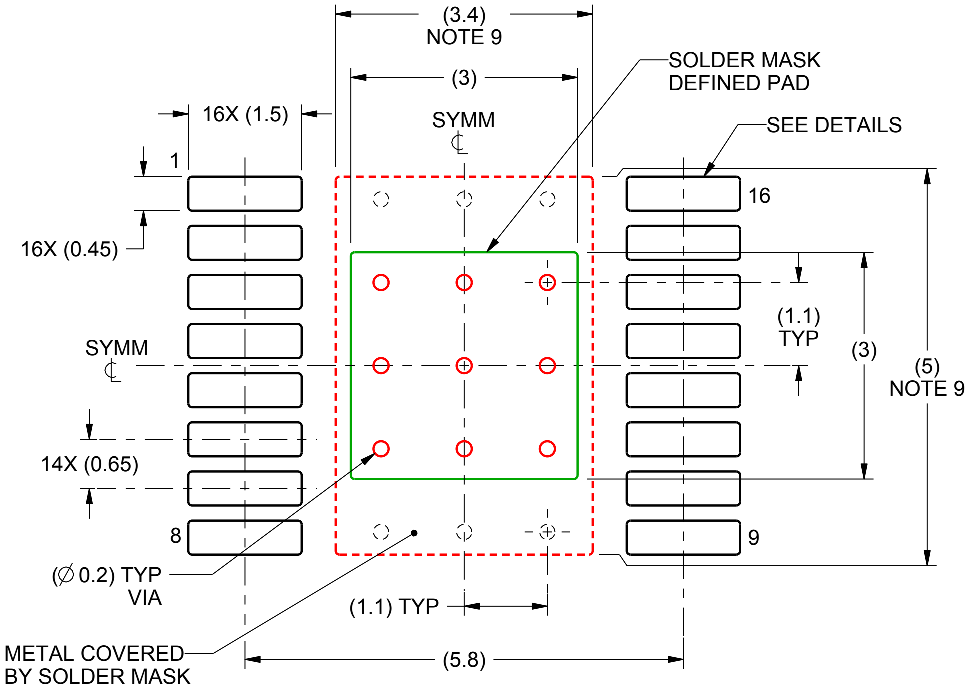
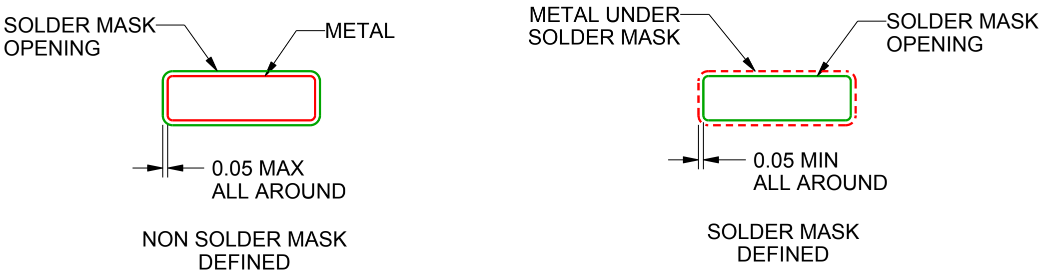
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.



LAND PATTERN EXAMPLE
SCALE:10X

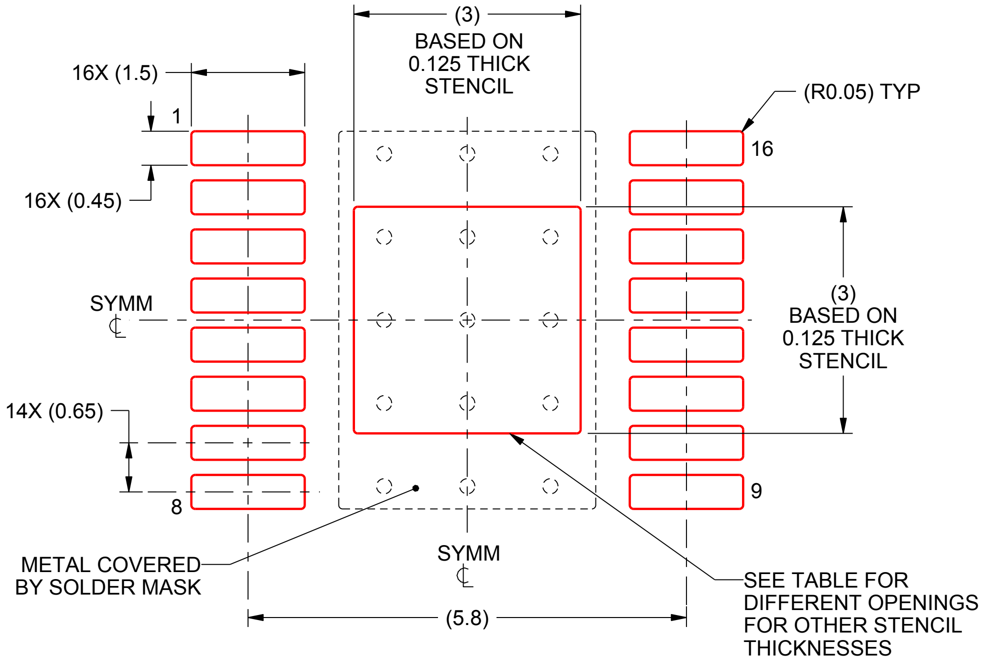


SOLDER MASK DETAILS
PADS 1-16

4218971/A 01/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

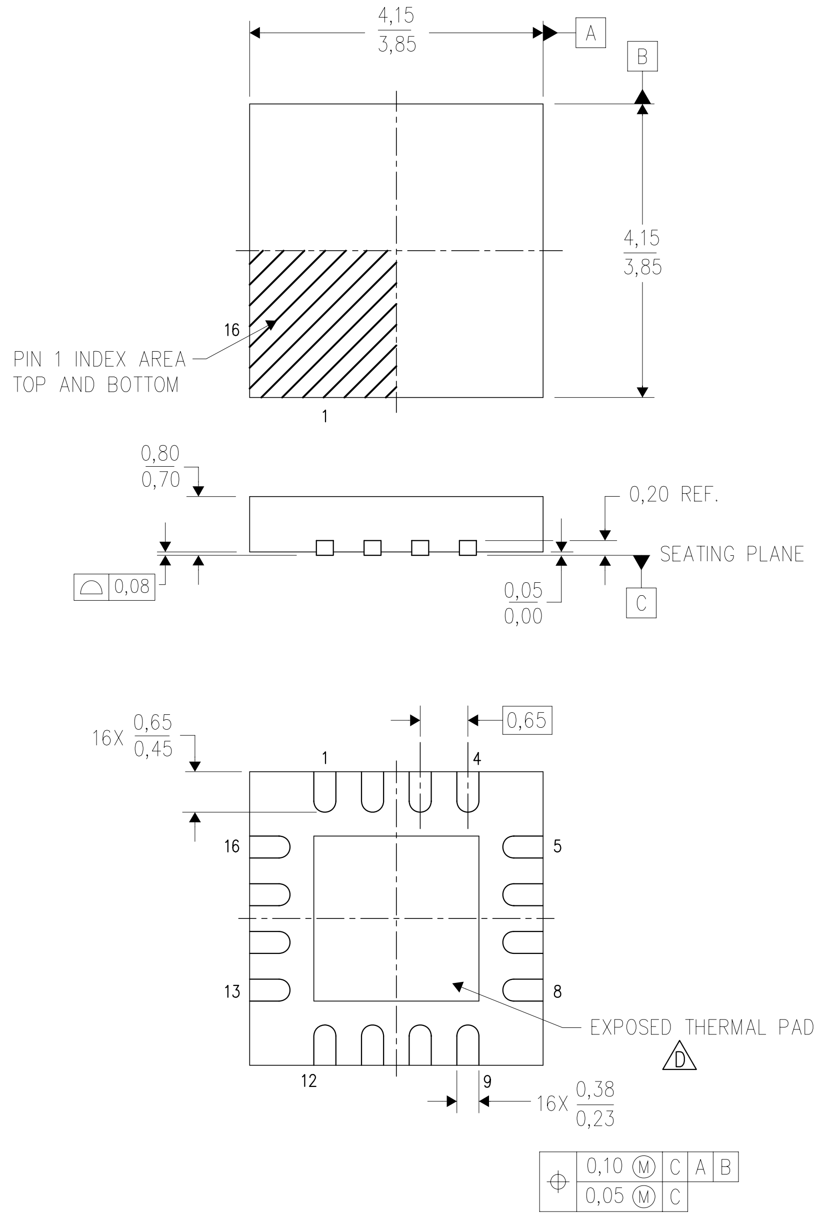
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.35 X 3.35
0.125	3 X 3 (SHOWN)
0.15	2.74 X 2.74
0.175	2.54 X 2.54

4218971/A 01/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

RTY (S-PWQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



4206276/B 03/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No-leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. Falls within JEDEC MO-220.

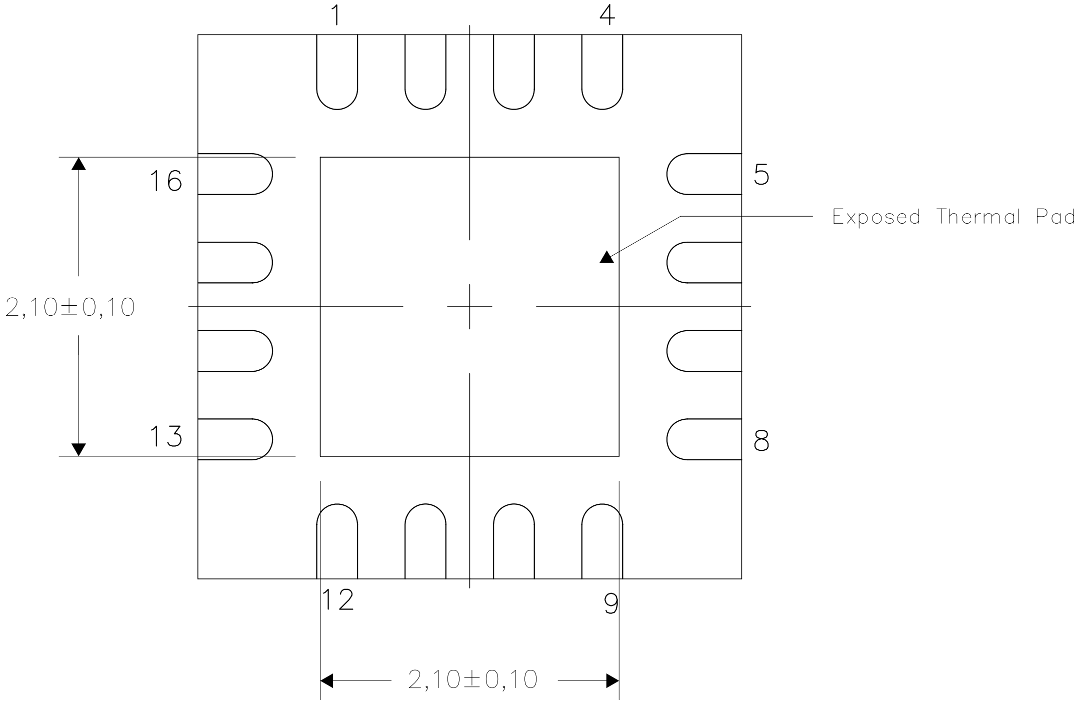
RTY (S-PWQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



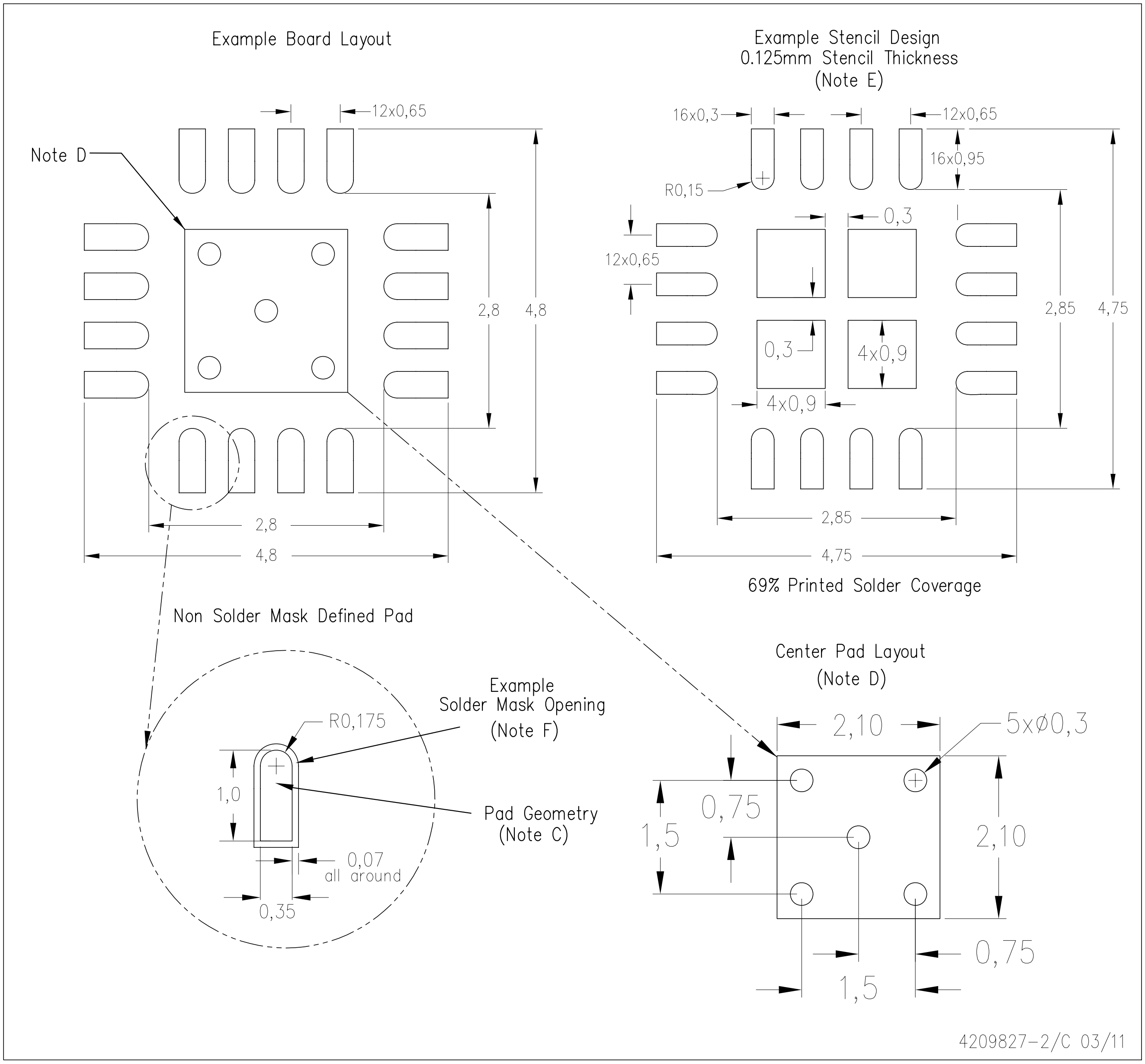
Bottom View

Exposed Thermal Pad Dimensions

4206277-2/E 03/11

NOTE: A. All linear dimensions are in millimeters

RTY (S-PWQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.

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