开关型、高效率、1.5A、锂电池充电管理控制器

特性

- 开关充电，相比线性充电，充电速度更快
- 充电恒压精度 4.2V±1%（AW3215A）
- 充电恒压精度 4.35V±1%（AW3216）
- 最大 1.5A 可配置恒流充电电流
- 专有的 K-DPM™ 基于 VBUS 电压的动态功率管理技术，自适应匹配 USB 或输出功率较小的适配器
- VBUS 引脚可承受>8kV（HBM）的 ESD 电压
- 效率最高可达 88%，有效降低大电流充电时 PCB 板温度
- 专有的 K-Temp™ 技术，可根据芯片温度线性调整充电电流
- VBUS 引脚最高直流耐压 18V
- 激活-涓流-恒流-恒压四段式充电，自动控制充电流程，自动再充电
- **NTC 引脚悬空时支持无电池软件 Download**
- 强壮的保护电路：VBUS OVP 保护，充电时的最低 VBUS 电压保护，电池 OVP 保护，芯片过温保护
- 集成防电流反灌功能，防止电流从电池反灌至芯片
- 纤小的 DFN3×3-12L 封装

应用

手机

概要

AW3215A/6 是高集成，开关型，高效率，大电流，锂离子电池充电管理控制芯片。集成 1.35MHz 同步降压 PWM 控制器和功率 MOSFET，有效降低了功率损耗。

AW3215A/6 充电流程包括：激活，涓流，恒流和恒压四个阶段。充电流程由芯片自动控制，充电完成后电池电压下降到 4.08V（AW3215A）/4.23V（AW3216）以下时芯片重新充电。

AW3215A/6 集成四个环路：恒压，恒流，K-DPM™ 和 K-Temp™，分别精确控制恒压电压，恒流电流，VBUS 电压和芯片结温，在充电过程中，其中的某一个环路起主要作用。专有的 K-DPM™ 技术，基于 VBUS 电压动态管理输出功率，减小充电电流而智能自适应匹配 USB 或输出功率较小的适配器。专有的 K-Temp™ 技术，可根据芯片温度线性调整充电电流，保证充电安全和防止过热的同时获得最大的充电速度。

AW3215A/6 采用纤小的 DFN3×3-12L 封装。

典型应用图

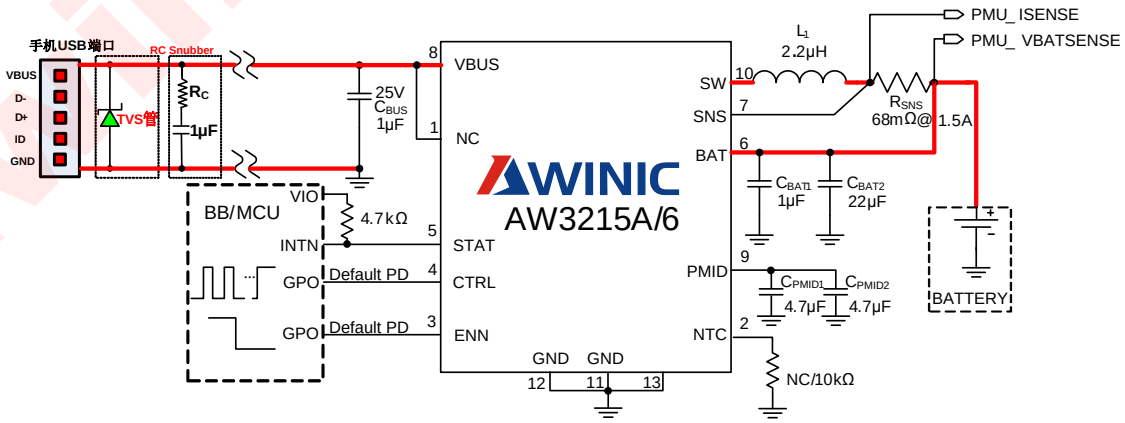

图 1　AW3215A/6 典型应用图

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1.5A Switch-mode Single Cell Li-ion Battery Charger

FEATURES

- Charge Faster than Linear Chargers
- Charge Voltage Regulation Accuracy:
  4.2V±1% (AW3215A) / 4.35V±1% (AW3216)
- Up to 1.5-A Programmable Charge Rate
- Specific K-DPM™: VBUS Based Dynamic Power Management
- VBUS Pin ESD >8kV（HBM）
- Up to 88% Charge Efficiency
- Specific K-TEMP™: Thermal Regulation Protection for Output Current Control
- 18V Absolute Maximum VBUS Rating
- Activation-Trickle-CC-CV Four-stage Automatic Charging Process, Automatic Recharge
- **Available for Software Download and System Start without Battery when NTC pin floated**
- Strong Charge Protection：VBUS OVP, Minimum VBUS during Charging, Battery OVP, Thermal Shutdown
- Charge Status Indication
- DFN 3mm×3mm-12L Package

APPLICATIONS

Mobile Phones

GENERAL DESCRIPTION

AW3215A/6 is a highly integrated, switch- mode high efficiency, large current Li-Ion battery charging management chip. Integrated 1.35 MHz synchronous Buck PWM controller and power MOSFETs, effectively reducing the power loss.

The charge process of AW3215A/6 includes: activation, trickle, constant current (CC) and constant voltage (CV). The charge process runs automatically and recharge occurs when the battery voltage drops below 4.08V (AW3215A) /4.23V (AW3216).

AW3215A/6 includes four loops: constant voltage, constant current, K-DPM™ and K-TEMP™, controlling the charge current, constant voltage, VBUS voltage and die temperature respectively. The K-DPM™ reduces charge current and adaptively matching USB or small power adapter. The K-Temp™ linearly adjusts charge current according to the die temperature, acquiring maximum charge-rate without overheating.

AW3215A/6 is available in DFN 3×3-12L package.

TYPICAL APPLICATION CIRCUIT

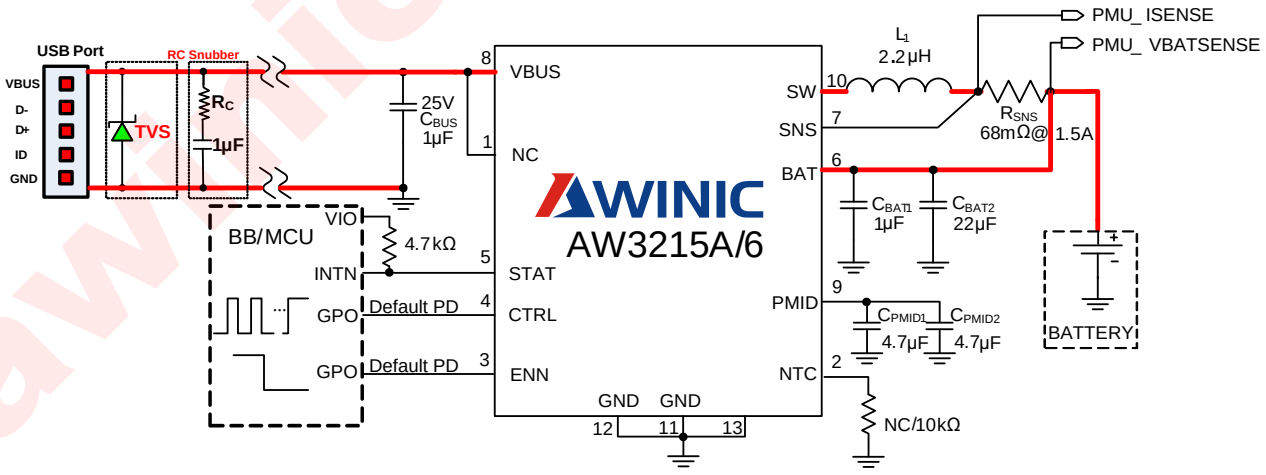

Figure 1 Typical Application Circuit of AW3215A/6

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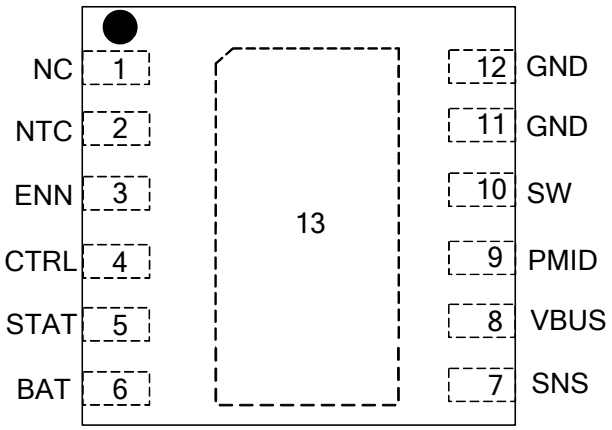
PIN CONFIGURATION AND TOP MARK

AW3215A/6 Top View



AW3215A DNR MARKING

3215A - AW3215A DNR
XXXX - Manufacture Date Code

AW3216 DNR MARKING

AW3216 - AW3216 DNR
XXXX - Manufacture Date Code

Figure 2 Pin Configuration and Top Mark

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PIN DEFINITION

No.	NAME	DESCRIPTION
1	NC	Not connect.
2	NTC	Connected to the NTC resistor inside battery, monitoring the battery temperature.
3	ENN	Charger enable input, drive ENN low or leave unconnected for normal operation.
4	CTRL	One-wire pulse input pin, to control the charge-termination current value. It's pulled down to ground by default, and the default charge-termination current is 10% of the CC charge current.
5	STAT	STAT is an open-drain output that signals charging status and fault interrupts. Low for charging, high for charge termination.
6	BAT	Battery Connection.
7	SNS	Charge current-sense input. Battery current is sensed across an external sense resistor.
8	VBUS	Charger input voltage, connected to AC adapter or USB
9	PMID	Connection point between OVP FET and high-side switching FET.
10	SW	Internal switch to output inductor connection.
11	GND	Ground.
12	GND	Ground.
13	Exposed pad	Beneath the IC for heat dissipation. Always solder to the PCB ground for high-current power converter.

AWINIC 1.5A-CHARGER FAMILY

	AW3215A	AW3216
VOREG(V)	4.2	4.35
VBUS threshold when K-DPM™ starts, VBUS falling（V）	4.75	4.65
Support software DOWNLOAD and system Power-on with No-battery when NTC pin floated, Y/N?	Y	Y

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FUNCTIONAL BLOCK DIAGRAM

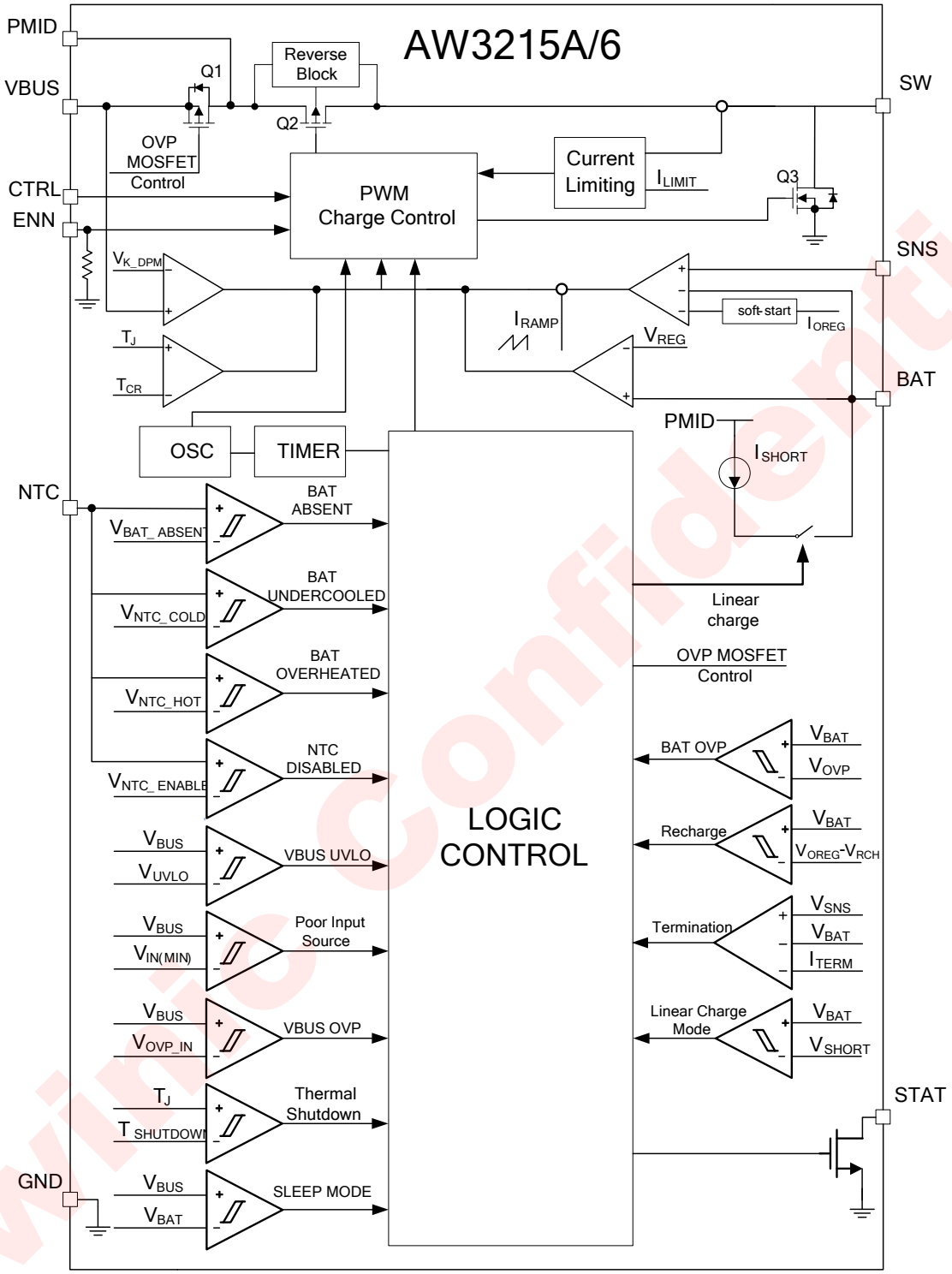

Figure 3 FUNCTIONAL BLOCK DIAGRAM

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TYPICAL APPLICATION CIRCUITS

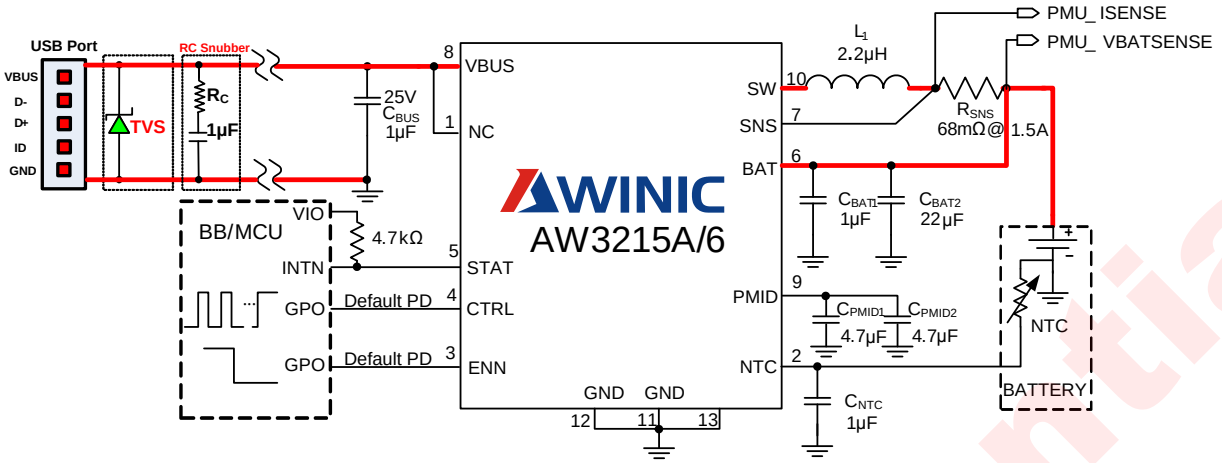

Figure 4 AW3215A/6 Application Circuit (NTC Pin connected to battery NTC resistor)

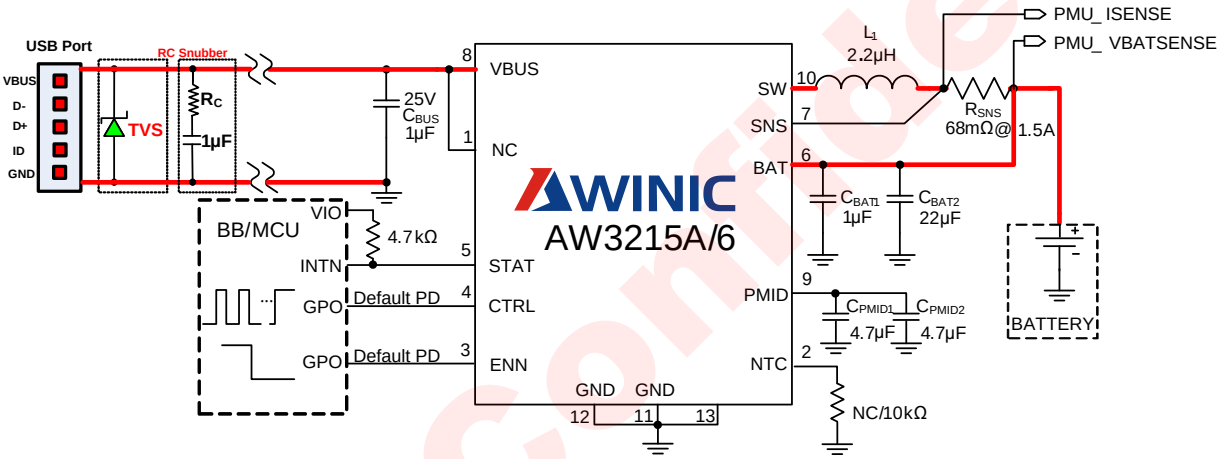

Figure 5 AW3215A/6 Application Circuit with NTC Pin floated or connected to ground through a 10kΩ resistor (disable the NTC monitor function of AW3215A/6）

Notice for Typical Application Circuits:

1：Please place C_{BUS1}，C_{BUS2}，C_{PMID1}，C_{PMID2}，C_{NTC}，C_{BAT1}，C_{BAT2} as close to the chip as possible, and C_{BUS2} close to PIN 8.

2：For the sake of driving capability, the power lines (especially the one to Pin 8), output lines, and the connection lines of L_1, R_{SNS}, and BATTERY should be short and wide as possible. The power path marked in red as shown in the figures above, please traces according to 1.5A power line alignment rules, of which the proposed width is about 60mil. (BAT PIN outputs current of 200mA, route the path with width of 14mil)

3：AW3215A/6 support software download with battery absent, when NTC pin floated. In such applications, the chip detects charge current after entering constant-voltage charge stage. When the current falls below charge-termination current threshold--ITERM, and last over 40ms (typical), the interrupt pin STAT behaves as a high impedance output. And it's the system to determine to whether close charging or not after detecting the high impedance state at STAT pin. AW3215A/6 does not turn off the charge until the constant-voltage phase timer (typ.4h) automatically stops after full.

4：Please connect the 1st pin of AW3215A which is NC to VBUS, for compatibility with AW3215.

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5：Surge voltage may be generated at VBUS when charger is hot plugged in, and high surge voltages may damage the chip or VBUS capacitance. In order to avoid this risk, a TVS tube or RC resistor can be placed in parallel with the VBUS port of USB interface. But according to the USB specification, the total capacitance at VBUS should between 1μF and 10μF. For detailed analysis, see the Applications Information section below, the robustness-increasing against hot-plug at the USB port.

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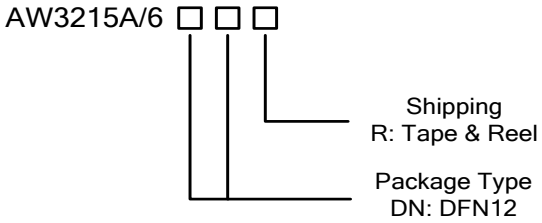
ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Delivery Form
AW3215A DNR	-40℃～85℃	3mm*3mm*0.75mm DFN3mm*3mm-12L	3215A	6000 units/ Tape and Reel
AW3216 DNR	-40℃～85℃	3mm*3mm*0.75mm DFN3mm*3mm-12L	AW3216	6000 units/ Tape and Reel



ABSOLUTE MAXIMUM RATINGS(NOTE1)

PARAMETERS		RANGE
Supply voltage range V_{BUS}		-0.3V to 18V
Input voltage range	NTC, SNS, CRTL, ENN	-0.3V to 7V
Output voltage range	STAT	-0.3V to 18V
	BAT, SW	-0.3V to 7V
Junction-to-ambient thermal resistance θ_{JA}		60℃/W
Operating free-air temperature range		-40℃ to 85℃
Maximum Junction temperature T_{JMAX}		160℃
Storage temperature T_{STG}		-65℃ to 150℃
Lead Temperature (Soldering 10 Seconds)		260℃
ESD(NOTE 2)		
VBUS PIN HBM (human body model)		±8kV
Other PINS HBM (human body model)		±2kV
Latch-up		
Test Condition: JEDEC STANDARD NO.78B DECEMBER 2008		+IT：450mA -IT：-450mA

NOTE1: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

NOTE2: *The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883G Method 3015.7*

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ELECTRICAL CHARACTERISTICS

Circuit of Figure 5, VBUS=5V, ENN=0, T_A=25℃ for typical values (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
INPUT CURRENTS						
I_{VBUS}	VBUS supply current control	V_{BUS}>V_{INMIN}, PWM switching		18		mA
		V_{BUS}>V_{INMIN}, PWM not switching			5	mA
		ENN=1 (VBUS=5V)		170		μA
I_{IKG}	Leakage current from battery to chip	V_{BAT}=4V, VBUS=0V or 2V or unconnected			1	μA
VBUS UVLO & VINMIN						
V_{UVLO}	IC active threshold voltage	VBUS rising - Exits UVLO	3.45	3.7	3.95	V
	IC active hysteresis	VBUS falling below UVLO- Enters UVLO	100	150	200	mV
	Deglitch time for IC active	VBUS rising - Exits UVLO		2		ms
V_{INMIN}	Input voltage lower limit for normal charging	VBUS rising	3.8	4.0	4.2	V
	Hysteresis for V_{INMIN}	VBUS falling	100	150	200	mV
	Deglitch time for V_{INMIN}	VBUS falling		2		ms
SLEEP MODE						
V_{SLP}	Sleep-mode entry threshold, V_{PMID}-V_{BAT}	VBUS falling	0	23	50	mV
V_{SLP_EXIT}	Sleep-mode exit hysteresis, V_{PMID}-V_{BAT}	VBUS rising	60	100	140	mV
	Deglitch time for VBUS rising above V_{SLP} +$V_{SLP-EXIT}$	VBUS rising		1.2		ms
CHARGE PROCESS						
V_{SHORT}	Activation to trickle charge threshold	VBAT rising	2.25	2.4	2.55	V
	V_{SHORT} hysteresis	VBAT falling		100		mV
V_{LOW}	Trickle to fast charge threshold	VBAT rising	2.65	2.85	3.05	V
	V_{LOW} hysteresis	VBAT falling		150		mV
V_{OREG}	Output regulation voltage	AW3215A	4.158	4.2	4.242	V
		AW3216	4.307	4.35	4.394	V

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PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
CHARGE CURRENT						
I_{OREG}	Output charge regulation current	$V_{LOW}≤V_{BAT}<V_{OREG}$, $V_{BUS}>V_{SLP}$, R_{SENSE}=68mΩ		1470		mA
		$V_{LOW}≤V_{BAT}<V_{OREG}$, $V_{BUS}>V_{SLP}$, R_{SENSE}=100mΩ		1000		mA
	Accuracy for charge current regulation			±8		%
I_{SHORT}	Activation charge current	$V_{BUS}>V_{SLP}$, V_{BAT}<2.4V	40	50	60	mA
I_{TKL}	Trickle charge current	$V_{BUS}>V_{SLP}$, 2.4V≤V_{BAT}<2.85V	160	200	240	mA
CHARGE TERMINATION DETECTION						
I_{TERM}	Termination charge current threshold	$V_{BAT}>V_{OREG}$-V_{RCH}, $V_{BUS}>V_{SLP}$		10		%I_{OREG}
	Deglitch time for charge termination			40		ms
	Accuracy for charge termination detection			±30		%
BATTERY RECHARGE THRESHOLD						
V_{RCH}	Recharge threshold voltage	VBAT falling after charge termination	80	120	160	mV
	Deglitch time for V_{RCH}	VBAT falling after charge termination		160		ms
K_DPM™						
V_{K_DPM}	K_DPM™ clamps VBUS	R_{SENSE}=68mΩ, I_{BUS_MAX}=500mA		4.5		V
STAT						
$V_{OL(STAT)}$	Low-level output saturation voltage, STAT Pin	I_O=10mA			0.35	V
	High-level leakage current for STAT	STAT is in high-impedance mode, V_{STAT}=5V			1	μA

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PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
PWM						
R_{OVP}	Internal OVP MOSFET on-resistance			210		mΩ
R_{PMOS}	Internal top P-channel MOSFET on-resistance			90		mΩ
R_{NMOS}	Internal bottom N-channel MOSFET on-resistance			170		mΩ
f_{OSC}	Oscillator frequency			1.35		MHz
	Frequency accuracy			±10		%
D_{MIN}	Minimum duty cycle		5			%
D_{MAX}	Maximum duty cycle				100	%
CHARGE PROCESS PROTECTION						
V_{OVP_VBUS}	Input VBUS OVP threshold voltage	VBUS rising	6.2	6.5	6.8	V
	V_{OVP_VBUS} hysteresis	VBUS falling from above V_{OVP_VBUS}		180		mV
V_{OVP_BAT}	Output VBAT OVP threshold voltage	VBAT rising	108	113	118	%V_{OREG}
	V_{OVP_BAT} hysteresis	VBAT falling		6		
I_{LIMIT}	Cycle-by-cycle current limit for charge			2.8		A
T_{OTP}	Overheating shutdown temperature	Chip temperature rising		160		℃
	Thermal hysteresis for T_{OTP}	Chip temperature falling		18		℃
T_{TIMER}	Timer for constant voltage charging			4		h
NTC						
R_{NTC}	NTC resistor value			10k		Ω
T_{DET_RANGE}	Battery temperature detection range		0		50	℃
V_{NTC_HOT}	NTC hot voltage threshold	Battery temperature rising		0.24		V
	NTC hot voltage hysteresis	Battery temperature falling		60		mV
V_{NTC_COLD}	NTC cold voltage threshold	Battery temperature falling		1.77		V
	NTC cold voltage hysteresis	Battery temperature rising		246		mV

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PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
ONE-WIRE PULSE						
V_{IH}	One-wire pulse input high threshold level		1.35			V
V_{IL}	One-wire pulse input low threshold level				0.35	V

TYPICAL CHARACTERISTICS

VBUS=5V, T_A=25℃, Circuit of figure 5 unless other noted.

Table 1 TABLE OF FIGURES

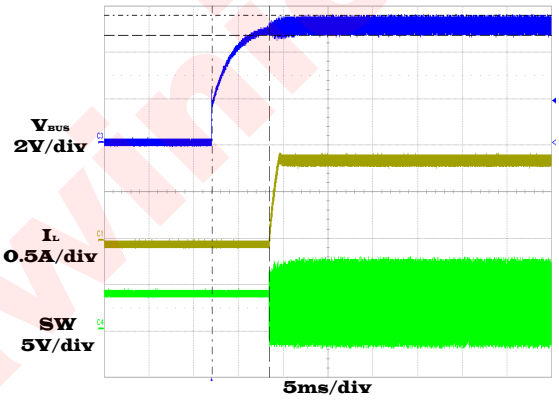

Figure 6 Adapter Insertion, VBUS=5V，VBAT=3.5V，ICHG=1A

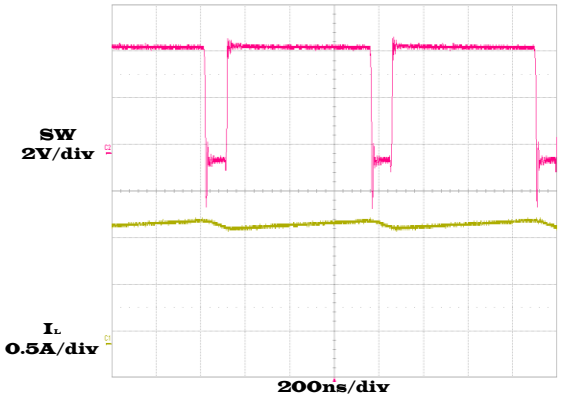

Figure 7 PWM Operation, VBUS=5V，VBAT=3.7V，ICHG=1.5A

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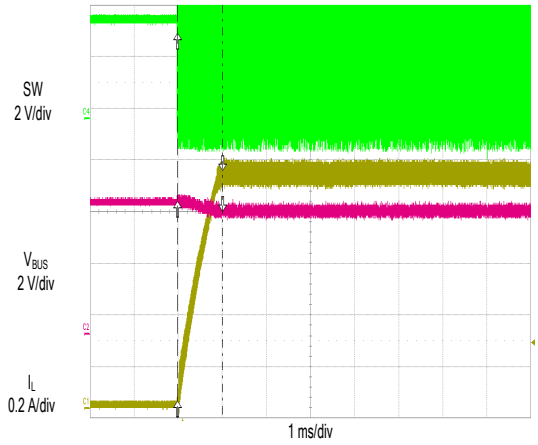

Figure 8 K_DPM™ Based on VBUS（USB Input）

VBAT=3.8V，RSNS=68mΩ

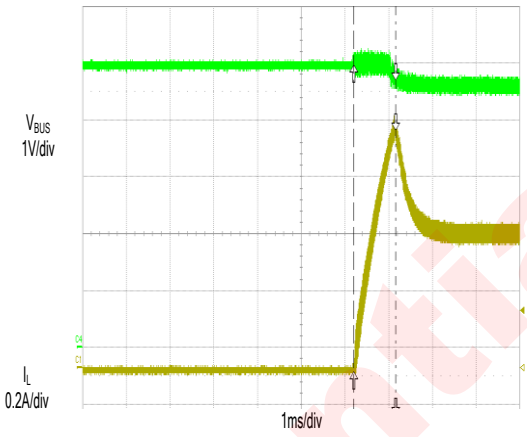

Figure 9 K-DPM™ Based on VBUS

（I_{SOURCE_MAX} limited to 500mA）RSNS=68mΩ

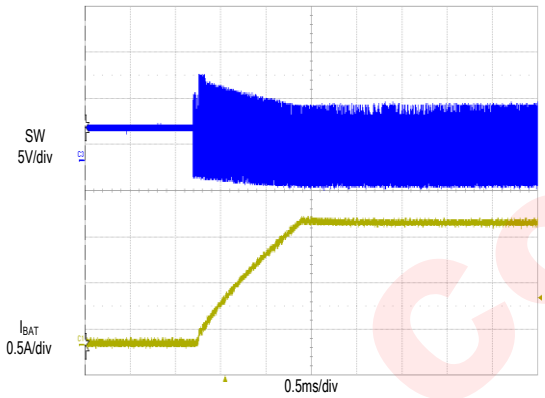

Figure 10 Charge Current Soft-start,

VBAT=3.5V，ICHG=1.5A

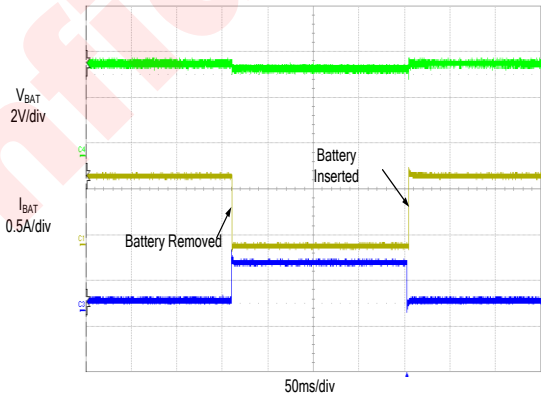

Figure 11 Battery Insertion/Removal,

VBAT=3.7V，ICHG=1.5A

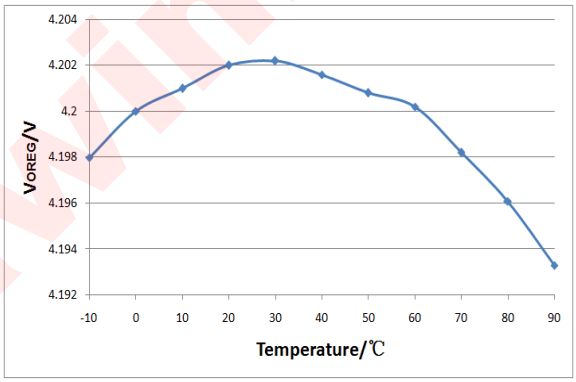

Figure 12 V_{OREG} vs. TEMPERATURE

AW3215A, NTC & BAT Pins Floated

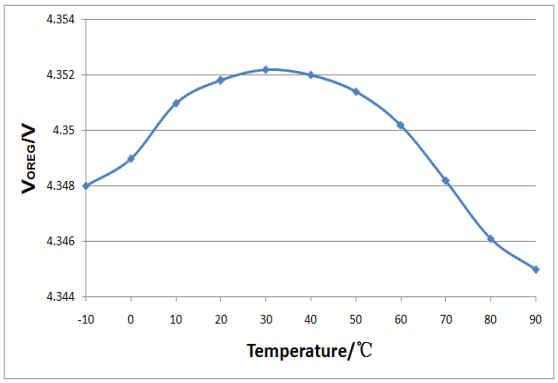

Figure 13 V_{OREG} vs. TEMPERATURE

AW3216, NTC & BAT Pins Floated

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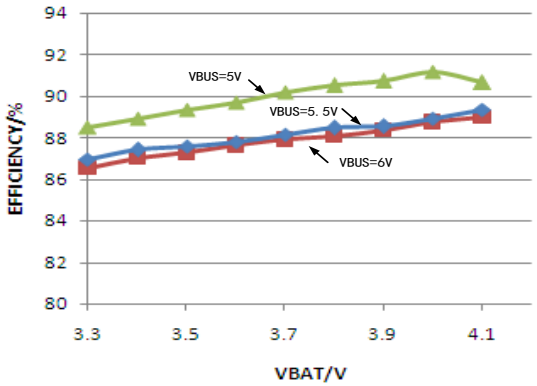

Figure 14 CHARGER Efficiency, ICHG=1.5A

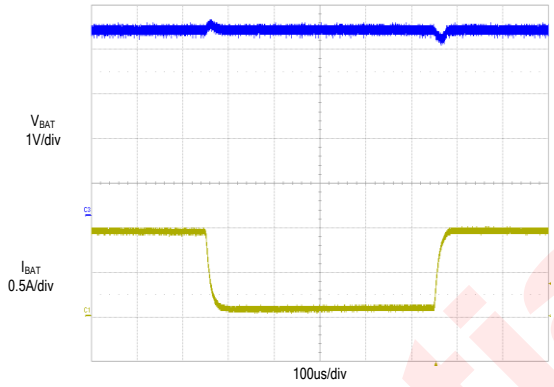

Figure 15 Download Mode, Load Regulation (0.1A-1A), NTC Pin Floated, Chip Enters Down-load Mode

TEMPERATURE RISING COMPARISION

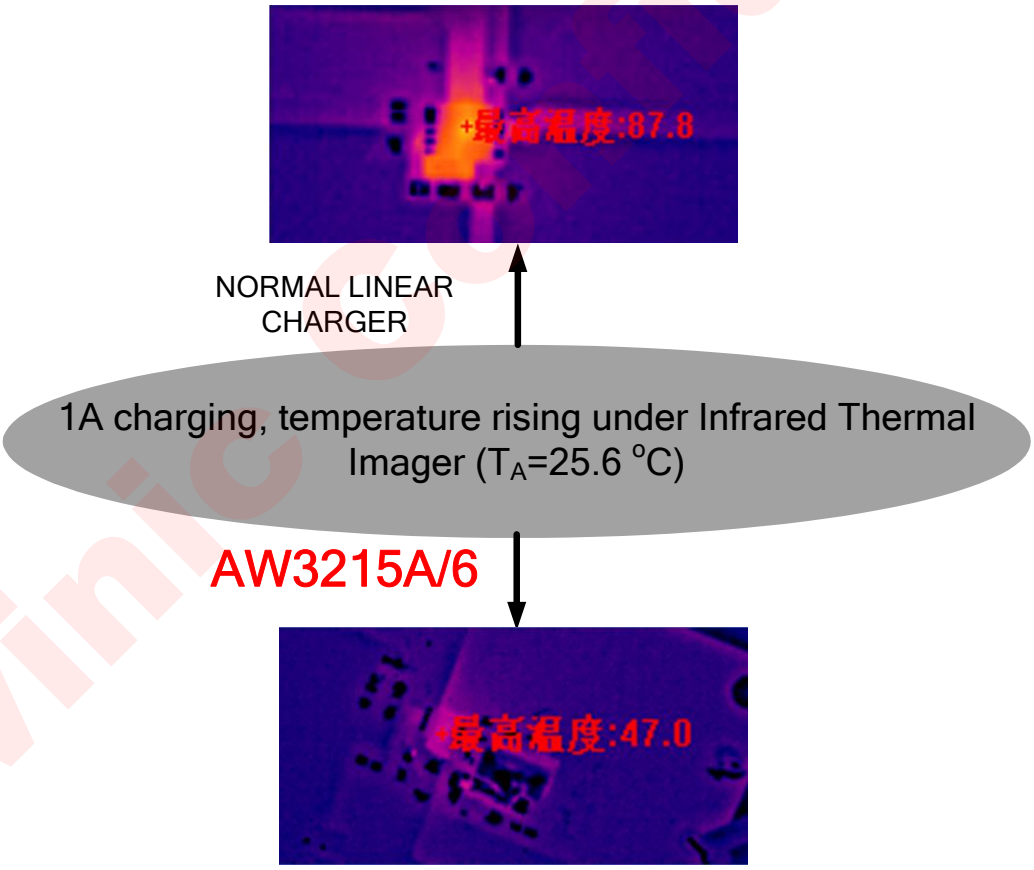

Figure 16 Temperature Rising Comparison between Normal Linear Charger and AW3215A/6 under 1A Charging

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DETAILED FUNCTIONAL DESCRIPTION

AW3215A/6 is a highly efficient, highly integrated synchronous switch charger chip. In a 4.5 ~ 5.5V of VBUS input voltage range, it provides maximum 1.5-A current for single-cell lithium ion or lithium polymer battery.

The charging process of AW3215A/6 includes four stages: activation, trickle, constant current and constant voltage. 50mA is the typical value of activation current, and 200mA for the typical value of trickle current, constant current charging current can be set by an external resistor RSNS（$I_{OREG}=\frac{100mV}{R_{SNS}}$）. The charge-termination current threshold can be configured via the CTRL pin with one-wire pulse, ranging from 10% to 90% of I_{OREG}, while the default is 10%× I_{OREG}.

AW3215A/6 VBUS pin can withstand >8kV (HBM) ESD voltage, and maximum 18V for DC voltage, other built-in protections of AW3215A/6 include: VBUS, BAT overvoltage protection, over temperature protection, protecting the chip from damages under abnormal working conditions.

The chip integrates VBUS under voltage lockout, sleep mode, monitoring battery temperature through NTC resistor, dynamic power management based on VBUS (K-DPM™) to ensure the smooth completion of charging process.

AW3215A/6 adopts DFN 3mm×3mm-12L package, and rated working temperature ranges from -40℃ to 85℃.

VBUS PROTECTION

The chip sets OVP, SLEEP MODE, K-DPM™, VINMIN protection mechanisms at the VBUS input port.

VBUS OVP

The IC provides a built-in input overvoltage protection to protect the device and other components against damage if the input voltage (Voltage from VBUS to GND) goes too high---- exceeds 6.5V typical. Then the chip stops charging, STAT pin behaves as a high impedance (open-drain) output. Once VBUS drops below the input overvoltage exit threshold (6.32V typical), charge process resumes.

VINMIN

If VBUS drops below VINMIN (3.85V typical) during charging, then an invalid adapter condition detected, charging stops, STAT pin becomes high impedance to GND. Charging continues after VBUS recovers to VINMIN exit threshold (4V typical).

SLEEP MODE

The IC enters the low-power sleep mode if the VBUS pin voltage falls below the sleep-mode entry threshold, VBAT+V_{SLP}, and lasts for 430μs(typ.). Furthermore, VBUS should be higher than the minimum input voltage, VINMIN then. This feature prevents draining the battery during the absence of VBUS. During sleep mode, both the OVPFET Q1 and PWM are turned off.

VBUS BASED DYNAMIC POWER MANAGEMENT——K-DPM™

The K-DPM™ allows AW3215A/6 to adaptively match USB or small power adapter. During the charging process, if the input power source is not able to provide the charging current set by R_{SNS}, the VBUS voltage will decrease. Once the VBUS drops below 4.75V(AW3215A, typ.) or 4.65V(AW3216, typ.), the K-DPM™ loop begins to taper down charge current, preventing any further drop of VBUS, and finally balance will be achieved between them. This feature makes the IC compatible with adapters having different current capabilities.

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BAT PROTECTION

VBAT OVP

The IC provides a built-in overvoltage protection to protect the device and other components against damage if the battery voltage goes too high, when the battery is suddenly removed. The IC would turn off the PWM converter if an overvoltage condition is detected, and STAT would behave as a high impedance (open-drain) output at the same time. Once VBAT drops to the battery overvoltage exit threshold, charge process resumes.

BATTERY SHORT PROTECTION

During the normal charging process, if the battery voltage is lower than the short-circuit threshold, V_{SHORT}(2.3V typical), the charger operates in short circuit mode with a lower charge rate of I_{SHORT}(50mA typical).

NTC PROTECTION

A negative temperature coefficient (NTC) resistor is built in lithium battery, used to monitor battery temperature. And charging must be stopped if the battery temperature exceeds acceptable limits. Connect the NTC resistor to the NTC pin, then the IC would output 60μA current to the NTC resistor. When the battery temperature rises to 50℃, NTC resistance becomes 4kΩ, namely hot voltage threshold is about 240mV; and 0℃ of battery temperature corresponds to about 30kΩ of the NTC resistance, i.e. cold voltage threshold is about 1.8V. After the NTC pin voltage exceeds the two thresholds, charging stops, STAT pin becomes high impedance to GND. The charging will not restart until NTC pin voltage recovers to the normal range.

The NTC function of AW3215A/6 can be disabled by connecting the NTC pin to ground or keep NTC pin floated.

CHARGE OPERATION

Once a good battery with voltage below the recharge threshold has been inserted and VBUS is among the normal range, the charging operation begins. During charging, the chip monitors VBUS voltage, charge current, constant regulation voltage and device junction temperature through four loops respectively. In the process of charging, one loop plays the main role. Figure 17 is a schematic diagram of AW3215A/6 charging process, which is divided into four stages: activation - trickle- constant current (CC) -constant voltage (CV). If NTC pin is connected to ground directly or via a 10kΩ resistor, after charging enters CV stage and a termination current is detected, charging stops. If the NTC pin is floated, charging would not stop immediately under the same condition, but send an interrupt signal to the system, offering whom a choice to determine whether to stop charging or not. If the system chooses to not stop it, AW3215A/6 would terminate charging automatically after the internal CV-timer(4h typ.) times up.

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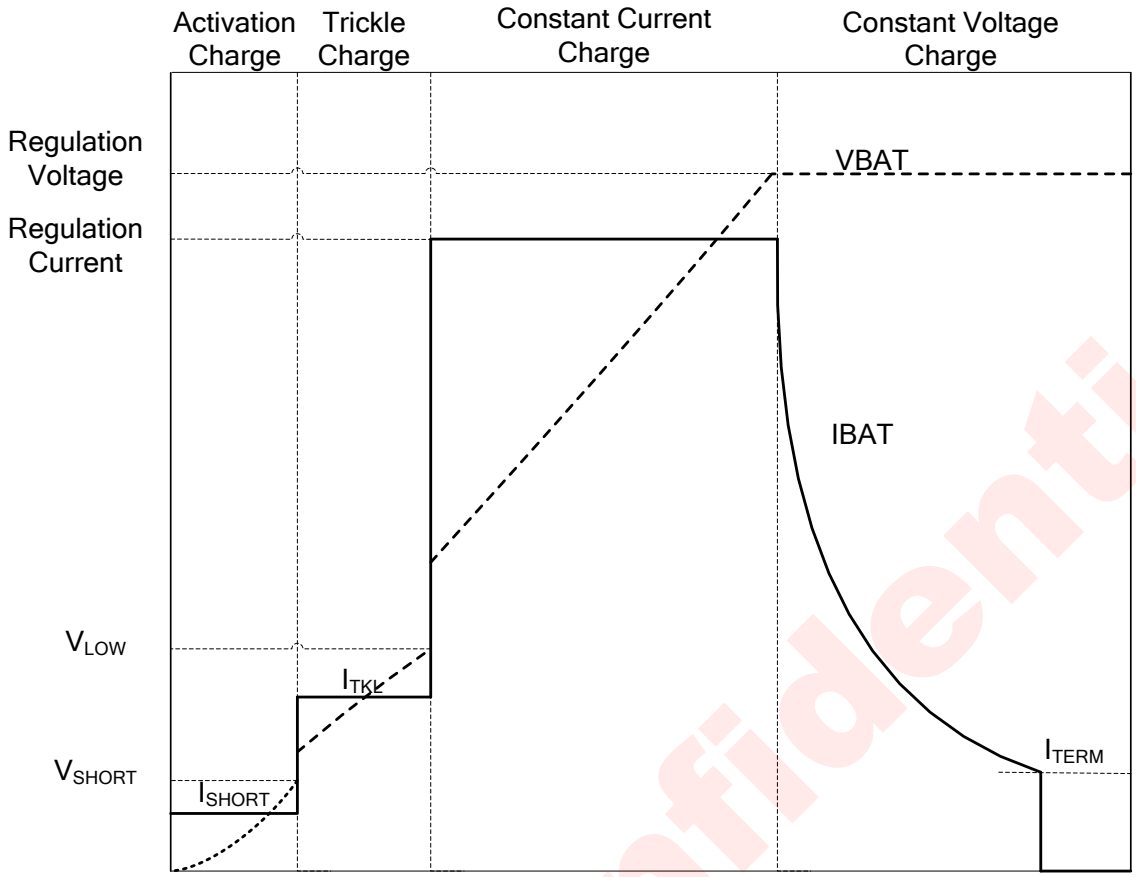

Figure 17 Typical Charging Profile of AW3215A/6

OPERATION OF THE LOOPS

In the process of charging, four loops of constant current, constant voltage, the K-DPM™ and K-TEMP™ interact, ensuring the charging goes smoothly.

Constant current loop adjusts the charge current by sampling the voltage difference across the external R_{SNS} resistor. The CC loop tends to make the duty cycle larger to increase the charging current as the voltage across R_{SNS} lower than the set value (100mV typical), and vice versa. Consequentially the IC regulates the charge current stably to the design value.

Constant voltage loop samples the BAT pin voltage. The CV loop doesn't take effect until the BAT pin voltage reaches the set value, and charging would be controlled by the CC loop before that. When BAT voltage gets close to the regulation value (4.2V typical), CC loop gradually looses the domination of charging, meanwhile the influence of CV loop in charging increases. Finally the domination of charging turns to CV loop. Thus realizes smooth switching from CC mode to CV, guaranteeing the charging process goes stably during the conversion of charging mode.

K-DPM™ loop decreases charging current if VBUS drop to the K-DPM™ threshold while charging. The reduction of current tends to stop VBUS from further drop. If the input current equals to the power supply capability of AC adapter or USB at that moment, VBUS stops to drop and the balance takes hold. The input current, as a consequence, stays at the maximum power supply value.

K-TEMP™ detects the device temperature during charging. The loop will reduce charge current when die temperature rises to the hot threshold (120℃ typical). This tends to prevent further increase of die temperature, and a thermal balance will be achieved, which makes the charge current stay at the value of not enable die temperature to continue to rise.

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PWM CONTROLLER

The IC integrates a fixed 1.35 MHz frequency synchronous Buck controller and power MOSFETs. At high side it adopts a P-channel FET(Q2), whose substrate is connected to the higher one among PMID and VBAT, to prevent reverse current from battery to VBUS. And at low side a N-channel FET(Q3) is used. DEADTIME exists among the normal charging cycle, during which both high and low sides FETs are shut down, and inductor current would pass through the body diode of low side FET.

Cycle-by-cycle current limit is sensed through the FETs Q2 and Q3. The threshold for Q2 is set to a nominal 2.8-A peak current. The low-side FET (Q3) also has a current limit that determines the PWM controller operates in either synchronous or non-synchronous mode. This threshold is set to 100mA and it turns off the low-side N-channel FET (Q3) before the current reverses, preventing the battery from discharging. Synchronous operation is used when the current of the low-side FET is greater than 100mA to minimize power losses.

BATTERY CHARGING PROCESS

Charge process would be in activation charge if battery voltage is below the V_{SHORT} threshold (2.4V typical). And the IC applies a short-circuit current, I_{SHORT} (50mA typical), to the battery then. When the battery voltage is above V_{SHORT} and below V_{LOW} (2.85V typical), the charge current increases to 200mA of I_{TKL}. And while battery voltage reaches V_{LOW}, the charge current ramps up to fast charge current, $I_{OCHARGE}$, until battery voltage rises to V_{OREG}. The slew rate for fast charge current is controlled to minimize the current and voltage over-shoot. Once the battery voltage reaches the regulation voltage, V_{OREG}, the charge current is tapered down as shown in Figure 17.

The IC monitors the charging current during the voltage regulation phase, and if the current reduces below the set termination threshold I_{TERM}, lasting for 40ms (typical value), then the battery charging completed. The IC would turn off the PWM charge, STAT pin behaves as a high impedance (open-drain) output. A new charge cycle will be initiated if the battery voltage falls below the V_{OREG}– V_{RCH} threshold and lasts for 160ms (typical value) after charging completed.

When the IC enters constant voltage stage, a timer for CV would be enabled. If the charging operation have not completed after the timer runs out (4h typical), timer will terminate the charging and STAT pin becomes high impedance to GND at the same time.

SYSTEM OPERATION WITHOUT BATTERY--DOWNLOAD MODE

AW3215A/6 enters DOWNLOAD mode when battery is absent and NTC pin is floated.

In DOWNLOAD mode, the IC outputs constant 4.2V(AW3215A) or 4.35V(AW3216) at the BAT pin, allowing AW3215A/6 supports system to power on and software download without a battery.

When the NTC pin is grounded directly or via a 10kΩ resistor, to power the system on or download software without the battery is not supported.

THERMAL LOOP K-TEMP™ AND OTP

To prevent overheating of the chip during charging, the IC monitors the junction temperature, T_J, of the die and begins to taper down the charge current once T_J reaches the thermal regulation threshold, T_{CR}(120℃ typ.). The charge current is reduced to zero when the junction temperature increases approximately 20°C above T_{CR}. In any state, if T_J exceeds T_{OTP}(160℃ typ.), the IC suspends charging. In thermal shutdown mode, PWM is turned off and timer is frozen. Charging resumes when T_J falls below T_{OTP} by approximately 18°C.

ONE-WIRE PULSE CONTROL

AW3215A/6 selects charging-termination threshold by detecting the mount of rising edges through one-wire pulse at CTRL pin, as shown in figure 18. When CTRL pin input low level, the IC chooses the default termination threshold of 10%×I_{OREG}. When CTRL pin pull high from low, there is one rising edge, then

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AW3215A/6 chooses the termination threshold of 20%×I_{OREG}. When high-low-high signal set to CTRL pin, there are two rising edges, the termination threshold becomes 30%×I_{OREG} and so on. AW3215A/6 can configure the range of termination threshold from 10%×I_{OREG} to 90%×I_{OREG}, 8 rising edges at most can be set into the CTRL pin. It is not allowed to input over 8 rising edges to the CTRL pin.

The high, low time of one-wire pulse range from 1μs to 10μs, and a level time of 2μs is advised.

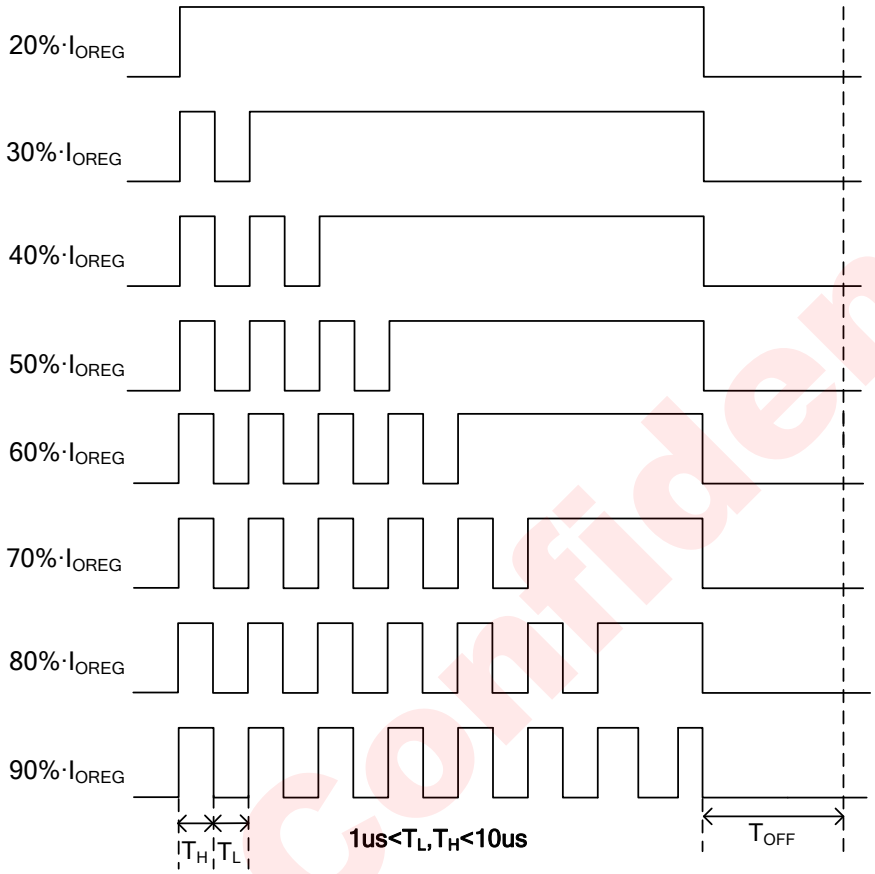

Figure 18 The State Diagram of One-wire Pulse Control

When we need to switch between different termination-current threshold, the CTRL pin must be pulled low at first. After the pulled-low level time exceeds the T_{OFF} limit (1ms advised), the inside register would be reset. Then input the pulses or rising edges we need. As shown in Figure 19.

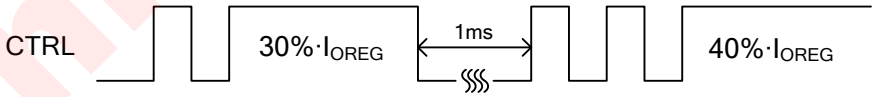

Figure 19 The Switching Control Sequence of One-wire Pulse States

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APPLICATION INFORMATION

INDUCTOR SELECTION GUIDELINE

The selection of inductance depends mainly on the inductor current ripple size requirement. Here is an example to illustrate the computational process of inductance selection.

Refer to the equation of BUCK inductor ripple current,

$\Delta I_L = \frac{VBAT \bullet (VBUS - VBAT)}{VBUS \bullet f_{SW} \bullet L}$, the worst case is when battery voltage is equal to half of the input voltage.

For AW3215A/6, the CC charging starts after VBAT higher than 3.25V (typical), and VBUS should be lower than 6.5V (typical) while charging, so the worst case occurs at VBUS= 6.5V, VBAT=3.25V. If the ripple current peak-to-peak is expected to below 600mA, we have

$$L = \frac{VBAT \bullet (VBUS - VBAT)}{VBUS \bullet f_{SW} \bullet \Delta I_L}$$
$$= \frac{3.25 \times (6.5\text{-}3.25)}{6.5 \times (1.35 \times 10^6) \times 0.6}$$

L=2.0μH. Select the output inductor to standard 2.2μH. Calculate the total ripple current with the 2.2μH inductor

$$\Delta I_L = \frac{VBAT \bullet (VBUS - VBAT)}{VBUS \bullet f_{SW} \bullet L}$$
$$= \frac{6.5 \times (6.5\text{-}3.25)}{6.5 \times (1.35 \times 10^6) \times 2.2 \times 10^{-6}}$$

Δ I_L=0.54A. Calculate the maximum output current:

$$I_{LPK} = I_{OUT} + \frac{\Delta I_L}{2}$$
$$= 1.47 + \frac{0.54}{2}$$

I_{LPK} =1.74A.

Select 2.5mm×2.0mm 2.2μH, rated current bigger than 1.74A inductor. The suggested inductor part numbers are shown as follow.

Part Number	Inductance	MFR	Size	DCR (Ω)	Saturation Current (A)	Heat Rating Current(A)
SPH252012H2R2MT	2.2μH	Sunlord	2.5×2×1.2mm	0.080	1.95	1.95
SPH4018H2R2MT	2.2μH	Sunlord	4×4×1.8mm	0.042	3.0	2.2

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CAPACITORS SELECTION

VBUS INPUT CAPACITOR C_{BUS}

AW3215A/6 advises to use a 1μF ceramic capacitor at VBUS pin as shown in Figure 4. This capacitor can decrease the overshoot of input voltage as well as decouple. Input voltage may produce transient overshoot because of the parasitic inductors on the input power lines when the hot insertion/removal of AC adapter occurs or input current suddenly falls. X7R or X5R ceramic capacitor with 25V rated voltage is recommended here.

There are parasitic inductors, resistors and capacitors along with the PCB line, when switch-mode current flow through parasitic inductors, there will be voltage-fall on them. If the potential change of power supply and ground at the IC pins are asynchronous, the inside logic signal may turn in error, leading to error action of the IC. Therefore, C_{BUS} should be placed as close to the IC as possible, the parasitic inductors from C_{BUS} to the V_{BUS} pins should not exceed 2nH.

BAT OUTPUT CAPACITOR C_{BAT}

BAT pin need the decoupling capacitor C_{BAT} as well. Meanwhile, C_{BAT} forms a LC filter together with the output inductor, which can filtering the high-frequency component in the output current and reduce the ripple of IBAT.

Take the L=2.2μH, C_{OUT}=22μF as an example, the resonant frequency of LC is

$$f_o = \frac{1}{2\pi\sqrt{L \bullet C_{OUT}}}$$

f=20kHz, which is far lower than the switching frequency 1.35 MHz, thus the output current can be well filtered. In addition, the ESR of the output capacitor has a significant effect on the output voltage ripple, so we parallel a 1μF capacitor with the 22μF, which decreases ESR. The table below shows the recommended capacitors.

Cap Location	Part Number	Manufacturer	Capacitance	Size	Rated Voltage
C_{BUS}	GRM185B31E105MA12	Murata	1μF	0603	25V
	C0603X5R105J250CY	EYANG	1μF	0603	25V
C_{BAT1}	C0402X5R105J6R3CY	EYANG	1μF	0402	6.3V
	GRM155B31C105MA12	Murata	1uF	0402	16V
C_{BAT2}	C0603X5R226J6R3CY	EYANG	22μF	0603	6.3V
	GRM319R61C226ME15	Murata	22μF	1206	16V
C_{PMID1}& C_{PMID2}	GRM188B31C475MAAJ	Murata	4.7μF	0603	16V
	C0603X5R475J100CY	EYANG	4.7μF	0603	10V

RSNS SELECTION

RSNS selection mainly depends on its resistance and power rating. For example, choose a 68mΩ-resistor, setting the constant current to 1.5A. The power dissipation across the resistor can be calculated according to $P=I^2 \bullet R$, which is 0.153W, that means you must select the resistor whose rated power is greater than 0.153W. Recommended part numbers of RSNS are given as follow.

Part Number	Resistance	Accuracy	Size	Rating Power	Manufacturer
RL0805FR-7W0R068L	68 mΩ	±1%	0805	1/4 W	Yageo
PT0805FR-070R1L	100 mΩ	±1%	0805	1/8 W	Yageo

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RECOMMENDED COMPONENTS LIST

Component	PART No.	DESCRIPTION	MFR	TYP.	UNIT
L_1	SPH252012H2R2MT	80mΩ,1.95A, 2.5×2×1.2mm	SUNLORD	2.2	μH
	SPH4018H2R2MT	42mΩ,2.2A, 4×4×1.8mm	SUNLORD	2.2	μH
C_{BUS}	GRM185B31E105MA12	25V, X5R, 0603	Murata	1	μF
	C0603X5R105J250CY	25V, X5R, 0603	EYANG	1	μF
C_{BAT1}	C0402X5R105J6R3CY	6.3V, X5R, 0402	EYANG	1	μF
	GRM155B31C105MA12	16V, X5R, 0402	Murata	1	μF
C_{BAT2}	C0603X5R226J6R3CY	6.3V, X5R, 0603	EYANG	22	μF
	GRM319R61C226ME15	16V, X5R, 1206	Murata	22	μF
C_{PMID1}& C_{PMID2}	GRM188B31C475MAAJ	16V, X5R, 0603	Murata	4.7	μF
	C0603X5R475J100CY	10V, X5R, 0603	EYANG	4.7	μF
R_{SNS}	RL0805FR-7W0R068L	1/4 W, ±1%, 0805	Yageo	68	mΩ
	PT0805FR-070R1L	1/8 W, ±1%, 0805	Yageo	100	mΩ

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INCREASE SYSTEM ROBUSTNESS AGAINST HOT-PLUG

A surge voltage would arise when charger is hot-plugged into a USB interface. The over-shoot depends on the relative value of the route resistance and the USB cable parasitic inductance as well as the USB output capacitance. To reduce over-shoot effectively, a snubber R_C or a TVS tube, or both of them is recommended to add to the USB power output port. Application circuit is shown below.

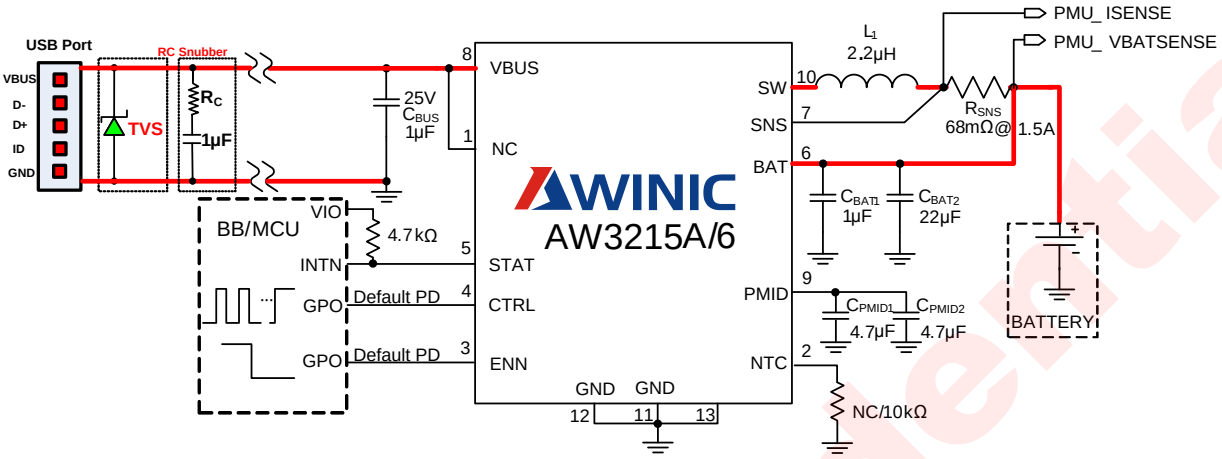

Figure 20 Application circuit of increasing robust against hot-plug for USB port

For the selection of TVS, a criterion as below can be used: the maximum clamp voltage of TVS when absorbs 1A peak-to-peak current should not exceed 8V, and a TVS of which part number is ESD9N5V-2/TR is recommended here.

The capacitor in series with R_C should not less than 1μF, and a X5R-0402 MLCC whose voltage rating no less than 25V is recommended.

For a typical RLC second-order system, if the resistance "R" across the USB cable to USB port capacitor satisfies a relationship of $R > 2 \times \sqrt{\frac{L}{C}}$, then the system would be over-damping, which makes the overshoot lower. Among the $R > 2 \times \sqrt{\frac{L}{C}}$, L represents the parasitic USB cable inductance, C represents the capacitance in series with R_C, and R consists of R_C+R_{ESR}, where R_{ESR} represents parasitic resistance from USB cable and the capacitor which is in series with R_C.

Whereas the system in the figure 20 has become a third-order system as the adding of C_{BUS}, which is close to the input port of AW3215A/6. For the third-order system, the relationship between R and L/C for over-damping is not linear any more. 1Ω is recommended as the optimized value of R_C, for typical condition of the capacitance in series with R_C ranges from 1μF and 10μF.

Both the TVS and R_C should be placed as close to the USB interface as possible.

Detailed test waveforms are shown as below in figure 21, whose test condition is a 5V AC adapter with a 1-meter USB cable hot-plugged into the USB port. As the results contrast shown in table 2, a TVS tube or snubber R_C added at the USB interface can reduce the VBUS overshoot effectively, as a consequence of which can increase the robustness of a system against hot-plug.

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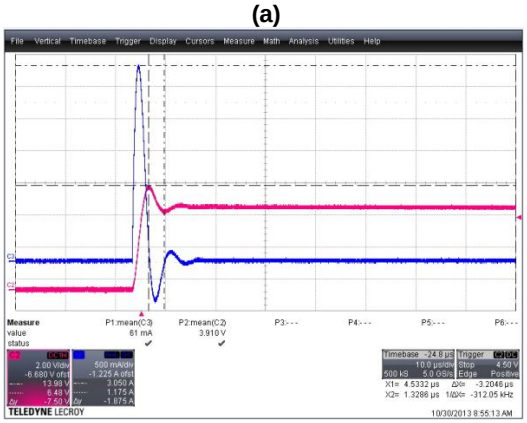
(a)

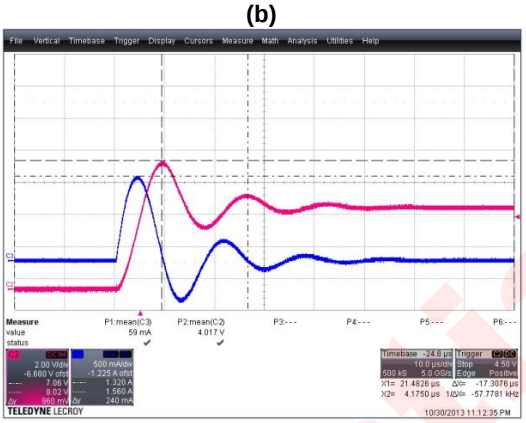


Red-VBUS，Blue- I_{IN}

V_{BUS_PEAK} = 6.5V, 10μs/div

5V adapter with original cable plugged in

(b)

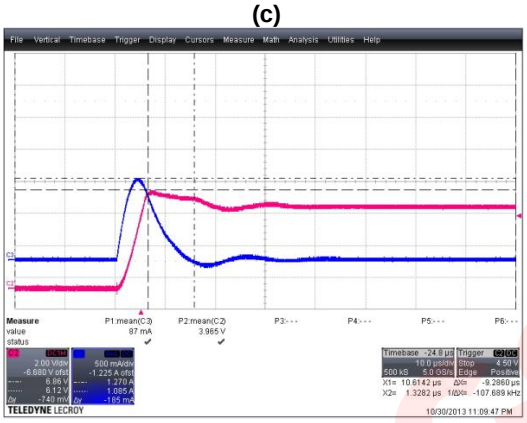


Red-VBUS，Blue- I_{IN}

V_{BUS_PEAK} = 8V, 10μs/div

Two 4.7μH inductors in series among the USB cable, hot plug

(c)

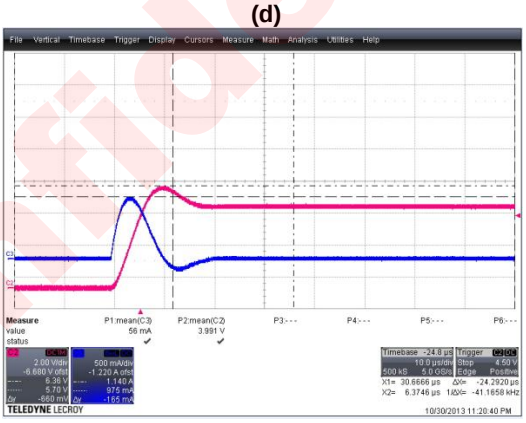


Red-VBUS，Blue- I_{IN}

V_{BUS_PEAK} = 6.12V, 10μs/div

Two 4.7μH inductors in series among the USB cable, and a TVS(V_C=5.4V) added at the USB port, hot plug

(d)



Red-VBUS，Blue- I_{IN}

V_{BUS_PEAK} = 6.36V, 10μs/div

Two 4.7μH inductors in series among the USB cable, and a 1Ω R_C in series with a 1μF capacitor added at the USB port, hot plug

Figure 21 The overshoot at the AW3215A/6 VBUS PIN when USB hot-plugged under different conditions

Table 2 Results contrast of Figure 21

Waveform	Test condition	VBUS_PEAK
(a)	5V adapter + original 1m USB cable	6.5V
(b)	5V adapter + 1m USB cable with two 4.7μH inductors in series	8V
(c)	5V adapter + 1m USB cable with two 4.7μH inductors in series + TVS (V_C=5.4V)	6.12V
(d)	5V adapter + 1m USB cable with two 4.7μH inductors in series + 1Ω R_C in series with 1μF capacitor	6.36V

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PCB LAYOUT CONSIDERATION

AW3215A/6 is a switch mode Buck charger chip, to obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

1、 All peripheral components should be placed as close to the chip as possible. C_{BUS1}、C_{BUS2}、C_{PMID1}、C_{PMID2}、C_{BAT1}、C_{BAT2}、L_1 should be close to VBUS、PMID、BAT、SW pins respectively. Avoid to connect device and chip pins with two different layers of copper, use the same layer of copper instead.

2、 PIN8 is the large current input of the chip, please route according to 1.5A rule, and the advised width is 60mil.

3、 The connection lines between the planes of C_{BUS1}、C_{BUS2}、C_{BAT1}、C_{BAT2} and respective chip pins should be as short and wide as possible, to reduce noise and EMI interference.

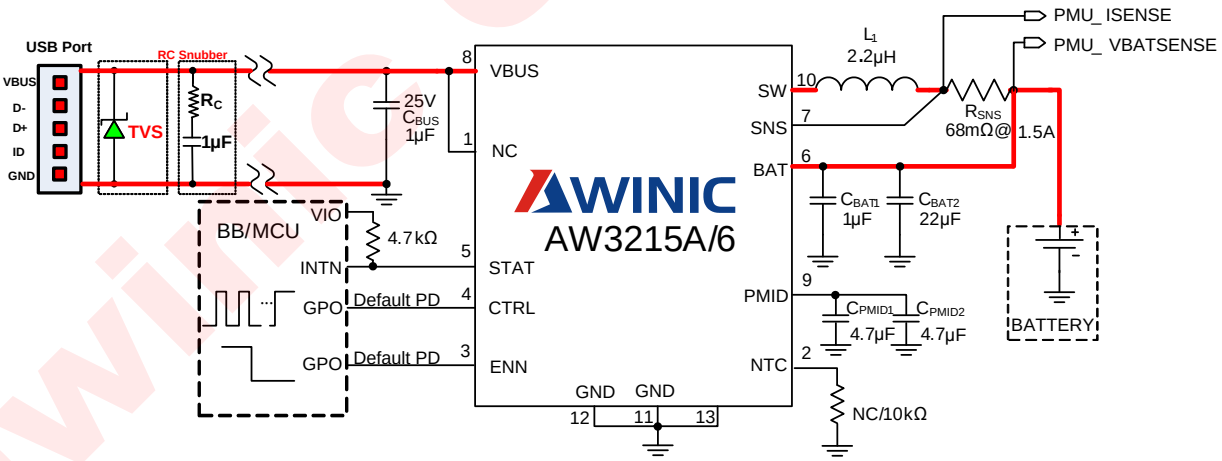
4、 The R_{SNS} leads should be connected directly to the corresponding chip pins, avoid the SENSE loop to overlap with large current path, ensuring the accuracy of sense.

5、 There will be strong switch-signal on the inductor while charging operation, to avoid interference, place the IC far from FM, RF and PA models.

6、 The exposed plane of chip and GND pins must be connected to the large-area ground layer of PCB directly, meanwhile place sufficient vias below the exposed plane. Thus we can decrease the thermal resistor on the board to optimize heat-diffusion performance.

7、 To achieve optimal large-current performance, the power path shown in red as the figure below must be widen. Please routing according to the 1.5A current rule, the advised width is 60mil (the BAT pin line can be routed as 14mil for the output current from BAT is 200mA).

8、 A surge voltage would arise when charger is hot-plugged into a USB interface. The over-shoot may damage the VBUS capacitor or chip. To avoid this risk, a snubber R_C or a TVS tube, or both of them is recommended to add to the USB power output port. See the section of “INCREASE SYSTEM ROBUSTNESS AGAINST HOT-PLUG” above for detail.



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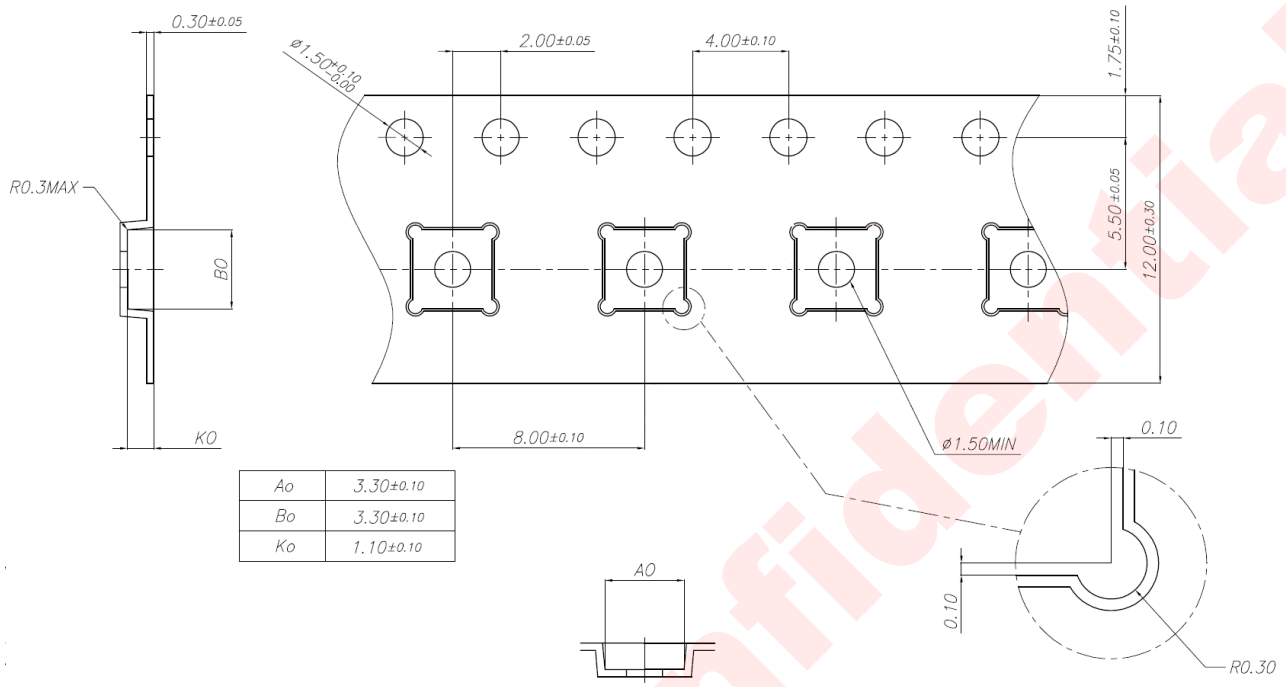
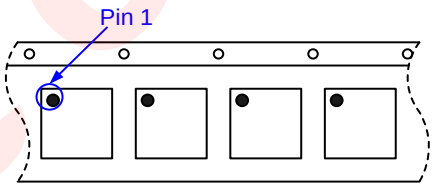
TAPE AND REEL INFORMATION

Carrier Tape



Ao	3.30±0.10
Bo	3.30±0.10
Ko	1.10±0.10

Pin 1 direction



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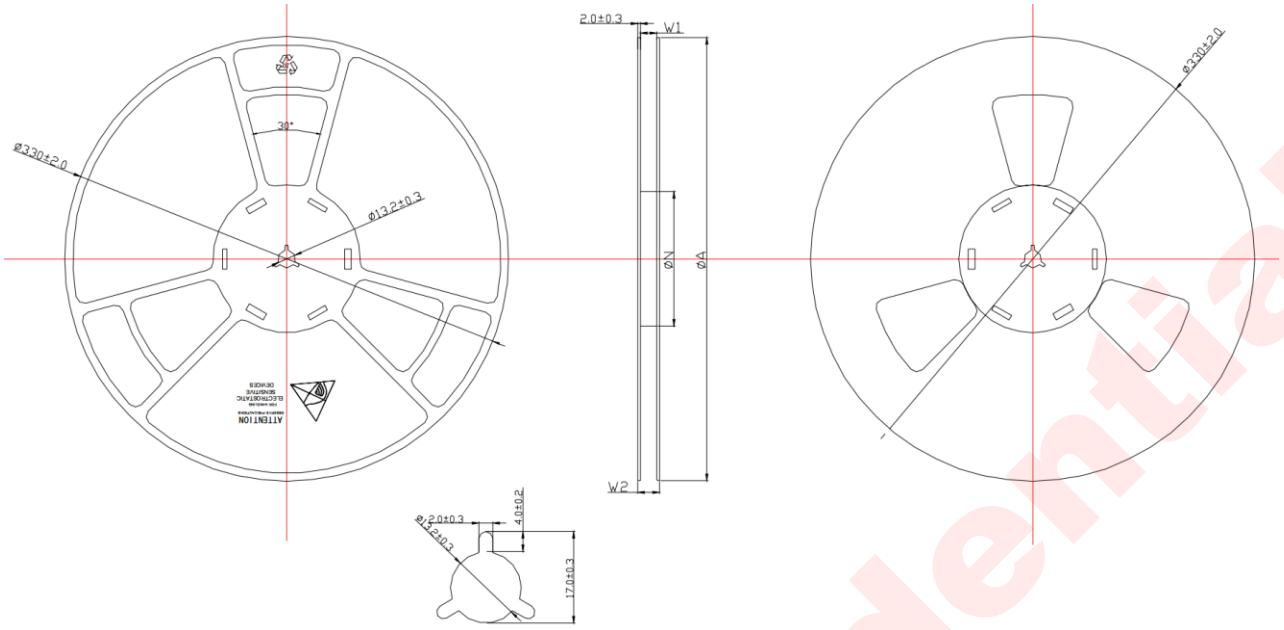
Reel



PRODUCT SPECIFICATIONS				
TYPE WIDTH	∅A	∅N	W1 (Min)	W2 (Max)
12MM	330±2.0	100±1.0	12.4	19.4
16mm	330±2.0	100±1.0	16.4	23.4
24MM	330±2.0	100±1.0	24.4	31.4
32MM	330±2.0	100±1.0	32.4	39.4
44MM	330±2.0	100±1.0	44.4	51.4

1、Unit：mm
2、Size tolerance is ±0.5mm unless noted

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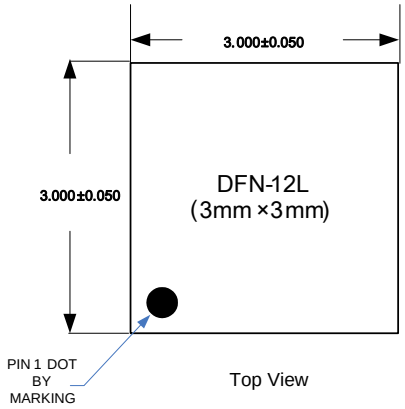
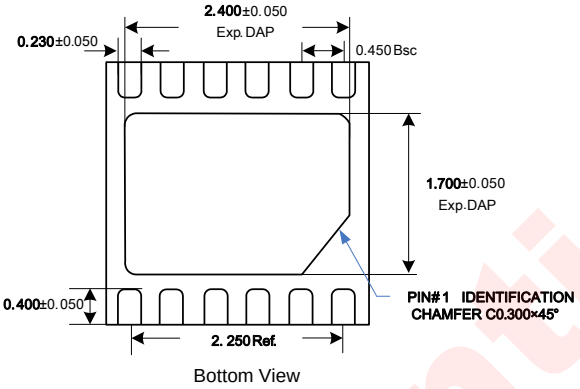
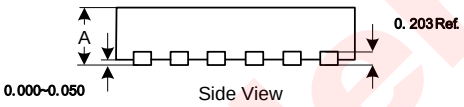
PACKAGE DESCRIPTION







		DFN-12L
A	MAX	0.800
	NOM	0.750
	MIN	0.700

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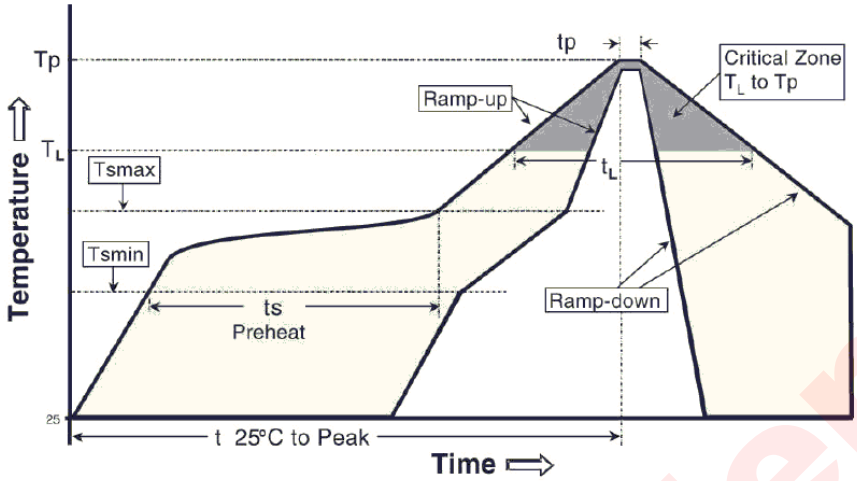
REFLOW



Reflow profile

Figure 22 Package Reflow Standard Profile

Table 3 Package Reflow Standard

Reflow condition	Sn-Pb eutectic assembly		Pb-Free assembly	
	Pkg. thickness ≥ 2.5 mm or Pkg. volume ≥ 350 mm^3	Pkg. thickness < 2.5 mm and Pkg. volume < 350 mm^3	Pkg. thickness ≥ 2.5 mm or Pkg. volume ≥ 350 mm^3	Pkg. thickness < 2.5 mm and Pkg. volume < 350 mm^3
Average ramp-up rate (Liquidus Temperature (T_L) to Peak)	3 °C/second max.		3 °C/second max.	
Preheat - Temperature Min ($T_{s(min)}$) - Temperature Max ($T_{s(max)}$) - Time (min to max) (t_s)	 100 °C 150 °C 60-120 seconds		 150 °C 200 °C 60-180 seconds	
$T_{s(max)}$ to T_L - Ramp-up Rate			3 °C/second max.	
Time maintained above: - Temperature (T_L) - Time (t_L)	 183 °C 60-150 seconds		 217 °C 60-150 seconds	
Peak Temperature (T_p)	225 +0/-5 °C	240 +0/-5 °C	245 +0/-5 °C	250 +0/-5 °C
Time within 5 °C of actual Peak Temperature (t_p)	10-30 seconds	10-30 seconds	10-30 seconds	20-40 seconds
Ramp-down Rate	6 °C/second max.		6 °C/second max.	
Time 25 °C to Peak Temperature	6 minutes max.		8 minutes max.	

NOTE 1: All data are compared with the package-top temperature, measured on the package surface;

NOTE 2: AW3215A/6 adopted the Pb-Free assembly.

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REVISION HISTORY

Vision	Date	Change Record
V1.0	May 2014	Officially Released
V1.1	May 2014	1、 Added a page after the first page, among which translated the first page into English. 2、 Added the footer. The first page with Chinese, the left ones with English. 3、 Page 24, exchanged the DCR/I_{SAT} data of the two recommended inductors which were reverse. 4、 Changed the non-bold figure / table titles into bold. 5、 Added a figure of typical application circuit on the first page. 6、 Added a trademark right claim on the first page： *All trademarks are the property of their respective owners.* 7、 Added Related Parts. 8、 Changed Disclaimer. 9、 Added a Table of Figures at the beginning of Typical Characteristics, and set all the figures into hyperlink. 10、 Added a Recommended Component Table for the typical application circuit after the first page. 11、 Moved the Reflow to the end of the document.
V1.2	July 2014	1、Modified the format according to the latest Awinic datasheet template.
V1.2.1	April 2015	1、 Corrected the Carrier Tape information, and refreshed the Reel information as well

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RELATED PARTS

Part No.	Description	Comments
AW3110 STR	30V, 3A, PNP Low V_{CESAT} BJT	32V V_{CE} Rating, 0.35V Max V_{CESAT}, 3W Power Dissipation Rating, SOT89-3L
AW3110 DNR		32V V_{CE} Rating, 0.35V Max V_{CESAT}, 3W Power Dissipation Rating, DFN3×2-8L
AW3112 DNR	30V, 3A, PNP Low V_{CESAT} BJT Integration with 20V Trench NMOSFET	Integrated with NMOS switch, 32V V_{CE} Rating, 0.35V Max V_{CESAT}, 1.5W Power Dissipation Rating, DFN2×2-6L
AW3206 DNR	Li-ion Battery Charger Integrated with Protective PMOSFET	15V Input Rating, K-Charge™ Thermal Regulation, DFN2×2-8L
AW3208 DNR	LDO mode Li-ion Battery Charger Integrated with Protective PMOSFET	10.5V OVP, 15V Input Rating, K-Charge™ Thermal Regulation, LDO output mode, DFN2×2-8L
AW3282 DNR	LDO mode Li-ion Battery Charge Protector	15V Input Rating, K-Charge™ Thermal Regulation, LDO output mode, DFN2×2-8L
AW3210A DNR	1A Li-ion Battery Charger Integrated with Protective PMOSFET	Up to 1A Charge Current, 15V Input Rating, K-Charge™ Thermal Regulation, DFN3×3-10L
AW3215A DNR	1.5A Switch-mode Single Cell Li-ion Battery Charger	Max 88% Efficient Switch-mode Conversion, 1.5A Max Charge Current, 18V Input Rating, K-DPM™ Maximizes Available Power from USB Port/Wall Adapter, K-TEMP™ Thermal Regulation, DFN3×3-12L
AW3216 DNR		

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