Applications Note:AN_SY8201

High Efficiency Fast Response, 1A, 27V Input Synchronous Step Down Regulator

General Description

SY8201 develops high efficiency synchronous step-down DC-DC converter capable of delivering 1A . SY8201 operates over a wide input voltage range from 4.5V to 27V and integrate main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

SY8201 adopts the instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads. In addition, it operates at pseudo-constant frequency of 500 kHz under heavy load conditions to minimize the size of inductor and capacitor.

Ordering Information

SY8201□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY8201ABC	SOT23-6	--

Features

- Low $R_{DS(ON)}$ for internal switches (top/bottom):350/150 mΩ
- 4.5-27V input voltage range
- Instant PWM architecture to achieve fast transient responses Internal softstart limits the inrush current
- 2% 0.6V reference
- RoHS Compliant and Halogen Free
- Compact package: SOT23-6

Applications

- Set Top Box
- Portable TV
- Access Point Router
- DSL Modem
- LCD TV

Typical Applications

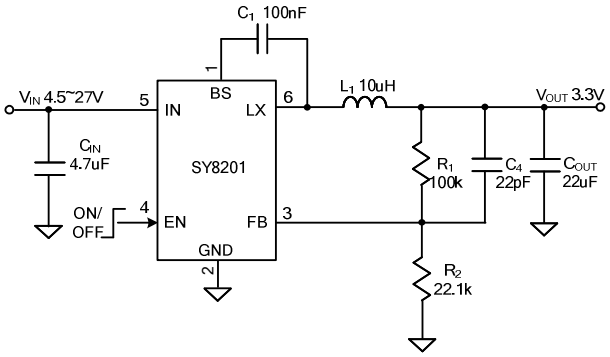


Figure 1. Schematic Diagram

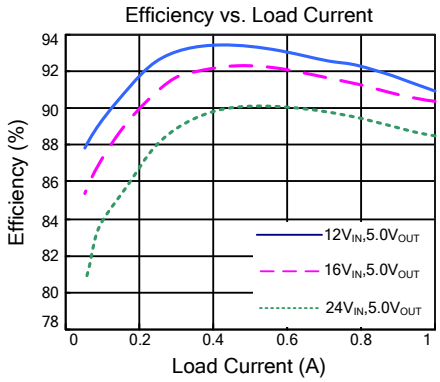
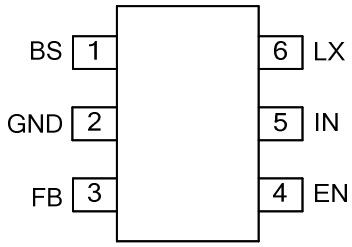


Figure 2. Efficiency vs Load Current

Pinout (top view)



(SOT23-6)

Top Mark: **EN*xyz***, (Device code: EN; ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
BS	1	Boot-Strap Pin. Supply high side gate driver. Decouple this pin to LX pin with 0.1uF ceramic cap.
GND	2	Ground pin
FB	3	Output Feedback Pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: Vout=0.6*(1+R1/R2)
EN	4	Enable control. Pull high to turn on. Do not float.
IN	5	Power input pin.
LX	6	Inductor pin. Connect this pin to the switching node of inductor

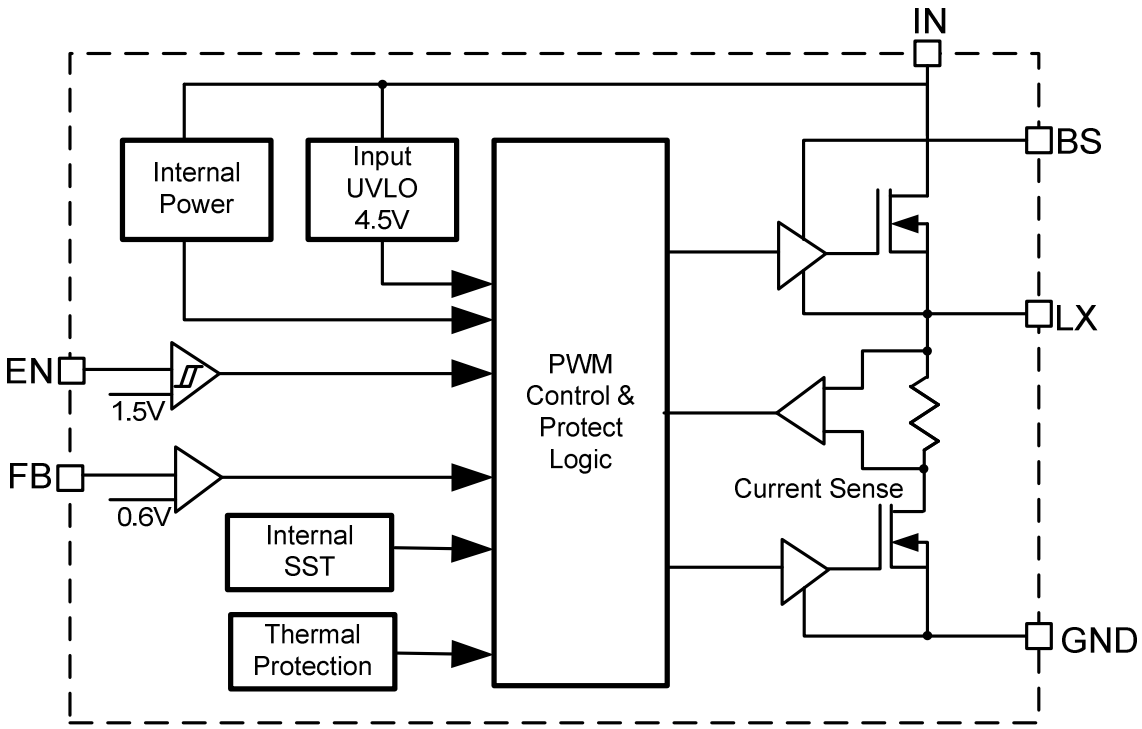
Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- 30V
LX, EN Voltage---------- V_{IN} + 0.3V
FB, BS-LX Voltage---------- 4V
Power Dissipation, P_D @ T_A = 25°C SOT23-6, ---------- 0.6W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 170°C/W
θ_{JC} ---------- 130°C/W
Junction Temperature Range ---------- ---------- 125°C
Lead Temperature (Soldering, 10 sec.)---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
Dynamic LX voltage in 50ns duration ----------IN+3V to GND-4V

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 4.5V to 27V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Block Diagram



Electrical Characteristics

(V_{IN} = 12V, V_{OUT} = 1.2V, L = 2.2uH, C_{OUT} = 10uF, T_A = 25°C, I_{OUT} = 1A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5		27	V
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}=V_{REF}×105%		400		μA
Shutdown Current	I_{SHDN}	EN=0		5	10	μA
Feedback Reference Voltage	V_{REF}		0.588	0.6	0.612	V
FB Input Current	I_{FB}	V_{FB}=V_{IN}	-50		50	nA
Top FET RON	$R_{DS(ON)1}$			0.35		Ω
Bottom FET RON	$R_{DS(ON)2}$			0.15		Ω
Bottom FET Valley Current Limit	I_{LIM}		1.5			A
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
Input UVLO Threshold	V_{UVLO}				4.5	V
UVLO Hysteresis	V_{HYS}			0.4		V
On Time	T_{ON}	V_{IN} = 12V ,V_{OUT}=1.2V, I_{OUT} = 1A		200		ns
Min ON Time				50		ns
Min Off Time				100		ns
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C

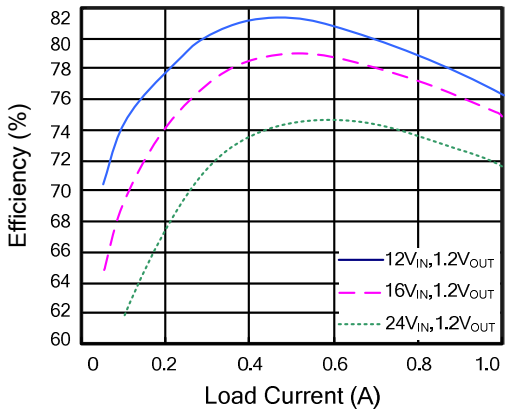
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θJA is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Pin 2 of SOT23-6 packages is the case position for θJC measurement. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane

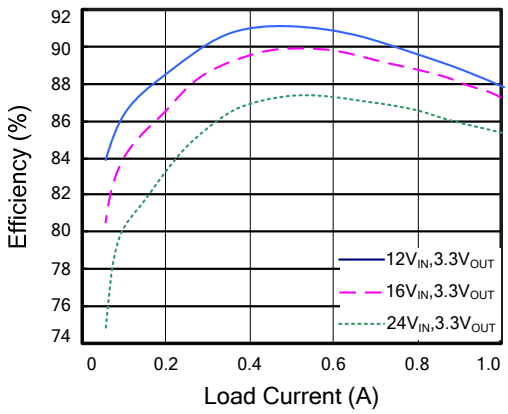
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

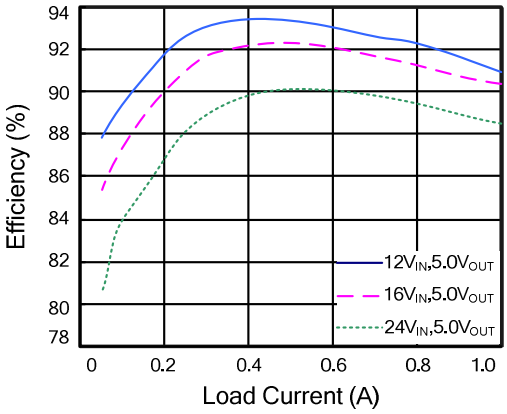
Efficiency vs. Load Current



Efficiency vs. Load Current

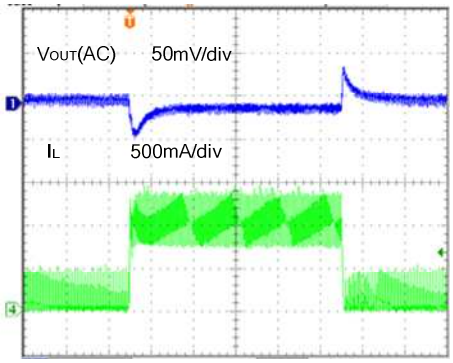


Efficiency vs. Load Current



Load Transient

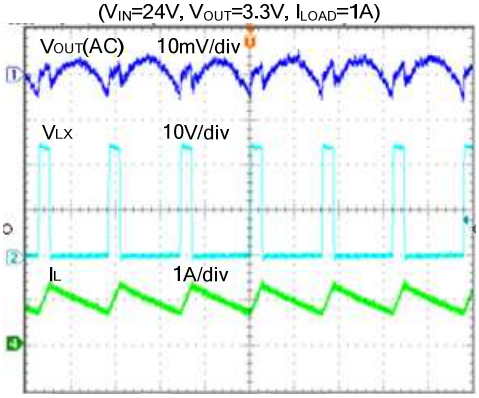
(VIN=24V, VOUT=3.3V, ILOAD=0.1-1A)



Time (40us/div)

Output Ripple

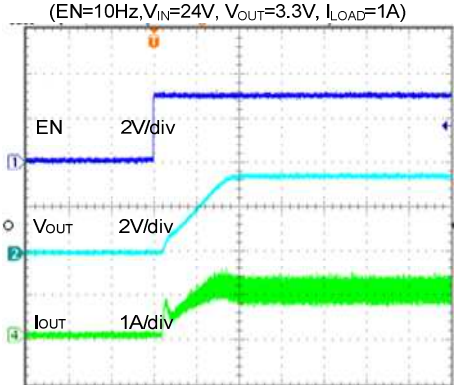
(VIN=24V, VOUT=3.3V, ILOAD=1A)



Time (1us/div)

Startup

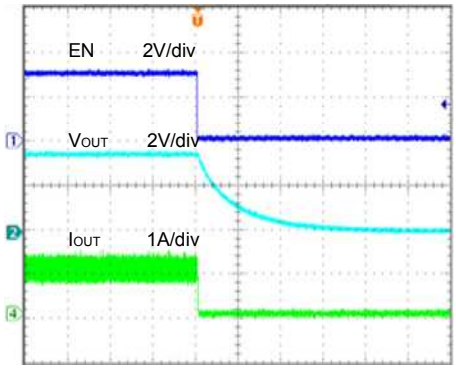
(EN=10Hz,VIN=24V, VOUT=3.3V, ILOAD=1A)



Time (200us/div)

Shutdown

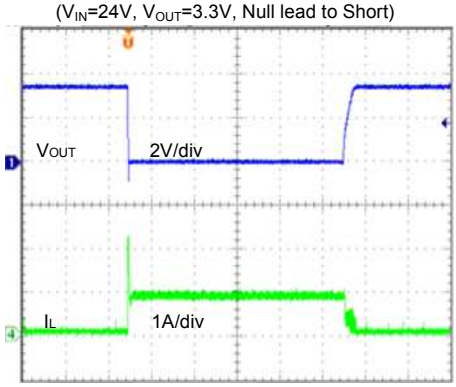
(EN=10Hz,V_{IN}=24V, V_{OUT}=3.3V, I_{LOAD}=1A)



Time (100us/div)

Short Circuit Protection

(V_{IN}=24V, V_{OUT}=3.3V, Null lead to Short)



Time (1ms/div)

Operation

SY8201 is a synchronous buck regulator IC that integrates the PWM control, top and bottom switches on the same die to minimize the switching transition loss and conduction loss. With ultra low $R_{DS(ON)}$ power switches and proprietary PWM control, this regulator IC can achieve the highest efficiency and the highest switch frequency simultaneously to minimize the external inductor and capacitor size, and thus achieving the minimum solution footprint.

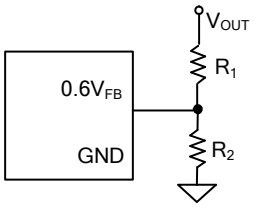
Applications Information

Because of the high integration in the SY8201 IC, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L and feedback resistors (R_1 and R_2) need to be selected for the targeted applications specifications.

Feedback resistor dividers R_1 and R_2:

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If Vout is 3.3V, R_1=100k is chosen, then using following equation, R_2 can be calculated to be 22.1k:

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1 .$$



Input capacitor C_{IN}:

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \cdot \sqrt{D(1-D)} \cdot$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins. In this case, a 4.7uF low ESR ceramic capacitor is recommended.

Output capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor greater than 22uF capacitance.

Output inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

where Fsw is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY8201 regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mΩ to achieve a good overall efficiency.

Soft-start

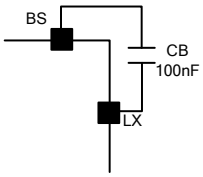
The SY8201 has a built-in soft-start to control the rise rate of the output voltage and limit the input current surge during IC start-up. The typical soft-start time is 300us.

Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During shutdown mode, the SY8201 shutdown current drops to lower than 5uA, Driving the EN pin high (>1.5V) will turn on the IC again.

External Bootstrap Cap

This capacitor provides the gate driver voltage for internal high side MOSEFET. A 100nF low ESR ceramic capacitor connected between BS pin and LX pin is recommended.



Load Transient Considerations:

The SY8201 regulator IC integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a 22pF ceramic cap in parallel with R1 may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.

Layout Design:

The layout design of SY8201 regulator is relatively simple. For the best efficiency and minimum noise problem, we should place the following components close to the IC: CIN, L, R1 and R2.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

4) The components R_1 and R_2, and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

Design Specifications

Input Voltage (V)	Output Current (A)	Output Voltage (V)	Test conditions
4.5-27	0~1	3.3	K_1, close

Schematic

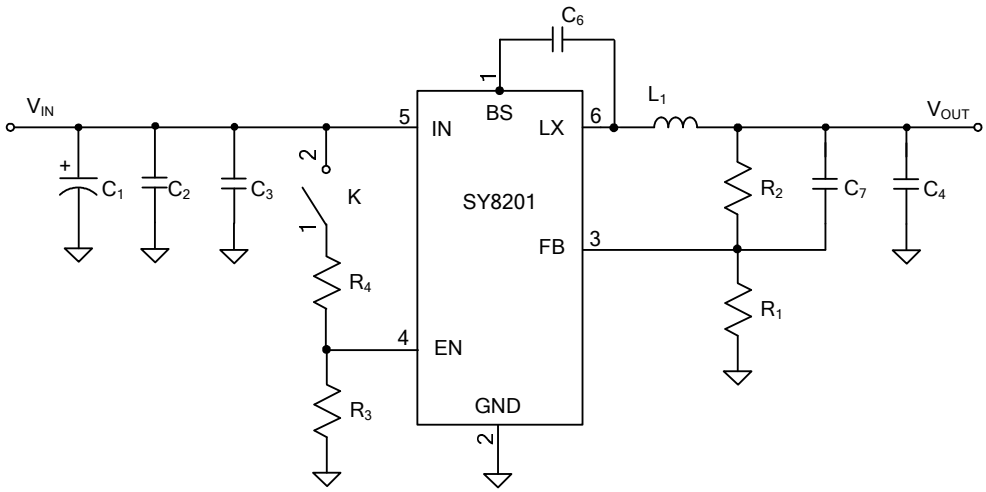


Figure1. Schematic Diagram

Table 1. Recommended Component Selection

V_{OUT}(V)	R_1(kΩ)	R_2(kΩ)	C_4 (uF)	L_1 (uH)
1.2	100	100	22	4.7
3.3	22.1	100	22	10
5.0	13.7	100	22	15

Quick Start Guide (Refer to Figure 3)

1. Connect the output load to V_{OUT} and GND output connectors. Preset the load current to between 0.1A and 1.0A.
2. Preset the input supply to a voltage between 4.5V and 27V. Turn the supply off. Connect the input supply to V_{IN} and GND input connectors.
3. Short jumper K_1. Change R_1 to achieve the desired output voltage. See Table 1.
4. Turn on the input supply and measure the output voltage.

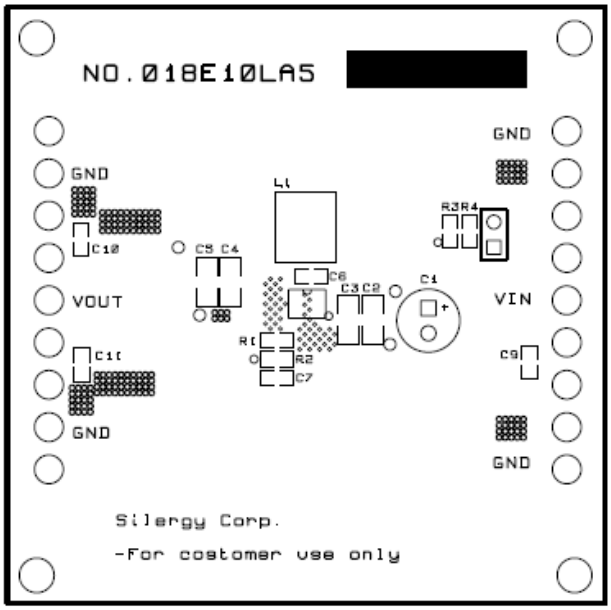
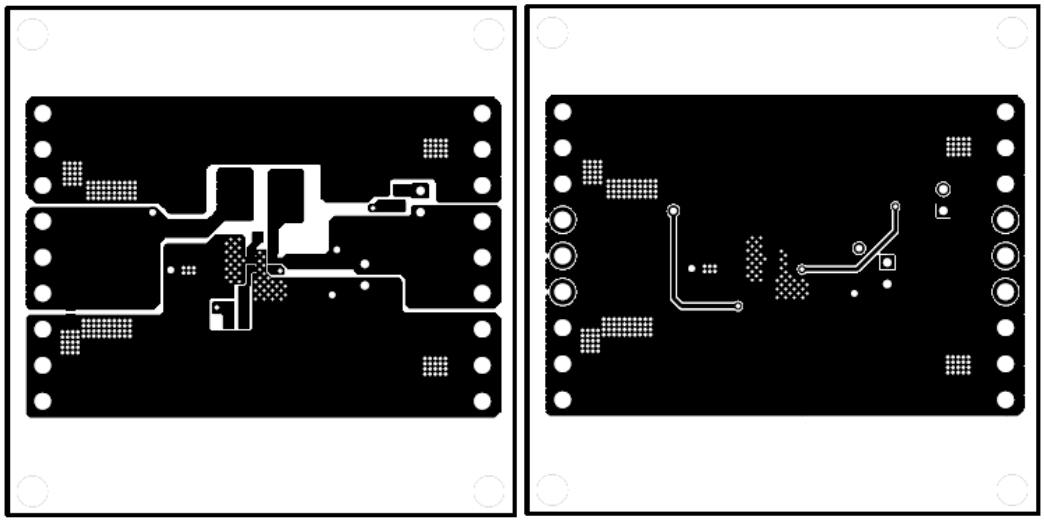


Figure 3. Top Silkscreen

PCB Layout



(a) (b)

Figure 4. PCB Layout Plots: (a) top layer, (b) bottom layer

BOM List

Reference Designator	Description	Part Number	Manufacturer
U_1	1.0A,27V Input Sync Buck	SY8201ABC	
L_1	10uH/2.5A inductor	VLC6045-100M	TDK
C_1	47uF/50V (electrolytic capacitor)		
C_2	2.2uF/50V/X5R,1206	C3216X5R1H225K	TDK
C_3	2.2uF/50V/X5R,1206	C3216X5R1H225K	TDK
C_4	22uF/16V/X5R,1206	GRM31CR61C226M	muRata
C_6	100nF/25V/X5R,0603	GRM188R61E104K	muRata
C_7	22pF/50V/C0G, 0603	GRM185C1H220J	muRata
R_1	22.1k Ω, 1%, 0603		
R_2	100k Ω, 1%, 0603		
R_3	1M Ω, 0603		
R_4	10k Ω, 0603		

Output Voltage Ripple Test

A proper output ripple measurement should be done according to Figure 5 setup. Output voltage ripple should be measured across the output ceramic cap near the IC.

1. Remove the ground clip and head of the probe. Wind thin wires around the ground ring of the probe. Solder the end of the ground ring wire to the negative node of the C_4. Touch the probe tip to the positive node of the C_4. Refer to Figure.5.
2. Minimize the loop formed by C_4 terminals, probe tip and ground ring.
3. Change the probing direction to decouple the electromagnetic noise generated from the nearby buck inductor (Refer to Figure.5).

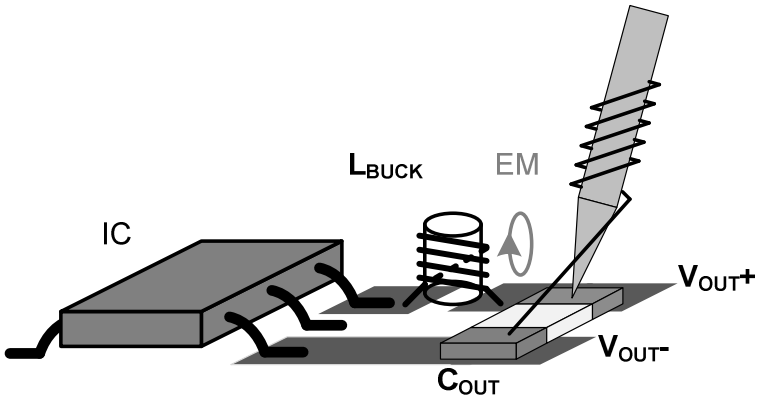
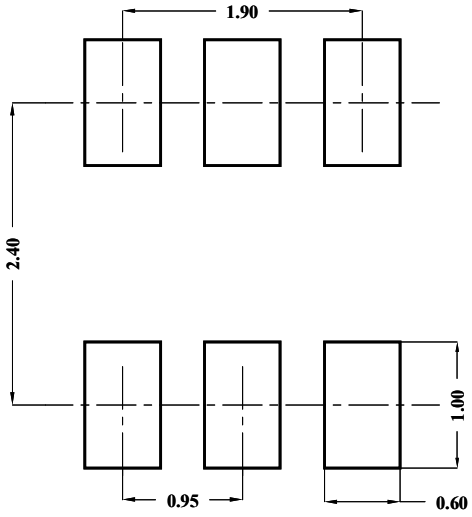
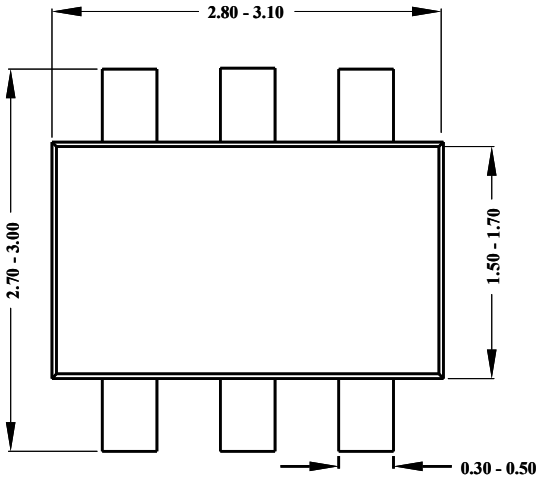


Figure.5 Recommended way to measure the output voltage ripple

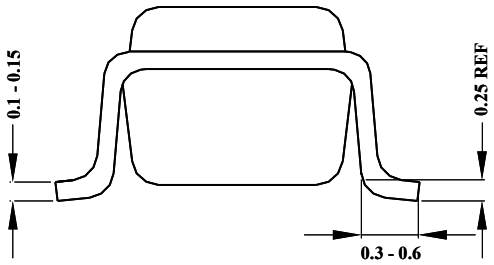
SOT23-6 Package Outline & PCB layout

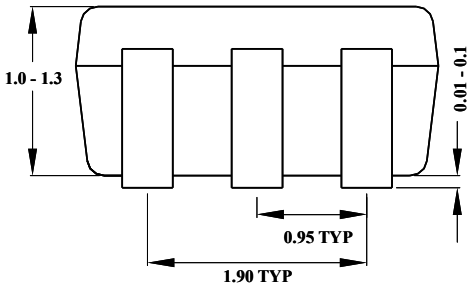


Recommended Pad Layout



Top View

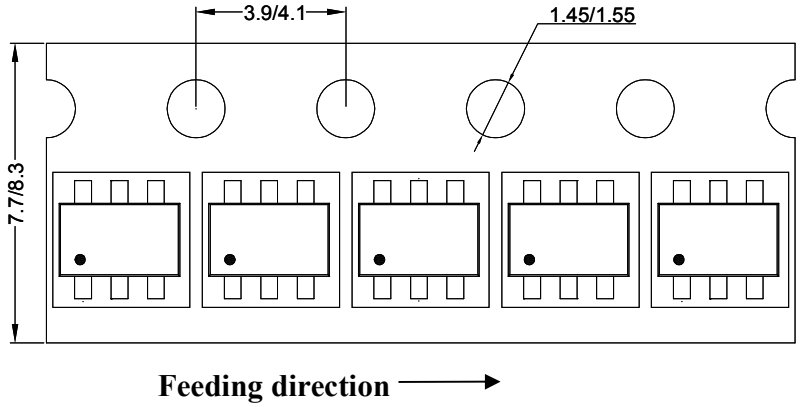




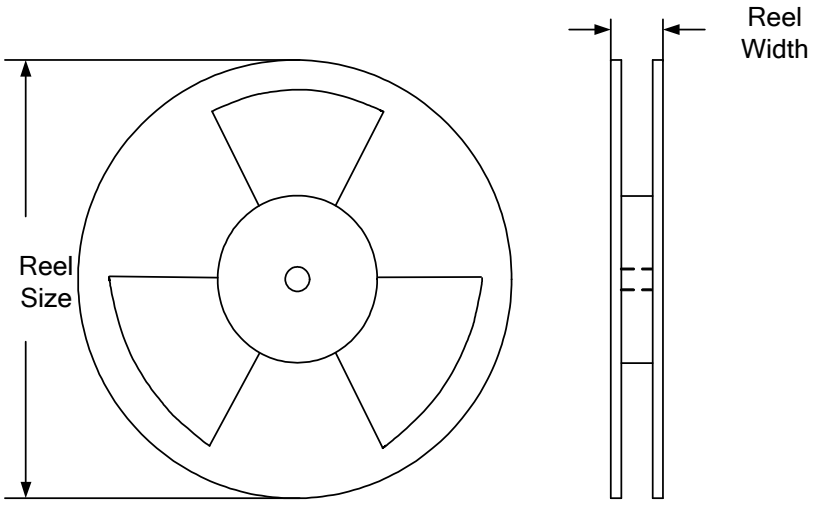
Notes: **All dimension in MM**
All dimension do not include mold flash & metal burr

Taping & Reel Specification

1. SOT23-6 taping orientation



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Reel width(mm)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-6	8	4	7"	8.4	280	160	3000

3. Others: NA