my-d™ move lean

SLE 66R01L

Intelligent 512 bit EEPROM with Contactless Interface compliant to ISO/IEC 14443 Type A and support of NFC Forum™ Type 2 Tag Operation

Preliminary Data Sheet

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Features

Intelligent 512 bit EEPROM with Contactless Interface compliant to ISO/IEC 14443 Type A and support of NFC Forum™ Type 2 Tag Operation

Contactless Interface

- Physical Interface and Anticollision compliant to ISO/IEC 14443 Type A
  - Contactless transmission of data and supply energy
  - Operation frequency 13.56 MHz
  - Data rate 106 kbit/s in both direction
- Read and Write Distance up to 10 cm (influenced by external circuitry i.e. reader and inlay design)

64 byte EEPROM

- Organized in 16 blocks of 4 bytes each
- 48 bytes freely programmable User Memory
- 16 bytes of Service Area reserved for UID, Configuration, Locking Bytes and OTP Block
- Data Retention minimum 5 years[1)]
- Endurance minimum 10,000 erase/write cycles[1)]
- Programming time per block < 4 ms

Privacy Features

- Double Size UID (7 byte) according to ISO/IEC 14443 Type A [2)]
- One Time Programmable (OTP) memory area[2)]
- Locking mechanism for each block[2)]
- Block Lock mechanism[2)]

Data Protection

- Data Integrity supported by 16 bit CRC, parity bit, command length check
- Anti-tearing mechanism for OTP

NFC Forum™ Operation

- Compliant to NFC Forum™ Type 2 Tag Operation
- Support of Static Memory Structure according to NFC Forum™ Type 2 Tag Operation

Electrical Characteristics

- On-Chip capacitance 17 pF $\pm$ 5%
- ESD protection minimum 2 kV
- Ambient Temperature -25℃ … +70℃ (for the chip)

1) Values are temperature dependent
2) Compliant to NFC Forum™ Type 2 Tag operation

1 Ordering and packaging information

Table 1 Ordering information

Type	Package	Total Memory / User Memory	Ordering code
SLE 66R01L C	wafer sawn / unsawn	64 / 48 bytes	on request
SLE 66R01L NB	NiAu Bumped (sawn wafer)		on request

For more ordering information about the form of delivery please contact your local Infineon sales office.

Pin description

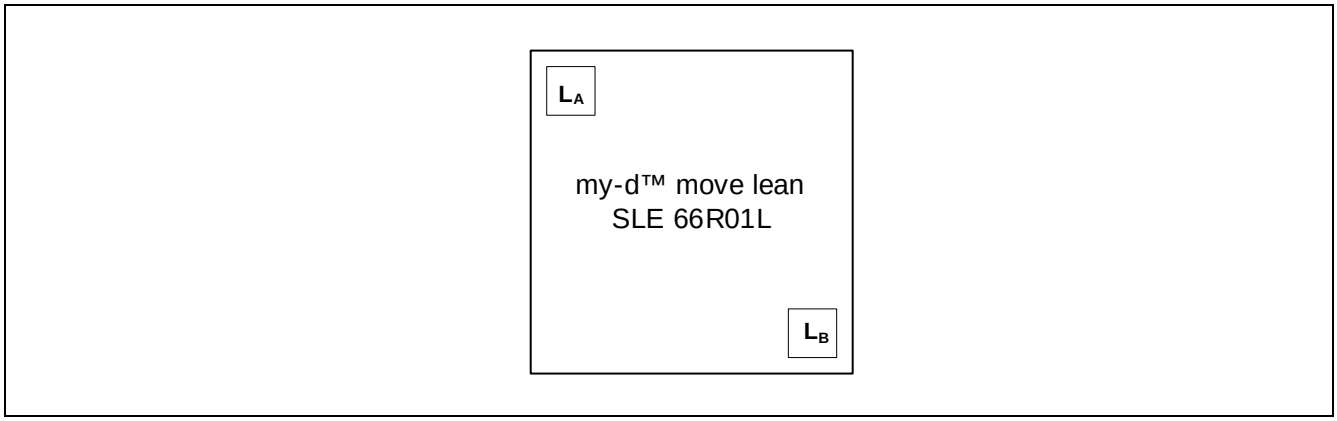

Figure 1 Pin configuration die

Table 2 Pin description and function

Symbol	Function
L_A	Antenna Connection
L_B	Antenna Connection

2 Scope of my-d™ move lean

The SLE 66R01L is part of the Infineon my-d™ product family and supports Infineon's transport and ticketing strategy. It is compliant to ISO/IEC 14443 Type A, to ISO/IEC 14443-3 Type A and to NFC Forum™ Type 2 Tag Operation. The SLE 66R01L is designed for cost optimized transport applications and its implemented command set eases the usage of the SLE 66R01L in existing applications and infrastructures.

Typical ticketing transactions can be operated in less than 100 ms.

2.1 Application Description

The SLE 66R01L is designed to address the needs of a public transport system for a single fare or limited use ticket. Further applications are event ticketing such as access control to waterparks, leisure parks, football stadiums or concert halls.

2.2 Functional Block Diagram

The SLE 66R01L is made up of an EEPROM memory unit, an analog interface for contactless operation, a data transmission path and a control unit. The following diagram shows the main blocks of the SLE 66R01L.

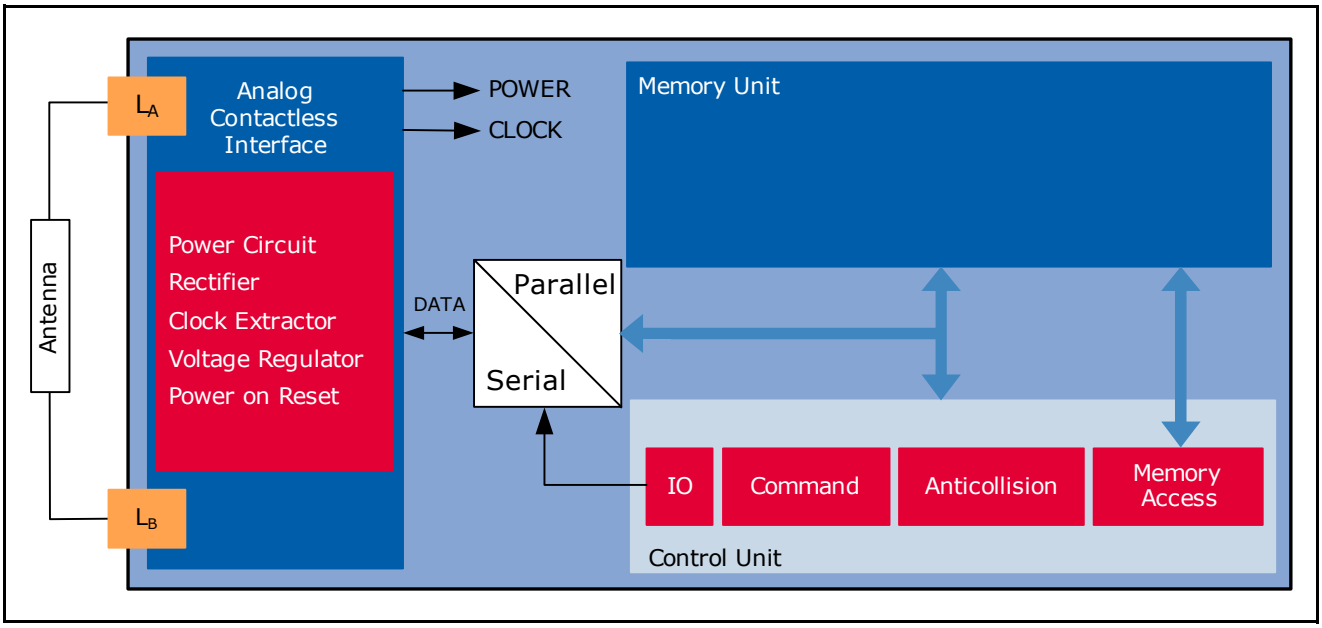

Figure 2 Block Diagram of the SLE 66R01L

The SLE 66R01L comprises the following three parts:

- **Analog Contactless Interface**
  - The Analog Contactless Interface comprises the voltage rectifier, voltage regulator and system clock to supply the IC with appropriate power. Additionally the data stream is modulated and demodulated.
- **Memory Unit**
  - The Memory Unit consists of 16 user blocks of 4 bytes each.
- **Control Unit**
  - The Control Unit decodes and executes all commands. Additionally the control unit is responsible for the correct anticollision flow.

2.3 Memory Principle

The total amount of addressable memory is 64 bytes.

It comprises

- 48 bytes of User Area reserved for User Data
- 16 bytes of Service Area reserved for UID, Configuration, Locking Bytes and OTP

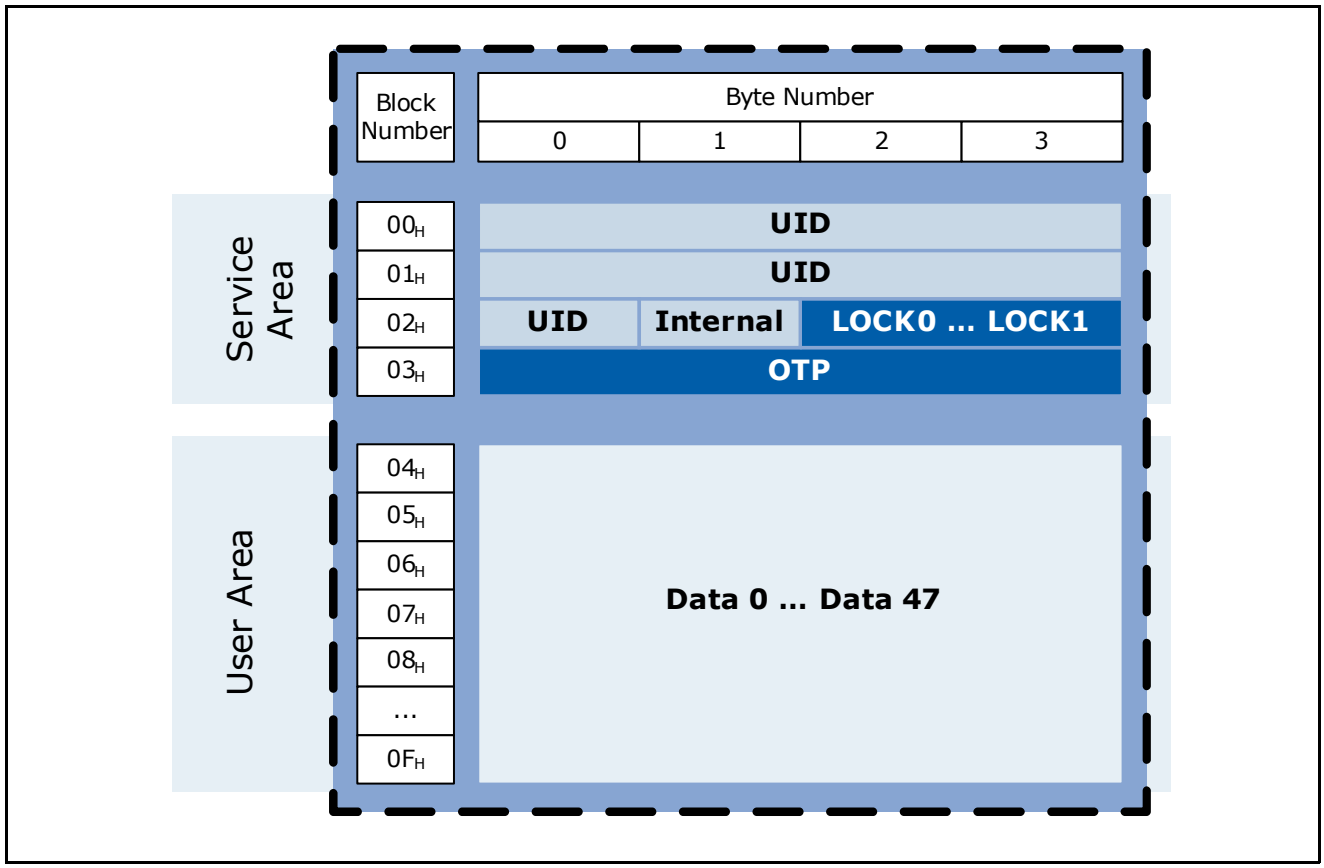

Figure 3 SLE 66R01L memory principle

2.4 Memory Principle for NFC Forum™ Type 2 Tag

The memory organization of the SLE 66R01L is configurable according to the NFC Forum™ Type 2 Tag Operation specification.

The following figure illustrates an example of the SLE 66R01L as a NFC Forum™ Type 2 Tag compatible chip and enables the memory access with NFC Forum™ Type 2 Tag commands.

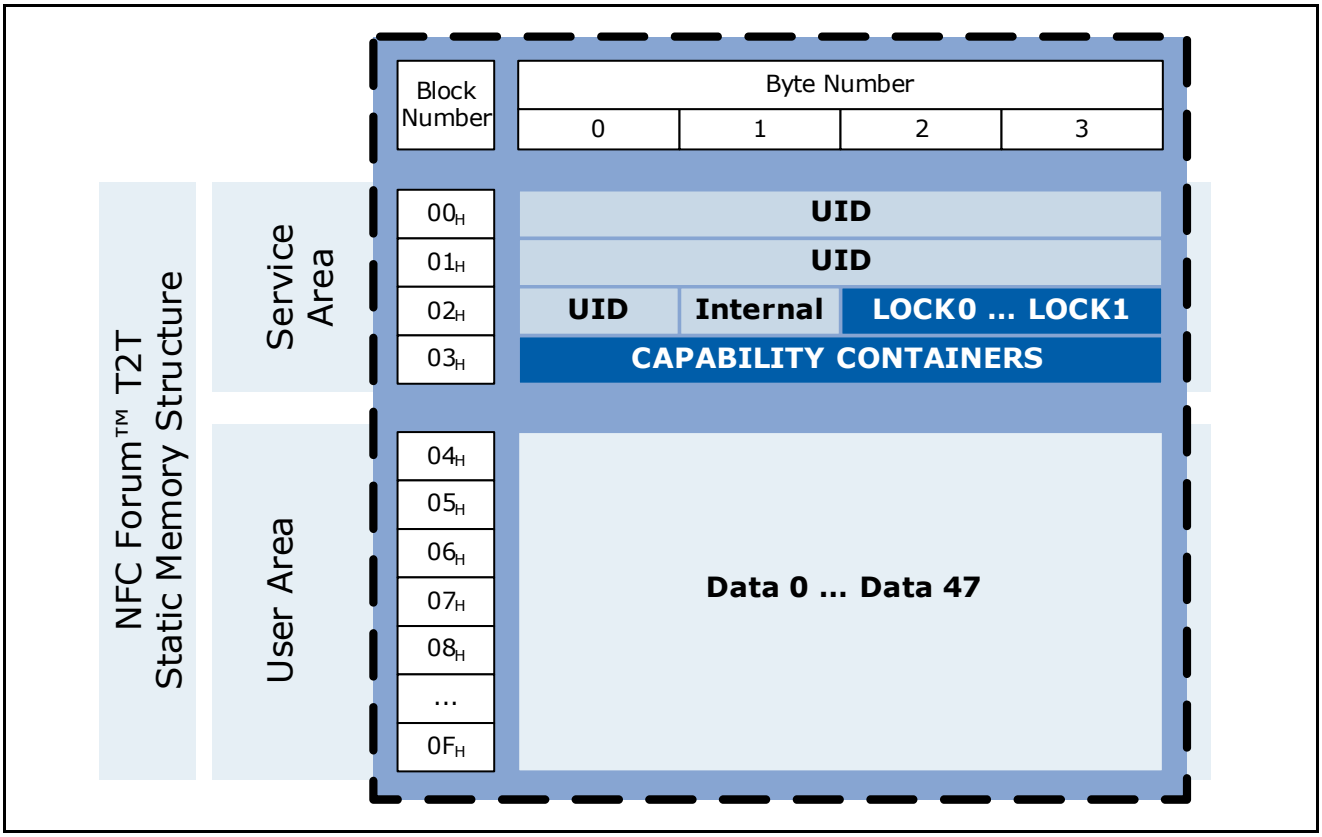

Figure 4 Memory structure for NFC Forum™ Type 2 Tag

2.5 System Overview

The system consists of a host system, one or more SLE 66R01L tags or other ISO/IEC 14443 Type A compliant cards and an ISO/IEC 14443 Type A compatible contactless reader. Alternatively, since the SLE 66R01L can be configured to hold a NFC Forum™ Type 2 Tag memory structure, a NFC Forum™ device in card reader/writer mode can be used to operate the chip.

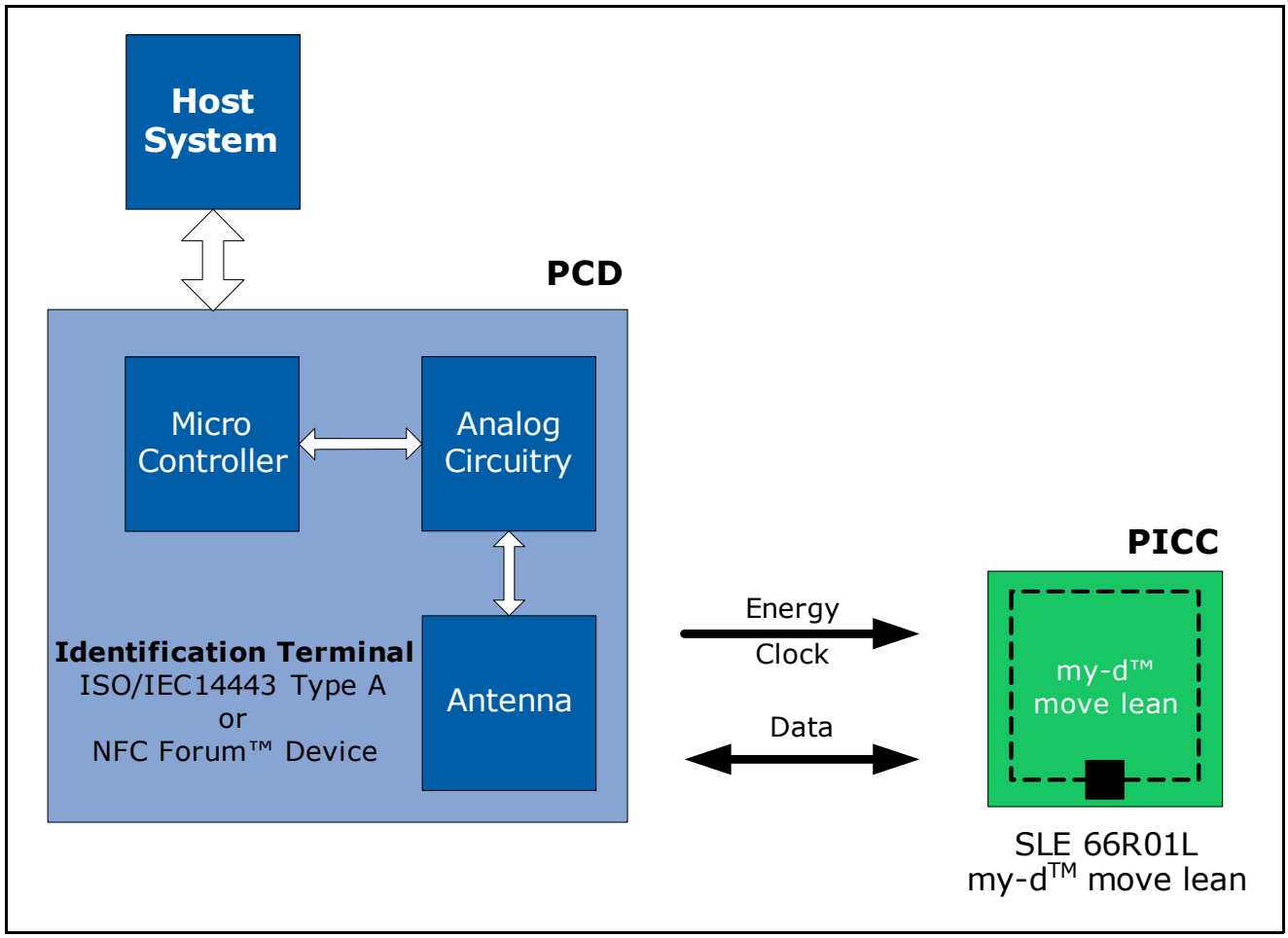

Figure 5 SLE 66R01L Contactless System Overview

2.6 UID Coding

To identify a SLE 66R01L chip the manufacturer code and a chip family identifier are coded into the UID as described in the **Table 3**. The chip family identifier can be used to determine the basic command set for the chip.

Table 3 UID Coding

UID Field	Value	Description
uid0	05_H	IC Manufacturer Code according to ISO/IEC 7816-6
uid1	$7x_H$	Chip Family Identifier Higher Nibble: 0111_b identifies SLE 66R01L Lower Nibble: part of the UID number

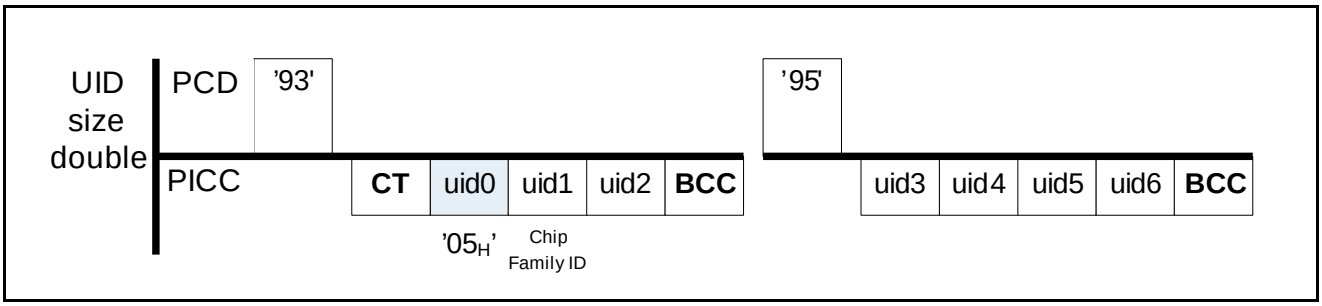

Figure 6 SLE 66R01L Double Size UID

2.7 Supported Standards

the SLE 66R01L supports the following standards:

- ISO/IEC 14443 Type A Parts 1, 2 and 3 tested according to ISO/IEC 10373-6 (PICC Test & Validation)
- ISO/IEC 14443-3 Type A
- NFC Forum™ Type 2 Tag Operation

2.8 Command Set

The SLE 66R01L is compliant to the ISO/IEC 14443 Type A standard.

A set of standard ISO/IEC 14443 Type A Part 3 commands is implemented to operate the chip.

Additionally NFC Forum™ Type 2 Tag commands and a my-d™ move lean specific command set is implemented.

3 Memory Organization

The total amount of user memory is 64 bytes and is organized in 4 byte blocks. It comprises:

- 48 bytes for user data
- 16 bytes for UID, OTP, locking information, IC configuration and manufacturer information.

The following figure shows the memory structure of the SLE 66R01L chip.

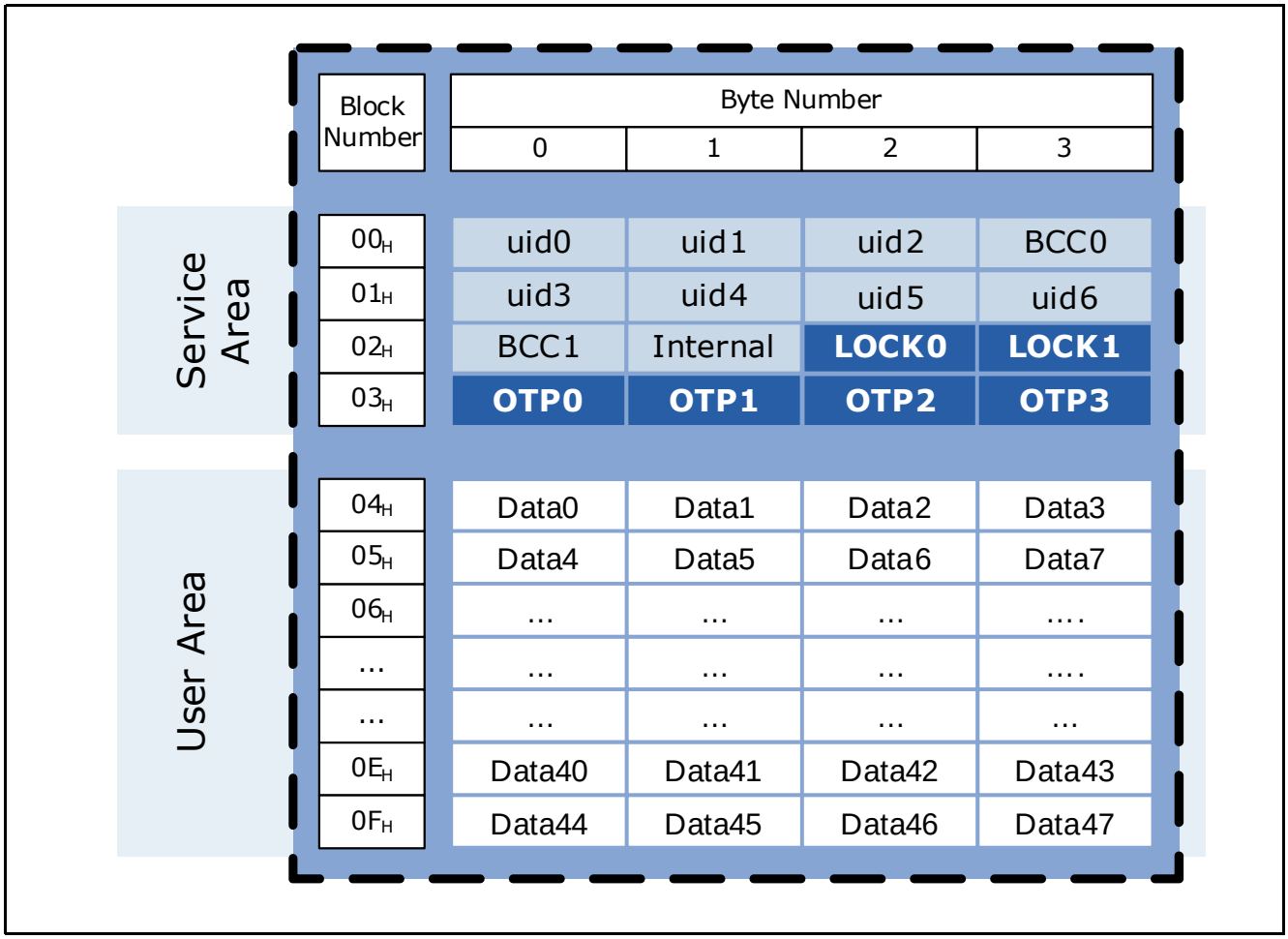

Figure 7 my-d™ move lean memory organization

3.1 User Memory Area

Blocks from 04_H to $0F_H$ belong to the User Memory Area. This part of the memory is readable / writable as well as lockable against unintentional overwriting using a locking mechanism.

At delivery all bytes of the User Memory Area are programmed to 00_H.

3.2 Service Area

The Service Area contains

- 7 byte UID plus 2 bytes of UID BCC information
- Internal Byte
- 32 bit OTP memory
- Lock bytes 0 and 1 for locking the OTP block and blocks in the User Area

In the following find the detailed description of the Service Area.

3.2.1 Unique Identifier (UID)

The 9 bytes of the UID (7 byte UID + 2 bytes BCC information) are allocated in Block 00_H, Block 01_H and Byte 1 of Block 02_H of the my-d™ move lean memory. All bytes are programmed and locked during the manufacturing process. Therefore these bytes are only readable for the user.

For the content of the UID the following definitions apply:

- SLE 66R01L supports only Cascade Level 2 (CL2) UID according to the ISO/IEC 14443-3 Type A which is a 7 byte unique number

The table below describes the content of the UID.

Table 4 UID Description

Cascade Level 2 - Double Size UID										
UID Byte	CT[1]	uid0[2]	uid1[3]	uid2	BCC0[4]	uid3	uid4	uid5	uid6	BCC1[4]

1) CT is the Cascade Tag and designates CL2. It has a value of 88_H. Please note that CT is hardwired and not stored in the memory
2) uid0 is the Manufacturer Code: 05_H according to ISO/IEC 7816-6
3) uid1 is the Chip Family Identifier. The higher significant nibble identifies a SLE 66R01L chip (0111_B), whereas the lower significant nibble is part of the serial number.
4) BCC is the UID CLn checkbyte calculated as Exclusive-OR over the four previous bytes (as described in ISO/IEC 14443-3 Type A). BCC is stored in the memory and read-out during the anti-collision.

3.2.2 OTP Block

The Block 03_H is a One Time Programmable (OTP) Block. Bits allocated in this block can only be logically set to 1_B, which is an irreversible process i.e. bits can not be reset to 0_B afterwards.

The Write One Block (WR1B) command should be used to program a specific OTP value. Incoming data of the WR1B command are bit-wise OR-ed with the current content of the OTP Block and the result is written back to the OTP Block.

Table 5 Writing to OTP Block (block 03_H) from the user point of view

OTP Block	Representation bit-wise	Description
Initial value	0000 0000 0000 0000 0000 0000 0000 0000_B	Production setting
Write $[55550003]_H$	0101 0101 0101 0101 0000 0000 0000 0011_B	Bit-wise “OR” with previous content of block 03_H
Write $[AA55001C]_H$	1111 1111 0101 0101 0000 0000 0001 1111_B	Bit-wise “OR” with previous content of block 03_H

An Anti-Tearing mechanism is implemented for the OTP Block on the my-d™ move lean. This mechanism prevents the stored value to be lost in case of a tearing event. This increases the level of data integrity and is transparent to the customer.

3.2.3 Locking mechanism

Bytes LOCK0, LOCK1 allocated in Block 02_H represent the one time field programmable bits which are used to lock the blocks in the specified address range from block 03_H (OTP Block) to $0F_H$.

Each block in this range can be individually locked to prevent further write access. A locking mechanism of each block is irreversible, i.e. once the locking information of a particular block (Lx) is set to 1_B it can not be reset back to 0_B any more. The **Figure 3** illustrates the locking bytes with the corresponding locking bits.

Furthermore, it is possible to freeze the locking information of some memory areas by setting Block Locking (BL) bits e.g. if the bit BL 15-10 is set to 1_B then the locking information for the corresponding area (L10 to L15) is not changeable any more. See the example in the **Table 6** below.

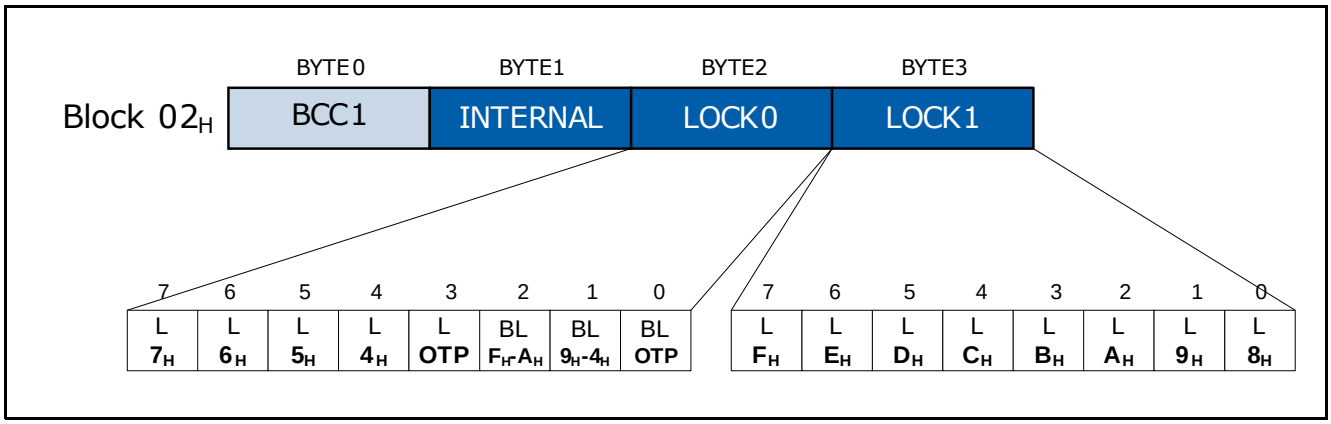

Figure 8 Locking and Block Locking Mechanism

The Write One Block (WR1B) command should be used to set the locking or block locking information of a certain block.

If WR1B is applied to Block 02_H then:

- the Byte 0 (BCC1) and Byte 1 (INTERNAL) will not be changed

The locking and block locking for a certain block is active immediately after writing. That means that it is not necessary to execute the REQA or WUPA command in order to activate the locking.

Note: If all three BL bits in the LOCK0 byte are set to 1_B then Block 02_H is locked. It is not possible to change the locking bits of this block any more. In this case the SLE 66R01L responds with NACK to a corresponding Write command.

Table 6 Example for OTP Block Lock and Block Lock

BL OTP	L OTP	OTP BLOCK STATE
0_B	0_B	OTP Block Unlocked
0_B	1_B	OTP Block Locked
1_B	0_B	OTP Block Unlocked and can not be locked ever more
1_B	1_B	OTP Block Locked

An Anti-Tearing mechanism is implemented for Lock bytes on the SLE 66R01L. This mechanism prevents a stored value to be lost in case of a tearing event. This increases the level of data integrity and it is transparent to the customer.

3.3 Memory Principle for NFC Forum™ Type 2 Tag

This section desribes how to map the my-d™ move lean memory into the memory structures defined in the NFC Forum™ Type 2 Tag technical specification. This enables the usage of the my-d™ move lean as a NFC Forum™ Type 2 Tag compatible chip.[1)]

3.3.1 NFC Forum™ Static Memory Structure

The Static Memory Structure is applied to a NFC Forum™ Type 2 Tag with a memory size equal to 64 bytes (see **Figure 9**). Blocks 04_H to $0F_H$ are available to store user data.

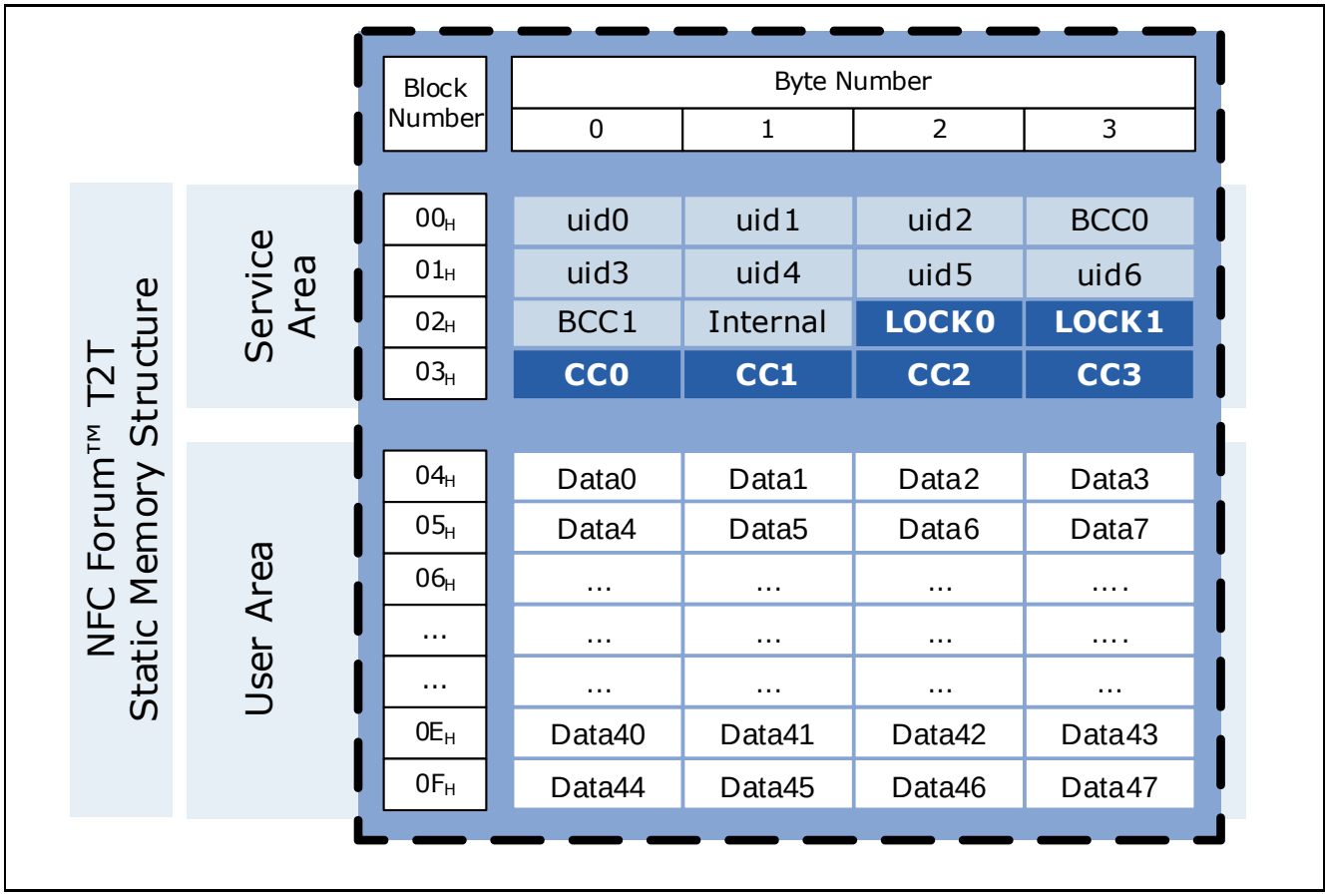

Figure 9 Static Memory Structure

1) The knowledge of NFC Forum™ Type 2 Tag Technical Specification is presumed to understand the memory structure.

4 Communication Principle

This chapter describes the functionality of the SLE 66R01L.

4.1 Communication between a card (PICC) and a reader (PCD)

It is recommended to read the ISO/IEC 14443 Type A and NFC Forum™ Type 2 Tag specifications in conjunction with this document in order to understand the communication protocol as well as the functionality of the SLE 66R01L as it is based on these specifications.

4.2 State Diagram

The SLE 66R01L is fully compliant to ISO/IEC 14443 Type A. All operations on this IC are initiated by an appropriate reader and controlled by the internal logic of the my-d™ move lean.

Prior to any memory access the card has to be selected according to the ISO/IEC 14443 Type A.

The following figure presents the state diagram of SLE 66R01L.

If an unexpected command is received, the chip always returns to IDLE or HALT state, depending from which path it came from (the red paths in the state diagram).

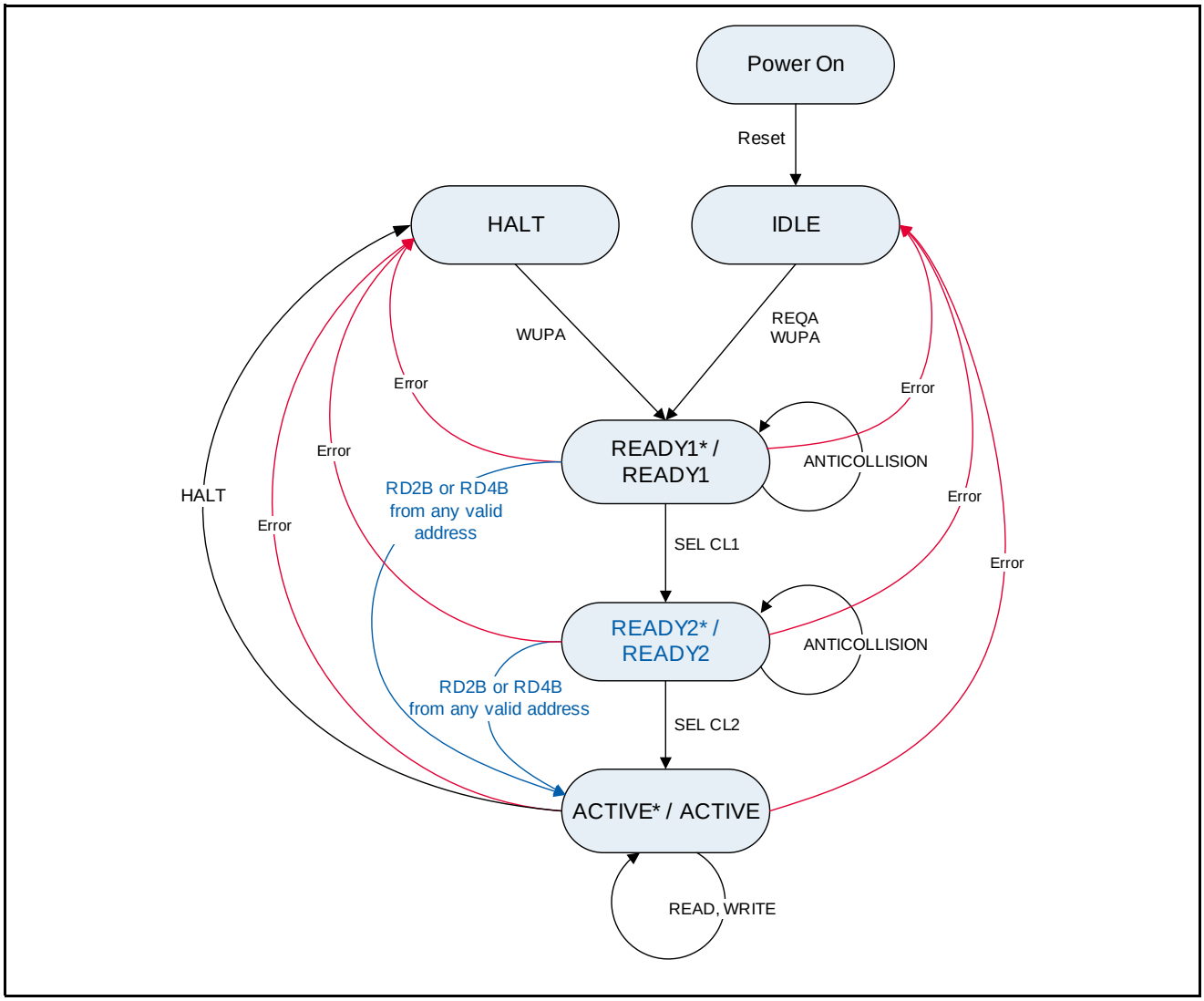

Figure 10 SLE 66R01L state diagram

4.2.1 IDLE/HALT State

After Power On, the SLE 66R01L is in IDLE state.

If REQA or WUPA is executed in this state, the SLE 66R01L transits to READY1 state. Any other command is interpreted as an error and the chip stays in IDLE state without any response.

If the HLTA command is executed in ACTIVE/ACTIVE* State, the SLE 66R01L will transit to HALT state. The HALT state can be left only if the chip receives a WUPA command. Any other command is interpreted as an error and the SLE 66R01L stays in the HALT state without any response.

4.2.2 READY1/READY1* State

In READY1/READY1* state the first part of the UID can be resolved by using ISO/IEC 14443 Type A anticollision and/or Select commands.

After the Select command is executed properly the IC transits to READY2/READY2* state in which the second part of the UID can be resolved. The answer to a Select command in READY1/READY1* state is Select Acknowledge (SAK) for cascade level 1, which indicates that the UID is incomplete and the next cascade level has to be started to resolve the whole UID (see also ISO/IEC 14443 Type A).

However the SLE 66R01L can directly transit from READY1/ READY1* state to ACTIVE/ACTIVE* state if a read command RD2B or R4BD with a valid address is executed. Note if more than one SLE 66R01L is in the reader field, all ICs are selected after the execution of the read command, although all of them have different UIDs.

Any other command or any other interruption is interpreted as an error and the SLE 66R01L returns back to IDLE or HALT state without any response, depending from which state it has come from.

4.2.3 READY2/READY2* State

In READY2/READY2* state the second part of the UID can be resolved using ISO/IEC 14443 Type A anticollision and/or Select commands.

After the Select command is executed properly the IC transits to ACTIVE/ACTIVE* state in which memory can be accessed. The answer to a Select command in READY2/READY2* state is SAK for cascade level 2, which indicates that the UID is complete and the selection process is finished.

However the SLE 66R01L can directly transit from READY2/READY2* state to ACTIVE/ACTIVE* state if a read command RD2B or RD4B is executed. Any valid block address can be used in the read command. Note if more than one SLE 66R01L is in the reader field, all ICs are selected after the execution of the read command, although all of them have different UIDs.

Any other command or any other interruption is interpreted as an error and the SLE 66R01L returns back to IDLE or HALT state without any response, depending from which part it has come from.

4.2.4 ACTIVE/ACTIVE* State

In the ACTIVE/ACTIVE* state memory access commands can be executed.

If a SLE 66R01L is configured to have read/write or write password protection, a password verification is required to access the protected memory pages. In case of a successful password verification, read/write access to the whole memory is possible. If no verification is done or the password verification fails, the memory area above block $0F_H$ is locked according to the access rights in the Configuration Byte.

The ACTIVE/ACTIVE* state is left if the HLTA command is executed properly; the SLE 66R01L then transits to HALT state and waits until a WUPA command is received.

If any error command is received, the SLE 66R01L sends “No Response” (NR) or “Not Acknowledge” (NACK) and transits to IDLE or HALT state, depending from which state it has come from.

4.2.5 HALT State

The HLTA command sets the SLE 66R01L in the HALT state. The SLE 66R01L sends no response to the HLTA command. In the HALT state the IC can be activated again by a Wake-UP command (WUPA).

Any other data received is interpreted as an error, the SLE 66R01L sends no response and remains in HALT state.

The exact behavior of a particular command in any of the states above is also described in the specific command description.

4.3 Start up

120 µs after entering the powering field (after the field reset) the SLE 66R01L is ready to receive a command. If a command is send earlier, the response to this command is not defined.

4.3.1 Start-up sequence of the SLE 66R01L

Each time after the execution of a REQA or WUPA, the SLE 66R01L reads the Configuration Byte and sets its internal states accordingly, see also the **Figure 11**. This information is not updated until the next execution of REQA or WUPA commands in IDLE or HALT state even when the Configuration Byte is changed in the EEPROM.

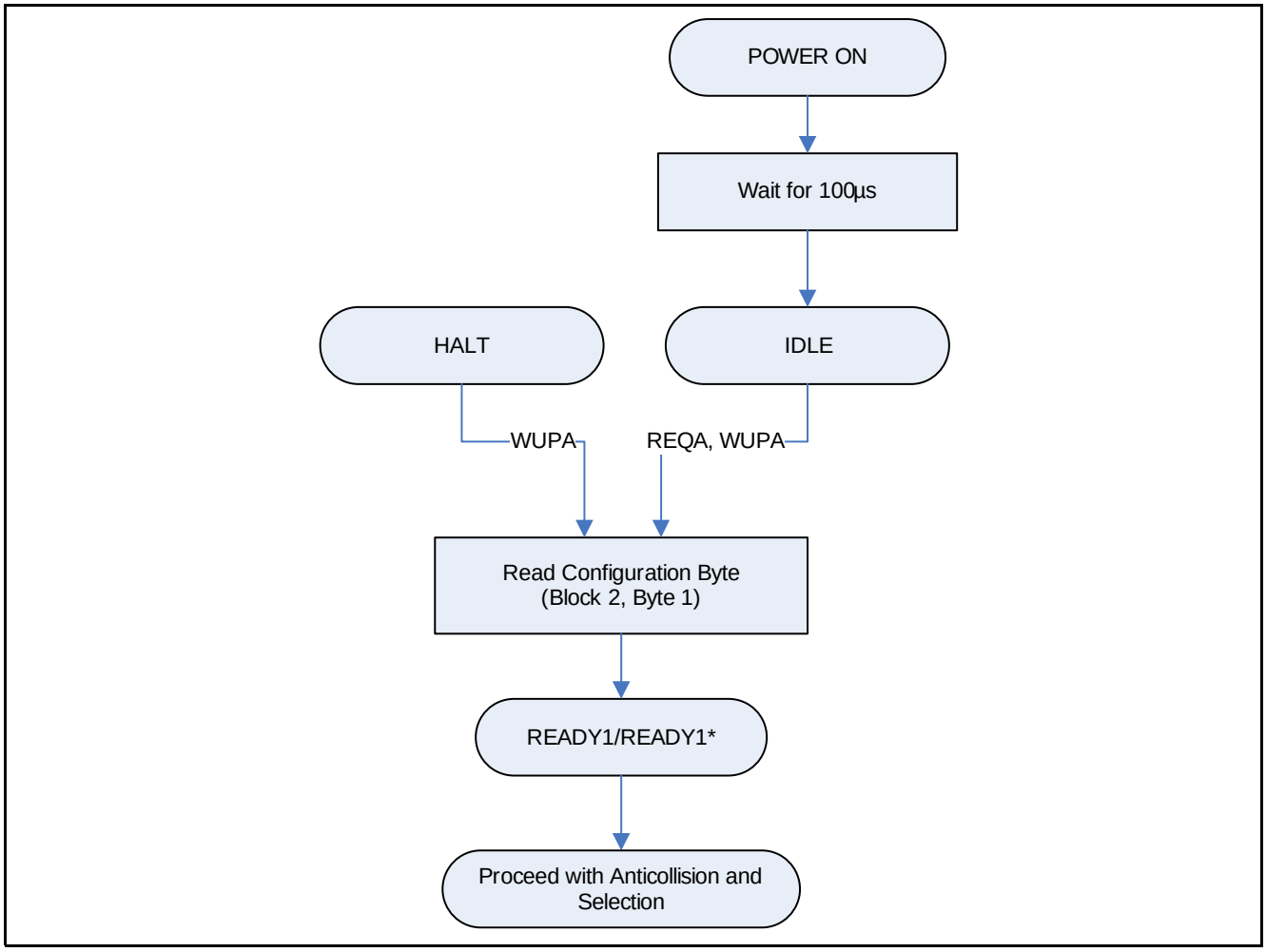

Figure 11 Start-up Sequence

4.4 Frame Delay Time

For information about Frame Delay Time (FDT), please refer to ISO/IEC 14443 Type A Specification.

Generally the FDT is measured between the last rising edge of the pause transmitted by the PCD and the falling edge of the first load modulation within the start bit transmitted by the my-d™ move lean. If more then one ISO/IEC 14443 Type A compatible chip is in the operating field of the reader all of them must respond in a synchronous way which is needed for the anticollision procedure.

For detailed timings see Table 1 of ISO/IEC 14443-3 Type A Specification.

Note: The response timing of a particular SLE 66R01L command is given in the specific command description. However, the timing values are rounded and are not on a grid according the ISO/IEC 14443 Type A.

4.5 Error Handling

The SLE 66R01L responds to valid frames only. The table below describes the behavior of the SLE 66R01L for different error cases.

Table 7 Behavior in case of an Error

Current States	Command or Error	Response SLE 66R01L	Next State
IDLE/HALT READY1/READY1* READY2/READY2*	Invalid Opcode	NR[1)]	IDLE/HALT[2)]
	Parity, Miller Error, CRC	NR	IDLE/HALT
	Command too short or too long	NR	IDLE/HALT
	Invalid Address	NR	IDLE/HALT
	Other Errors	NR	IDLE/HALT
ACTIVE/ACTIVE*	Invalid Opcode	NR	IDLE/HALT
	Parity, Miller Error, CRC	NACK1	IDLE/HALT
	Command too short or too long	NR	IDLE/HALT
	Invalid Address	NACK0	IDLE/HALT
	Other Errors	NACK0	IDLE/HALT

1) RD4B and RD2B commands in READY1/READY1* and READY2/READY2* exceptionally behave as in ACTIVE/ACTIVE* state.

2) The SLE 66R01L returns to IDLE or HALT state depending on the state where it has come from.

5 Command Set

5.1 Supported ISO/IEC 14443 Type A Command Set

The following table describes the ISO/IEC 14443-3 Type A command set which is supported by the SLE 66R01L.

For the command description please see ISO/IEC 14443-3 Type A functional specification.

Table 8 ISO/IEC 14443-3 Type A Command Set

Command	Abbreviation	Op-Code	Description
Request A	REQA	26_H	Short Frame Command Type A request to all ISO/IEC 14443 Type A compatible chips in IDLE State
Wake Up A	WUPA	52_H	Short Frame Command,Type A Wake Up request to all ISO/IEC 14443 Type A compatible chips
Anticollision	AC	93_H NVB_H 95_H NVB_H	Cascade level 1 with the Number of Valid Bits Cascade level 2 with the Number of Valid Bits
Select	SELA	93_H 70_H, 95_H 70_H	Select the UID of Cascade level 1 Select the UID of Cascade level 2
HaltA	HLTA	50_H	Set a chip to a HALT State Important remark: The parameter field of the HLTA command represents the valid address range which is 00_H -$0F_H$.

5.2 Memory Access Command Set

The command set of the SLE 66R01L comprises the NFC Forum™ Type 2 Tag commands as well as proprietary commands which are additionally implemented to increase data transaction time and increase the protection of the data stored in the memory.

The following table lists the memory access command set of the SLE 66R01L.

Table 9 my-d™ move lean memory access command set

Command	Abbreviation	Op-Code	Description
Read 4 Blocks[1)]	RD4B	30_H	This command reads 16 bytes data out of the memory starting from the specified address. A Roll-Back mechanism is implemented: - if block $0F_H$ is reached the read continues from block 00_H
Write 1 Block[2)]	WR1B	$A2_H$	If write access is granted, this command programs 4 bytes data to the specified memory address.
Compatibility Write Command	CPTWR	$A0_H$	This command sends 16 bytes to the SLE 66R01L but writes only the first 4 bytes of the incoming data to the specified memory address.
Read 2 Blocks	RD2B	31_H	This command reads 8 bytes out of the memory, starting from the specified address. A Roll-Back mechanism is implemented: - if block $0F_H$ is addressed, the read continues from block 00_H
Write 2 Blocks	WR2B	$A1_H$	If write access is granted, this command writes 8 bytes to the specified address memory. Note that the programming time is 4ms.

1) NFC Forum™ Type 2 Tag Read Command

2) NFC Forum™ Type 2 Tag Write Command

5.2.1 Read 4 Blocks (RD4B)

RD4B command reads 16 bytes data out of the memory starting from the specified address.

The Valid Address Range is 00_H to $0F_H$.

If any other address is specified the SLE 66R01L responds with a NACK. A roll back mechanism is implemented:

- if e.g. block $0E_H$ is addressed blocks $0E_H$, $0F_H$, 00_H and 01_H are replied

Table 10 Read 4 Blocks (RD4B)

Command Length	Code	Parameter	Data	Integrity Mechanism	Response
4 bytes	30_H	Valid Address Range 00_H-$0F_H$	n.a.	2 bytes CRC (1 parity bit per byte)	16 bytes data + 2 bytes CRC or NACK or NR

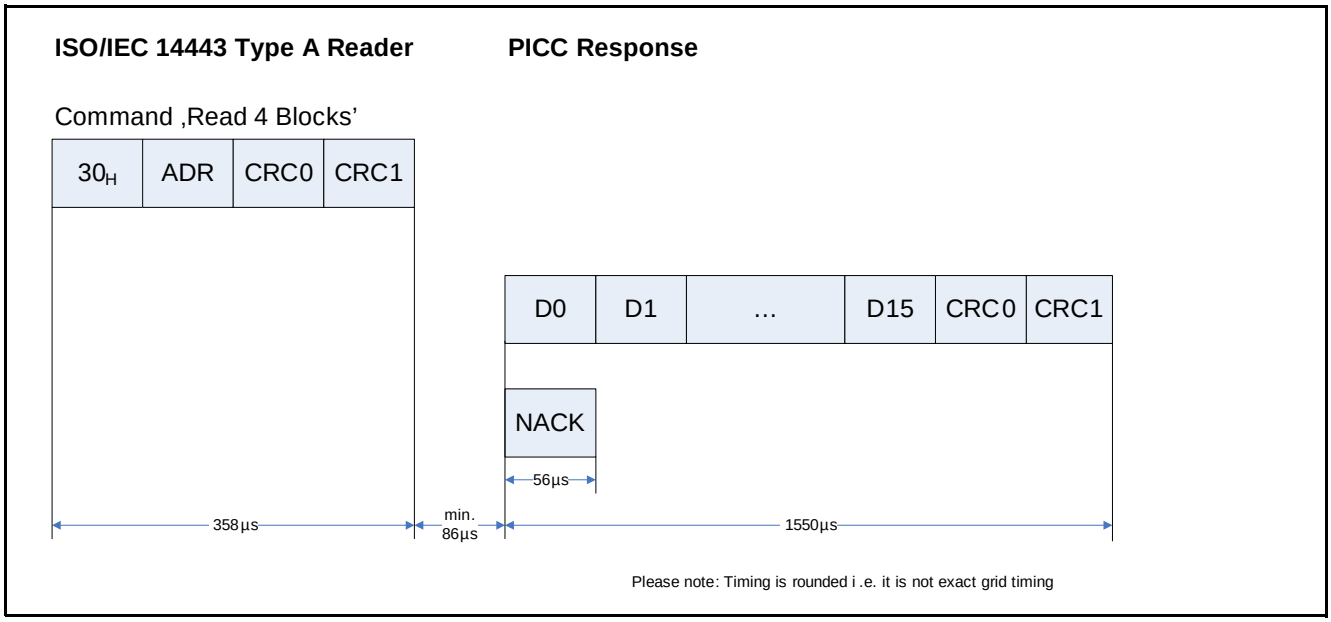

Figure 12 Read 4 Blocks Command

5.2.2 Write 1 Block (WR1B)

If the write access is granted the WR1B command is used to program 4 bytes of data to the specified address in the memory. This command should be used to program OTP block and Locking Bytes as well.

The Valid Address Range is from 02_H to $0F_H$. If any other address is specified the SLE 66R01L responds with a NACK.

Table 11 Write 1 Block (WR1B)

Command Length	Code	Parameter	Data	Integrity Mechanism	Response
8 bytes	$A2_H$	Valid Address Range 02_H-$0F_H$	4 bytes data	2 bytes CRC (1 parity bit per byte)	ACK or NACK or NR

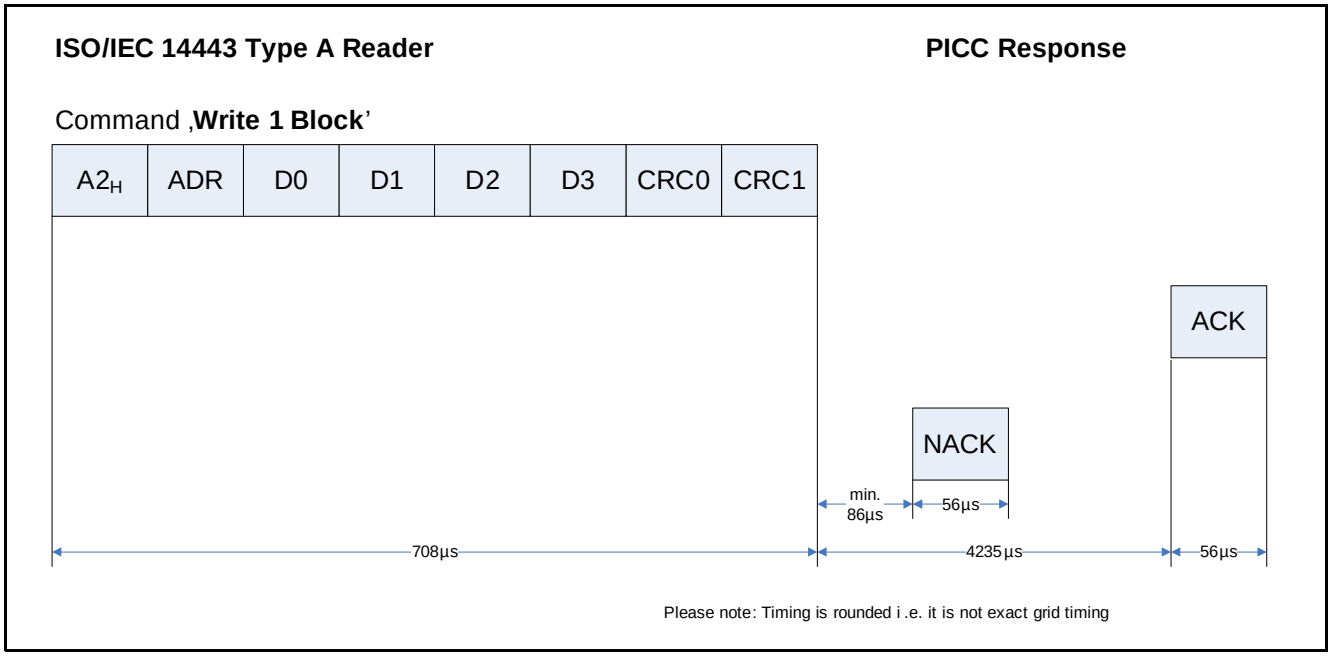

Figure 13 Write 1 Block Command

5.2.3 Compatibility Write Command (CPTWR)

If the write access is granted only the four least significant 4 bytes are written to the specified address. The remaining bytes will be ignored by the SLE 66R01L. It is recommended to set the remaining bytes 04_H-$0F_H$ to 00_H.

Table 12 Compatibility Write (CPTWR)

Command Length	Code	Parameter	Data	Integrity Mechanism	Response
20 bytes	$A0_H$	Valid Address Range 02_H-$0E_H$	16 bytes data	2 bytes CRC (1 parity bit per byte)	ACK or NACK or NR

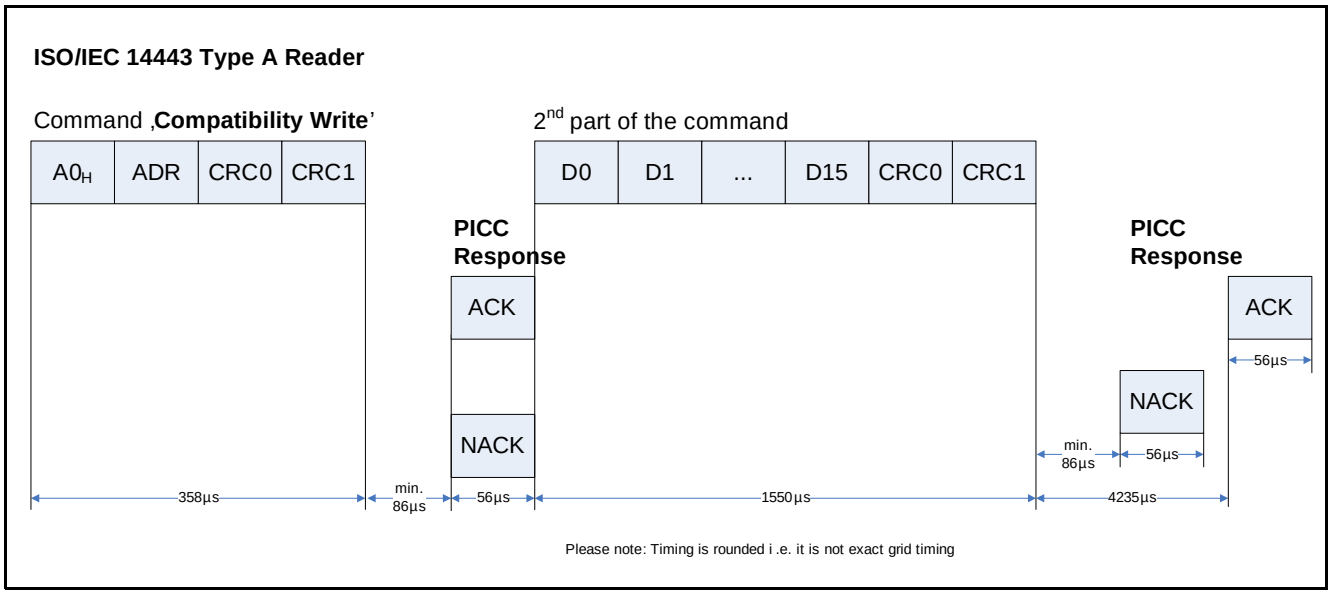

Figure 14 Compatibility Write Command

5.2.4 Read 2 Blocks (RD2B)

RD2B command reads 8 bytes out of the memory, starting from the specified address.

The Valid Address Range is from 00_H to $0F_H$. If any other address is specified the SLE 66R01L responds with a NACK. A roll back mechanism is implemented:

- if e.g. block $0F_H$ is addressed blocks $0F_H$ and 00_H are replied.

Table 13 Read 2 Block (RD2B)

Command Length	Code	Parameter	Data	Integrity Mechanism	Response
4 bytes	31_H	Valid Address Range 00_H-$0F_H$	n.a.	2 bytes CRC (1 parity bit per byte)	8 bytes data + 2 bytes data CRC or NACK

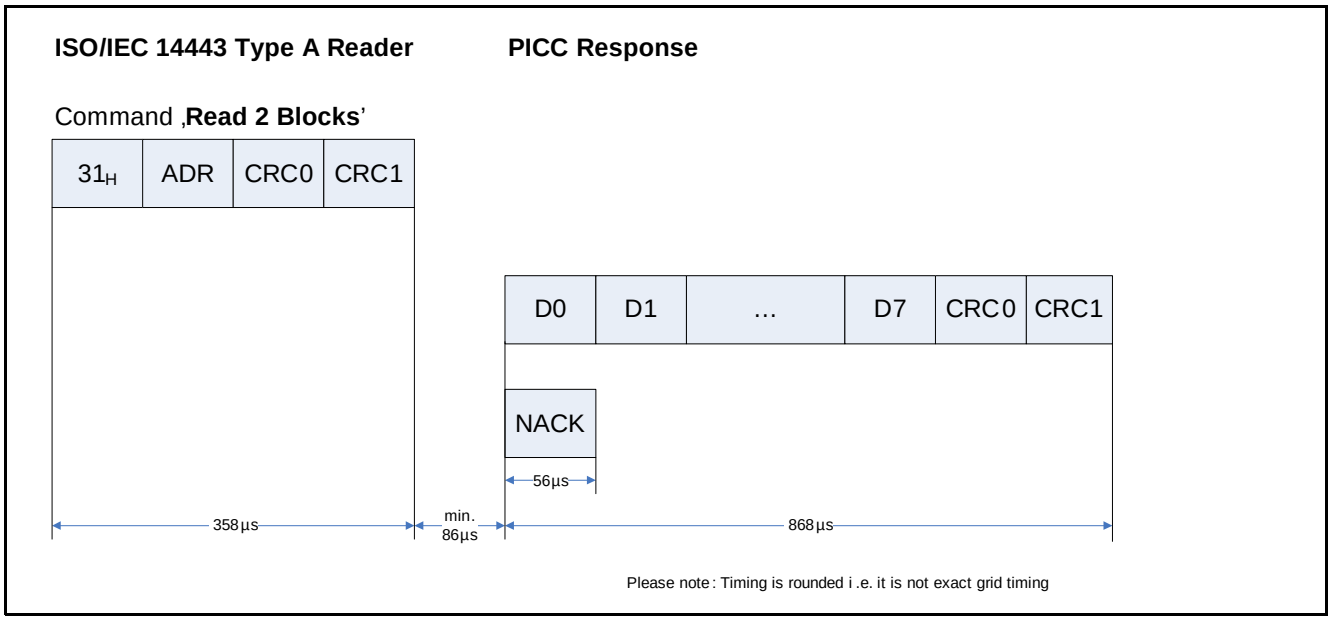

Figure 15 Read 2 Blocks Command

5.2.5 Write 2 Blocks (WR2B)

If write access is granted, i.e. if both addressed blocks are writable, the WR2B command is used to program two blocks (8 bytes of data) to the specified address in the memory.

The Valid Address Range is 04_H-$0E_H$. Only even start addresses are allowed. If any other address is specified, the SLE 66R01L responds with a NACK.

The WR2B command has the same programming time (approximately 4ms) for writing 8 bytes as the WR1B command which writes 4 bytes of data to the specified memory.

Table 14 Write 2 Block (WR2B)

Command Length	Code	Parameter	Data	Integrity Mechanism	Response
12 bytes	$A1_H$	Valid Address Range 04_H-$0E_H$; only even start addresses allowed	8 bytes data	2 bytes CRC (1 parity bit per byte)	ACK or NACK or NR

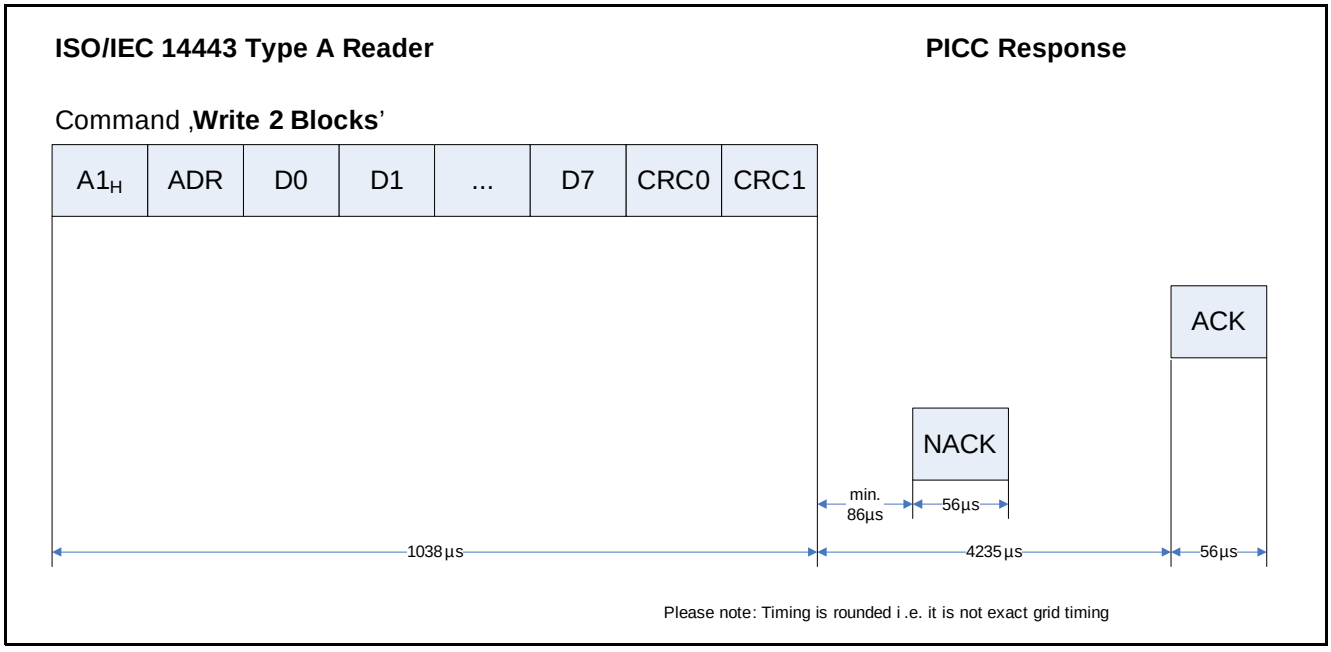

Figure 16 Write 2 Blocks Command

5.2.6 HLTA command

The HLTA command is used to set the SLE 66R01L into the HALT state. The HALT State allows user to separate already identified SLE 66R01L chips and the others. Contrary to the definition in the ISO/IEC 14443-3 Type A standard, the SLE 66R01L accepts as a parameter the whole address range of 00_H to $0F_H$ with correct CRC for a proper execution of a HLTA command.

Table 15 Halt (HLTA)

Command Length	Code	Parameter	Data	Integrity Mechanism	Response
4 bytes	50_H	Valid Address Range 00_H-$0F_H$	n.a.	2 bytes CRC 1 parity bit per byte	NACK or NR

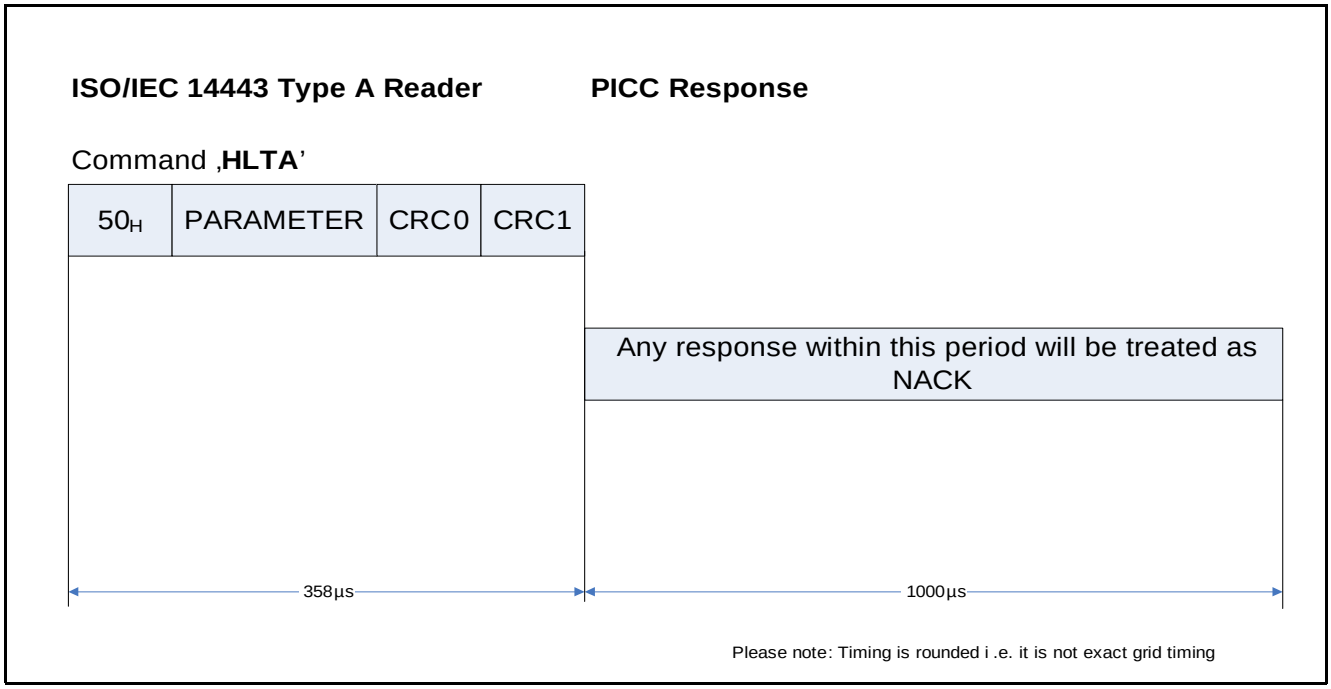

Figure 17 HLTA Command

5.3 my-d™ move lean responses

Following sections list valid responses of the SLE 66R01L

5.3.1 Command responses

The Acknowledge (ACK) and Not-Acknowledge (NACK) are command responses of the SLE 66R01L.

Table 16 ACK and NACK as responses

Response	Code (4 bits)	Integrity Mechanism
ACK	A_H	n.a.
NACK0	0_H	n.a.
NACK1	1_H	n.a.
NR[1)]	n.a.	n.a.

1) Depending on the current state, the SLE 66R01L does not respond to some errors.

The response code is A_H for ACK and 0_H or 1_H for NACK. The ACK and NACK are sent as 4 bit response with no CRC and/or parity.

5.3.2 my-d™ move lean identification data

During the anti-collision the SLE 66R01L sends responses to the REQA and SEL commands.

Table 17 Summary of SLE 66R01L identification data

Code	Data	Description
ATQA	0044_H	Answer to Request, response to REQA and WUPA command, hard coded 2 bytes. Indicates a double-size UID.
SAK (cascade level 1)	04_H	Select Acknowledge answer to selection of 1st cascade level. Indicates that the UID is incomplete.
SAK (cascade level 2)	00_H	Select Acknowledge answer to selection of 2nd cascade level. Indicates that the UID is complete.
CT	88_H	Cascade Tag Indicates that UID is not single size UID.

6 Operational Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at $T_{ambient}$ = 25°C and the given supply voltage.

6.1 Electrical Characteristics

f_{CAR} = 13.56 MHz sinusoidal waveform, voltages refer to VSS.

Table 18 Electrical Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Chip input capacitance L_A-L_B	C_{IN}	16.15	17	17.85	pF	$V_{AB\ RMS}$ = 2.0 V, f_{CAR} = 13.56 MHz, $T_{ambient}$ = 25 ℃
Chip load resistance L_A-L_B	R_{IN}	3	4.5	6	kΩ	$V_{AB\ RMS}$ = 2.0 V, f_{CAR} = 13.56 MHz, $T_{ambient}$ = 25 ℃
Endurance (erase/write cycles)[1)]		10^4				–
Data retention[1)]		5			years	
EEPROM Erase and Write time	t_{prog}			3.8	ms	Combined erase + write; excluding time for command / response transfer between interrogator and chip, $T_{ambient}$ = 25 ℃
ESD Protection voltage (L_A, L_B pins)	V_{ESD}	2			kV	JEDEC STD EIA / JESD22 A114-B
Ambient temperature	$T_{ambient}$	-25		+70	℃	for chip
Junction temperature	$T_{junction}$	-25		+110	℃	for chip

1) Values are temperature dependent

6.2 Absolute Maximum Ratings

Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability, including EEPROM data retention and erase/write endurance. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied.

Table 19 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input peak voltage between L_A-L_B	V_{INpeak}			6	V_{peak}	
Input current through L_A-L_B	I_{IN}			30	mA	
Storage temperature	$T_{storage}$	-40		+125	℃	

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