International
IOR Rectifier

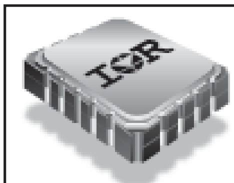
PD - 90713F

RADIATION HARDENED POWER MOSFET SURFACE MOUNT (LCC-18)

IRHE7230
JANSR2N7262U
200V, N-CHANNEL
REF: MIL-PRF-19500/601
RAD-Hard™ HEXFET® TECHNOLOGY

Product Summary

Part Number	Radiation Level	$R_{DS(on)}$	I_D	QPL Part Number
IRHE7230	100K Rads (Si)	0.35Ω	5.5A	JANSR2N7262U
IRHE3230	300K Rads (Si)	0.35Ω	5.5A	JANSF2N7262U
IRHE4230	500K Rads (Si)	0.35Ω	5.5A	JANSG2N7262U
IRHE8230	1000K Rads (Si)	0.35Ω	5.5A	JANSH2N7262U



LCC - 18

International Rectifier's RAD-Hard™ HEXFET® technology provides high performance power MOSFETs for space applications. This technology has over a decade of proven performance and reliability in satellite applications. These devices have been characterized for both Total Dose and Single Event Effects (SEE). The combination of low Rdson and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features:
- Single Event Effect (SEE) Hardened
- Low $R_{DS(on)}$
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Surface Mount
- Light Weight

Absolute Maximum Ratings

Pre-Irradiation

	Parameter		Units
I_D @ V_{GS} = 12V, T_C = 25°C	Continuous Drain Current	5.5	A
I_D @ V_{GS} = 12V, T_C = 100°C	Continuous Drain Current	3.5	
I_{DM}	Pulsed Drain Current ①	22	
P_D @ T_C = 25°C	Max. Power Dissipation	25	W
	Linear Derating Factor	0.2	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	240	mJ
I_{AR}	Avalanche Current ①	5.5	A
E_{AR}	Repetitive Avalanche Energy ①	2.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J T_{STG}	Operating Junction Storage Temperature Range	-55 to 150	°C
	Pckg. Mounting Surface Temp.	300 (for 5s)	
	Weight	0.42 (Typical)	g

For footnotes refer to the last page

05/15/06

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	200	—	—	V	V_{GS} =0 V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	0.25	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.35	Ω	V_{GS} = 12V, I_D = 3.5A ④
		—	—	0.36		V_{GS} = 12V, I_D = 5.5A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 1.0mA
g_{fs}	Forward Transconductance	2.5	—	—	S (℧)	V_{DS} > 15V, I_{DS} = 3.5A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	25	µA	V_{DS}= 160V,V_{GS}=0V
		—	—	250		V_{DS} = 160V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	50	nC	V_{GS} = 12V, I_D = 5.5A, V_{DS} = 100V
Q_{gs}	Gate-to-Source Charge	—	—	10		
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	25		
$t_{d(on)}$	Turn-On Delay Time	—	—	25	ns	V_{DD} = 100V, I_D = 5.5A, V_{GS} = 12V, R_G = 7.5Ω
t_r	Rise Time	—	—	40		
$t_{d(off)}$	Turn-Off Delay Time	—	—	60		
t_f	Fall Time	—	—	45		
$L_S + L_D$	Total Inductance	—	6.1	—	nH	Measured from drain lead (6mm/0.25in. from package) to source lead (6mm/0.25in. from package)
C_{iss}	Input Capacitance	—	1100	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz
C_{oss}	Output Capacitance	—	250	—		
C_{rss}	Reverse Transfer Capacitance	—	55	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	5.5	A	
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	22		
V_{SD}	Diode Forward Voltage	—	—	1.4	V	T_j = 25°C, I_S = 5.5A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	400	ns	T_j = 25°C, I_F = 5.5A, di/dt ≤ 100A/µs
Q_{RR}	Reverse Recovery Charge	—	—	3.0	µC	V_{DD} ≤ 25V ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJC}	Junction-to-Case	—	—	5.0	°C/W	
R_{thJPCB}	Junction-to-PC Board	—	19	—		Solder to a copper clad PC Board

Note: Corresponding Spice and Saber models are available on the International Rectifier Website.

For footnotes refer to the last page

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	100K Rads(Si)[1]		300K - 1000K Rads (Si)[2]		Units	Test Conditions
		Min	Max	Min	Max		
BV_{DSS}	Drain-to-Source Breakdown Voltage	200	—	200	—	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.0	1.25	4.5		$V_{GS} = V_{DS}$, I_D = 1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	—	100	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	-100	—	-100		V_{GS} = -20 V
I_{DSS}	Zero Gate Voltage Drain Current	—	25	—	50	µA	V_{DS}=160V, V_{GS} =0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	0.35	—	0.48	Ω	V_{GS} = 12V, I_D =3.5A
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (LCC-18)	—	0.35	—	0.48	Ω	V_{GS} = 12V, I_D =3.5A
V_{SD}	Diode Forward Voltage ④	—	1.4	—	1.4	V	V_{GS} = 0V, I_S = 5.5A

1. Part number IRHE7230 (JANSR2N7262U)
2. Part numbers IRHE3230 (JANSF2N7262U), IRHE4230 (JANSG2N7262U) and IRHE8230 (JANSH2N7262U)

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Ion	LET	Energy	Range	V_{DS}(V)				
	(MeV/(mg/cm²))	(MeV)	(µm)	@V_{GS}=0V	@V_{GS}=-5V	@V_{GS}=-10V	@V_{GS}=-15V	@V_{GS}=-20V
Cu	28	285	43	190	180	170	125	—
Br	36.8	305	39	100	100	100	50	—

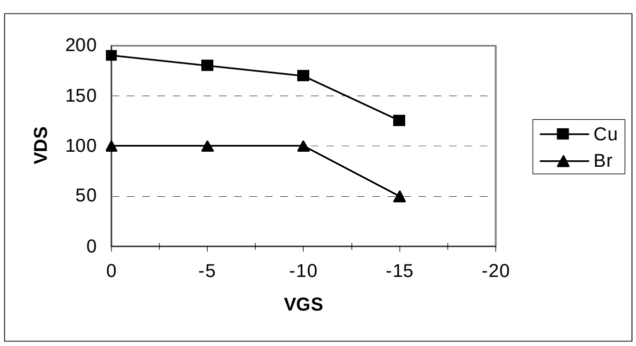


Fig a. Single Event Effect, Safe Operating Area

For footnotes refer to the last page

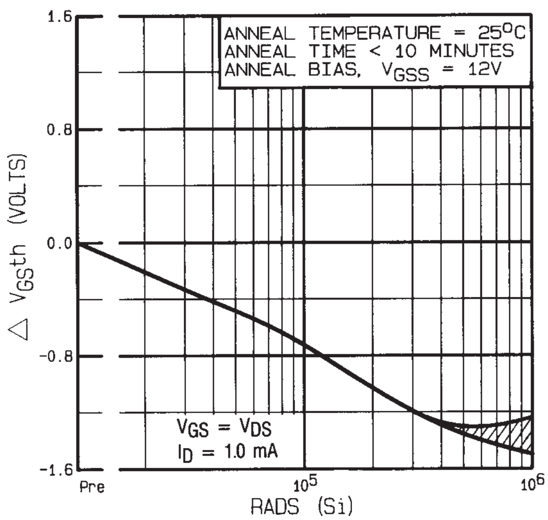


Fig 1. Typical Response of Gate Threshhold Voltage Vs. Total Dose Exposure

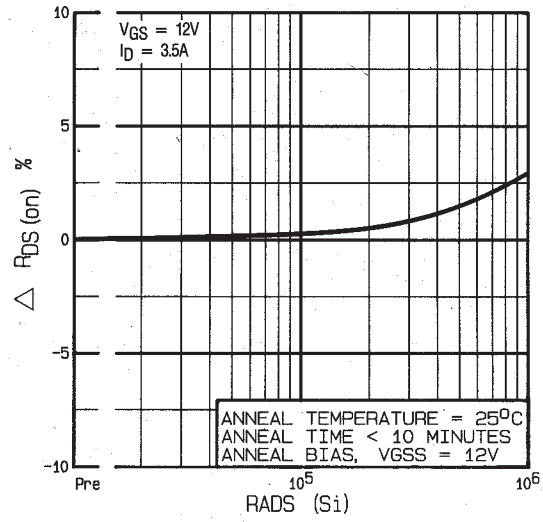


Fig 2. Typical Response of On-State Resistance Vs. Total Dose Exposure

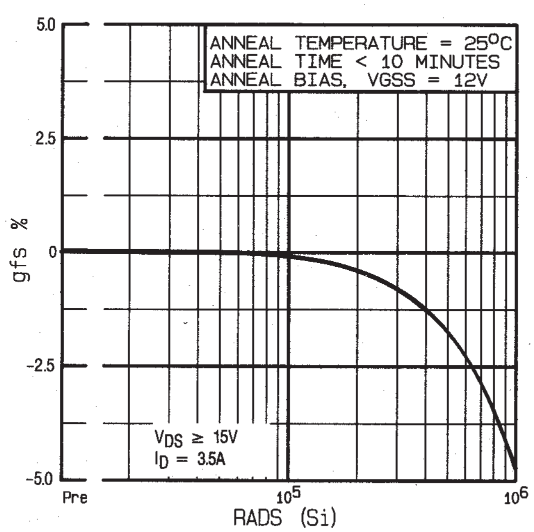


Fig 3. Typical Response of Transconductance Vs. Total Dose Exposure

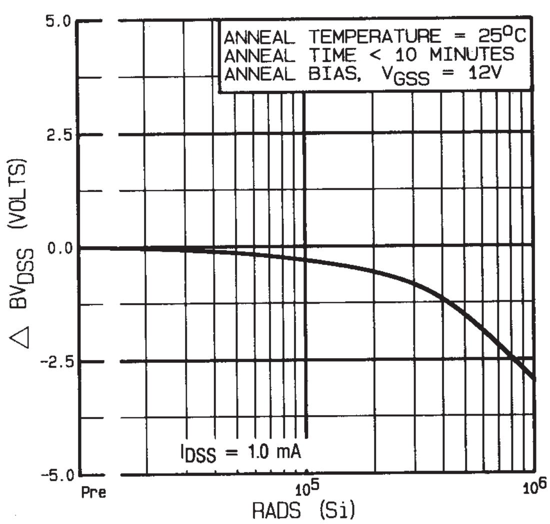


Fig 4. Typical Response of Drain to Source Breakdown Vs. Total Dose Exposure

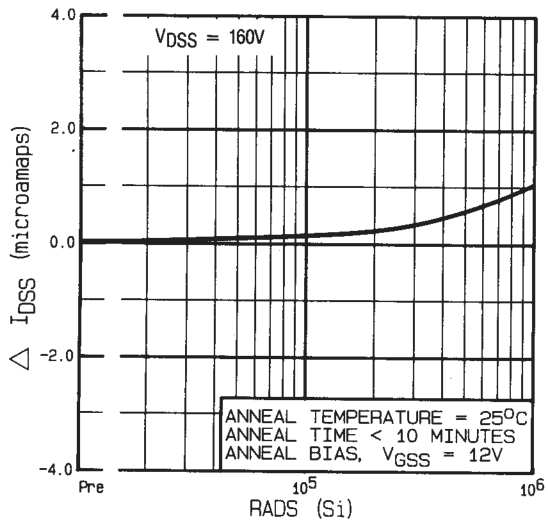


Fig 5. Typical Zero Gate Voltage Drain Current Vs. Total Dose Exposure

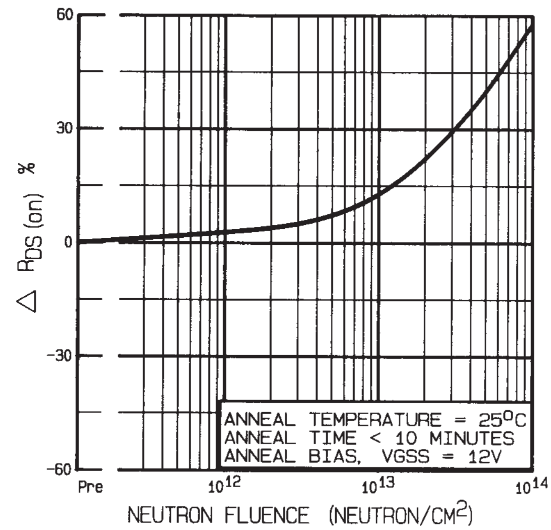


Fig 6. Typical On-State Resistance Vs. Neutron Fluence Level

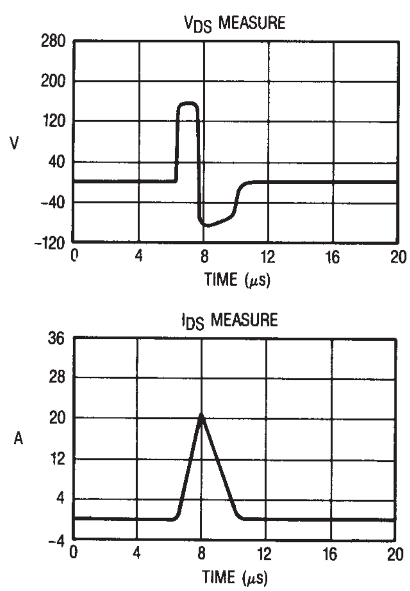


Fig 7. Typical Transient Response of Rad Hard HEXFET During $1x10^{12}$ Rad (Si)/Sec Exposure

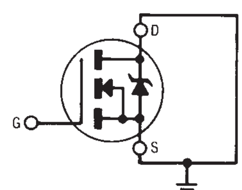


Fig 8a. Gate Stress of V_{GSS} Equals 12 Volts During Radiation

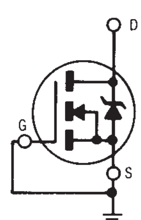


Fig 8b. V_{DSS} Stress Equals 80% of B_{VDSS} During Radiation

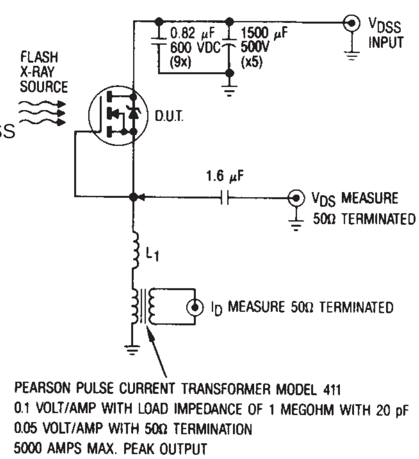


Fig 9. High Dose Rate (Gamma Dot) Test Circuit

Note: Bias Conditions during radiation: V_{GS} = 12 Vdc, V_{DS} = 0 Vdc

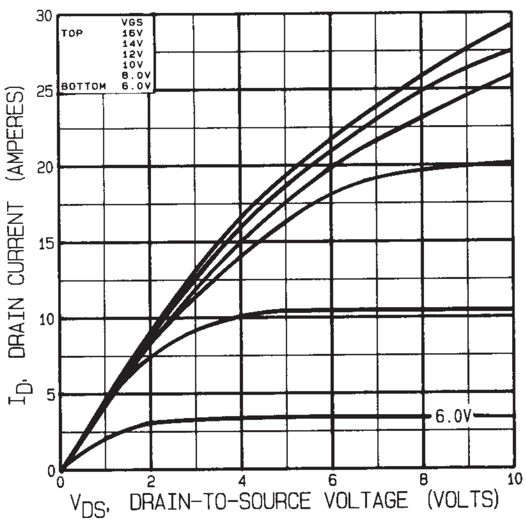


Fig 10. Typical Output Characteristics
Pre-Irradiation

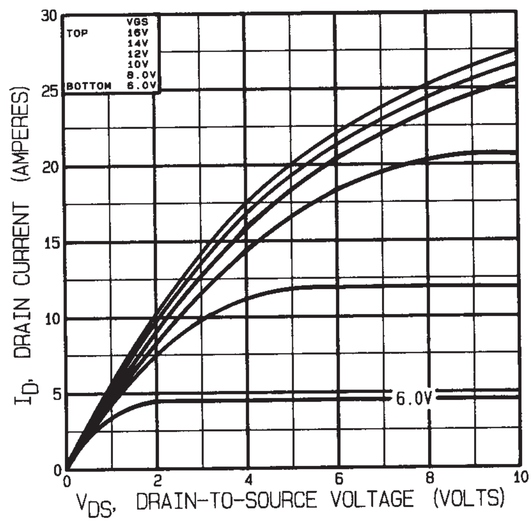


Fig 11. Typical Output Characteristics
Post-Irradiation 100K Rads (Si)

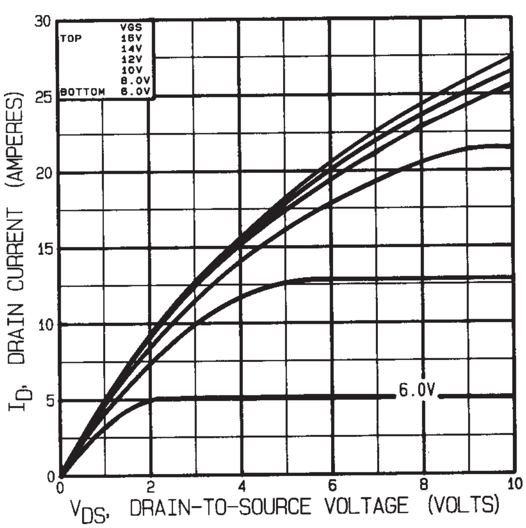


Fig 12. Typical Output Characteristics
Post-Irradiation 300K Rads (Si)

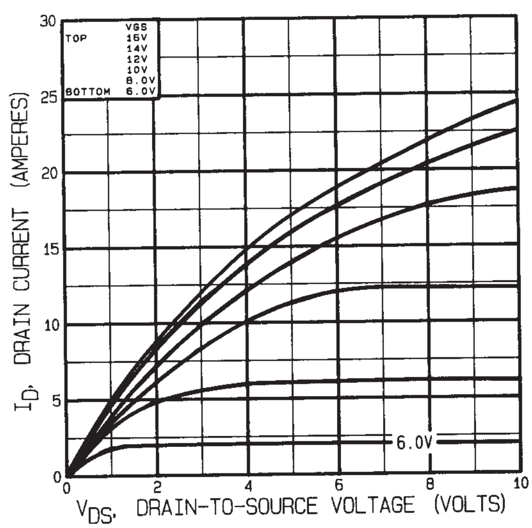


Fig 13. Typical Output Characteristics
Post-Irradiation 1 Mega Rads (Si)

Note: Bias Conditions during radiation: V_{GS} = 0 Vdc, V_{DS} = 160 Vdc

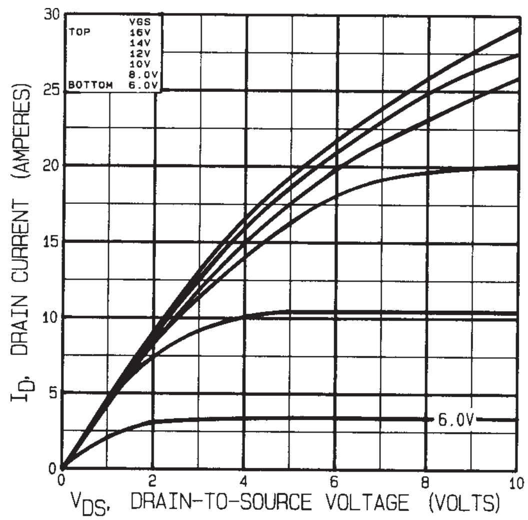


Fig 14. Typical Output Characteristics Pre-Irradiation

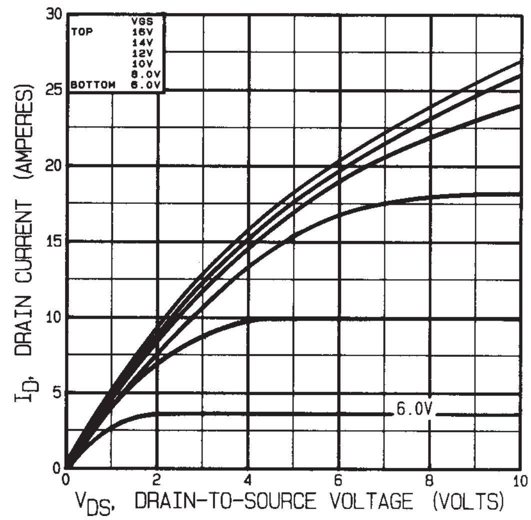


Fig 15. Typical Output Characteristics Post-Irradiation 100K Rads (Si)

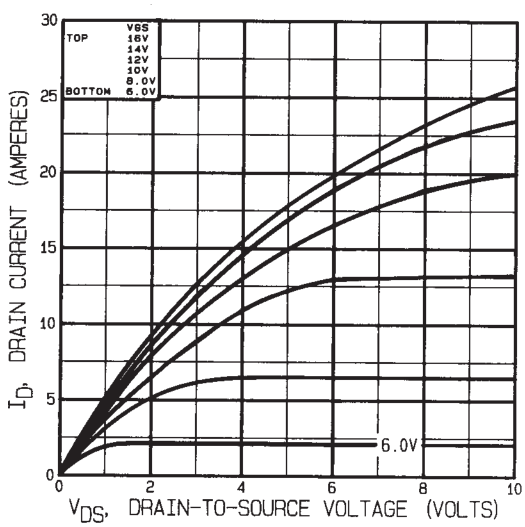


Fig 16. Typical Output Characteristics Post-Irradiation 300K Rads (Si)

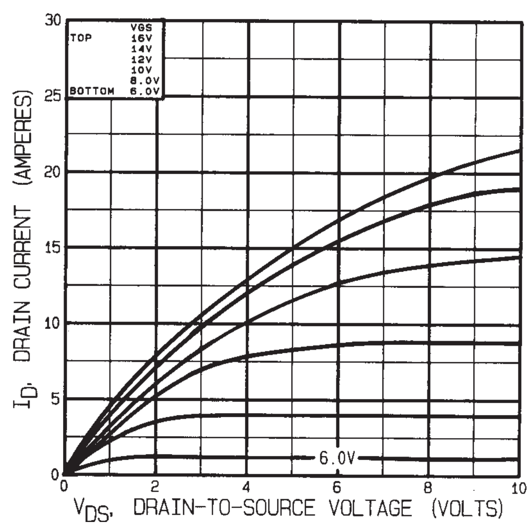


Fig 17. Typical Output Characteristics Post-Irradiation 1 Mega Rads (Si)

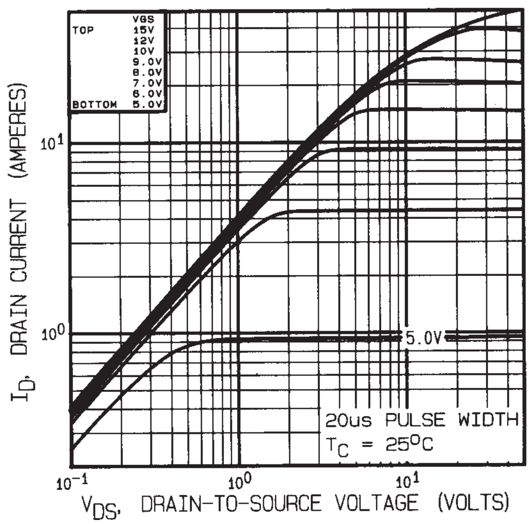


Fig 18. Typical Output Characteristics

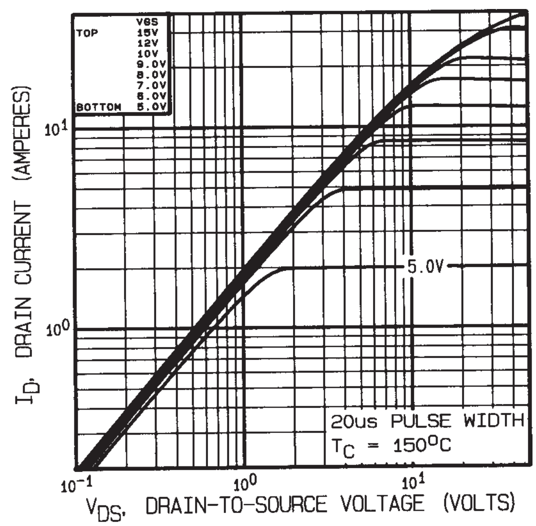


Fig 19. Typical Output Characteristics

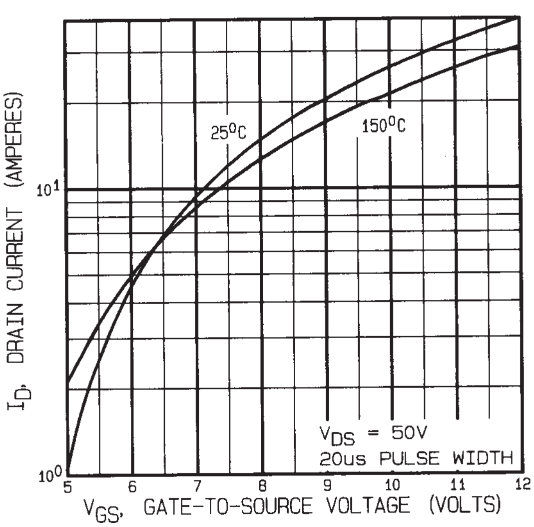


Fig 20. Typical Transfer Characteristics

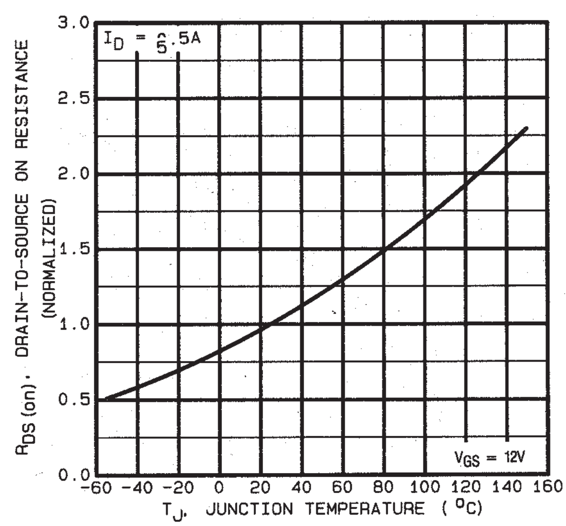


Fig 21. Normalized On-Resistance Vs. Temperature

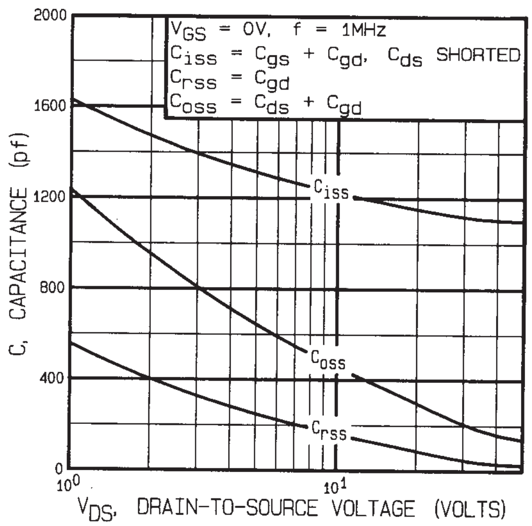


Fig 22. Typical Capacitance Vs. Drain-to-Source Voltage

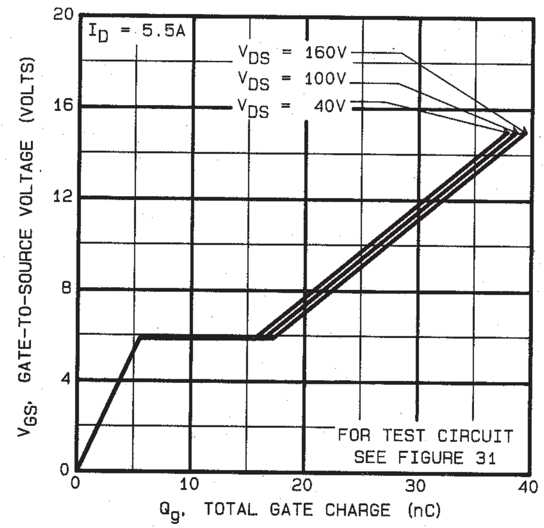


Fig 23. Typical Gate Charge Vs. Gate-to-Source Voltage

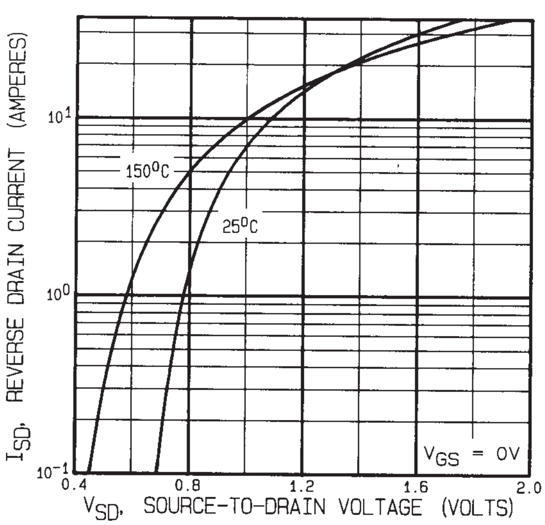


Fig 24. Typical Source-Drain Diode Forward Voltage

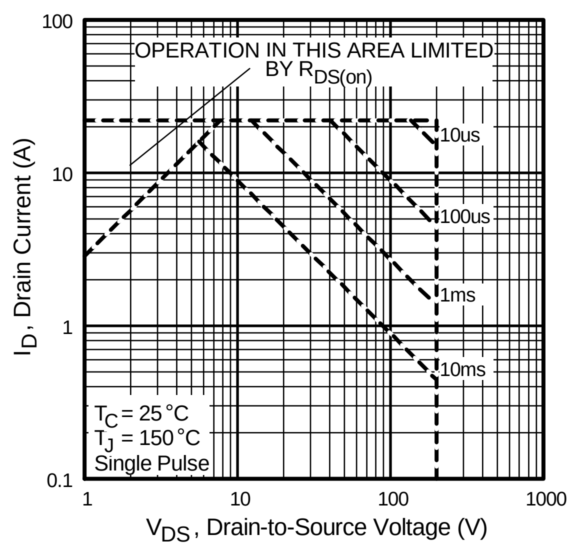


Fig 25. Maximum Safe Operating Area

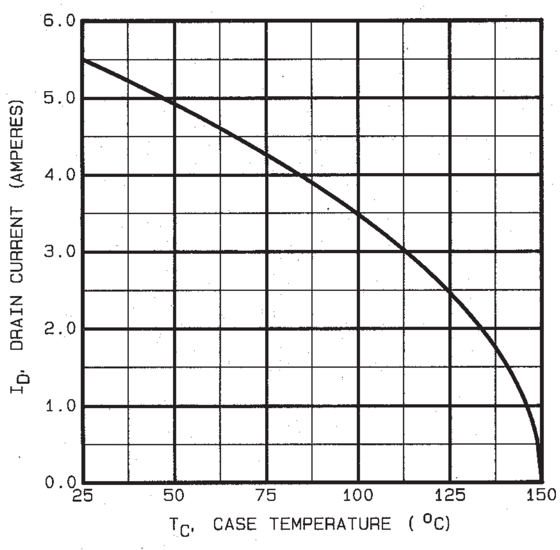


Fig 26. Maximum Drain Current Vs. Case Temperature

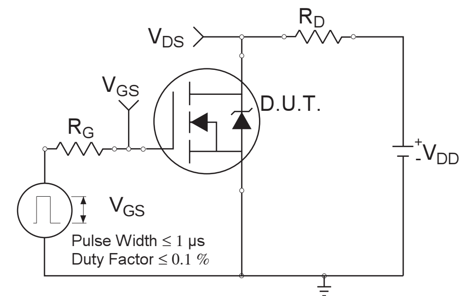


Fig 27a. Switching Time Test Circuit

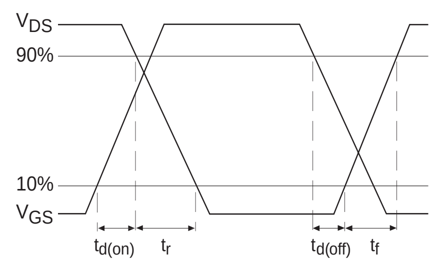


Fig 27b. Switching Time Waveforms

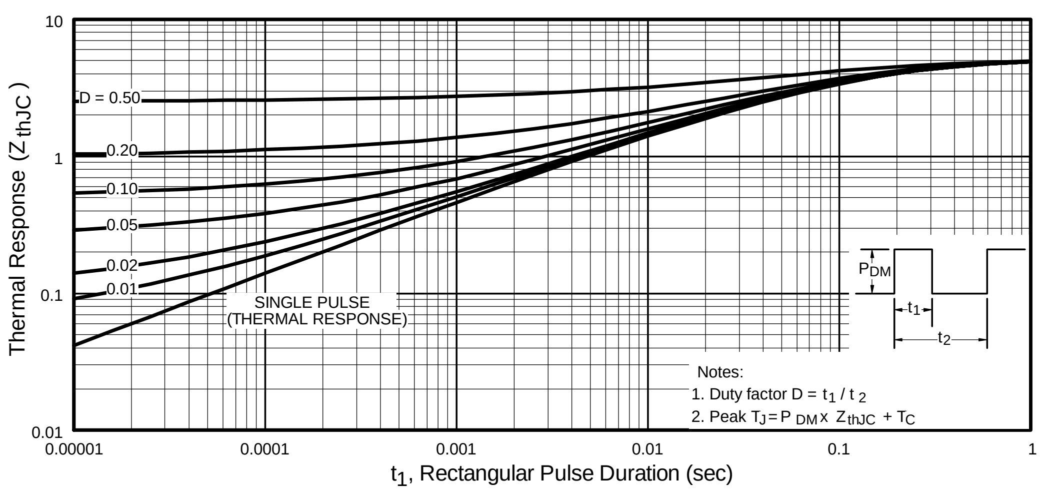


Fig 28. Maximum Effective Transient Thermal Impedance, Junction-to-Case

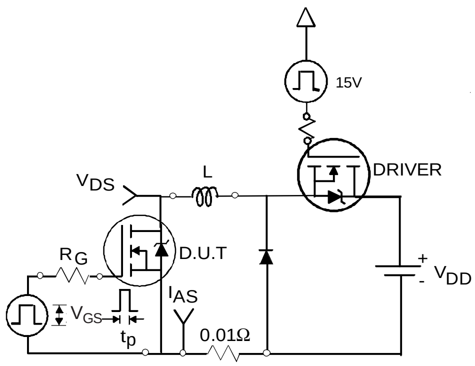


Fig 29a. Unclamped Inductive Test Circuit

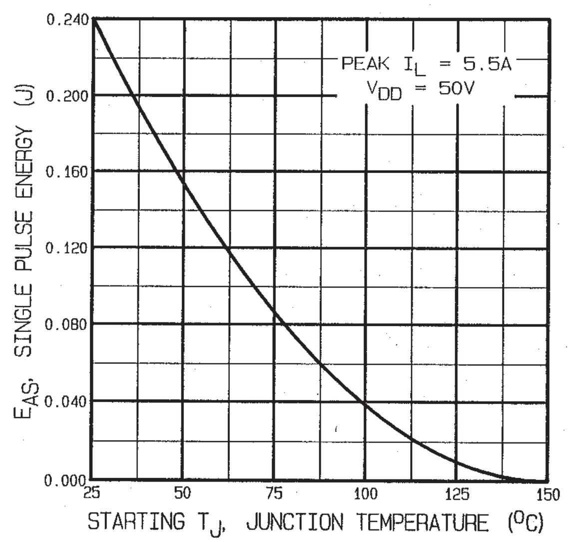


Fig 29c. Maximum Avalanche Energy Vs. Drain Current

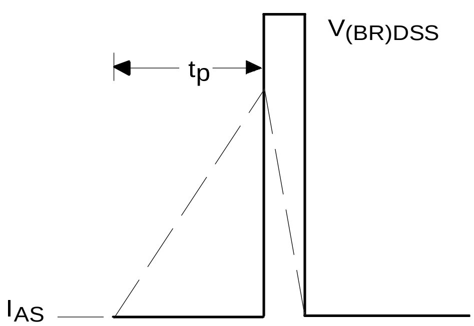


Fig 29b. Unclamped Inductive Waveforms

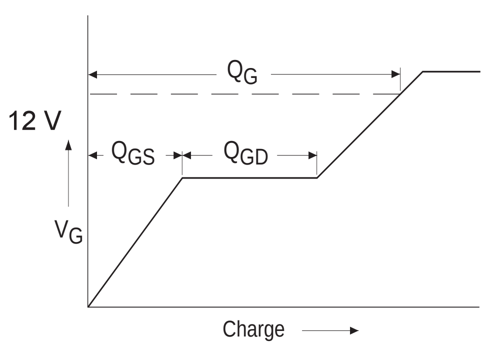


Fig 30a. Basic Gate Charge Waveform

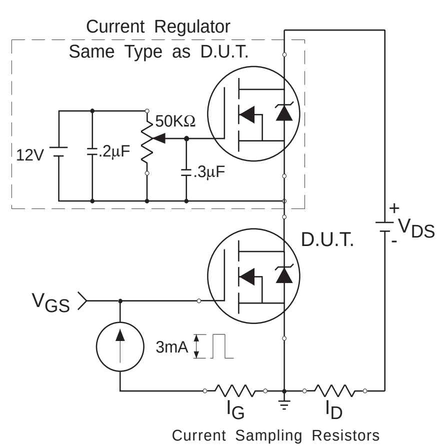


Fig 30b. Gate Charge Test Circuit

Foot Notes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = 25V, starting T_J = 25°C, L= 15.9mH
Peak I_L = 5.5A, V_{GS} = 12V

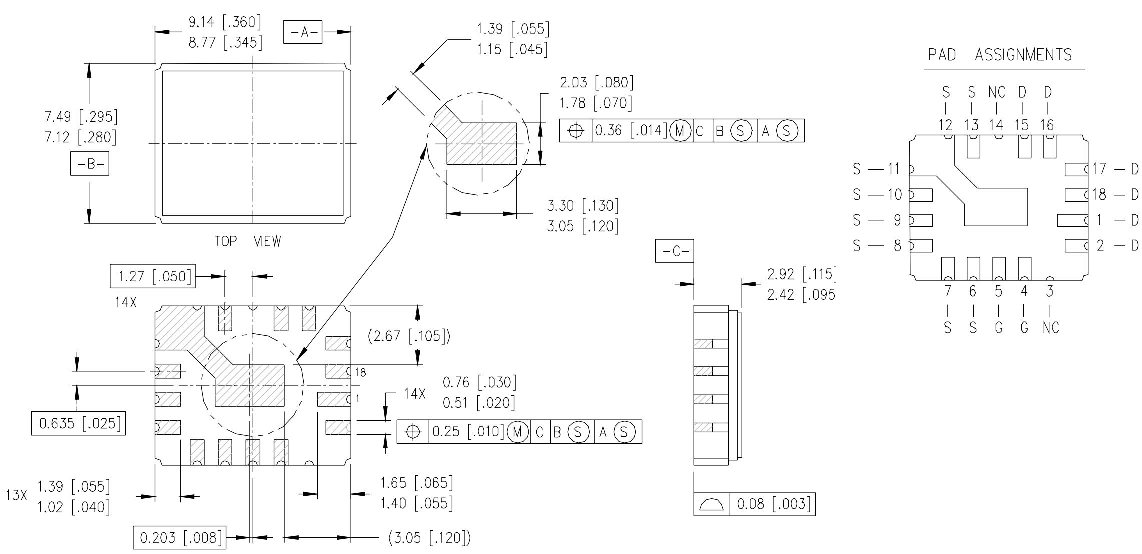
③ $I_{SD} \le$ 5.5A, di/dt $\le$ 120A/µs,
$V_{DD} \le$ 200V, $T_J \le$ 150°C

④ Pulse width $\le$ 300 µs; Duty Cycle $\le$ 2%

⑤ **Total Dose Irradiation with V_{GS} Bias.**
12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.

⑥ **Total Dose Irradiation with V_{DS} Bias.**
160 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.

Case Outline and Dimensions — LCC-18



NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

LEGEND

G = GATE
D = DRAIN
S = SOURCE
NC = NO CONNECTION

International
IOR Rectifier

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[>>Infineon Technologies(英飞凌)]