MP6651

2A, Single-Phase BLDC Driver with Integrated Hall Sensor

DESCRIPTION

The MP6651 is a single-phase brushless DC (BLDC) motor driver with integrated power MOSFETs and a Hall-effect sensor. The input voltage (V_{IN}) is between 3.3V and 18V.

The motor speed is controlled by the input PWM duty from PWM pin. The MP6651 features a configurable soft-on/off commutation. It also features a Hall offset angle across the full speed range to flexibly optimize low-speed and high-speed performance.

The MP6651 provides rotational speed detection. The rotational speed detector (the FG/RD pin) is an open-drain output. It outputs a high or low voltage relative to the internal Hall comparator's output. The FG/RD pin can also configured for rotor lock indication.

Robust protections include input over-voltage protection (OVP), under-voltage lockout (UVLO), locked rotor protection, over-current protection (OCP), and thermal shutdown protection.

The MP6651 is available in a straight-lead SOIC-8 package and a QFN-10 (2mmx3mm) package.

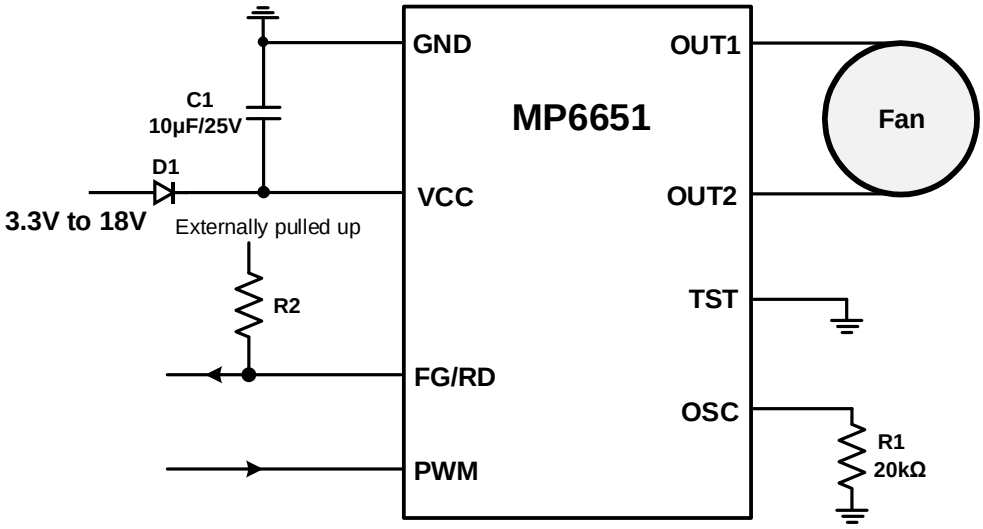
FEATURES

- On-Chip Hall Sensor
- Wide 3.3V to 18V Operating Input Voltage (V_{IN}) Range
- 2A Continuous Current with QFN-10 Package
- 1.5A Continuous Current with SOIC-8 SL Package
- Integrated Power MOSFETs
- Configurable Starting Duty Cycle
- Configurable Min Output Duty Cycle
- Configurable Soft-On/Off Commutating Angle (Max: 45°)
- Configurable Hall Offset Angle (Max: ±45°)
- 4-Step Configurable Current Limit
- 2kHz to 100kHz PWM Input Range
- 2.4s to 19.2s Configurable Soft-Start Time
- Fixed 27kHz Output Switching Frequency (f_{SW})
- Rotor Lock Protection with Auto-Recovery
- Thermal Protection with Auto-Recovery
- Built-in Input OVP and UVLO with Auto-Recovery
- Available in SOIC-8 SL and QFN-10 (2mmx3mm) Packages

APPLICATIONS

- High-Current Cooling Fans
- Personal Computers or CPU Fans
- Single-Phase BLDC Fans

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6651GSS-xxxx**	SOIC-8 SL	*See Below*	1
MP6651GD-xxxx**	QFN-10 (2mmx3mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP6651GSS-xxxx-Z).

** "-xxxx" is the configuration code identifier. The first four digits of the suffix (-xxxx) can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number, even if ordering the "-0000" code.

TOP MARKING (MP6651GSS-xxxx)

MP6651
LLLLLLLL
MPSYWW

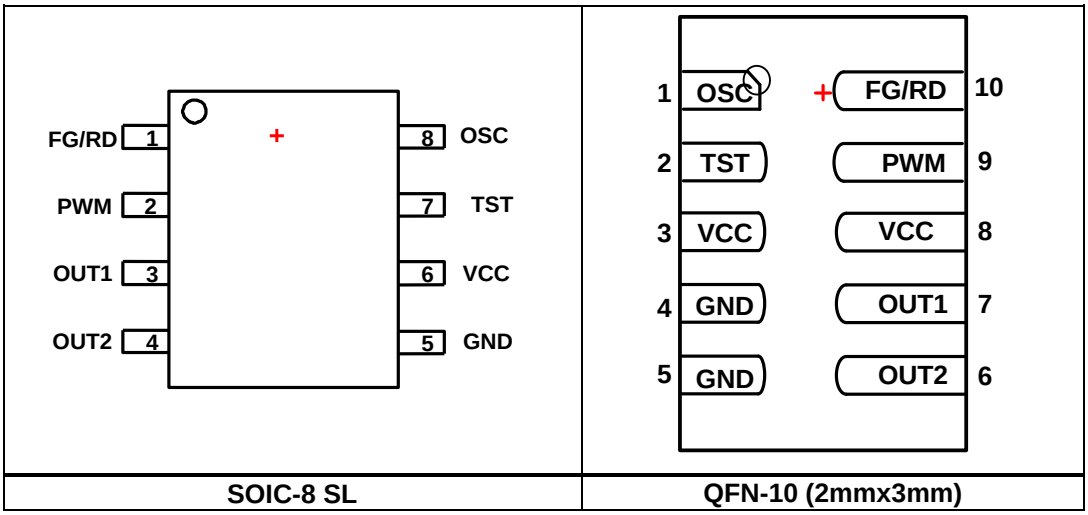
MP6651: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

TOP MARKING (MP6651GD-xxxx)

BMZ
YWW
LLLL

BMZ: Product code of MP6651GD-xxxx
Y: Year code
WW: Week code
LLLL: Lot number

PACKAGE REFERENCE



SOIC-8 SL	QFN-10 (2mmx3mm)

PIN FUNCTIONS

SOIC-8 SL Pin #	QFN-10 Pin #	Name	Description
1	10	FG/RD	**Selectable for speed indication or rotor lock indication.**
2	9	PWM	**PWM input pin for speed control.** A 2kHz to 100kHz PWM input is recommended in normal operation.
3	7	OUT1	**Motor driver output 1.** The OUT1 pin is low when the Hall signal is low logic.
4	6	OUT2	**Motor driver output 2.** The OUT2 pin is low when the Hall signal is high logic.
5	4, 5	GND	**Ground.**
6	3, 8	VCC	**Input power pin.**
7	2	TST	**Test pin.** Connect to GND.
8	1	OSC	**Internal oscillator setting pin.** Connect a 20kΩ (1% or higher accuracy) resistor from OSC to ground.

ABSOLUTE MAXIMUM RATINGS (1)

V_{CC}, FG/RD, PWM ..... -0.3V to +24V
$V_{OUT1/2}$ .....-0.3V to V_{CC} + 0.3V
All other pins..... -0.3V to +5.5V
Continuous power dissipation (T_A = 25°C) (2)
SOIC-8 SL 1.3W
QFN-10.....1.9W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature..... -60°C to +150°C

ESD Ratings

Human body model (HBM)……±2kV
Charged device model (CDM)……..±2kV

Recommended Operating Conditions (3)

Supply voltage (V_{CC}) ..... 3.3V to 18V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC-8 SL……96.....45.....°C/W
QFN-10 (2mmx3mm)……..65.....12....°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{VCC} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol		Min	Typ	Max	Units
Input UVLO rising threshold	V_{UVLO}			3	3.3	V
Input UVLO hysteresis				0.17		V
Operating supply current	I_{CC}			5.4	6.6	mA
PWM input high voltage	V_{PWMH}		1.5			V
PWM input low voltage	V_{PWML}				0.4	V
PWM input internal pull-up resistance				190		kΩ
HS switch on resistance	$R_{HS(ON)}$	SOIC-8 SL package, I_{OUT} = 100mA		120		mΩ
		QFN 10, I_{OUT} = 100mA		52		mΩ
LS switch on resistance	$R_{LS(ON)}$	SOIC-8 SL package, I_{OUT} = 100mA		95		mΩ
		QFN-10 package, I_{OUT} = 100mA		44		mΩ
Cycle-cycle current limit	I_{OCP}	OCP_SEL = 11		4		A
		OCP_SEL = 10		3		A
Over-voltage protection rising threshold	V_{OVP_R}		18	19	20	V
Over-voltage protection falling threshold	V_{OVP_F}		17	18	19	V
Over-voltage protection hysteresis	V_{OVP_HYS}			1		V
PWM output frequency	f_{SW}	R_{OSC} = 20kΩ		27		kHz
FG output low-level voltage	V_{FG_L}	$I_{FG/RD}$ = 1mA		0.19		V
Soft turn-on angle at 100% PWM out duty cycle	θ_{SON}	SON_ANG = 11111		45		deg
Soft turn-off angle at 100% PWM out duty cycle	θ_{SOFF}	SOFF_ANG = 11111		45		deg
Rotor lock detection time	t_{RD}		0.52	0.6		sec
Minimum recommended magnetic field					±2	mT
Thermal shutdown threshold (5)			150	160	180	°C
Thermal shutdown hysteresis (5)				40		°C

Note:

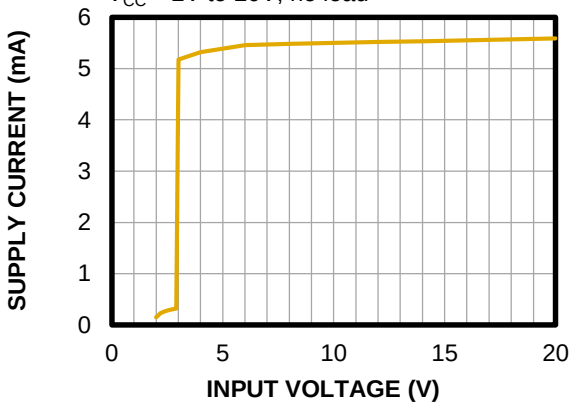
5) Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 12V, T_A = 25°C, unless otherwise noted.

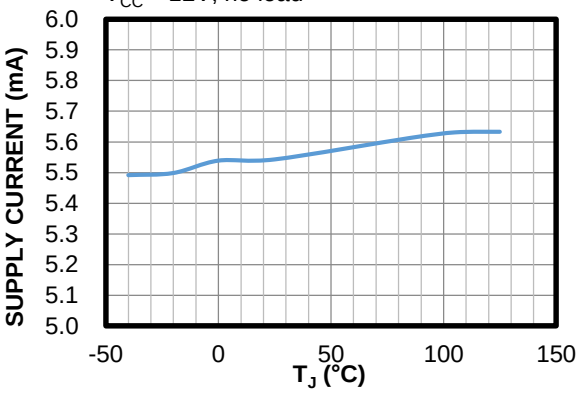
Supply Current vs. Input Voltage

V_{CC} = 2V to 20V, no load

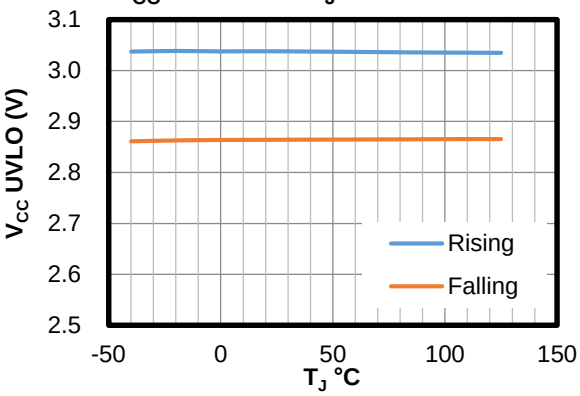


Supply Current vs. T_J

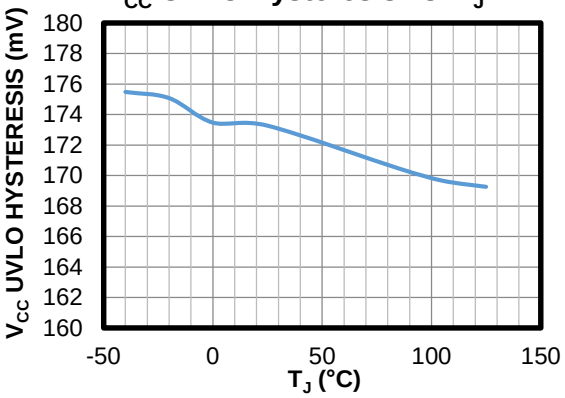
V_{CC} = 12V, no load



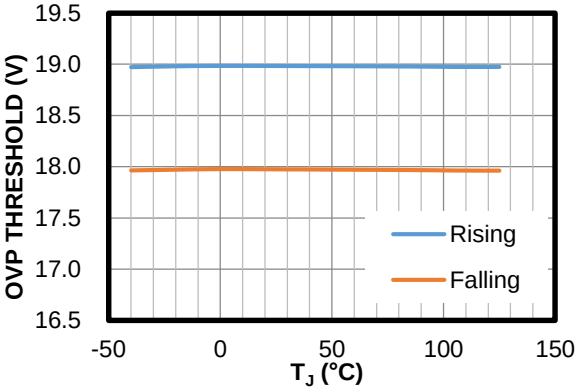
V_{CC} UVLO vs. T_J



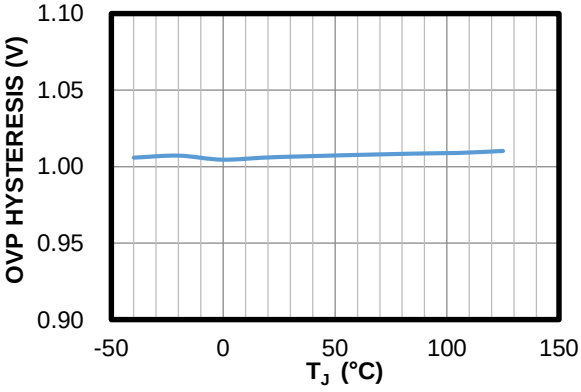
V_{CC} UVLO Hysteresis vs. T_J



OVP Threshold vs. T_J



OVP Hysteresis vs. T_J

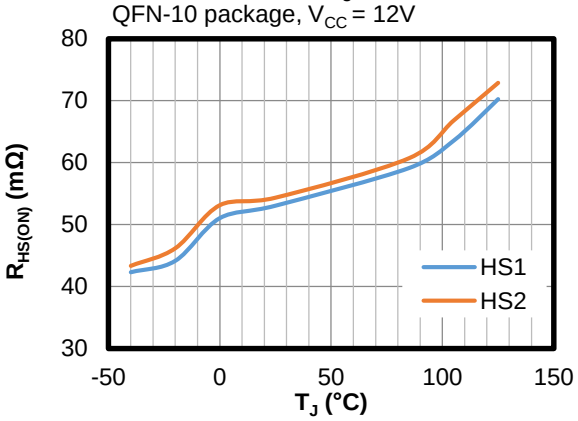


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{CC} = 12V, T_A = 25°C, unless otherwise noted.

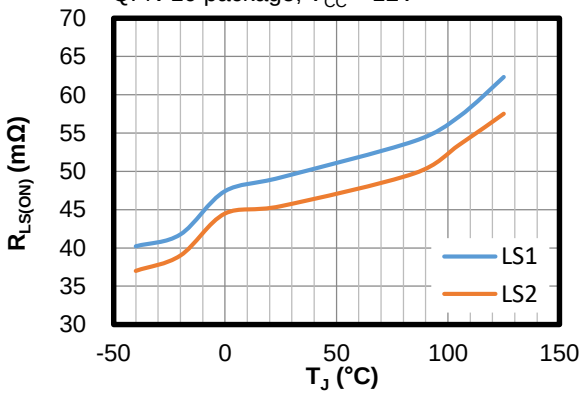
High-Side MOSFET On Resistance vs. T_J

QFN-10 package, V_{CC} = 12V



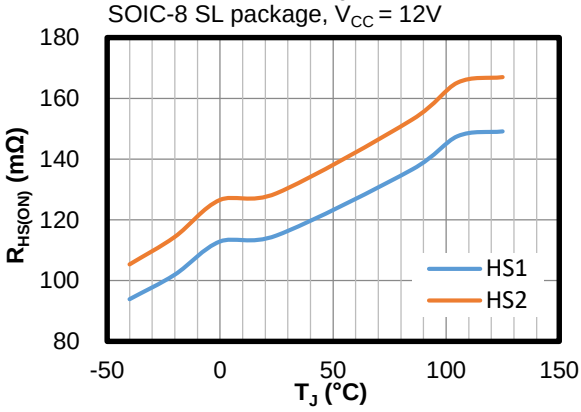
Low-Side MOSFET On Resistance vs. T_J

QFN-10 package, V_{CC} = 12V



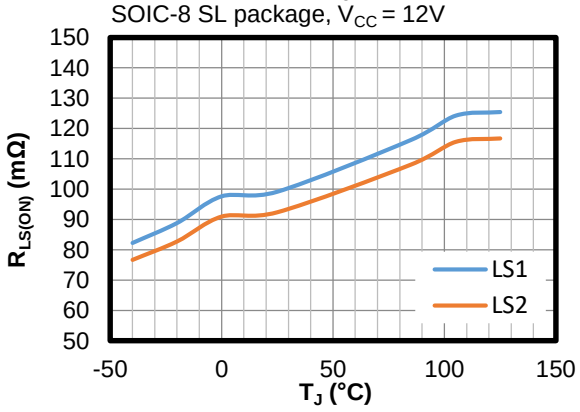
High-Side MOSFETs On Resistance vs. T_J

SOIC-8 SL package, V_{CC} = 12V



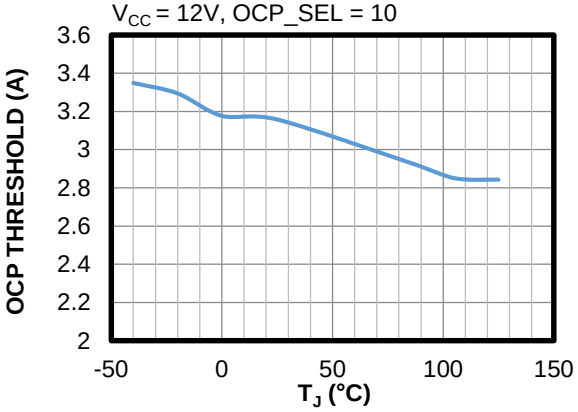
Low-Side MOSFETs On Resistance vs. T_J

SOIC-8 SL package, V_{CC} = 12V



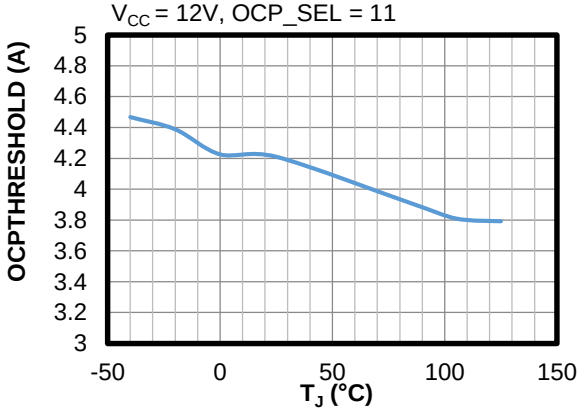
OCP Threshold Vs. T_J

V_{CC} = 12V, OCP_SEL = 10



OCP Threshold vs. T_J

V_{CC} = 12V, OCP_SEL = 11

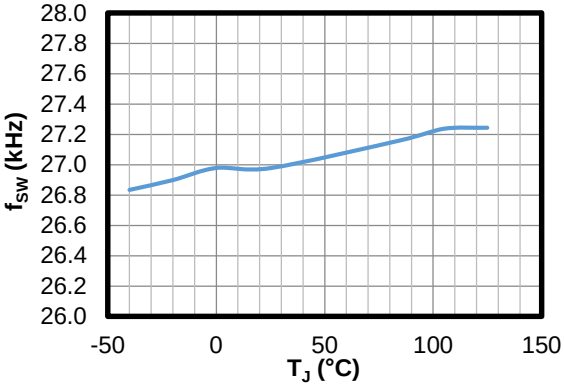


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{CC} = 12V, T_A = 25°C, unless otherwise noted.

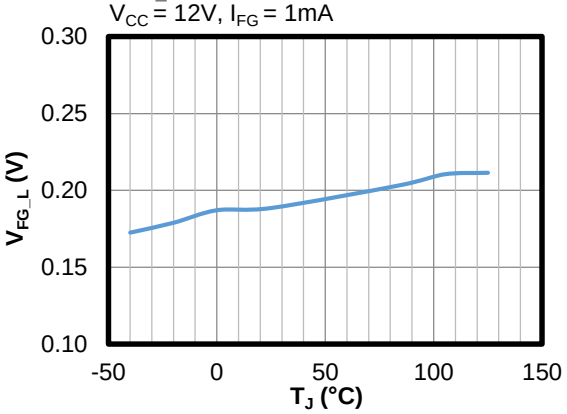
PWM Output Frequency vs. T_J

V_{CC} = 12V



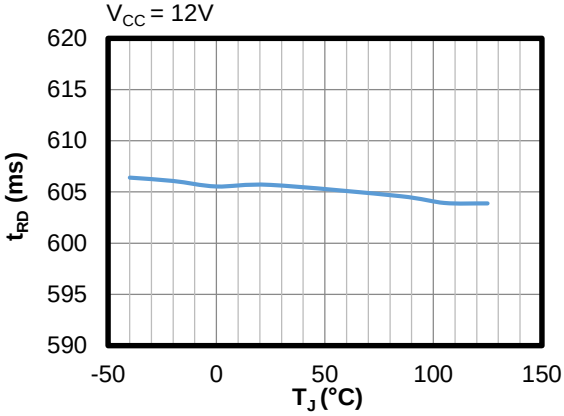
V_{FG_L} Vs. T_J

V_{CC} = 12V, I_{FG} = 1mA



Rotor Lock Detection Time vs. T_J

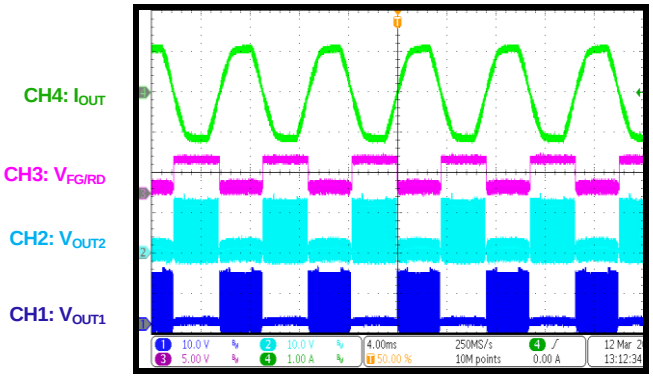
V_{CC} = 12V



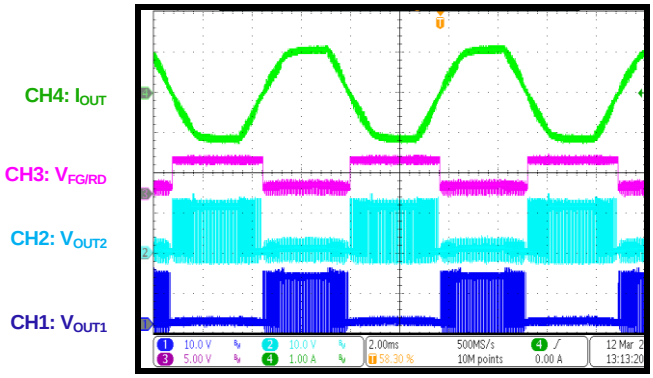
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{CC} = 12V, T_A = 25°C, 12V/0.8A, 8025 axial fan, DIN_MIN = 5%, DO_MIN = 5%, SPD_ZERO = 1, unless otherwise noted.

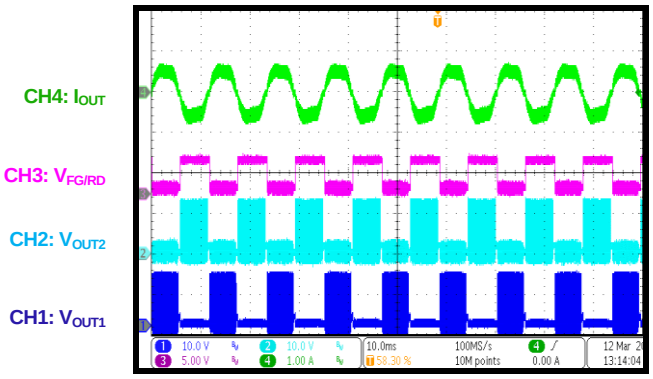
Steady State
Input PWM duty cycle = 100%



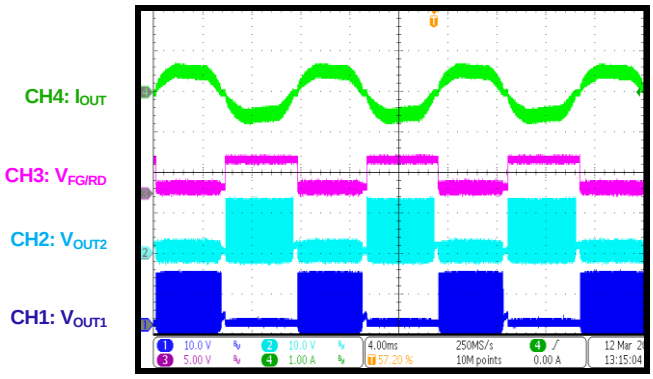
Steady State
Input PWM duty cycle = 100%



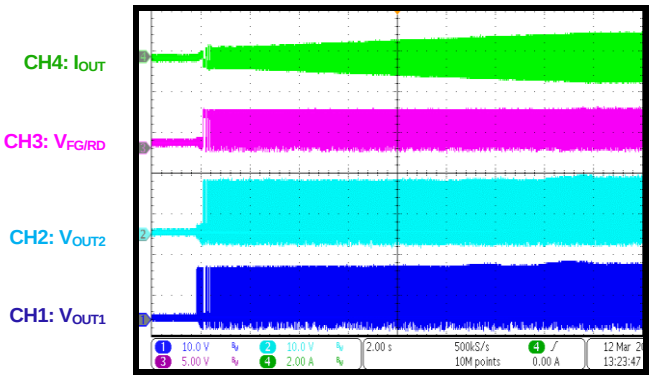
Steady State
Input PWM duty cycle = 50%



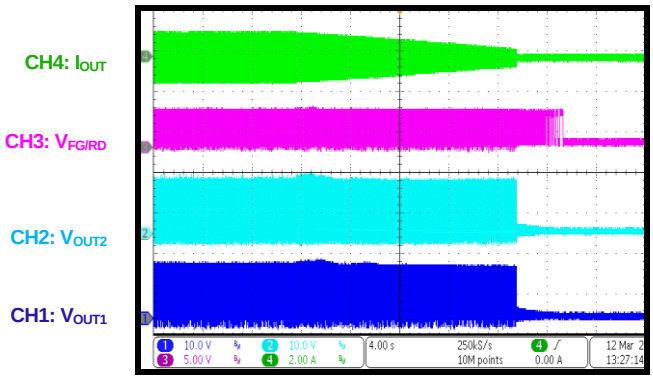
Steady State
Input PWM duty cycle = 50%



PWM On
Input PWM duty cycle rises from 0% to 100%



PWM Off
PWM duty cycle falls from 100% to 0%

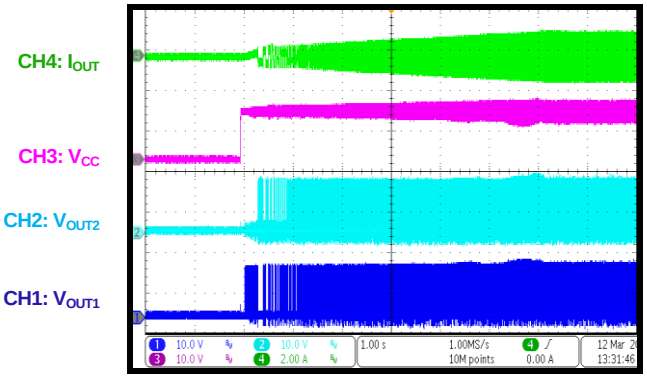


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{CC} = 12V, T_A = 25°C, 12V/0.8A, 8025 Axial Fan, DIN_MIN = 5%, DO_MIN = 5%, SPD_ZERO = 1, unless otherwise noted.

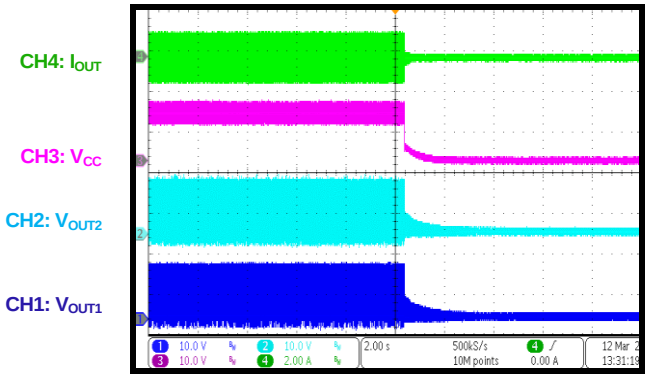
VIN On

VCC rises from 0V to 12V, input PWM duty is 100%



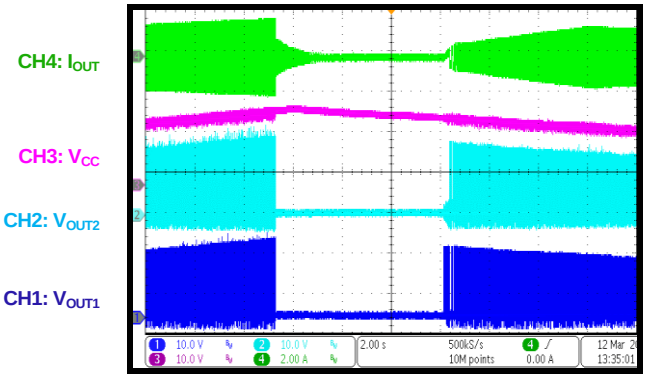
VIN Off

VCC falls from 12V to 0V, input PWM duty is 100%



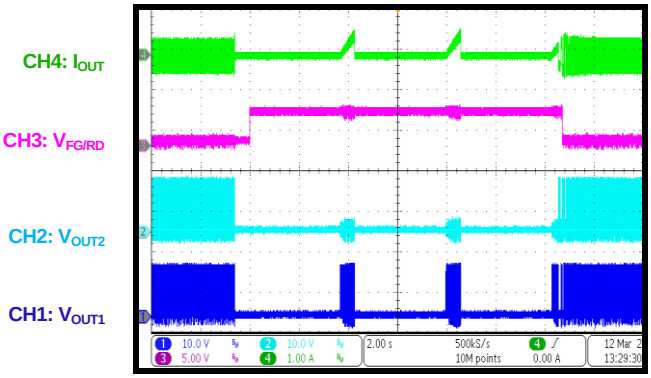
OVP

Input PWM duty = 100%, ramp up/down VCC

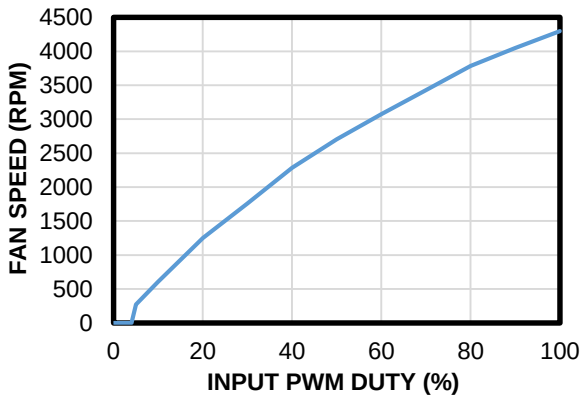


Rotor Lock

Input PWM duty = 25%, lock rotor, FG/RD pin configured as RD



Fan Speed Vs. Input PWM Duty



FUNCTIONAL BLOCK DIAGRAM

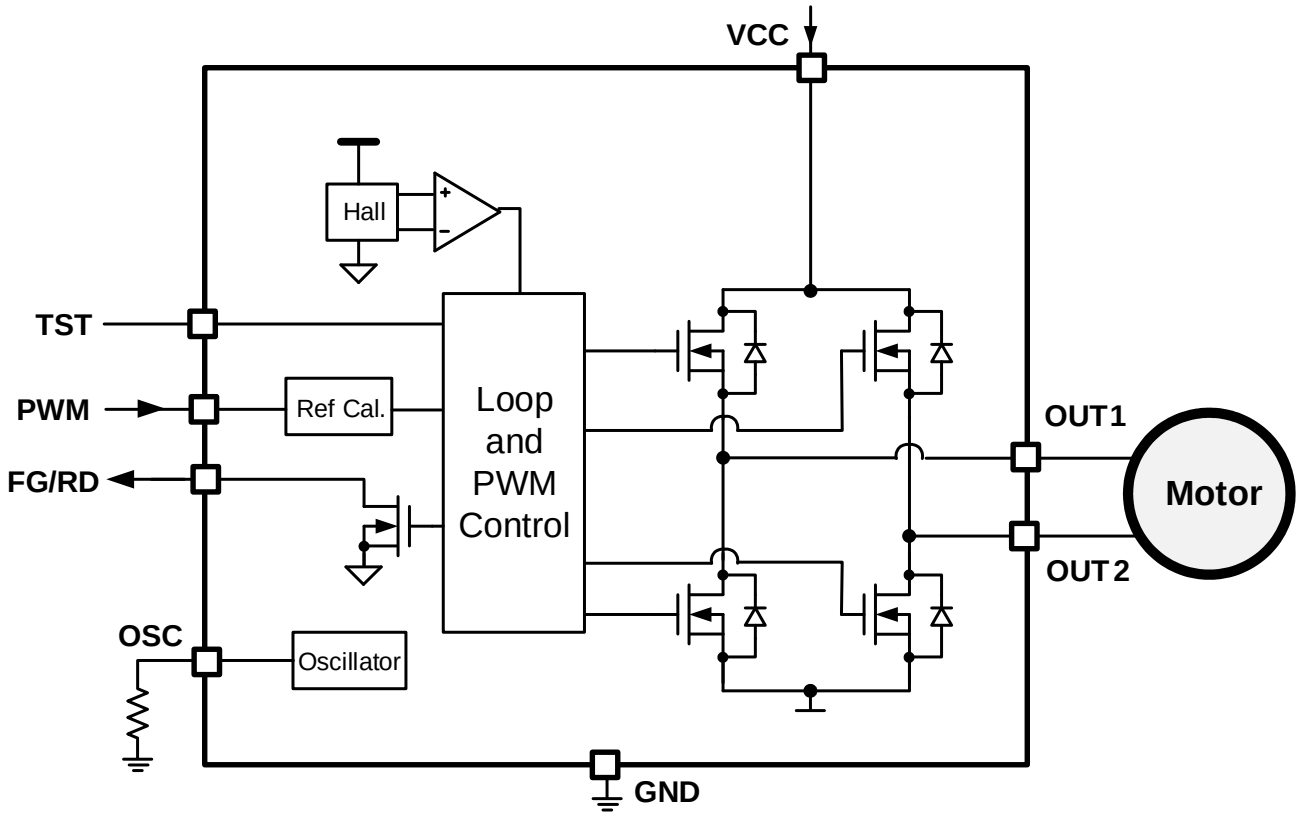


Figure 1: Functional Block Diagram

OPERATION

The MP6651 is a single-phase, brushless DC (BLDC) motor driver with integrated power MOSFETs and a Hall-Effect sensor. The MP6651 controls the motor speed through the PWM signal on the PWM pin. It features a configurable soft-on/off commutation and a Hall offset angle across the full speed range. This offset angle can be adjusted to optimize low-speed and high-speed performance.

Robust protection includes input over-voltage protection (OVP), under-voltage lockout (UVLO), locked rotor protection, over-current protection (OCP), and thermal shutdown protection.

Speed Control

The PWM signal on the PWM pin accepts a wide input frequency range (2kHz to 100kHz). The device adjusts the motor speed by detecting the PWM signal duty cycle.

The OUT1/2 pins' output duty cycle directly depends on the PWM input duty cycle. The DIN_MIN bits set the starting duty cycle, while the DO_MIN bits set the OUT1/2 output duty cycle when the input PWM duty cycle is set to DIN_MIN.

When the PWM input duty cycle is below the duty cycle set by DIN_MIN, the fan speed supports three modes, described below.

1. If SPD_ZERO = 0 and MAX_EN = 0: When the input duty cycle is below the value set by DIN_MIN, the OUT1/2 output duty cycle stays at the minimum duty cycle set by DO_MIN (see Figure 2).

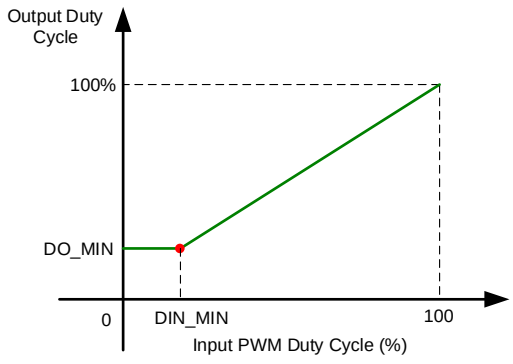


Figure 2: Speed Curve (SPD_ZERO = 0, MAX_EN = 0)

2. SPD_ZERO = 0, MAX_EN = 1: When the input duty cycle is below the value set by DIN_MIN, the OUT1/2 output duty cycle is at 100% (see Figure 3).

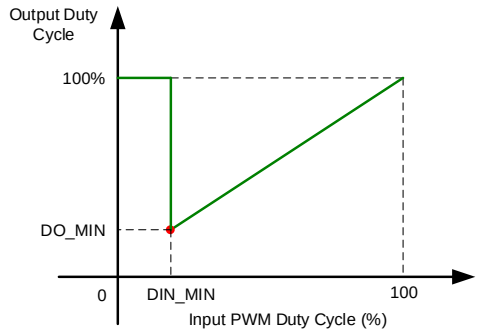


Figure 3: Speed Curve (SPD_ZERO = 0, MAX_EN = 1)

3. SPD_ZERO = 1: The OUT1/2 output duty stays at 0 (see Figure 4).

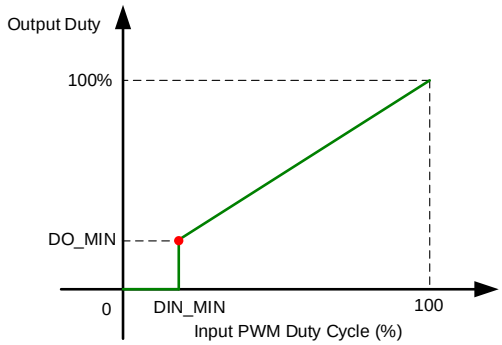


Figure 4: Speed Curve (SPD_ZERO = 1)

OUT1/2 Normal Operation

To reduce speed variation and increase system efficiency during normal operation, the MP6651 controls the H-bridge MOSFET switching according to the timing sequence (see Figure 5). The operation sequence is based on the embedded Hall-effect sensor signal:

All operation sequences are based on the Hall signal coming from the embedded hall sensor (see Figure 5 on page 14). HALL_TRIM is the signal with a Hall offset angle (maximum 45° phase shift), based on Hall signal. When the HALL_TRIM signal is high, OUT2 stays low while OUT1 switches. When the HALL_TRIM signal is low, OUT1 stays low while OUT2 switches.

In addition, the hall offset angle can be set by the PWM input duty cycle.

- The Hall offset angle is dependent on HAL_ANG1 when the input duty cycle is below DIN_HAL_L/ 64.
- The Hall offset angle is dependent on HAL_ANG2 when the input duty cycle is between (DIN_HAL_L/ 64) and (DIN_HAL_H/ 64).
- The Hall offset angle is dependent on HAL_ANG3 when the input duty cycle exceeds DIN_HAL_H/ 64.
- The hall offset angle leading/lagging direction is set by HAL_FLAG

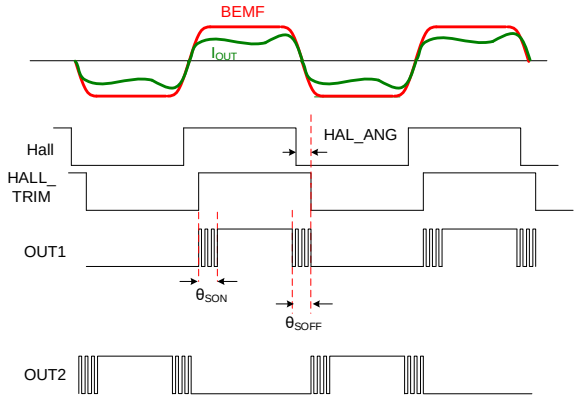


Figure 5: Hall Offset Angle and Soft Commutation

Soft-On Commutation

During soft-on commutation the switching phase's output duty cycle gradually rises from 0% duty cycle to a steady duty cycle (see θ_{SON} in Figure 5). The soft-on commutation angle is configured by SON_ANG. The maximum commutation angle is 45°, and the resolution is 1.4°.

Soft-Off Commutation

During soft-off commutation, the switching phase's output duty gradually drops from a steady duty cycle to 0% duty cycle (see θ_{SOFF} in Figure 5). The soft-off commutation angle is configured by SOFF_ANG. The maximum commutation angle is 45°, and the resolution is 1.4°.

Advanced Soft Off

The advanced soft-off angle can make soft-off commutation begin earlier. During soft-on and soft-off commutation, the PWM output duty cycle ramps up and ramp down (see Figure 6). The advanced soft-off angle (θ_{ADV} in Figure 6) gives a leading angle at which soft-off commutation begins. The advanced soft-off angle is set by register SOFFADV, with a maximum of 45°.

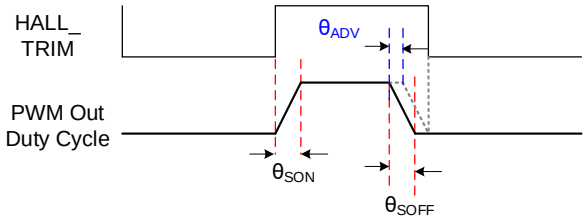


Figure 6: Advanced Soft Off Angle

Standby Mode

Standby mode is enabled or disabled by the internal STB bit. Standby mode is disabled by default. When standby mode is enabled, the device enters standby mode if the following conditions are met:

- VCC is powered
- The PWM input stay low
- No Hall signal edge is detected for 600ms

In standby mode, most internal circuitry is turned off to reduce power consumption. The standby current is about 750μA. Once the PWM pulse is received on the PWM pin, the device exits from standby mode.

Pre Start-Up Timer

With VCC is powered, the device first increases the output duty cycle gradually before the speed is taken over by the PWM duty cycle. This transition is triggered by the timer set by DUTY_SLOPE[1:0].

- DUTY_SLOPE = 0: Timer period is 9.3ms
- DUTY_SLOPE = 1: Timer period is 4.6ms
- DUTY_SLOPE = 2: Timer period is 2.3ms
- DUTY_SLOPE = 3: Timer period is 1.2ms

A longer timer period leads to a lower soft pre-start current and a longer pre start-up time.

Soft-Start Time

To reduce the input inrush current during start-up, the MP6651 provides a configurable soft-start time for the speed reference by setting TIME_SS (from 2.4s to 19.2s).

Oscillator Frequency Setting

To provide an accurate clock time for speed control, a high-accuracy, 20kΩ resistor must be connected between the OSC pin and ground. The switching frequency (f_{SW}) is about 27kHz.

The OSC resistor must be 20kΩ.

Digital Oscillator Frequency

The internal digital clock is used for digital block including the Hall angle calculation, which is selected by the SPD_SEL bits. A higher frequency leads to a higher calculation resolution and a higher minimum speed.

Cycle-by-Cycle Over-Current Protection (OCP)

During normal switching, if the current flowing through the high-side MOSFET (HS-FET) of the H-bridge exceeds the threshold set by the OCP_SEL bits after a blanking time, the HS-FET turns off and low-side MOSFET (LS-FET) turns on immediately. The device resumes to normal switching in the next switching cycle. The overload current limit threshold has four configurable thresholds with a maximum of 4A.

Speed Detection

The FG signal on the FG/RD pin outputs an internal Hall change signal for speed indication. Different FG signal frequencies include 1x, 1/2x, 2/3x and 2x the Hall frequency. This is selected by corresponding register bits.

FG/RD is an open-drain output that must be externally pulled up in normal operation.

Rotor Dead Lock Protection (RD)

In motor rotor lock protection, the MP6651 turns on both LS-FETs if there is no Hall signal edge detected during the 0.6s detection time. The device automatically restarts after a recovery time set by the LOCK_SEL bits. By setting FGRD_SEL to 11, the signal on the FG/RD pin is selected for rotor lock indication. During a rotor lock fault, the signal stays high by setting RD_H_L to 1 while the signal stays low by setting RD_H_L to 0.

Over-Voltage Protection (OVP)

If VCC pin voltage exceeds the over-voltage (OV) threshold (about 19V), the device turns off the HS-FETs and turns on the LS-FETs. The device resumes normal operation after V_{CC} drops below 18V.

Thermal Shutdown (TSD)

Thermal monitoring is provided. If the die temperature rises above 160°C, the MOSFETs of the switching half-bridge turn off. Operation automatically resumes when the die temperature drops below 120°C.

Under-Voltage Lockout (UVLO)

When the voltage on the VCC pin falls below the under-voltage lockout (UVLO) threshold, all circuitry in the device is disabled, and the internal logic is reset. Operation resumes when V_{CC} rises above the UVLO threshold.

Test Mode and Factory Mode

To configure the internal register, the MP6651 has a test mode. In test mode, all internal registers can be read/written. After the design finalized, the register value can be configured non-volatile memory (NVM). The NVM can be configured twice. Refer to the MPS Fan Driver GUI Software for more details.

REGISTER MAP

Add	D7	D6	D5	D4	D3	D2	D1	D0
00h OTP/REG (6)	RESERVED	SPD_SEL[1:0]		SOFFADV[4:0]				
03h OTP/REG	DO_MIN[7:0]							
04h OTP/REG	DIN_MIN[7:0]							
06h OTP/REG	TIME_SS[2:0]			RVSI_EN	RESERVED			
07h OTP/REG	SPD_ZERO	OCP_SEL[1:0]		SON_ANG[4:0]				
08h OTP/REG	RD_H_L	LOCK_SEL[1:0]		SOFF_ANG[4:0]				
09h OTP/REG	RESERVED		HAL_FLAG	HAL_ANG1[4:0]				
0Ah OTP/REG	RESERVED			HAL_ANG2[4:0]				
0Bh OTP/REG	DUTY_SLOPE[1:0]		RESERVED	HAL_ANG3[4:0]				
0Ch OTP/REG	FGRD_SEL[1:0]		DIN_HAL_L[5:0]					
0Dh OTP/REG	RESERVED		DIN_HAL_H[5:0]					
0Eh OTP/REG	RESERVED			STB	2FG	MAX_EN	Reserved	
0Fh REG (7)	OTP_PAGE[1:0]		RESERVED					

Note:

6) OTP/REG means that programming is accomplished through the one-time programmable (OTP) memory and the register write/read options.
7) REG means that programming is accomplished through the register, and not through OTP memory.

REG00h

Addr: 0x00				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7	RESERVED	N/A	0	Reserved.
[6:5]	SPD_SEL[1:0]	OTP/REG	00	Selects the digital clock. A higher frequency results in a higher calculation resolution and a higher minimum speed. 00: Minimum speed is 100rpm 01: Minimum speed is 400rpm 10: Minimum speed is 800rpm 11: Minimum speed is 1600rpm
[4:0]	SOFFADV	OTP/REG	00	Sets the advanced soft-off angle, which is the angle when the soft-off transition begins. 0x00: 1.4° 0x01: 2.8° … 0x1F: 45°, 1.4°/step

REG03h

Addr: 0x03				
Bit	**Bit Name**	**Access**	**Default**	**Description**
[7:0]	DO_MIN[7:0]	OTP/REG	0x33	Sets the output PWM duty when the input PWM duty = DIN_MIN. The minimum output duty cycle can be calculated with the following calculation: Minimum output duty cycle = DO_MIN / 255

REG04h

Addr: 0x04				
Bit	**Bit Name**	**Access**	**Default**	**Description**
[7:0]	DIN_MIN[7:0]	OTP/REG	0x33	Sets the input PWM starting duty cycle. The corner duty, MAX_EN, and SPD_ZERO selects different curve. The starting duty cycle can be calculated with the following equation: Starting duty cycle = DIN_MIN / 255

REG06h

Addr: 0x06				
Bit	**Bit Name**	**Access**	**Default**	**Description**
[7:5]	TIME_SS[2:0]	OTP/REG	010	Sets the soft transition time. The transition time for the PWM output duty cycle is between 0% and 100% 000: 2.4s 001: 4.8s 010:7.2s (default) 011:9.6s 100: 12s 101:14.4s 110: 16.8s 111: 19.2s
4	RVSI_EN	OTP/REG	1	Enables reverse current detection. 0: Disabled 1: Enabled
[3:0]	RESERVED	N/A	0x0B	Reserved.

REG07h

Addr: 0x07				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7	SPD_ZERO	OTP/REG	1	Sets the speed when the input PWM duty cycle is below DIN_MIN. 0: Keep the speed set by DIN_MIN or maximum speed 1: The speed is zero
[6:5]	OCP_SEL[1:0]	OTP/REG	11	Sets the current limit. 00:1A 01: 2A 10:3A 11: 4A
[4:0]	SON_ANG[4:0]	OTP/REG	0x1F	Sets the soft-on phase transition angle. 0x00: 1.4° 0x01: 2.8° … 0x1F: 45°, 1.4°/step

REG08h

Addr: 0x08				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7	RD_H_L	OTP/REG	1	Selects whether RD outputs high or low during rotor lock protection. 0: RD outputs low in rotor lock protection, 1: RD outputs high in rotor lock protection.
[6:5]	LOCK_SEL[1:0]	OTP/REG	00	Sets the rotor lock retry time. 00:3.6s 01: 4.8s 10:8s 11: 8.4s
[4:0]	SOFF_ANG[4:0]	OTP/REG	0x1F	Sets the soft-off phase transition angle. 0x00: 1.4° 0x01: 2.8° … 0x1F: 45°, 1.4°/step

REG09h

Addr: 0x09				
Bit	**Bit Name**	**Access**	**Default**	**Description**
[7:6]	RESERVED	N/A	0	Reserved.
5	HAL_FLAG	OTP/REG	0	Sets whether the Hall offset angle is leading or lagging. 0: Lagging 1: Leading
[4:0]	HAL_ANG1[4:0]	OTP/REG	0x00	Sets the hall offset angle when the PWM duty cycle < DIN_HAL_L. 0x00: 1.4° 0x01:2.8° … 0x1F: 45°, 1.4°/step

REG0Ah

Addr: 0x0A				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:5	NA	NA	0	Reserved
4:0	HAL_ANG2[4:0]	OTP/REG	0x00	Sets the hall offset angle when DIN_HAL_L < PWM duty cycle < DIN_HAL_H. 0x00: 1.4° 0x01:2.8° … 0x1F: 45°, 1.4°/step

REG0Bh

Addr: 0x0B				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:6	DUTY_SLOPE[1:0]	OTP/REG	00	Sets the pre start-up timer. 00: 9.3ms 01: 4.6ms 10: 2.3ms 11: 1.2ms
5	NA	NA	1	Reserved.
4:0	HAL_ANG3[4:0]	OTP/REG	0x00	Sets the Hall offset angle when the PWM duty cycle > DIN_HAL_H. 0x00: 1.4° 0x01:2.8° …0x1F: 45°, 1.4°/step

REG0Ch

Addr: 0x0C				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:6	FGRD_SEL[1:0]	OTP/REG	00	Selects the FG/RD pin's output. 00: 1x 01: 1/2x 11: RD When FGRD_SEL = 10, select 2/3x or 2x based on the depending 2FG bit (REG0Eh, bit[3]). If 2FG = 0, then FGRD_SEL = 10: 2/3x If 2FG = 1, then FGRD_SEL = 10: 2x
5:0	DIN_HAL_L[5:0]	OTP/REG	0x10	Selects the input PWM duty cycle low threshold for Hall offset angle compensation. The duty cycle can be calculated with the following equation: Duty = DIN_HAL_L / 64

RED0Dh

Addr: 0x0D				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:6	RESERVED	N/A	00	Reserved.
5:0	DIN_HAL_H[5:0]	OTP/REG	0x30	Selects the input PWM duty cycle high threshold for Hall offset angle compensation. The duty cycle can be calculated with the following equation: Duty = DIN_HAL_H / 64

REG0Eh

Addr: 0x0E				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:5	RESERVED	N/A	0	Reserved.
4	STB	OTP/REG	0	Enables standby mode. 0: Disabled 1: Enabled
3	2FG	OTP/REG	0	When FGRD_SEL = 10, this bit selects whether the FG/RD's output is 2/3x or 3x. If 2FG = 0, then FGRD_SEL = 10: 2/3x If 2FG = 1, then FGRD_SEL = 10: 2x
2	MAX_EN	OTP/REG	0	Enables maximum speed when the input PWM duty cycle < DIN_MIN. This bit is active only when SPD_ZERO = 0. 0: Disabled 1: Enabled
1:0	RESERVED	N/A	00	Reserved.

REG0Fh

Addr: 0x0F				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:6	OTP_PAGE[1:0]	REG	00	One-time programmable (OTP) memory page indicator, read-only. 00: No OTP (default) 01: 1st page of OTP is programmed 10: 2nd page of OTP is programmed
5:0	RESERVED	N/A	N/A	Reserved.

APPLICATION INFORMATION

Selecting the Input Capacitor

Place an input capacitor near VCC and GND pins, and as close as possible to these pins to keep the input voltage stable and reduce input voltage noise. The input capacitor impedance must be low at the switching frequency.

Ceramic capacitors with X7R dielectrics are recommended for their low-ESR characteristics.

The capacitance of ceramic capacitor drops when the voltage across capacitor rises, the ceramic capacitor can lose more than 50% of its capacitance when the voltage across capacitor reaches its rated voltage. Leave enough voltage margin when select capacitor, and the input capacitance must exceed 10μF.

For certain applications, add an additional, larger-value electrolytic capacitor to absorb motor energy.

Embedded Hall Position

Figure 7 shows the MP6651's embedded Hall position with the SOIC-8 SL package.

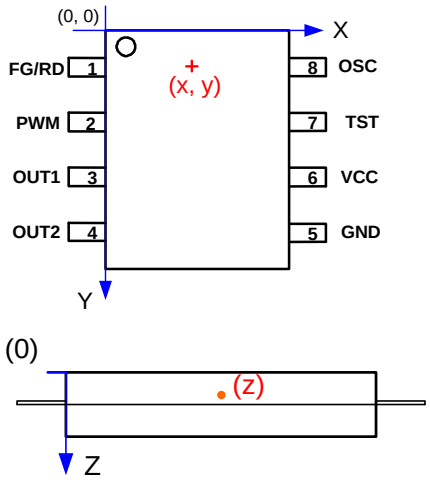


Figure 7: Hall Position with SOIC-8 SL Package

Where x = 1951μm ±50μm; y = 1487μm ±50μm; and z = 540μm ±25μm.

Figure 8 shows the MP6651's embedded Hall position with the QNF-10 package.

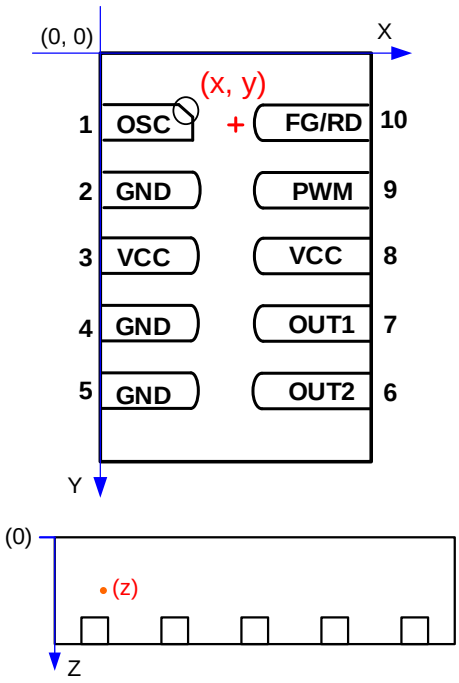


Figure 8: Hall Position with QFN-10 Package

Where x = 1003μm ±40μm; y = 620μm ±40μm; and z = 370μm ±40μm.

Selecting the Reverse Blocking Diode

To avoid damage when the fan experiences a reverse plug-in, a reverse blocking diode is required. The reverse blocking diode can also prevent the bus voltage from charging in the event of a reverse current.

The maximum reverse voltage rating of the reverse blocking diode should exceed 30V, and the forward current rating must exceed the input current.

Selecting the OSC Resistor

An OSC resistor is required to set up the internal clock. The resistance is 20kΩ. A resistor with a higher accuracy is recommended (e.g. a 1% accuracy resistor).

The OSC resistor must be placed closed to IC, and the OSC resistor's GND must be separated from the power path. Otherwise, the internal clock frequency can change under different operating currents.

Input Clamping Circuit

To avoid high-voltage spikes from the energy stored in the motor, a voltage-clamping circuit may be required for applications with a large current or large fan inertial applications (see ZD1 in Figure 10). A 15V/SOD-123 package TVS or Zener diode is sufficient for most 12V input applications. The clamping voltage should be below the OVP threshold.

Typically, the clamping voltage threshold shifts to high when the operating ambient temperature rises.

High-Current Applications

For the MP6651 with the SOIC-8 SL package (the MP6651GSS), the MOSFETs have a higher turn-on resistance, and they cannot support currents above 1.5A. For this device, it is recommended to set the over-current protection (OCP) threshold below 3A. This means that OCP_SEL should be set to 00, 01, or 10.

For the MP6651 with the QFN-10 package, the MOSFETs have a lower turn-on resistance. This device can support applications with currents up to 2A.

In high-current applications, two Schottky diodes (SBD1 and SBD2) are required (see Figure 10 on page 22) The Schottky diodes are paralleled with internal high-side MOSFETs.

The voltage rating of the Schottky diodes must exceed 30V to avoid an over-voltage condition.

Schottky diodes with higher forward current sand lower forward voltages are recommended.

Consider operations under high temperatures; the package with the lower thermal resistance is recommended.

Note that the reverse current of Schottky diode increases when the temperature rises. Ensure that the reverse current is below 5mA when the Schottky diode is at its maximum reverse voltage and at its highest temperature.

PCB Layout Guidelines

For the best results, follow Figure 9 and the guidelines below:

1. Place the input capacitor as close to IC as possible to reduce the noise. The capacitance must exceed 10μF.
2. Use a small-package input capacitor to reduce high-frequency noise. Typically, a 10nF to 100nF capacitor with a 0402 package is recommended.
3. Place the input capacitor close to the IC.
4. Place the OSC resistor close to IC, route this resistor's GND from any power paths.

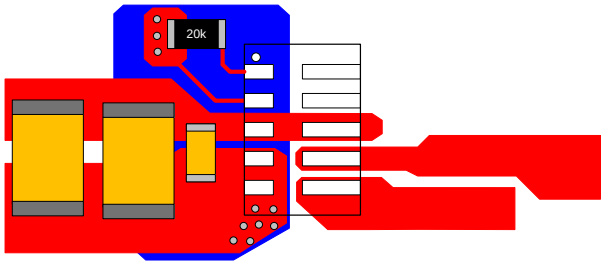


Figure 9: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

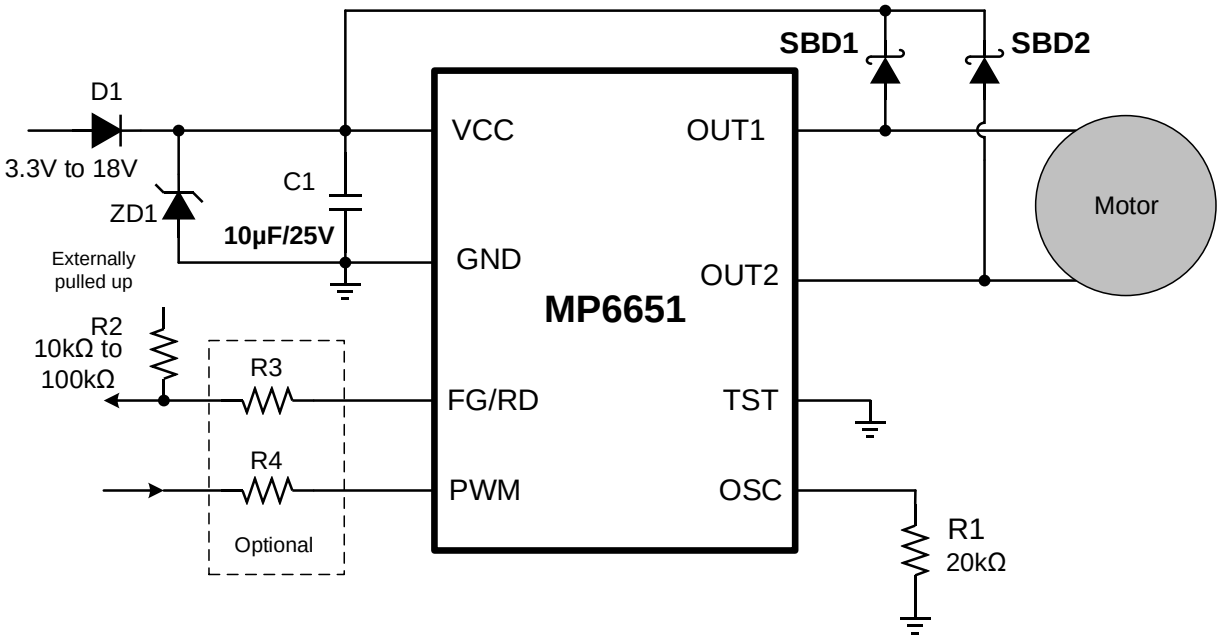


Figure 10: Typical Circuit for High-Current Applications (≥1.5A)

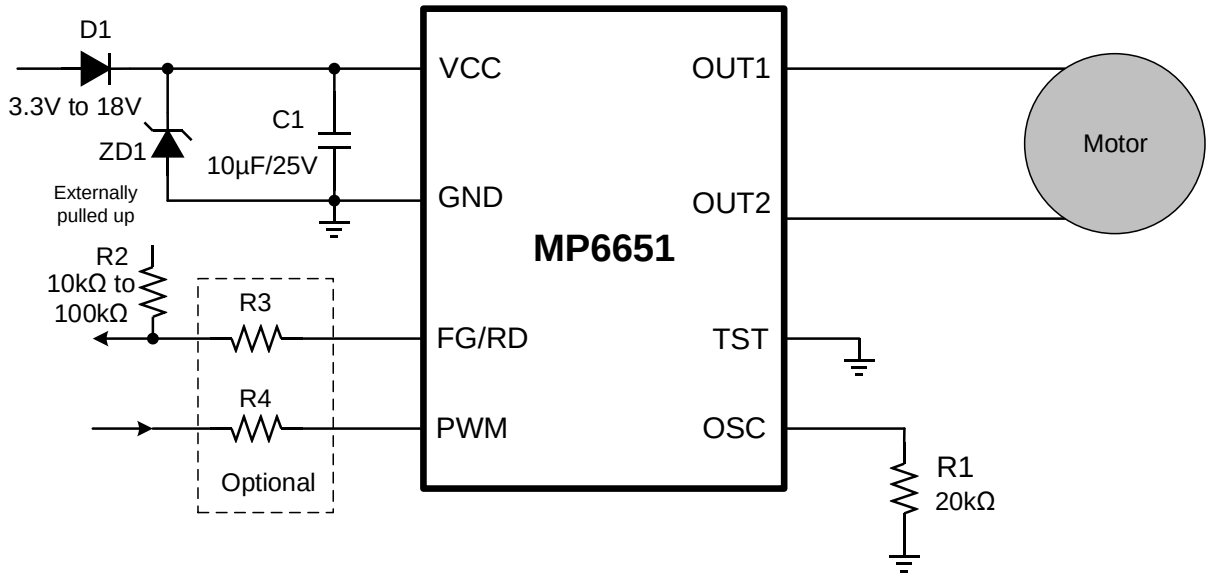
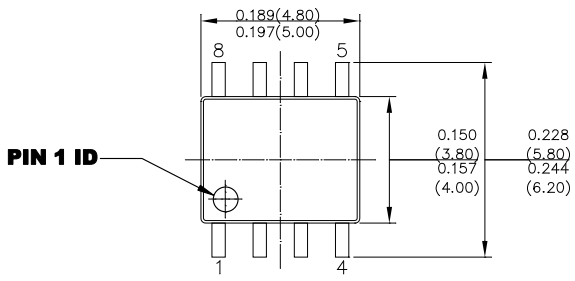


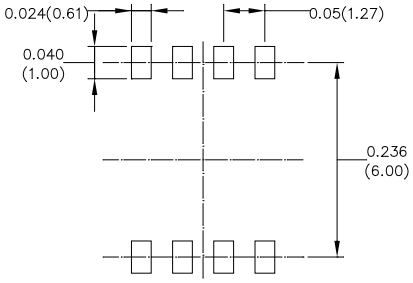
Figure 11: Typical Application Circuit

PACKAGE INFORMATION

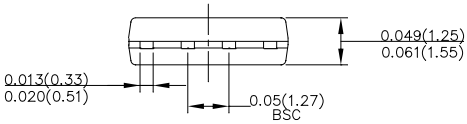
SOIC-8 SL



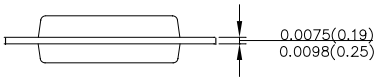
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



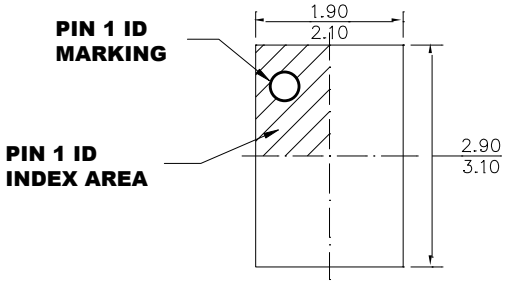
SIDE VIEW

NOTE:

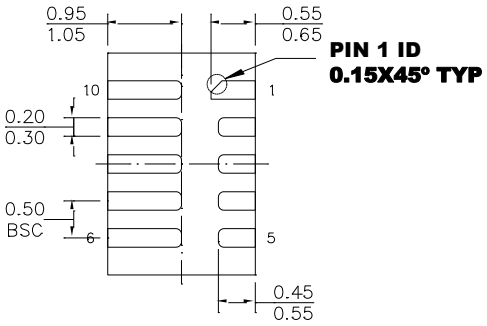
1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING REFERENCE TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

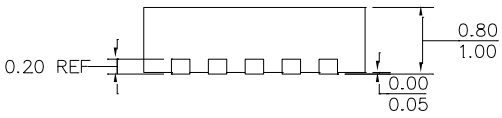
QFN-10 (2mmx3mm)



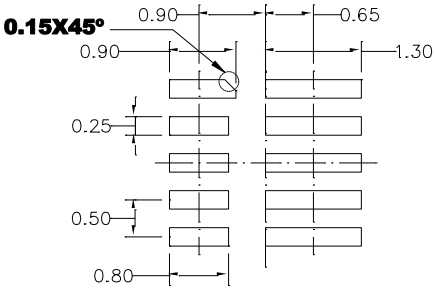
TOP VIEW



BOTTOM VIEW



SIDE VIEW



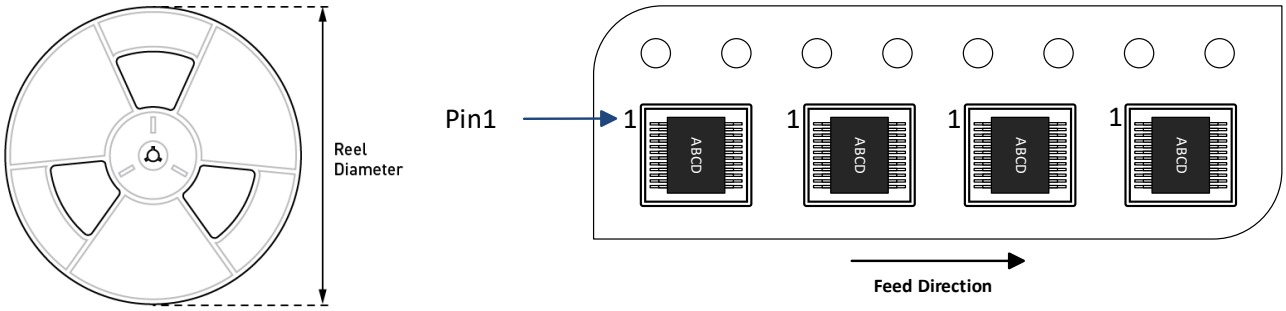
RECOMMENDED LAND PATTERN

NOTE:

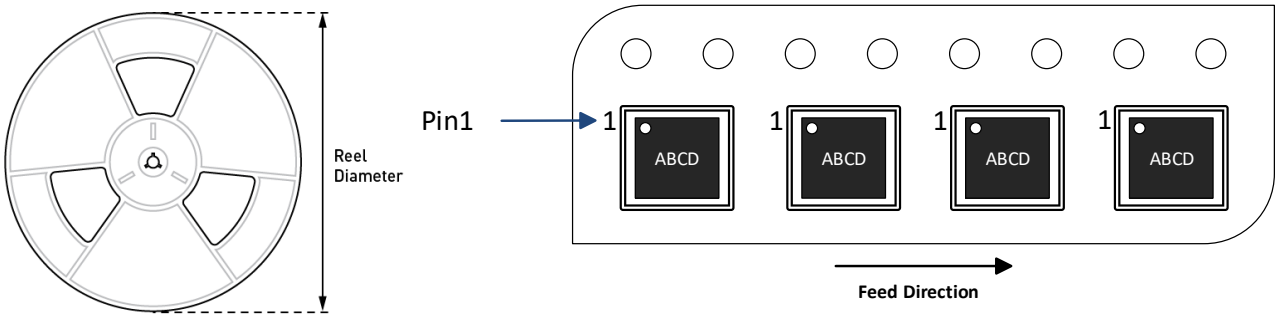
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION

SOIC-8 SL



QFN-10 (2mmx3mm)



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6651GSS-xxxx-Z	SOIC-8 SL	2500	100	N/A	13in	12mm	8mm
MP6651GD-xxxx-Z	QFN-10 (2mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/08/2021	Initial Release	-

单击下面可查看定价，库存，交付和生命周期等信息

>>MPS(芯源系统)