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**maXTouch 640-node Touchscreen Controller**

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**maXTouch<sup>®</sup> Adaptive Sensing Touchscreen Technology**

- Up to 32 X (transmit) lines and 20 Y (receive) lines
- A maximum of 640 nodes can be allocated to the touchscreen
- Touchscreen size 8.91 inches (16:10 aspect ratio), assuming a sensor electrode pitch of 6 mm. Other sizes may be possible with different electrode pitches and appropriate sensor material
- Multiple touch support with up to 16 concurrent touches tracked in real time

**Automotive Applications**

- AEC-Q100 Qualified
- Developed following Automotive SPICE<sup>®</sup> Level 3 certified processes
- CISPR-25 compliant (for both mutual and self capacitance measurements)

**Touch Sensor Technology**

- Discrete/out-cell support including glass and PET film-based sensors
- On-cell/touch-on display support including TFT, IPS and OLED
- Support for standard (for example, Diamond) and proprietary sensor patterns (review of designs by Microchip recommended)

**Front Panel Material**

- Works with PET or glass, including curved profiles (configuration and stack-up to be approved by Microchip)
- Glass 0.5 mm to 2.0 mm (dependent on screen size, touch size, configuration and stack-up)
- Plastic 0.2 mm to 3.0 mm (dependent on screen size, touch size, configuration and stack-up)

**Touch Performance**

- Moisture/Water Compensation
  - No false touch with condensation or water drop up to 22 mm diameter
  - One-finger tracking with condensation or water drop up to 22 mm diameter

- Glove Support
  - Multiple-finger glove touches up to 1.5 mm thickness (subject to stack-up design)
  - Single-finger glove touch up to 5 mm thickness (subject to stack-up design)
- Mutual capacitance and self capacitance measurements supported for robust touch detection
- Noise suppression technology to combat ambient and power-line noise
  - Up to 240 Vpp between 1 Hz and 1 kHz sinusoidal waveform
  - Up to 20 Vpp between 1 kHz and 1 MHz sinusoidal waveform
- Burst Frequency
  - Controlled Tx burst frequency drift over process and temperature range
- Scan Speed
  - Up to 190 Hz one finger reporting rate (subject to configuration)
  - Typical report rate for 10 touches  $\geq 60$  Hz (subject to configuration)
  - Initial touch latency  $< 25$  ms for first touch from idle (subject to configuration)
  - Configurable to allow for power and speed optimization

**On-chip Gestures**

- Reports one-touch and two-touch gestures

**Keys**

- Up to 32 nodes can be allocated as mutual capacitance sensor keys (subject to other configurations)
- Adjacent Key Suppression (AKS) technology is supported for false key touch prevention

**Enhanced Algorithms**

- Lens bending algorithms to remove display noise
- Touch suppression algorithms to remove unintentional large touches, such as palm
- Palm Recovery Algorithm for quick restoration to normal state

**Product Data Store Area**

- Up to 60 bytes of user-defined data can be stored during production

# MXT641T-AT/MXT641T-AB 1.0

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## Power Saving

- Programmable timeout for automatic transition from active to idle states
- Pipelined analog sensing detection and digital processing to optimize system power efficiency

## Application Interfaces

- I<sup>2</sup>C-compatible slave with support for Standard mode (up to 100 kHz), Fast mode (up to 400 kHz), Fast-mode Plus (up to 1 MHz), High-speed mode (up to 3.4 MHz)
- SPI slave interface (up to 8 MHz)
- Interrupt to indicate when a message is available
- SPI Debug Interface to read the real-time raw data for tuning and debugging purposes

## Power Supply

- Digital (V<sub>dd</sub>) 3.3 V nominal
- Digital I/O (V<sub>ddIO</sub>) 3.3 V nominal
- Analog (AV<sub>dd</sub>) 3.3 V nominal
- High voltage internal X line drive (XV<sub>dd</sub>) 6.6 V with internal voltage pump (XV<sub>dd</sub> = V<sub>dd</sub> if voltage pump not used)

## Package

- 100-pin TQFP 14 × 14 × 1 mm, 0.5 mm pitch

## Operating Temperature

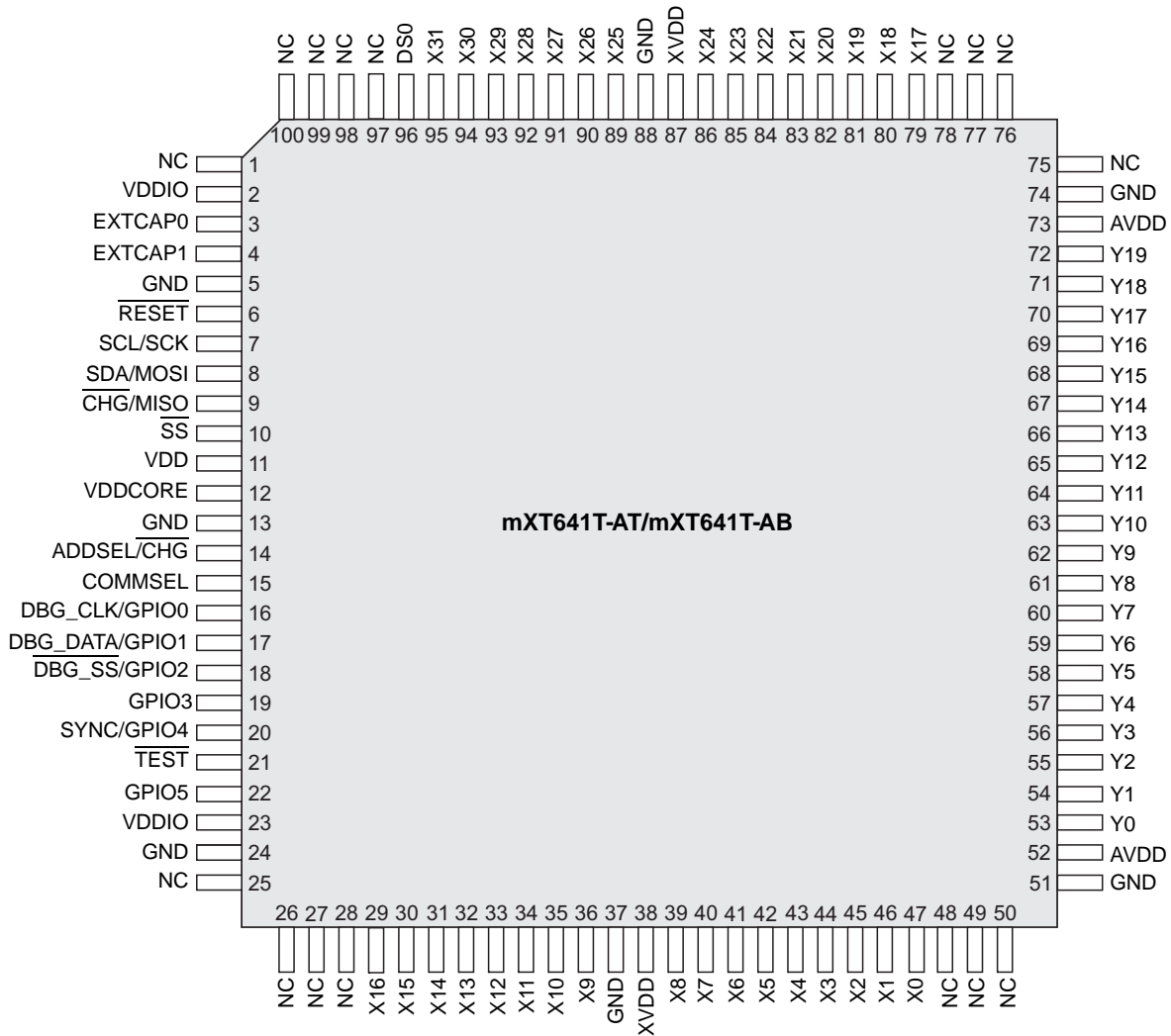
- mXT641T-AT: -40°C to +85°C (Grade 3)
- mXT641T-AB: -40°C to +105°C (Grade 2)

## Design Services

- Review of device configuration, stack-up and sensor patterns
- Custom firmware versions can be considered
- Contact your Microchip representative for more information

## PIN CONFIGURATION

### 100-pin TQFP



Top view

# MXT641T-AT/MXT641T-AB 1.0

**TABLE 1: PIN LISTING – 100-PIN TQFP**

Pin	Name	Type	Supply	Description	If Unused...
1	NC	–	–	No connection	Leave open
2	VDDIO	P	–	Digital IO interface power	–
3	EXTCAP0	P	–	Connect to EXTCAP1 via capacitor; see <a href="#">Section 2.3 “Schematic Notes”</a>	Leave open
4	EXTCAP1	P	–	Connect to EXTCAP0 via capacitor; see <a href="#">Section 2.3 “Schematic Notes”</a>	Leave open
5	GND	P	–	Ground	–
6	$\overline{\text{RESET}}$	I	VddIO	Reset low. Connection to host system is recommended	Pull up to VddIO
7	SCL	OD	VddIO	I <sup>2</sup> C Mode: Serial clock	–
	SCK	I		SPI Mode: Serial clock	
8	SDA	OD	VddIO	I <sup>2</sup> C Mode: Serial data	–
	MOSI	I		SPI Mode: Serial data – Master Output Slave Input	
9	$\overline{\text{CHG}}$	OD	VddIO	I <sup>2</sup> C Mode: State change interrupt (active low)	–
	MISO	O		SPI Mode: Serial data – Master Input Slave Output	
10	$\overline{\text{SS}}$	I	VddIO	SPI Mode: Slave Select line (active low)	Pull up to VddIO
11	VDD	P	–	Digital power	–
12	VDDCORE	P	–	Digital core power	–
13	GND	P	–	Ground	–
14	ADDSEL	I	VddIO	I <sup>2</sup> C Mode: I <sup>2</sup> C address select; see <a href="#">Section 7.2 “I<sup>2</sup>C Address Selection – ADDSEL Pin”</a>	–
	$\overline{\text{CHG}}$	OD		SPI Mode: State change interrupt (active low)	
15	COMMSEL	I	VddIO	Selects communications mode; see <a href="#">Section 7.1 “Host Communication Mode Selection – COMMSEL Pin”</a>	–
16	DBG_CLK	O	VddIO	Debug clock; see <a href="#">Section 2.3.10 “SPI Debug Interface”</a>	Connect to test point leave open
	GPIO0	I/O		General purpose I/O	
17	DBG_DATA	O	VddIO	Debug data; see <a href="#">Section 2.3.10 “SPI Debug Interface”</a>	Connect to test point leave open
	GPIO1	I/O		General purpose I/O	
18	$\overline{\text{DBG\_SS}}$	O	VddIO	Debug SS line; pull up to VddIO; see <a href="#">Section 2.3.10 “SPI Debug Interface”</a>	Connect to test point leave open
	GPIO2	I/O		General purpose I/O	
19	GPIO3	I/O	VddIO	General purpose I/O	Input: connect to GND Output: leave open
20	SYNC	I	VddIO	External synchronization	Input: connect to GND Output: leave open
	GPIO4	I/O		General purpose I/O	
21	$\overline{\text{TEST}}$	I	VddIO	Reserved for factory use; pull up to VddIO	–
22	GPIO5	I/O	VddIO	General purpose I/O	Input: connect to GND Output: leave open
23	VDDIO	P	–	Digital IO interface power	–
24	GND	P	–	Ground	–
25	NC	–	–	No connection	Leave open
26	NC	–	–	No connection	Leave open
27	NC	–	–	No connection	Leave open

**TABLE 1: PIN LISTING – 100-PIN TQFP (CONTINUED)**

Pin	Name	Type	Supply	Description	If Unused...
28	NC	–	–	No connection	Leave open
29	X16	S	XVdd	X line connection	Leave open
30	X15	S	XVdd	X line connection	Leave open
31	X14	S	XVdd	X line connection	Leave open
32	X13	S	XVdd	X line connection	Leave open
33	X12	S	XVdd	X line connection	Leave open
34	X11	S	XVdd	X line connection	Leave open
35	X10	S	XVdd	X line connection	Leave open
36	X9	S	XVdd	X line connection	Leave open
37	GND	P	–	Ground	–
38	XVDD	P	–	X line drive power; see <a href="#">Section 2.3.4 “Internal Voltage Pump”</a>	–
39	X8	S	XVdd	X line connection	Leave open
40	X7	S	XVdd	X line connection	Leave open
41	X6	S	XVdd	X line connection	Leave open
42	X5	S	XVdd	X line connection	Leave open
43	X4	S	XVdd	X line connection	Leave open
44	X3	S	XVdd	X line connection	Leave open
45	X2	S	XVdd	X line connection	Leave open
46	X1	S	XVdd	X line connection	Leave open
47	X0	S	XVdd	X line connection	Leave open
48	NC	–	–	No connection	Leave open
49	NC	–	–	No connection	Leave open
50	NC	–	–	No connection	Leave open
51	GND	P	–	Ground	–
52	AVDD	P	–	Analog power	–
53	Y0	S	AVdd	Y line connection	Leave open
54	Y1	S	AVdd	Y line connection	Leave open
55	Y2	S	AVdd	Y line connection	Leave open
56	Y3	S	AVdd	Y line connection	Leave open
57	Y4	S	AVdd	Y line connection	Leave open
58	Y5	S	AVdd	Y line connection	Leave open
59	Y6	S	AVdd	Y line connection	Leave open
60	Y7	S	AVdd	Y line connection	Leave open
61	Y8	S	AVdd	Y line connection	Leave open
62	Y9	S	AVdd	Y line connection	Leave open
63	Y10	S	AVdd	Y line connection	Leave open
64	Y11	S	AVdd	Y line connection	Leave open
65	Y12	S	AVdd	Y line connection	Leave open
66	Y13	S	AVdd	Y line connection	Leave open
67	Y14	S	AVdd	Y line connection	Leave open
68	Y15	S	AVdd	Y line connection	Leave open

# MXT641T-AT/MXT641T-AB 1.0

**TABLE 1: PIN LISTING – 100-PIN TQFP (CONTINUED)**

Pin	Name	Type	Supply	Description	If Unused...
69	Y16	S	AVdd	Y line connection	Leave open
70	Y17	S	AVdd	Y line connection	Leave open
71	Y18	S	AVdd	Y line connection	Leave open
72	Y19	S	AVdd	Y line connection	Leave open
73	AVDD	P	–	Analog power	–
74	GND	P	–	Ground	–
75	NC	–	–	No connection	Leave open
76	NC	–	–	No connection	Leave open
77	NC	–	–	No connection	Leave open
78	NC	–	–	No connection	Leave open
79	X17	S	XVdd	X line connection	Leave open
80	X18	S	XVdd	X line connection	Leave open
81	X19	S	XVdd	X line connection	Leave open
82	X20	S	XVdd	X line connection	Leave open
83	X21	S	XVdd	X line connection	Leave open
84	X22	S	XVdd	X line connection	Leave open
85	X23	S	XVdd	X line connection	Leave open
86	X24	S	XVdd	X line connection	Leave open
87	XVDD	P	–	X line drive power; see <a href="#">Section 2.3.4 “Internal Voltage Pump”</a>	–
88	GND	P	–	Ground	–
89	X25	S	XVdd	X line connection	Leave open
90	X26	S	XVdd	X line connection	Leave open
91	X27	S	XVdd	X line connection	Leave open
92	X28	S	XVdd	X line connection	Leave open
93	X29	S	XVdd	X line connection	Leave open
94	X30	S	XVdd	X line connection	Leave open
95	X31	S	XVdd	X line connection	Leave open
96	DS0	S	XVdd	Driven Shield signal; used as guard track between X/Y signals and ground	Leave open
97	NC	–	–	No connection	Leave open
98	NC	–	–	No connection	Leave open
99	NC	–	–	No connection	Leave open
100	NC	–	–	No connection	Leave open

**Key:**

I	Input only	O	Output only	I/O	Input or output
OD	Open drain output	P	Ground or power	S	Sense pin

## TABLE OF CONTENTS

Pin configuration .....	3
Table of Contents .....	7
To Our Valued Customers .....	8
1.0 Overview of mXT641T-AT/mXT641T-AB .....	9
2.0 Schematics .....	10
3.0 Touchscreen Basics .....	14
4.0 Sensor Layout .....	15
5.0 Power-up / Reset Requirements .....	17
6.0 Detailed Operation .....	20
7.0 Host Communications .....	23
8.0 I2C Communications .....	24
9.0 SPI Communications .....	30
10.0 PCB Design Considerations .....	38
11.0 Getting Started with mXT641T-AT/mXT641T-AB .....	41
12.0 Debugging and Tuning .....	46
13.0 Specifications .....	47
14.0 Packaging Information .....	60
Appendix A. Associated Documents .....	62
Appendix B. Revision History .....	63
Product Identification System .....	67
The Microchip Web Site .....	68
Customer Change Notification Service .....	68
Customer Support .....	68

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To determine if an errata sheet exists for a particular device, please check with one of the following:

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## 1.0 OVERVIEW OF MXT641T-AT/MXT641T-AB

The Microchip maXTouch family of touch controllers brings industry-leading capacitive touch performance to customer automotive applications. The mXT641T-AT/mXT641T-AB (mXT641T-AT) features the latest generation of Microchip adaptive sensing technology that utilizes a hybrid mutual and self capacitive sensing system in order to deliver unparalleled touch features and a robust user experience.

- **Patented capacitive sensing method** – The mXT641T-AT uses a unique charge-transfer acquisition engine to implement Microchip's patented capacitive sensing method. Coupled with a state-of-the-art CPU, the entire touchscreen sensing solution can measure, classify and track a number of individual finger touches with a high degree of accuracy in the shortest response time.
- **Capacitive Touch Engine (CTE)** – The mXT641T-AT features an acquisition engine, which uses an optimal measurement approach to ensure almost complete immunity from parasitic capacitance on the receiver input lines. The engine includes sufficient dynamic range to cope with anticipated touchscreen self and mutual capacitances, which allows great flexibility for use with the Microchip proprietary sensor pattern designs. One- and two-layer ITO sensors are possible using glass or PET substrates.
- **Touch detection** – The mXT641T-AT allows for both mutual and self capacitance measurements, with the self capacitance measurements being used to augment the mutual capacitance measurements to produce reliable touch information.

When self capacitance measurements are enabled, touch classification is achieved using both mutual and self capacitance touch data. This has the advantage that both types of measurement systems can work together to detect touches under a wide variety of circumstances.

The system may be configured for different types of default measurements in both idle and active modes. For example, the device may be configured for Mutual Capacitance Touch as the default in idle mode and Self Capacitance Touch as the default in active mode. Note that other types of scans (such as other types of self capacitance scans) may also be made depending on configuration.

Mutual capacitance touch data is used wherever possible to classify touches as this has greater granularity than self capacitance measurements and provides positional information on touches. For this reason, multiple touches can only be determined by mutual capacitance touch data. In Self Capacitance Touch Default mode, if the self capacitance touch processing detects multiple touches, touchscreen processing is skipped until mutual capacitance touch data is available.

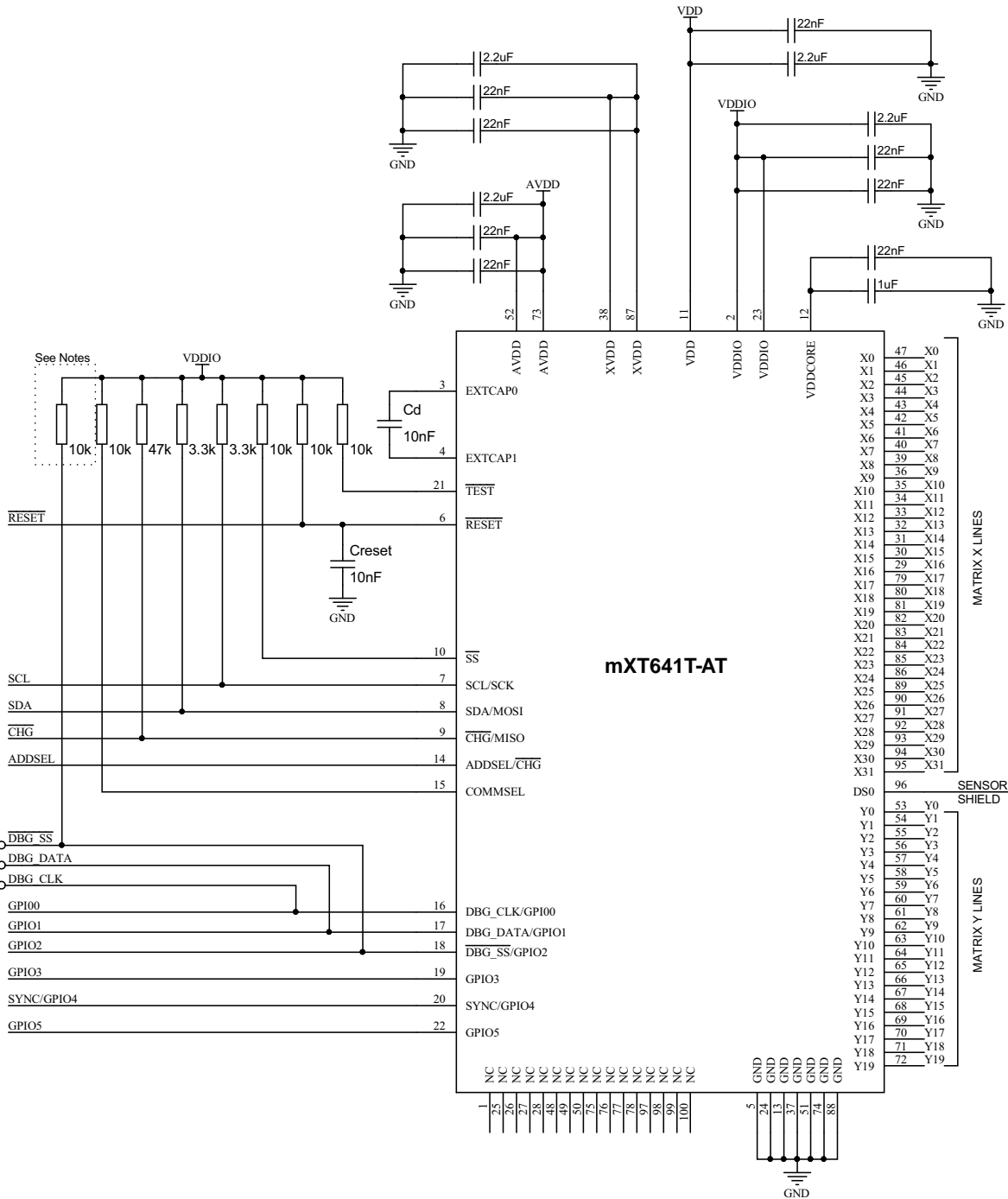
Self capacitance measurements allow for the detection of single touches in extreme cases, such as thick glove touches, when mutual capacitance touch detection alone may miss touches.

- **Display Noise Cancellation** – A combination of analog circuitry, hardware noise processing, and firmware that combats display noise without requiring additional listening channels or synchronization to display timing. This enables the use of shieldless touch sensor stacks, including touch-on-lens.
- **Noise filtering** – Hardware noise processing in the capacitive touch engine provides enhanced autonomous filtering and allows a broad range of noise profiles to be handled. The result is good performance in the presence of LCD noise.
- **Processing power** – The main CPU has two powerful microsequencer coprocessors under its control consuming low power. This system allows the signal acquisition, preprocessing, postprocessing and housekeeping to be partitioned in an efficient and flexible way.
- **Interpreting user intention** – The Microchip hybrid mutual and self capacitance method provides unambiguous multitouch performance. Algorithms in the mXT641T-AT provide optimized touchscreen position filtering for the smooth tracking of touches, responding to a user's intended touches while preventing false touches triggered by ambient noise, conductive material on the sensor surface, such as moisture, or unintentional touches from the user's resting palm or fingers.

# MXT641T-AT/MXT641T-AB 1.0

## 2.0 SCHEMATICS

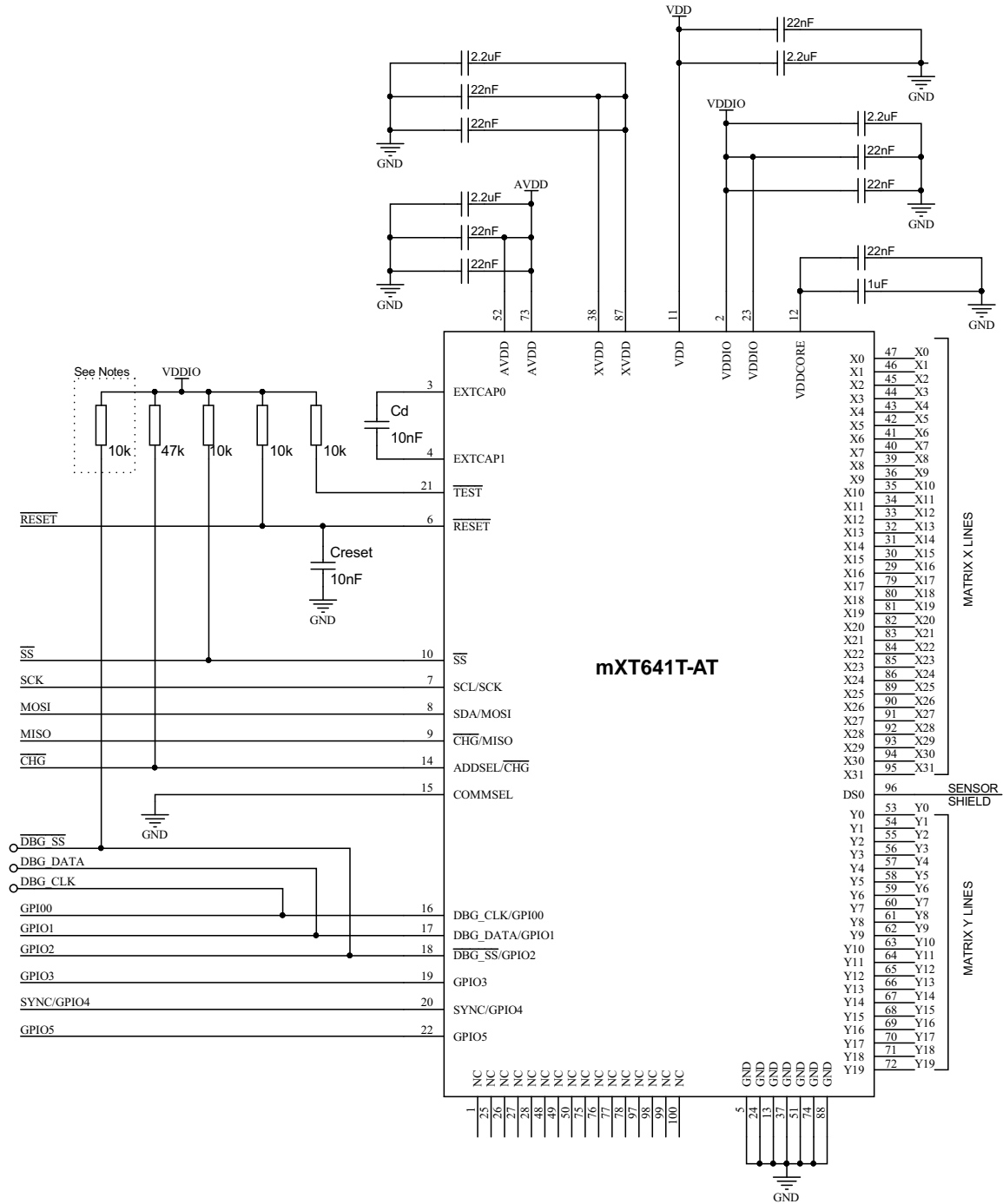
### 2.1 128-pin TQFP – I<sup>2</sup>C Mode



See Section 2.3 "Schematic Notes"

# MXT641T-AT/MXT641T-AB 1.0

## 2.2 128-pin TQFP – SPI Mode



See Section 2.3 "Schematic Notes"

# MXT641T-AT/MXT641T-AB 1.0

## 2.3 Schematic Notes

### 2.3.1 POWER SUPPLY

The sense and I/O pins are supplied by the power rails on the device as listed in [Table 2-1](#). This information is also indicated in “[Pin configuration](#)”.

**TABLE 2-1: POWER SUPPLY FOR SENSE AND I/O PINS**

Power Supply	Pins
XVdd	X sense pins, DS0
AVdd	Y sense lines
VddIO	$\overline{\text{RESET}}$ , $\text{GPIO}_n$ , SDA, SCL, MOSI, MISO, SCK, $\overline{\text{SS}}$ , COMMSEL, ADDSEL, FSYNC, PSYNC, $\overline{\text{CHG}}$ , DBG_CLK, DBG_DATA, DBG_SS

### 2.3.2 DECOUPLING CAPACITORS

All decoupling capacitors must be X7R or X5R and placed less than 5 mm away from the pins for which they act as bypass capacitors. Pins of the same type can share a capacitor provided no pin is more than 10 mm from the capacitor.

The schematics on the previous pages show the optimum capacitors required. The parallel combination of capacitors is recommended to give high and low frequency filtering, which is beneficial if the voltage regulators are likely to be some distance from the device (for example, if an active tail design is used). Note that this requires that the voltage regulator supplies for AVdd, Vdd and VddIO are clean and noise free. It also assumes that the track length between the capacitors and on-board power supplies is less than 50 mm.

The number of base capacitors can be reduced if the pinout configuration means that sharing a bypass capacitor is possible (subject to the distance between the pins satisfying the conditions above and there being no routing difficulties).

### 2.3.3 PULL-UP RESISTORS

The pull-up resistors shown in the schematics are suggested typical values and may be modified to meet the requirements of an individual customer design. This applies, in particular, to the I<sup>2</sup>C pull-up resistors (see [Section 2.3.7 “I<sup>2</sup>C Interface”](#)).

### 2.3.4 INTERNAL VOLTAGE PUMP

The voltage pump requires one external capacitor:

- EXTCAP0 must be connected to EXTCAP1 via a capacitor (Cd)
- The capacitor on XVDD should be rated at least 10 V if the voltage doubler is used

Capacitor Cd should provide a capacitance of 10 nF.

**If XVdd voltage doubler is not required:**

- Capacitor Cd must be omitted and EXTCAP0 and EXTCAP1 left unconnected
- XVDD line(s) must be connected to VDD

### 2.3.5 VDDCORE

VddCore is internally generated from the Vdd power supply. To guarantee stability of the internal voltage regulator, an external capacitor is required.

### 2.3.6 $\overline{\text{CHG}}$ LINE

The  $\overline{\text{CHG}}$  line is shown on the schematics with a 47 K $\Omega$  pull-up resistor. This will result in a very low voltage level during reset, which can be mistaken by the host for an active signal, so it is recommended that the host ignores this signal until at least 1 ms after the rising edge of the  $\overline{\text{RESET}}$  signal.

Note that a 470  $\Omega$  pull-up resistor can be used instead when the VddIO is set to 1.8 V, in which case there is no requirement for the host to ignore this signal until after the rising edge of the  $\overline{\text{RESET}}$  signal.

## 2.3.7 I<sup>2</sup>C INTERFACE

The schematic shows pull-up resistors on the SDA and SCL lines. The values of these resistors depends on the speed of the I<sup>2</sup>C interface. See [Section 13.9 “I2C Specification”](#) for details.

Note that if a VddIO supply at the low end of the allowable range is used, the pull-up resistor values may need to be reduced.

## 2.3.8 MULTIPLE FUNCTION PINS

Some pins may have multiple functions. In this case, only one function can be chosen and the circuit should be designed accordingly.

## 2.3.9 GPIO PINS

The mXT641T-AT has 6 GPIO pins. The pins can be set to be either an input or an output, as required, using the GPIO Configuration T19 object.

Unused GPIO pins can be left externally unconnected as long as they are given a defined state by using the GPIO Configuration T19 object. By default GPIO pins are set to be inputs and if they are not used they should be connected to GND. Alternatively, they can be set as outputs using the GPIO Configuration T19 object and left open.

If the GPIO Configuration T19 object is not enabled for use, all the GPIO pins are unused.

Some GPIO pins have alternative functions. If an alternative function is used then this takes precedence over the GPIO function and the pin cannot be used as a GPIO pin. In particular:

- GPIO4 cannot be used if the SYNC function is in use
- The SPI Debug Interface functionality is shared with some of the GPIO pins. See [Section 2.3.10 “SPI Debug Interface”](#) for more details on the SPI Debug Interface and how to handle these pins if they are totally unused.

## 2.3.10 SPI DEBUG INTERFACE

The DBG\_CLK, DBG\_DATA and DBG\_SS lines form the SPI Debug Interface. These pins should be routed to test points on all designs, such that they can be connected to external hardware during system development. See also [Section 12.1 “SPI Debug Interface”](#).

The debug lines may share pins with other functionality. Only one function for each pin can be chosen and the circuit should be designed accordingly. Note that the pull-up resistor for DBG\_SS in the schematics is optional and should be present only if the line is used as DBG\_SS.

The DBG\_CLK, DBG\_DATA and DBG\_SS lines should not be connected to power or GND. For this reason, where these pins are shared with GPIO pins and they are totally unused (that is, they are not being used as debug or GPIO pins), they should be set as outputs.

## 3.0 TOUCHSCREEN BASICS

### 3.1 Sensor Construction

A touchscreen is usually constructed from a number of transparent electrodes. These are typically on a glass or plastic substrate. They can also be made using non-transparent electrodes, such as copper or carbon. Electrodes are constructed from Indium Tin Oxide (ITO) or metal mesh. Thicker electrodes yield lower levels of resistance (perhaps tens to hundreds of  $\Omega$ /square) at the expense of reduced optical clarity. Lower levels of resistance are generally more compatible with capacitive sensing. Thinner electrodes lead to higher levels of resistance (perhaps hundreds to thousands of  $\Omega$ /square) with some of the best optical characteristics.

Interconnecting tracks can cause problems. The excessive RC time constants formed between the resistance of the track and the capacitance of the electrode to ground can inhibit the capacitive sensing function. In such cases, the tracks should be replaced by screen printed conductive inks (non-transparent) outside the touchscreen viewing area.

### 3.2 Electrode Configuration

The specific electrode designs used in Microchip touchscreens are the subject of various patents and patent applications. Further information is available on request.

The device supports various configurations of electrodes as summarized in [Section 4.0 "Sensor Layout"](#).

### 3.3 Scanning Sequence

All nodes are scanned in sequence by the device. There is a full parallelism in the scanning sequence to improve overall response time. The nodes are scanned by measuring capacitive changes at the intersections formed between the first X line and all the Y lines. Then the intersections between the next X line and all the Y lines are scanned, and so on, until all X and Y combinations have been measured.

The device can be configured in various ways. It is possible to disable some nodes so that they are not scanned at all. This can be used to improve overall scanning time.

### 3.4 Touchscreen Sensitivity

#### 3.4.1 ADJUSTMENT

Sensitivity of touchscreens can vary across the extents of the electrode pattern due to natural differences in the parasitic capacitance of the interconnections, control chip, and so on. An important factor in the uniformity of sensitivity is the electrode design itself. It is a natural consequence of a touchscreen pattern that the edges form a discontinuity and hence tend to have a different sensitivity. The electrodes at the far edges do not have a neighboring electrode on one side and this affects the electric field distribution in that region.

A sensitivity adjustment is available for the whole touchscreen. This adjustment is a basic algorithmic threshold that defines when a node is considered to have enough signal change to qualify as being in detect.

#### 3.4.2 MECHANICAL STACKUP

The mechanical stackup refers to the arrangement of material layers that exist above and below a touchscreen. The arrangement of the touchscreen in relation to other parts of the mechanical stackup has an effect on the overall sensitivity of the screen. QMatrix technology has an excellent ability to operate in the presence of ground planes close to the sensor. QMatrix sensitivity is attributed more to the interaction of the electric fields between the transmitting (X) and receiving (Y) electrodes than to the surface area of these electrodes. For this reason, stray capacitance on the X or Y electrodes does not strongly reduce sensitivity.

Front panel dielectric material has a direct bearing on sensitivity. Plastic front panels are usually suitable up to about 3 mm, and glass up to about 2 mm (dependent upon the screen size and layout). The thicker the front panel, the lower the signal-to-noise ratio of the measured capacitive changes and hence the lower the resolution of the touchscreen. In general, glass front panels are near optimal because they conduct electric fields almost twice as easily as plastic panels.

<b>NOTE</b> Care should be taken using ultra-thin glass panels as retransmission effects can occur, which can significantly degrade performance.
--

## 4.0 SENSOR LAYOUT

The specific electrode designs used in Microchip touchscreens are the subject of various patents and patent applications. Further information is available on request.

The physical matrix can be configured to have one or more touch objects. These are configured using the appropriate touch objects (Multiple Touch Touchscreen and Key Array). It is not mandatory to have all the allowable touch objects present. The objects are disabled by default so only those that you wish to use need to be enabled. Refer to the *mXT641T-AT/mXT641T-AB 1.0 Protocol Guide* for more information on configuring the touch objects.

The device supports various configurations of electrodes as summarized below:

- Touchscreen: 32 X × 20 Y maximum (subject to other configurations)
- Keys: Up to 32 keys in an X/Y grid (Key Array)

When designing the physical layout of the touch panel, obey the following rules:

- Each touch object should be a regular rectangular shape in terms of the lines it uses.
- A Touchscreen object cannot share an X or Y line with another touch object if self-capacitance measurements are enabled.
- It is recommended that the Touchscreen should start at X0, Y0; if self-capacitance measurements are enabled, the Touchscreen **must** start at X0, Y0. If a design requires the touchscreen to be located in a region that does not start at X0, Y0, seek advice from Microchip first.
- It is recommended that a standard Key Array should occupy the highest X and Y lines.

## 4.1 Screen Size

Table 4-1 lists some typical screen size and electrode pitch combinations to achieve various aspect ratios.

**TABLE 4-1: TYPICAL SCREEN SIZES**

Aspect Ratio	Matrix Size	Node Count	Screen Diagonal (Inches)		
			4.5 mm Pitch	5 mm Pitch	5.5 mm Pitch
16:10	X = 32, Y = 20	640	6.69	7.43	8.17
16:9	X = 32, Y = 18	576	6.5	7.23	7.95
4:3	X = 27, Y = 20	540	5.95	6.61	7.28

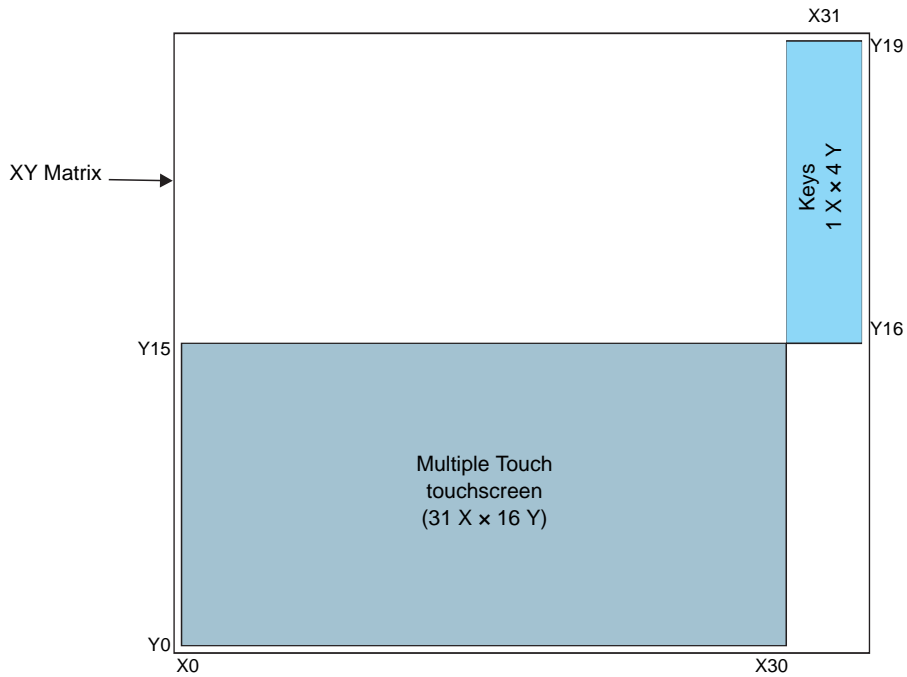
## 4.2 Key Array

For optimal performance in terms of cycle time overhead, it is recommended that the number of X (drive) lines used for the standard Key Array is kept to the minimum and designs should favor using Y lines where possible.

Figure 4-1 shows an example layout for a Key Array of 1 X × 4 Y lines. Note that in this case using 1 X × 4 Y lines would give better performance than using 4 X × 1 Y lines.

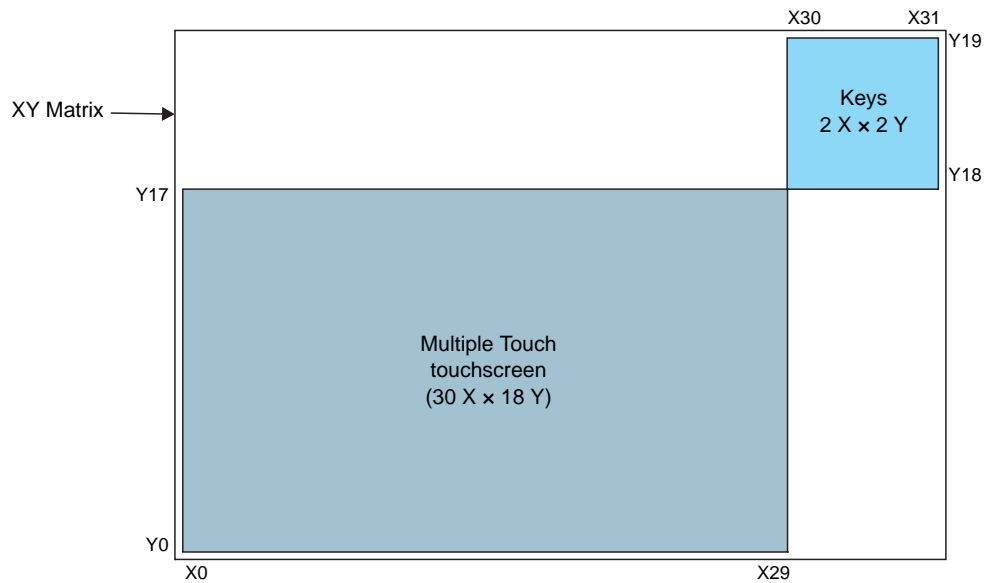
# MXT641T-AT/MXT641T-AB 1.0

FIGURE 4-1: EXAMPLE LAYOUT – OPTIMAL CYCLE TIME



If, however, the intention is to preserve a larger touchscreen size and maintain an optimal aspect ratio, then using equal X and Y lines for the key array can be considered, as in [Figure 4-2](#).

FIGURE 4-2: EXAMPLE LAYOUT – OPTIMAL ASPECT RATIO





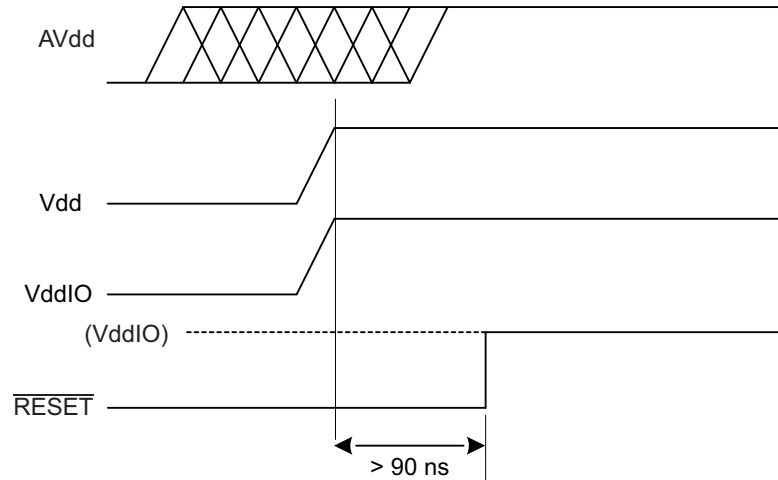
## 5.0 POWER-UP / RESET REQUIREMENTS

### 5.1 Power-on Reset

There is an internal Power-on Reset (POR) in the device.

If an external reset is to be used the device must be held in  $\overline{\text{RESET}}$  (active low) while the digital (Vdd), analog (AVdd) and digital I/O (VddIO) power supplies are powering up. The supplies must have reached their nominal values before the  $\overline{\text{RESET}}$  signal is deasserted (that is, goes high). This is shown in Figure 5-1. See Section 13.2 “Recommended Operating Conditions” for nominal values for the power supplies to the device.

**FIGURE 5-1: POWER SEQUENCING ON THE MXT641T-AT**



Note: When using external  $\overline{\text{RESET}}$  at power-up, VddIO must not be enabled after Vdd

It is recommended that customer designs include the capability for the host to control all the maXTouch power supplies and pull the  $\overline{\text{RESET}}$  line low.

After power-up, the device typically takes 93 ms before it is ready to start communications.

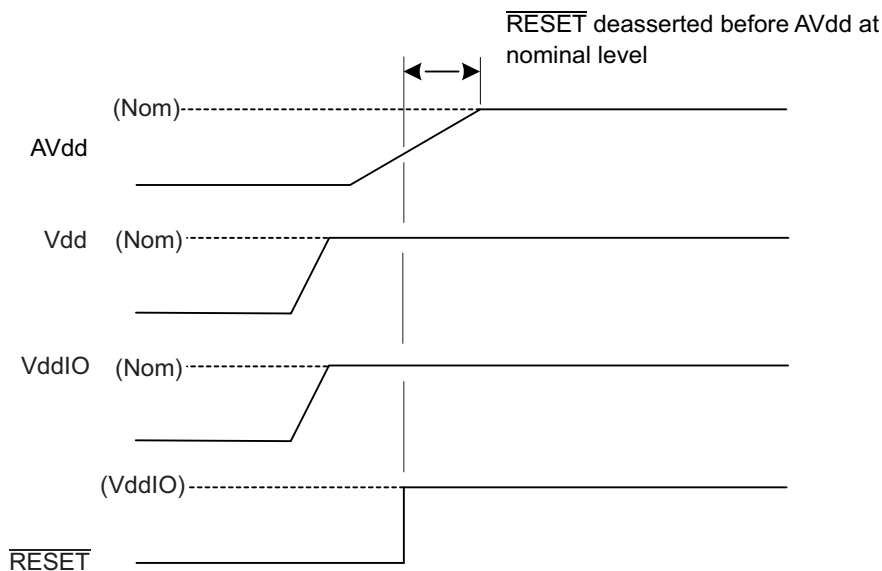
**NOTE** Device initialization will not complete until after all the power supplies are present. If any power supply is not present, internal initialization stalls and the device will not communicate with the host.

If the  $\overline{\text{RESET}}$  line is released before the AVdd supply has reached its nominal voltage (see Figure 5-2), then some additional operations need to be carried out by the host. There are two options open to the host controller:

- Start the part in deep sleep mode and then send the command sequence to set the cycle time to wake the part and allow it to run normally. Note that in this case a calibration command is also needed.
- Send a RESET command.

# MXT641T-AT/MXT641T-AB 1.0

FIGURE 5-2: POWER SEQUENCING ON THE MXT641T-AT – LATE RISE ON AVDD



The  $\overline{\text{RESET}}$  pin can be used to reset the device whenever necessary. The  $\overline{\text{RESET}}$  pin must be asserted low for at least 90 ns to cause a reset. After releasing the  $\overline{\text{RESET}}$  pin the device typically takes 93 ms before it is ready to start communications. It is recommended to connect the  $\overline{\text{RESET}}$  pin to a host controller to allow it to initiate a full hardware reset without requiring a power-down.

**WARNING** The device should be reset only by using the  $\overline{\text{RESET}}$  line. If an attempt is made to reset by removing the power from the device without also sending the signal lines low, power will be drawn from the interface lines and the device will not reset correctly.

Make sure that any lines connected to the device are below or equal to Vdd during power-up. For example, if  $\overline{\text{RESET}}$  is supplied from a different power domain to the VDDIO pin, make sure that it is held low when Vdd is off. If this is not done, the  $\overline{\text{RESET}}$  signal could parasitically couple power via the  $\overline{\text{RESET}}$  pin into the Vdd supply.

**NOTE** The voltage level on the  $\overline{\text{RESET}}$  pin of the device must never exceed VddIO (digital supply voltage).

A software RESET command (using the Command Processor T6 object) can be used to reset the chip. A software reset typically takes 115 ms. After the chip has finished it asserts the CHG line to signal to the host that a message is available. The reset flag is set in the Message Processor object to indicate to the host that it has just completed a reset cycle. This bit can be used by the host to detect any unexpected brownout events. This allows the host to take any necessary corrective actions, such as reconfiguration.

**NOTE** The CHG line is briefly set as an input during power-up or reset. It is therefore particularly important that the line should be allowed to float high via the CHG line pull-up resistor during this period. It should not be driven by the host (see Section 13.6.4 “Reset Timings”).

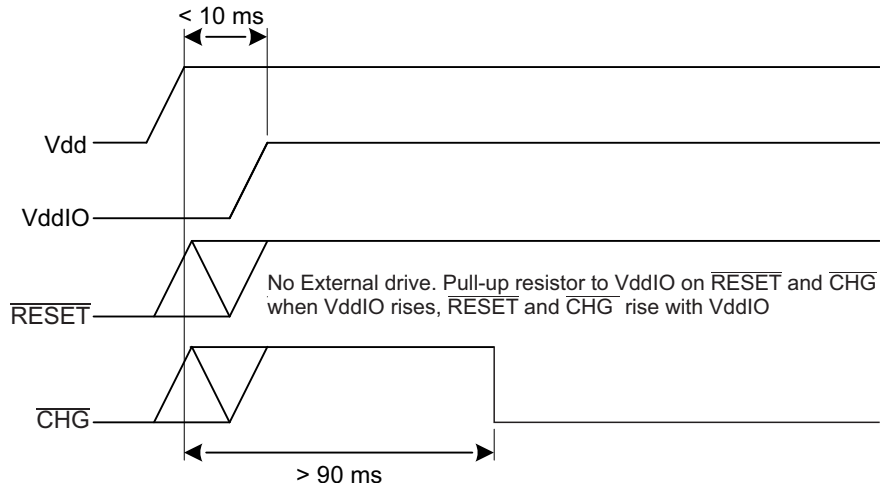
At power-on, the device performs a self-test routine (using the Self Test T25 object) to check for shorts that might cause damage to the device.

## 5.2 Power-up and Reset Sequence – VddIO Enabled after Vdd

The power-up sequence that can be used in applications where VddIO must be powered up after Vdd, is shown in Figure 5-3.

In this case the communication interface to the maXTouch device is not driven by the host system. The  $\overline{\text{RESET}}$  and CHG pins are connected to VddIO using suitable pull-up resistors. Vdd is powered up, followed by VddIO, no more than 10 ms after Vdd. Due to the pull-up resistors,  $\overline{\text{RESET}}$  and CHG will rise with VddIO. The internal POR system ensures reliable boot up of the device and the CHG line will go low approximately 93 ms after Vdd to notify the host that the device is ready to start communication.

**FIGURE 5-3: POWER-UP SEQUENCE**



## 5.3 Power-up and Initialization

The device uses a number of different power domains for optimum performance and contains circuitry to interface internal signals crossing between the different domains. There is also circuitry to ensure that the device interface logic will be initialized correctly as the device powers on. Note, however, that this does not negate specific instructions elsewhere in this section about the order that the different supplies should power up. Also, as previously mentioned, RESET should be held low until after all power rails are stable. In addition, the device will not initialize until all the voltage rails have powered up and are present.

If one domain loses power, however (for example, due to a fault or an ESD event), the device should be power-cycled to ensure that the interface logic is once again initialized. It is therefore recommended that customer designs include the capability for the host to control all the maXTouch power supplies and pull the RESET line low.

## 5.4 Summary

The power-up and reset requirements for the maXTouch devices are summarized in [Table 5-1](#).

**TABLE 5-1: POWER-UP AND RESET REQUIREMENTS**

Condition	External $\overline{\text{RESET}}$	VddIO Delay (After Vdd)	AVdd Power-Up	Comments
1	Low at Power-up	0 ms	Before $\overline{\text{RESET}}$ is released	If AVdd bring-up is delayed, then additional actions will be required by the host (see <a href="#">Section 5.1 "Power-on Reset"</a> )
2	Not driven	<10 ms	Before VddIO	

# MXT641T-AT/MXT641T-AB 1.0

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## 6.0 DETAILED OPERATION

### 6.1 Touch Detection

The mXT641T-AT allows for both mutual and self capacitance measurements, with the self capacitance measurements being used to augment the mutual capacitance measurements to produce reliable touch information.

When self capacitance measurements are enabled, touch classification is achieved using both mutual and self capacitance touch data. This has the advantage that both types of measurement systems can work together to detect touches under a wide variety of circumstances.

Mutual capacitance touch data is used wherever possible to classify touches as this has greater granularity than self capacitance measurements and provides positional information on touches.

Self capacitance measurements, on the other hand, allow for the detection of single touches in extreme cases, such as single thick glove touches, when touches can only be detected by self capacitance data and may be missed by mutual capacitance touch detection.

### 6.2 Operational Modes

The device operates in two modes: **Active** (touch detected) and **Idle** (no touches detected). Both modes operate as a series of burst cycles. Each cycle consists of a short burst (during which measurements are taken) followed by an inactive sleep period. The difference between these modes is the length of the cycles. Those in idle mode typically have longer sleep periods. The cycle length is configured using the IDLEACQINT and ACTVACQINT settings in the Power Configuration T7. In addition, an *Active to Idle Timeout* setting is provided.

### 6.3 Detection Integrator

The device features a touch detection integration mechanism. This acts to confirm a detection in a robust fashion. A counter is incremented each time a touch has exceeded its threshold and has remained above the threshold for the current acquisition. When this counter reaches a preset limit the sensor is finally declared to be touched. If, on any acquisition, the signal is not seen to exceed the threshold level, the counter is cleared and the process has to start from the beginning.

The detection integrator is configured using the appropriate touch objects (Multiple Touch Touchscreen T100, Key Array T15).

### 6.4 Sensor Acquisition

The charge time is set using the Acquisition Configuration T8 object.

A number of factors influence the acquisition time for a single drive line and the total acquisition time for the sensor as a whole must not exceed 250 ms. If this condition is not met, a SIGERR will be reported.

Care should be taken to configure all the objects that can affect the measurement timing, for example, Acquisition Configuration T8, CTE Configuration T46 and Self Capacitance Configuration T111, so that this limit is not exceeded.

### 6.5 Calibration

Calibration is the process by which a sensor chip assesses the background capacitance on each node. Nodes are only calibrated on reset and when:

- The node is enabled (that is, activated)

or

- The node is already enabled and one of the following applies:
  - The node is held in detect for longer than the Touch Automatic Calibration setting (TCHAUTOCAL in the Acquisition Configuration T8 object)
  - The signal delta on a node is at least the touch threshold (TCHTHR – TCHHYST) in the anti-touch direction, while it meets the criteria in the Touch Recovery Processes that results in a recalibration
  - The host issues a recalibrate command
  - Certain configuration settings are changed

A status message is generated on the start and completion of a calibration.

Note that the device performs a global calibration; that is, all the nodes are calibrated together.

## 6.6 Digital Filtering and Noise Suppression

The mXT641T-AT supports on-chip filtering of the acquisition data received from the sensor. Specifically, the Noise Suppression T72 object provides an algorithm to suppress the effects of noise (for example, from a noisy charger plugged into the user's product). This algorithm can automatically adjust some of the acquisition parameters on-the-fly to filter the analog-to-digital conversions (ADCs) received from the sensor.

Additional noise suppression is provided by the Self Capacitance Noise Suppression T108 object. Similar in both design and configuration to the Noise Suppression T72 object, the Self Capacitance Noise Suppression T108 object is the noise suppression interface for self capacitance touch measurements.

Noise suppression is triggered when a noise source is detected.

- The host driver code can indicate when a noise source is present.
- The noise suppression is also triggered based on the noise levels detected using internal line measurements. The Noise Suppression T72 and Self Capacitance Noise Suppression T108 object selects the appropriate controls to suppress the noise present in the system.

## 6.7 Shieldless Support and Display Noise Suppression

The mXT641T-AT can support shieldless sensor design even with a noisy LCD.

The Optimal Integration feature is not filtering as such, but enables the user to use a shorter integration window. The integration window optimizes the amount of charge collected against the amount of noise collected, to ensure an optimal SNR. This feature also benefits the system in the presence of an external noise source. This feature is configured using the Shieldless T56 object.

Display noise suppression allows the device to overcome display noise simultaneously with external noise. This feature is based on filtering provided by the Lens Bending T65 object (see [Section 6.10 "Lens Bending"](#)).

## 6.8 Retransmission Compensation

The device can limit the undesirable effects on the mutual capacitance touch signals caused by poor device coupling to ground, such as poor sensitivity and touch break-up. This is achieved using the Retransmission Compensation T80 object. This object can be configured to allow the touchscreen to compensate for signal degradation due to these undesirable effects. If self capacitance measurements are also scheduled, the Retransmission Compensation T80 object will use the resultant data to enhance the compensation process.

The Retransmission Compensation T80 object is also capable of compensating for water presence on the sensor if self capacitance measurements are scheduled. In this case, both mutual capacitance and self capacitance measurements are used to detect moisture and then, once moisture is detected, self capacitance measurements are used to detect single touches in the presence of moisture.

## 6.9 Grip Suppression

The device has grip suppression functionality to suppress false detections from a user's grip.

Mutual capacitance grip suppression works by specifying a boundary around a touchscreen, within which touches can be suppressed whilst still allowing touches in the center of the touchscreen. This ensures that an accidental hand touch on the edge is suppressed while still allowing a "real" (finger) touch towards the center of the screen. Mutual capacitance grip suppression is configured using the Grip Suppression T40 object.

Self Capacitance grip suppression works by looking for characteristic shapes in the self capacitance measurement along the touchscreen boundary, and thereby distinguishing between a grip and a touch further into the sensor. Self capacitance grip suppression is configured using the Self Capacitance Grip Suppression T112 object.

## 6.10 Lens Bending

The device supports algorithms to eliminate disturbances from the measured signal.

When the sensor suffers from the screen deformation (lens bending) the signal values acquired by normal procedure are corrupted by the disturbance component (bend). The amount of bend depends on:

- The mechanical and electrical characteristics of the sensor
- The amount and location of the force applied by the user touch to the sensor

# MXT641T-AT/MXT641T-AB 1.0

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The Lens Bending T65 object measures the bend component and compensates for any distortion caused by the bend. As the bend component is primarily influenced by the user touch force, it can be used as a secondary source to identify the presence of a touch. The additional benefit of the Lens Bending T65 object is that it will eliminate LCD noise as well.

## 6.11 Glove Detection

The device has glove detection algorithms that process the measurement data received from the touchscreen classifying touches as potential gloved touches.

The Glove Detection T78 object is used to detect glove touches. In Normal Mode the Glove Detection T78 object applies vigorous glove classification to small signal touches to minimize the effect of unintentional hovering finger reporting. Once a gloved touch is found, the Glove Detection T78 object enters Glove Confidence Mode. In this mode the device expects the user to be wearing gloves so the classification process is much less stringent.

## 6.12 Stylus Support

The mXT641T-AT allows for the particular characteristics of passive stylus touches, whilst still allowing conventional finger touches to be detected. The touch sensitivity and threshold controls for stylus touches are configured separately from those for conventional finger touches so that both types of touches can be accommodated.

Stylus support ensures that the small touch area of a stylus registers as a touch, as this would otherwise be considered too small for the touchscreen. Additionally, there are controls to distinguish a stylus touch from an unwanted approaching finger (such as on the hand holding the stylus).

Passive stylus touches are configured by the Passive Stylus T47 object. There is one instance of the Passive Stylus T47 object for each Multiple Touch Touchscreen T100 object present on the device.

## 6.13 Unintentional Touch Suppression

The Touch Suppression T42 object provides a mechanism to suppress false detections from unintentional touches from a large body area, such as from a face, ear or palm. The Touch Suppression T42 object also provides Maximum Touch Suppression to suppress all touches if more than a specified number of touches has been detected. There is one instance of the Touch Suppression T42 object for each Multiple Touch Touchscreen T100 object present on the device.

## 6.14 Adjacent Key Suppression Technology

Adjacent Key Suppression (AKS) technology is a patented method used to detect which touch object (Multiple Touch Touchscreen T100 or Key Array T15) is touched, and to suppress touches on the other touch objects, when touch objects are located close together.

The device has two levels of AKS:

- The first level works between the touch objects (Multiple Touch Touchscreen T100 and Key Array T15). The touch objects are assigned to AKS groups. If a touch occurs within one of the touch objects in a group, then touches within other objects inside that group are suppressed. For example, if a touchscreen and a Key Array are placed in the same AKS group, then a touch in the touchscreen will suppress touches in the Key Array, and vice versa. Objects can be in more than one AKS group.
- The second level of AKS is internal AKS within an individual Key Array object. If internal AKS is enabled, then when one key is touched, touches on all the other keys within the Key Array are suppressed. Note that internal AKS is not present on other types of touch objects.

## 7.0 HOST COMMUNICATIONS

Communication between the mXT641T-AT and the host is achieved using one of the following interfaces:

- I<sup>2</sup>C (see [Section 8.0 “I<sup>2</sup>C Communications”](#))
- SPI (see [Section 9.0 “SPI Communications”](#))

Either host interface can be used, depending on the needs of the user’s project, but only one interface should be used in any one design.

### 7.1 Host Communication Mode Selection – COMMSEL Pin

The selection of the host I<sup>2</sup>C or SPI interface is determined by connecting the COMMSEL pin according to [Table 7-1](#).

**TABLE 7-1: HOST INTERFACE SELECTION**

COMMSEL	Interface Selected
Connected to GND	SPI
Pulled up to VddIO <sup>(1)</sup>	I <sup>2</sup> C

**Note 1:** Requires a pull-up resistor; see [Section 2.0 “Schematics”](#)

### 7.2 I<sup>2</sup>C Address Selection – ADDSEL Pin

The I<sup>2</sup>C address is selected by connecting the ADDSEL pin according to [Table 7-2](#).

**TABLE 7-2: I<sup>2</sup>C ADDRESS SELECTION**

ADDSEL	I <sup>2</sup> C Address
Connected to GND	0x4A
Pulled up to VddIO <sup>(1)</sup>	0x4B

**Note 1:** Requires a pull-up resistor; see [Section 2.0 “Schematics”](#)

# MXT641T-AT/MXT641T-AB 1.0

## 8.0 I<sup>2</sup>C COMMUNICATIONS

Communication with the device can be carried out over the I<sup>2</sup>C interface.

The I<sup>2</sup>C interface is used in conjunction with the  $\overline{\text{CHG}}$  line. The  $\overline{\text{CHG}}$  line going active signifies that a new data packet is available. This provides an interrupt-style interface and allows the device to present data packets when internal changes have occurred. See [Section 8.6 “CHG Line”](#) for more information.

### 8.1 I<sup>2</sup>C Addresses

The device supports two I<sup>2</sup>C device addresses that are selected using the ADDSEL line at start up. The two internal I<sup>2</sup>C device addresses are 0x4A and 0x4B. The selection of the address (and the communication mode) is described in [Section 7.2 “I<sup>2</sup>C Address Selection – ADDSEL Pin”](#).

The I<sup>2</sup>C address is shifted left to form the SLA+W or SLA+R address when transmitted over the I<sup>2</sup>C interface, as shown in [Table 8-1](#).

**TABLE 8-1: FORMAT OF AN I<sup>2</sup>C ADDRESS**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0x4A or 0x4B							Read/write

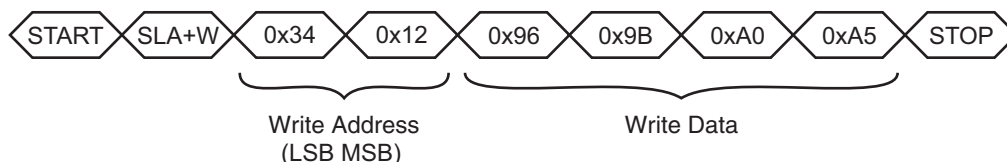
### 8.2 Writing To the Device

A WRITE cycle to the device consists of a START condition followed by the I<sup>2</sup>C address of the device (SLA+W). The next two bytes are the address of the location into which the writing starts. The first byte is the Least Significant Byte (LSByte) of the address, and the second byte is the Most Significant Byte (MSByte). This address is then stored as the address pointer.

Subsequent bytes in a multi-byte transfer form the actual data. These are written to the location of the address pointer, location of the address pointer + 1, location of the address pointer + 2, and so on. The address pointer returns to its starting value when the WRITE cycle STOP condition is detected.

[Figure 8-1](#) shows an example of writing four bytes of data to contiguous addresses starting at 0x1234.

**FIGURE 8-1: EXAMPLE OF A FOUR-BYTE WRITE STARTING AT ADDRESS 0X1234**

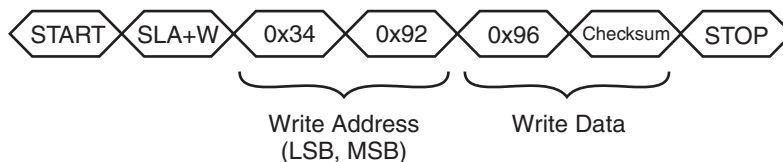


### 8.3 I<sup>2</sup>C Writes in Checksum Mode

In I<sup>2</sup>C checksum mode an 8-bit CRC is added to all I<sup>2</sup>C writes. The CRC is sent at the end of the data write as the last byte before the STOP condition. All the bytes sent are included in the CRC, including the two address bytes. Any command or data sent to the device is processed even if the CRC fails.

To indicate that a checksum is to be sent in the write, the most significant bit of the MSByte of the address is set to 1. For example, the I<sup>2</sup>C command shown in [Figure 8-2](#) writes a value of 150 (0x96) to address 0x1234 with a checksum. The address is changed to 0x9234 to indicate checksum mode.

**FIGURE 8-2: EXAMPLE OF A WRITE TO ADDRESS 0X1234 WITH A CHECKSUM**





## 8.4 Reading From the Device

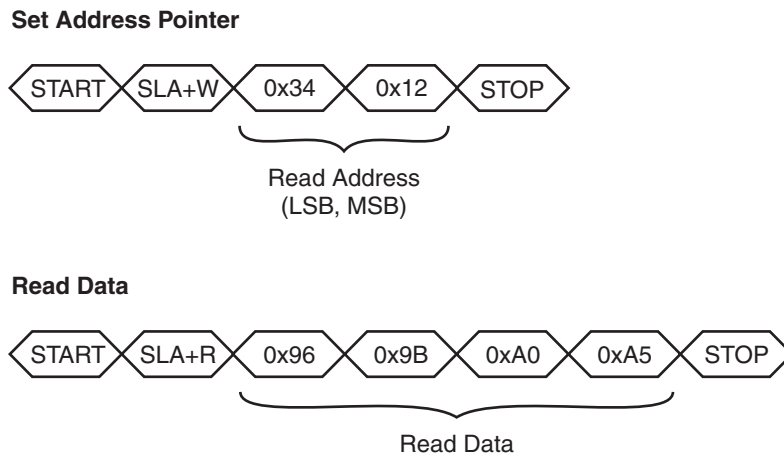
Two I<sup>2</sup>C bus activities must take place to read from the device. The first activity is an I<sup>2</sup>C write to set the address pointer (LSByte then MSByte). The second activity is the actual I<sup>2</sup>C read to receive the data. The address pointer returns to its starting value when the read cycle NACK is detected.

It is not necessary to set the address pointer before every read. The address pointer is updated automatically after every read operation. The address pointer will be correct if the reads occur in order. In particular, when reading multiple messages from the Message Processor T5 object, the address pointer is automatically reset to allow continuous reads (see Section 8.5 “Reading Status Messages with DMA”).

The WRITE and READ cycles consist of a START condition followed by the I<sup>2</sup>C address of the device (SLA+W or SLA+R respectively). Note that in this mode, calculating a checksum of the data packets is not supported.

Figure 8-3 shows the I<sup>2</sup>C commands to read four bytes starting at address 0x1234.

**FIGURE 8-3: EXAMPLE OF A FOUR-BYTE READ STARTING AT ADDRESS 0X1234**



## 8.5 Reading Status Messages with DMA

The device facilitates the easy reading of multiple messages using a single continuous read operation. This allows the host hardware to use a direct memory access (DMA) controller for the fast reading of messages, as follows:

1. The host uses a write operation to set the address pointer to the start of the Message Count T44 object, if necessary. Note that the STOP condition at the end of the read resets the address pointer to its initial location, so it may already be pointing at the Message Count T44 object following a previous message read. If a checksum is required on each message, the most significant bit of the MSByte of the read address must be set to 1.
2. The host starts the read operation of the message by sending a START condition.
3. The host reads the Message Count T44 object (one byte) to retrieve a count of the pending messages.
4. The host calculates the number of bytes to read by multiplying the message count by the size of the Message Processor T5 object. Note that the host should have already read the size of the Message Processor T5 object in its initialization code.

Note that the size of the Message Processor T5 object as recorded in the Object Table includes a checksum byte. If a checksum has not been requested, one byte should be deducted from the size of the object.

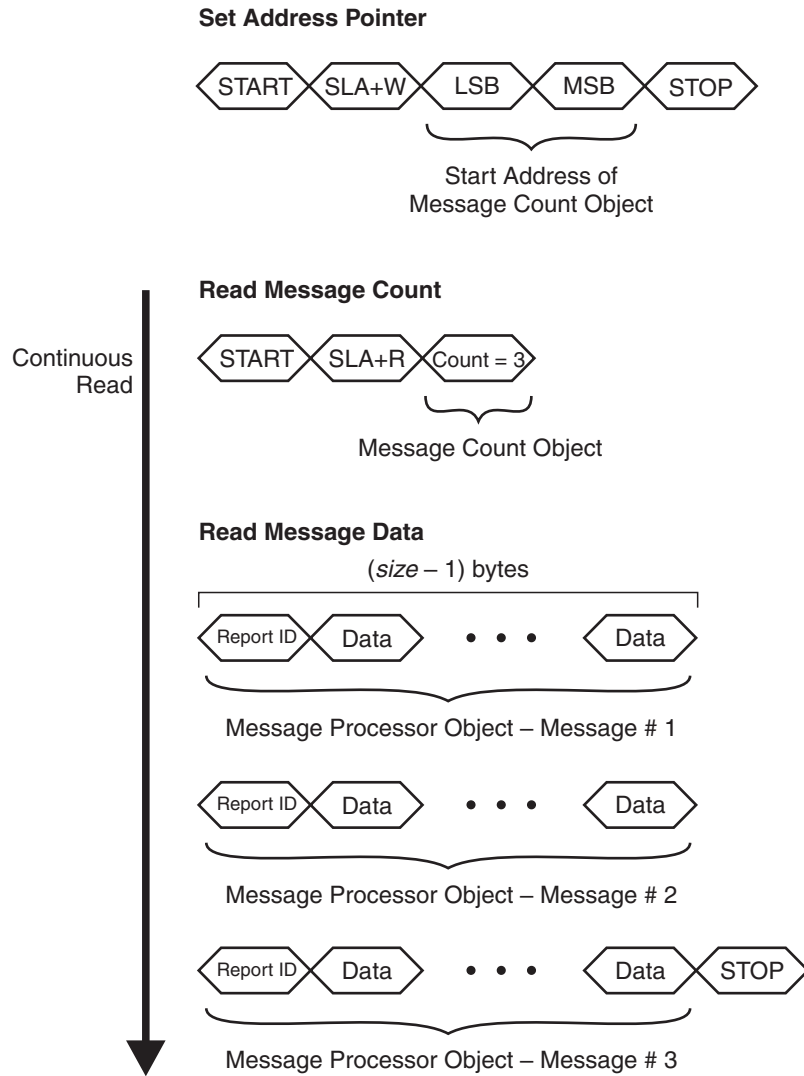
That is: number of bytes = count × (size – 1).

5. The host reads the calculated number of message bytes. It is important that the host does *not* send a STOP condition during the message reads, as this will terminate the continuous read operation and reset the address pointer. No START and STOP conditions must be sent between the messages.
6. The host sends a STOP condition at the end of the read operation after the last message has been read. The NACK condition immediately before the STOP condition resets the address pointer to the start of the Message Count T44 object.

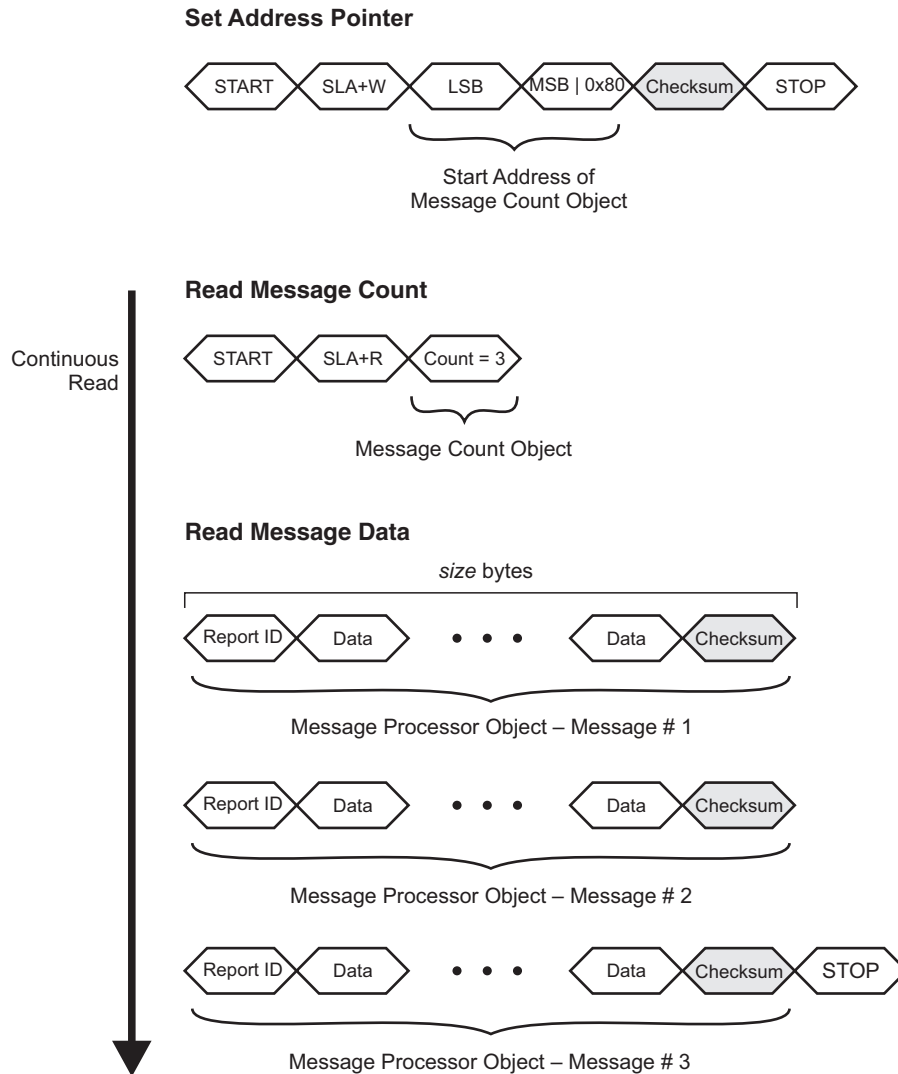
# MXT641T-AT/MXT641T-AB 1.0

Figure 8-4 shows an example of using a continuous read operation to read three messages from the device without a checksum. Figure 8-5 shows the same example with a checksum.

**FIGURE 8-4: CONTINUOUS MESSAGE READ EXAMPLE – NO CHECKSUM**



**FIGURE 8-5: CONTINUOUS MESSAGE READ EXAMPLE – I<sup>2</sup>C CHECKSUM MODE**



There are no checksums added on any other I<sup>2</sup>C reads. An 8-bit CRC can be added, however, to all I<sup>2</sup>C writes, as described in [Section 8.3 “I<sup>2</sup>C Writes in Checksum Mode”](#).

An alternative method of reading messages using the  $\overline{\text{CHG}}$  line is given in [Section 8.6 “CHG Line”](#).

## 8.6 $\overline{\text{CHG}}$ Line

The  $\overline{\text{CHG}}$  line is an active-low, open-drain output that is used to alert the host that a new message is available in the Message Processor T5 object. This provides the host with an interrupt-style interface with the potential for fast response times. It reduces the need for wasteful I<sup>2</sup>C communications.

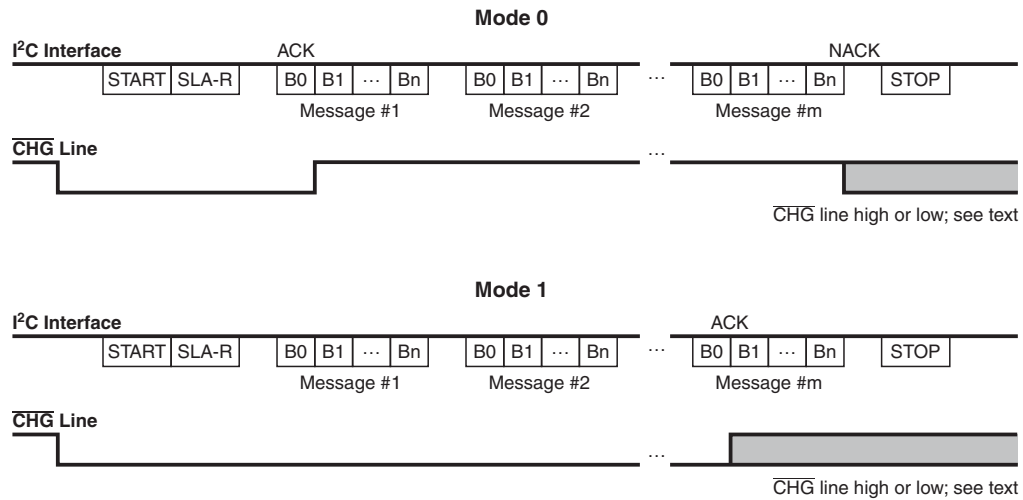
The  $\overline{\text{CHG}}$  line should always be configured as an input on the host during normal usage. This is particularly important after power-up or reset (see [Section 5.0 “Power-up / Reset Requirements”](#)).

A pull-up resistor is required to VddIO (see [Section 2.0 “Schematics”](#)).

The  $\overline{\text{CHG}}$  line operates in two modes when it is used with I<sup>2</sup>C communications, as defined by the Communications Configuration T18 object.

# MXT641T-AT/MXT641T-AB 1.0

FIGURE 8-6:  $\overline{\text{CHG}}$  LINE MODES FOR I<sup>2</sup>C-COMPATIBLE TRANSFERS



In Mode 0 (edge-triggered operation):

1. The  $\overline{\text{CHG}}$  line goes low to indicate that a message is present.
2. The  $\overline{\text{CHG}}$  line goes high when the first byte of the first message (that is, its report ID) has been sent and acknowledged (ACK sent) and the next byte has been prepared in the buffer.
3. The STOP condition at the end of an I<sup>2</sup>C transfer causes the  $\overline{\text{CHG}}$  line to stay high if there are no more messages. Otherwise the  $\overline{\text{CHG}}$  line goes low to indicate a further message.

Note that Mode 0 also allows the host to continually read messages by simply continuing to read bytes back without issuing a STOP condition. Message reading should end when a report ID of 255 (“invalid message”) is received. Alternatively the host ends the transfer by sending a NACK after receiving the last byte of a message, followed by a STOP condition. If there is another message present, the  $\overline{\text{CHG}}$  line goes low again, as in step 1. In this mode the state of the  $\overline{\text{CHG}}$  line does not need to be checked during the I<sup>2</sup>C read.

In Mode 1 (level-triggered operation):

1. The  $\overline{\text{CHG}}$  line goes low to indicate that a message is present.
2. The  $\overline{\text{CHG}}$  line remains low while there are further messages to be sent after the current message.
3. The  $\overline{\text{CHG}}$  line goes high again only once the first byte of the last message (that is, its report ID) has been sent and acknowledged (ACK sent) and the next byte has been prepared in the output buffer.

Mode 1 allows the host to continually read the messages until the  $\overline{\text{CHG}}$  line goes high, and the state of the  $\overline{\text{CHG}}$  line determines whether or not the host should continue receiving messages from the device.

**NOTE** The state of the  $\overline{\text{CHG}}$  line should be checked only between messages and not between the bytes of a message. The precise point at which the  $\overline{\text{CHG}}$  line changes state cannot be predicted and so the state of the  $\overline{\text{CHG}}$  line cannot be guaranteed between bytes.

The Communications Configuration T18 object can be used to configure the behavior of the  $\overline{\text{CHG}}$  line. In addition to the  $\overline{\text{CHG}}$  line operation modes described above, this object allows direct control over the state of the  $\overline{\text{CHG}}$  line.

## 8.7 SDA and SCL

The I<sup>2</sup>C bus transmits data and clock with SDA and SCL, respectively. These are open-drain. The device can only drive these lines low or leave them open. The termination resistors (Rp) pull the line up to VddIO if no I<sup>2</sup>C device is pulling it down.

The termination resistors should be chosen so that the rise times on SDA and SCL meet the I<sup>2</sup>C specifications for the interface speed being used, bearing in mind other loads on the bus. For best latency performance, it is recommended that no other devices share the I<sup>2</sup>C bus with the maXTouch controller.

## 8.8 Clock Stretching

The device supports clock stretching in accordance with the I<sup>2</sup>C specification. It may also instigate a clock stretch if a communications event happens during a period when the device is busy internally. The maximum clock stretch is approximately 10 to 15 ms.

# MXT641T-AT/MXT641T-AB 1.0

## 9.0 SPI COMMUNICATIONS

### 9.1 Communications Protocol

Communication with the device can be carried out over the Serial Peripheral Interface (SPI). The host communicates with the mXT641T-AT over the SPI using a master-slave relationship, with the mXT641T-AT acting in slave mode.

### 9.2 SPI Operation

The SPI uses four logic signals:

- **Serial Clock (SCK)** – output from the host.
- **Master Output, Slave Input (MOSI)** – output from the host, input to the mXT641T-AT. Used by the host to send data to the mXT641T-AT.
- **Master Input, Slave Output (MISO)** – input to the host, output from the mXT641T-AT. Used by the mXT641T-AT to send data to the host.
- **Slave Select ( $\overline{SS}$ )** – active low output from the host.

In addition the following pin is used:

- **Change Line ( $\overline{CHG}$ )** – active low input to the host, output from the mXT641T-AT. Used by the mXT641T-AT to indicate that a response is ready for transmission (see [Section 9.2.1 “Change Line \(CHG\)”](#)) or that an OBP message is pending.

The master pulls  $\overline{SS}$  low at the start of the SPI transaction and it remains low until the end of it.

At each byte, the master generates 8 clock pulses on SCK. With these 8 clock pulses, a byte of data is transmitted from the master to the slave over MOSI, most significant bit first.

Simultaneously a byte of data is transmitted from the slave to the master over MISO, also most significant bit first.

The mXT641T-AT requires that the clock idles “high” (CPOL=1). The data on MOSI and MISO pins are set at the falling edges and sampled at the rising edges (CPHA=1). This is known as SPI Mode 3.

The mXT641T-AT SPI interface can operate at a SCK frequency of up to 8 MHz.

<p><b>NOTE</b> The SPI interface is used in half duplex mode, even though it is a full duplex communication bus by its nature. This simplifies the protocol, minimizes the CPU processing required and avoids possible timing critical scenarios. This means that only one of the two in/out data lines (MOSI/MISO) will be meaningful at a time. During a read operation, therefore, the host must transmit 0xFF bytes on the MOSI line while it is reading data from the slave device. Similarly, during a write operation, the host must ignore the data on the MISO line.</p>
---

An SPI transaction is considered as initiated when the  $\overline{SS}$  line is asserted (active low) by the host and terminated when it is deasserted. The host can abort a transfer at any time by deasserting the  $\overline{SS}$  line.

#### 9.2.1 CHANGE LINE ( $\overline{CHG}$ )

The  $\overline{CHG}$  line is an active-low, open-drain output that is used as an interrupt to alert the host that the slave is ready to send a response or that an OBP message is pending and ready to be read from the Host.

The change line must be handled by the host as a falling edge triggered line. It must not be used a level triggered line. This avoids the situation in which the host initiates a new read/write operation (because the interrupt line is still asserted following a previous SPI transaction) but the target is not yet ready to handle it.

To prevent the host missing an interrupt, the target device can use a retriggering mechanism for the interrupt line. This guarantees that any pending message is always delivered. This mechanism must be enabled in the Communications Configuration T18 object.

## 9.2.2 SPI PROTOCOL OPCODES

The allowed operations and responses codes used by the SPI protocol are shown in [Table 9-1](#).

**TABLE 9-1: SPI OPCODES**

Name	Value	Operation
<b>Write Operation and Responses</b> (see <a href="#">Section 9.3 "Write Operation and Responses"</a> )		
SPI_WRITE_REQ	0x01	Write operation request
SPI_WRITE_OK	0x81	Write operation succeeded (response)
SPI_WRITE_FAIL	0x41	Write operation failed (response)
<b>Read Operation and Responses</b> (see <a href="#">Section 9.4 "Read Operation and Responses"</a> )		
SPI_READ_REQ	0x02	Read operation request
SPI_READ_OK	0x82	Read operation succeeded (response)
SPI_READ_FAIL	0x42	Read operation failed (response)
<b>General Responses</b> (see <a href="#">Section 9.5 "General Operations"</a> )		
SPI_INVALID_REQ	0x04	Invalid operation (response)
SPI_INVALID_CRC	0x08	Invalid CRC (response)

All the responses reported in [Table 9-1](#) require the Interrupt line to go from inactive (deasserted) to active (asserted) before the host can read a response following an SPI\_READ\_REQ or SPI\_WRITE\_REQ operation.

## 9.2.3 SPI TRANSACTION HEADER

Every SPI transaction includes a 6-byte HEADER that has the format shown in [Table 9-2](#).

**TABLE 9-2: HEADER FORMAT**

Byte	Field	Description
0	Opcode	Op code for the transaction
1	Address LSByte	The memory address of the slave device where the Host wants to write to or read from.
2	Address MSByte	
3	Length LSByte	The number of bytes that the host wants to write to or read from the slave device.
4	Length MSByte	
5	CRC	8-bit CRC

An 8-bit CRC is used to detect errors on the 5 bytes of the header (that is: Opcode, Address LSB, Address MSB, Length LSByte, Length MSByte) in order to prevent the writing to or reading from unwanted objects if the header gets corrupted during the SPI transfer. The 8-bit CRC algorithm is the same as that used to calculate the CRC for Message Processor T5 messages.

## 9.3 Write Operation and Responses

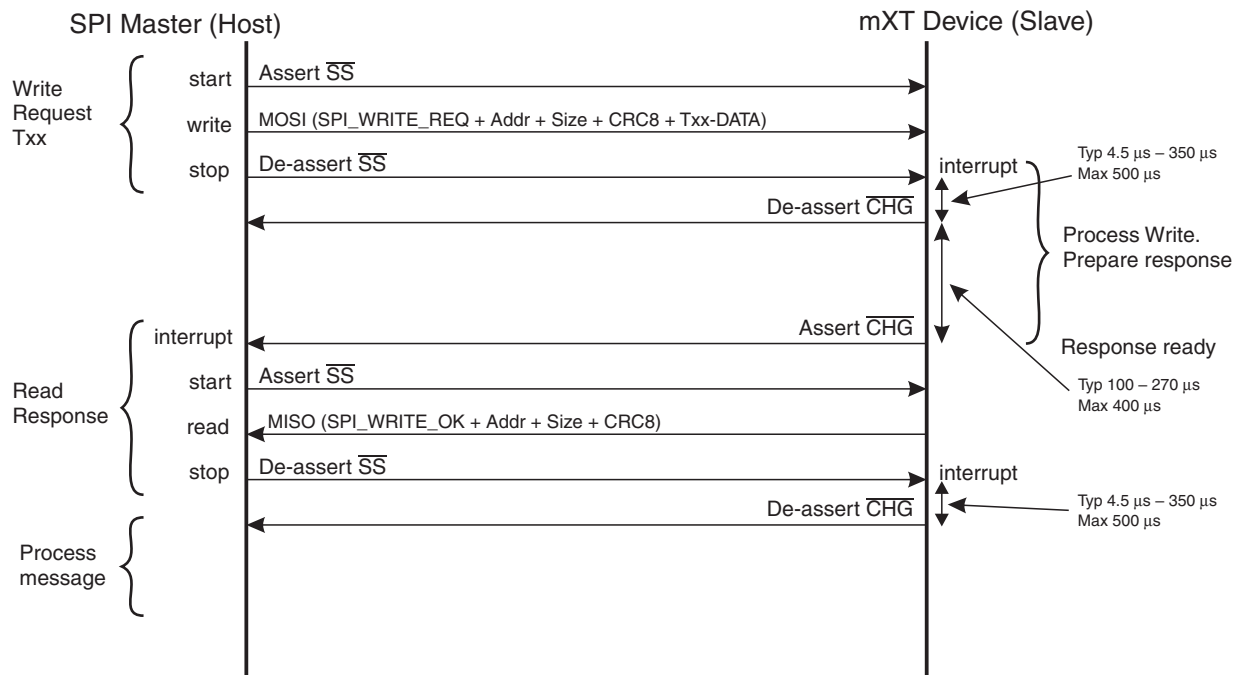
The write operation and its responses allows the host to write to an object configuration area.

The flow and timing are shown in [Figure 9-1](#).

Note that no detection mechanism is provided at the SPI network layer level on the data written, but the host can check the correctness of the data that is read back by using a checksum. This allows the host to detect whether the payload of the write operation was corrupted or not during the SPI transaction (see [Figure 9-5](#)).

# MXT641T-AT/MXT641T-AB 1.0

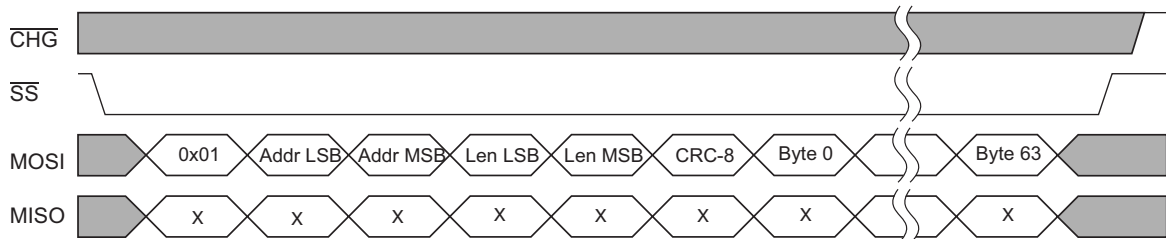
**FIGURE 9-1: SPI WRITE CONFIGURATION MESSAGE FLOW AND TIMING**



## 9.3.1 SPI\_WRITE\_REQ

Figure 9-2 shows the message format used for the write request operation.

**FIGURE 9-2: SPI\_WRITE\_REQ**



In Figure 9-2:

- **0x01** is the opcode
- **Addr LSB and Addr MSB** together specify the address to which the host wishes to write
- **Len LSB and Len MSB** together specify the length of the data in bytes. This is the total number of bytes that the Host wishes to write to the slave device (excluding the header bytes)
- **CRC-8** is the 8-bit CRC
- **Byte 0 .. Byte 63** contain the data that is to be written (64 bytes maximum).

If the host needs to write more than 64 bytes of data then multiple SPI\_WRITE\_REQ operations are required.

Following an SPI\_WRITE\_REQ operation, the host must wait for a response from the device before accessing the SPI bus again. If the slave system does not assert the interrupt line within 10 ms, a HW reset or a retry from the Host is necessary. When the response is ready to be sent, the target device asserts the interrupt line to notify the host that a message is ready to be read. Only at this point is the host allowed to initiate a new SPI transaction to read back the response related to the previous write operation.

This means that an object message will be blocked during the time that a response related to a previous read or write request is pending and has not yet been read back by the Host.



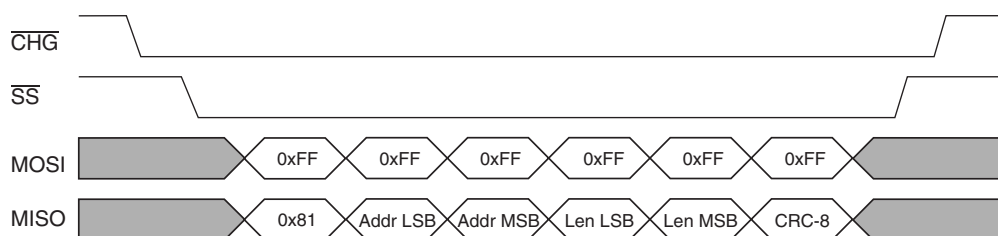
The following responses are possible following an SPI\_WRITE\_REQ operation:

- **SPI\_WRITE\_OK** – Generated if the write operation was successfully completed (the memory address and length specified by the host were within the allowed accessible memory map regions). See [Section 9.3.2 “SPI\\_WRITE\\_OK”](#)
- **SPI\_WRITE\_FAIL** – Generated if the write operation failed, for example if the host tries to write to an address outside the available memory map. See [Section 9.3.3 “SPI\\_WRITE\\_FAIL”](#)
- **SPI\_INVALID\_REQ** – See [Section 9.5.1 “SPI\\_INVALID\\_REQ”](#)
- **SPI\_INVALID\_CRC** – See [Section 9.5.2 “SPI\\_INVALID\\_CRC”](#)

## 9.3.2 SPI\_WRITE\_OK

[Figure 9-3](#) shows the message format used for the write OK response.

**FIGURE 9-3: SPI\_WRITE\_OK**



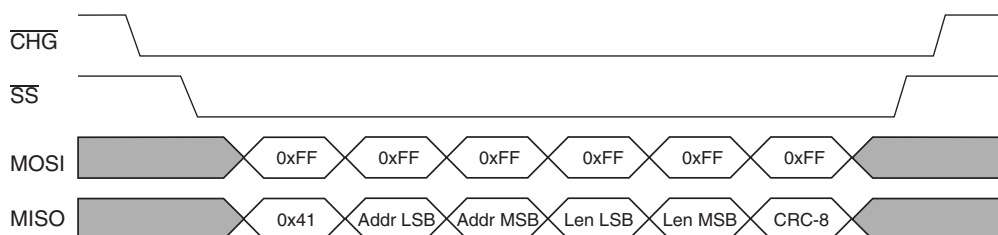
In [Figure 9-3](#):

- **0x81** is the opcode
- **Addr LSB and Addr MSB** together specify the address to which the data was written
- **Len LSB and Len MSB** together specify the length of the data in bytes. This is the total number of bytes that was written to the slave device (excluding the header bytes)
- **CRC-8** is the 8-bit CRC

## 9.3.3 SPI\_WRITE\_FAIL

[Figure 9-4](#) shows the message format used for the write fail response.

**FIGURE 9-4: SPI\_WRITE\_FAIL**



In [Figure 9-4](#):

- **0x41** is the opcode
- **Addr LSB and Addr MSB** together specify the address to which the host requested the write
- **Len LSB and Len MSB** together specify the length of the data in bytes. This is the total number of bytes that the Host attempted to write to the slave device (excluding the header bytes)
- **CRC-8** is the 8-bit CRC

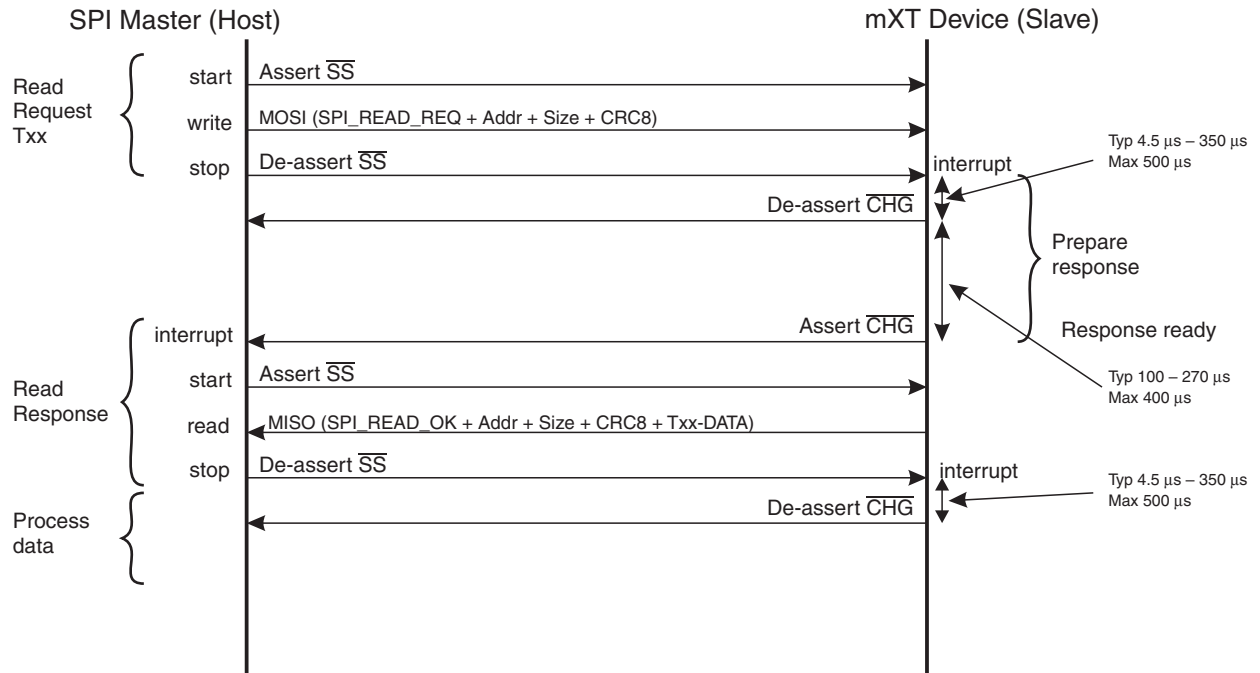
# MXT641T-AT/MXT641T-AB 1.0

## 9.4 Read Operation and Responses

The read request operation allows the host to read from the object memory map for the device. This allows the host to read a message from the Message Processor T5 object or read from an object configuration area.

The flow and timing are shown in [Figure 9-5](#).

**FIGURE 9-5: SPI READ CONFIGURATION MESSAGE FLOW AND TIMING**



Normally a limit of 64 bytes is allowed for data reads. If the host tries to read more than 64 bytes, the slave returns SPI\_READ\_FAIL (see [Section 9.4.3 "SPI\\_READ\\_FAIL"](#)). A mechanism is provided, however, that supports the DMA transfer of a large block of data that exceeds this limit. This is achieved by the provision of multiple instances of the Data Container T117 object within the device that allow up to 1290 bytes of data to be read in a contiguous manner.

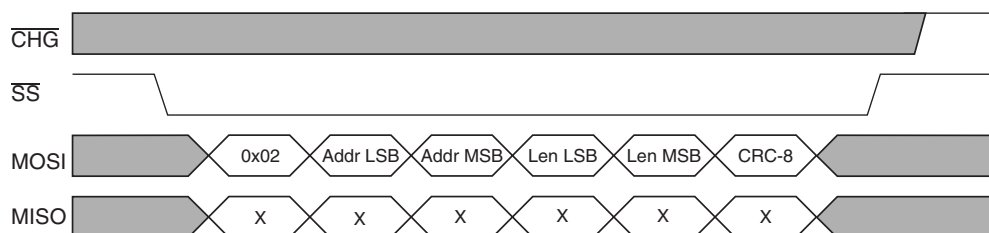
Under certain circumstances, a CRC can be used as an error detection mechanism when reading an object:

- Message Processor T5 – When reading a message from the Message Processor T5 object, an optional CRC as an error detection mechanism is provided. This is enabled in the Message Processor T5 object.
- Data Container T117 – When performing a block data transfer from Data Container T117 instances, however, the header bytes within the data can be configured to provide a CRC on the data.
- All other objects – When reading from any other object configuration area, no error detection mechanism is provided, as this operation is typically performed only at system startup. It is possible, however, to verify a read operation by performing it twice and comparing the results.

### 9.4.1 SPI\_READ\_REQ

[Figure 9-6](#) shows the message format used for the read request operation.

**FIGURE 9-6: SPI\_READ\_REQ**



The SPI\_READ\_REQ operation can be initiated by the host at any time, regardless of the state of the interrupt line. The slave device will assert the interrupt line when there are object messages pending. When the master asserts  $\overline{SS}$  (whether to respond to the slave asserting the interrupt line or because the master wants to initiate a transaction), the interrupt line is deasserted until the message from the master has been received and processed.

In [Figure 9-6](#):

- **0x02** is the opcode
- **Addr LSB and Addr MSB** together specify the address from which the host wishes to read
- **Len LSB and Len MSB** together specify the length of the data in bytes. This is the total number of bytes (excluding the header bytes) that the Host wishes to read from the slave device. The limit is 64 bytes for normal reads, and 1290 maximum for a block data transfer from Data Container T117 instances
- **CRC-8** is the 8-bit CRC

The actual data is sent in the subsequent SPI\_READ\_OK operation.

Following an SPI\_READ\_REQ operation, the host must wait for a response to be ready from the device before accessing the SPI bus again. If the slave system does not assert the interrupt line within 10 ms, a HW reset or a retry from the Host is necessary. When the response is ready to be sent, the target device asserts the interrupt line to notify the host that a message is ready to be read. Only at this point is the host allowed to initiate a new SPI transaction to read back the response related to the previous write operation.

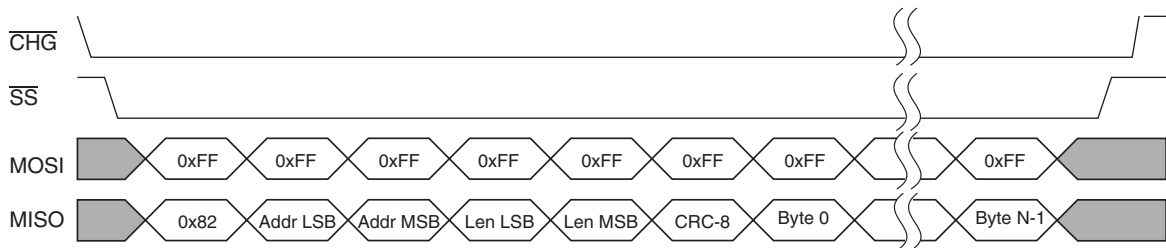
The following responses are possible following an SPI\_READ\_REQ operation:

- **SPI\_READ\_OK** – Generated if the read operation was successfully completed (the memory address and length specified by the host were within the allowed accessible memory map regions). See [Section 9.4.2 “SPI\\_READ\\_OK”](#)
- **SPI\_READ\_FAIL** – Generated if the read operation failed, for example if the host tries to read from an address outside the available memory map. See [Section 9.4.3 “SPI\\_READ\\_FAIL”](#)
- **SPI\_INVALID\_REQ** – See [Section 9.5.1 “SPI\\_INVALID\\_REQ”](#)
- **SPI\_INVALID\_CRC** – See [Section 9.5.2 “SPI\\_INVALID\\_CRC”](#)

## 9.4.2 SPI\_READ\_OK

[Figure 9-7](#) shows the message format used for the read OK response.

**FIGURE 9-7: SPI\_READ\_OK**



In [Figure 9-7](#):

- **0x82** is the opcode
- **Addr LSB and Addr MSB** together specify the address from which the host requested the data should be read
- **Len LSB and Len MSB** together specify the length of the data in bytes. This is the total number of bytes that the Host requested to read from the slave device (excluding the header bytes)
- **CRC-8** is the 8-bit CRC
- **Byte 0 .. Byte N-1** contain the data that is to be written, where  $N$  the number of bytes (maximum 64 bytes for normal reads, and 1290 for block data transfers from Data Container T117 instances)

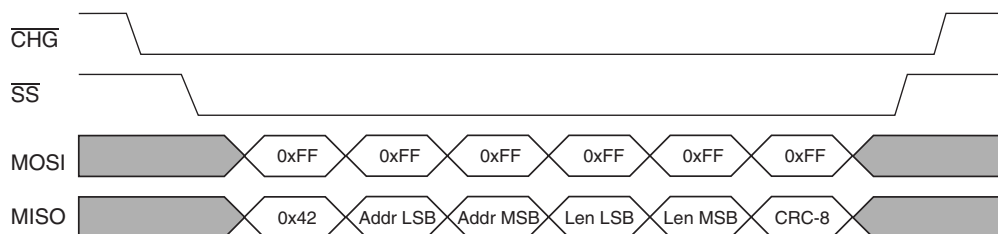
Note that, although the slave device flushes the transmit buffer when the host performs a read operation, any attempt by the Host to read more data than expected (that is, greater than Len bytes) could cause the slave device to transmit junk data on the MISO line.

# MXT641T-AT/MXT641T-AB 1.0

## 9.4.3 SPI\_READ\_FAIL

Figure 9-8 shows the message format used for the read fail response.

**FIGURE 9-8: SPI\_READ\_FAIL**



In Figure 9-8:

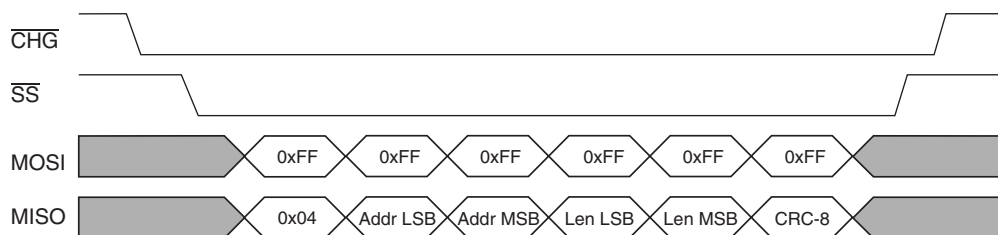
- **0x42** is the opcode
- **Addr LSB and Addr MSB** together specify the address from which the host requested the data should be read
- **Len LSB and Len MSB** together specify the length of the data in bytes. This is the total number of bytes that the Host attempted to read from the slave device (excluding the header bytes)
- **CRC-8** is the 8-bit CRC

## 9.5 General Operations

### 9.5.1 SPI\_INVALID\_REQ

Figure 9-9 shows the message format used for the Invalid Request response. The purpose of this opcode is to report to the host that the opcode of the last request was not recognized or that the Host has tried to perform another read or write operation without waiting for the response from the previous request.

**FIGURE 9-9: SPI\_INVALID\_REQ**



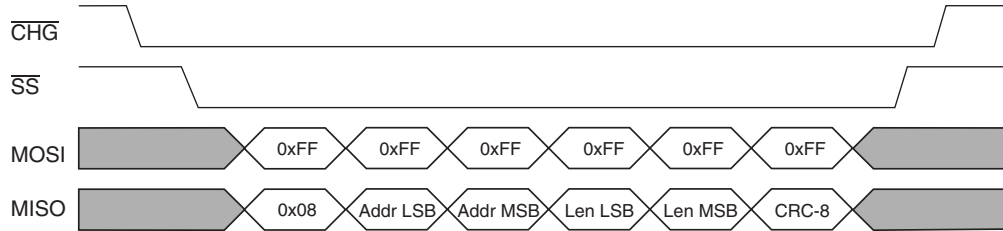
In Figure 9-9:

- **0x04** is the opcode
- **Addr LSB and Addr MSB** together specify the address received in the invalid request
- **Len LSB and Len MSB** together specify the length of the data in bytes. This is the total number of bytes that the Host attempted to read from or write to from the slave device (excluding the header bytes)
- **CRC-8** is the 8-bit CRC

## 9.5.2 SPI\_INVALID\_CRC

Figure 9-10 shows the message format used for the Invalid CRC response. The purpose of this opcode is to report an error in the CRC check performed on the received data.

**FIGURE 9-10: SPI\_INVALID\_CRC**



In Figure 9-10:

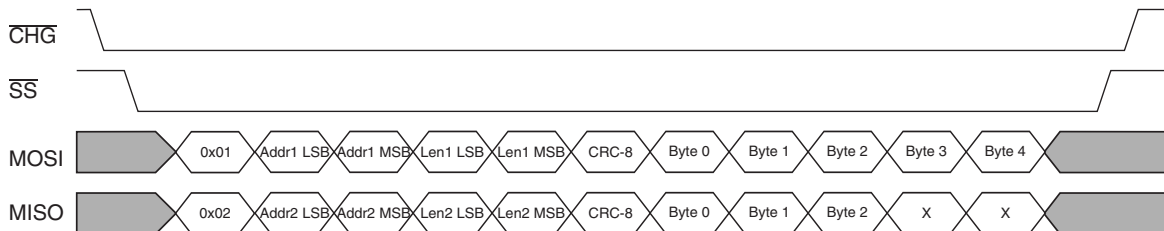
- **0x08** is the opcode
- **Addr LSB and Addr MSB** together specify the address received in the last request
- **Len LSB and Len MSB** together specify the length of the data in bytes. This is the total number of bytes that the Host attempted to read from or write to from the slave device in the last request (excluding the header bytes)
- **CRC-8** is the 8-bit CRC

## 9.6 Example of a Failed Transaction

In order to prevent unpredictable system behavior, the host *must* always wait for the response of the last request issued to be ready before initiating a new SPI request transaction. If the host does not comply with the protocol specification, clashes can occur.

For example, Figure 9-11 shows the situation in which an SPI\_READ\_OK (0x82) response with a payload of 3 bytes is expected, but the host performs an SPI\_WRITE\_REQ (0x01) operation instead to write 5 bytes to address *Addr1*. In this case, the slave device outputs the SPI\_READ\_OK data on the MISO line (this will have been prepared in advance before the interrupt line was asserted) and ignores the new Host request received on the MOSI line. The slave device will send the Host an SPI\_INVALID\_REQ response, in response to the following read or write request, to indicate a violation of the SPI protocol.

**FIGURE 9-11: EXAMPLE CLASH – SPI\_WRITE\_REQ WHEN SPI\_READ\_OK IS EXPECTED**



# MXT641T-AT/MXT641T-AB 1.0

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## 10.0 PCB DESIGN CONSIDERATIONS

### 10.1 Introduction

The following sections give the design considerations that should be adhered to when designing a PCB layout for use with the mXT641T-AT. Of these, power supply and ground tracking considerations are the most critical.

By observing the following design rules, and with careful preparation for the PCB layout exercise, designers will be assured of a far better chance of success and a correctly functioning product.

### 10.2 Printed Circuit Board

Microchip recommends the use of a four-layer printed circuit board for mXT641T-AT applications. This, together with careful layout, will ensure that the board meets relevant EMC requirements for both noise radiation and susceptibility, as laid down by the various national and international standards agencies.

#### 10.2.1 PCB CLEANLINESS

Modern no-clean-flux is generally compatible with capacitive sensing circuits.

**CAUTION!** If a PCB is reworked to correct soldering faults relating to any device, or to any associated traces or components, be sure that you fully understand the nature of the flux used during the rework process. Leakage currents from hygroscopic ionic residues can stop capacitive sensors from functioning. If you have any doubts, a thorough cleaning after rework may be the only safe option.

### 10.3 Power Supply

#### 10.3.1 SUPPLY QUALITY

While the device has good Power Supply Rejection Ratio properties, poorly regulated and/or noisy power supplies can significantly reduce performance.

Particular care should be taken of the AVdd supply, as it supplies the sensitive analog stages in the device.

#### 10.3.2 SUPPLY RAILS AND GROUND TRACKING

Power supply and clock distribution are the most critical parts of any board layout. Because of this, it is advisable that these be completed before any other tracking is undertaken. After these, supply decoupling, and analog and high speed digital signals should be addressed. Track widths for all signals, especially power rails should be kept as wide as possible in order to reduce inductance.

The Power and Ground planes themselves can form a useful capacitor. Flood filling for either or both of these supply rails, therefore, should be used where possible. It is important to ensure that there are no floating copper areas remaining on the board: all such areas should be connected to the ground plane. The flood filling should be done on the outside layers of the board.

#### 10.3.3 POWER SUPPLY DECOUPLING

Decoupling capacitors should be fitted as specified in [Section 2.3 “Schematic Notes”](#).

The decoupling capacitors must be placed as close as possible to the pin being decoupled. The traces from these capacitors to the respective device pins should be wide and take a straight route. They should be routed over a ground plane as much as possible. The capacitor ground pins should also be connected directly to a ground plane.

Surface mounting capacitors are preferred over wire-leaded types due to their lower ESR and ESL. It is often possible to fit these decoupling capacitors underneath and on the opposite side of the PCB to the digital ICs. This will provide the shortest tracking, and most effective decoupling possible.

#### 10.3.4 VOLTAGE PUMP

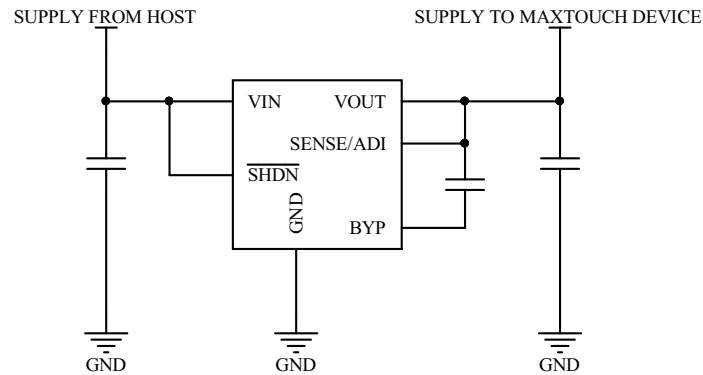
The voltage pump capacitors between EXTCAP0 and EXTCAP1 (Cd on the schematic in [Section 2.0 “Schematics”](#)) must be placed as close as possible to the EXTCAP $n$  pins. The two traces must be kept as short and as wide as possible for best pump performance. They should also be routed as parallel and as close as possible to each other in order to reduce emissions, and ideally both traces should be the same length.

## 10.4 Voltage Regulators

Each supply rail requires a Low Drop-Out (LDO) voltage regulator, although an LDO can be shared where supply rails share the same voltage level.

Figure 10-1 shows an example circuit for an LDO.

**FIGURE 10-1: EXAMPLE LDO CIRCUIT**



An LDO regulator should be chosen that provides adequate output capability, low noise, good load regulation and step response. The voltage regulators listed in Table 10-1 have been tested and found to work well with maXTouch devices. If it is desired to use an alternative LDO, however, certain performance criteria should be verified before using the device. These are:

- Stable with high value multi-layer ceramic capacitors on the output
- Low output noise – less than 100  $\mu\text{V}$  RMS over the range 10 Hz to 1 MHz
- Good load transient response – this should be less than 35 mV peak when a load step change of 100 mA is applied at the device output terminal
- No-load stable – Some LDOs become unstable if the output current falls below a certain minimum. If this is the case, then this minimum must be lower than the minimum current consumed by the mXT641T-AT (for example, in deep sleep).

**TABLE 10-1: SUITABLE LDO REGULATORS**

Manufacturer	Device	Current Rating (mA)
Microchip Technology Inc.	MCP1824	300
Microchip Technology Inc.	MCP1824S	300
Microchip Technology Inc.	MAQ5300	300
Microchip Technology Inc.	MCP1725	500
Analog Devices	ADP122/ADP123	300
Diodes Inc.	AP2125	300
Diodes Inc.	AP7335	300
Linear Technology	LT1763CS8-3.3	500
NXP	LD6836	300
Texas Instruments	LP3981	300

**Note:** Some manufacturers claim that minimal or no capacitance is required for correct regulator operation. However, in all cases, a minimum of a 1.0  $\mu\text{F}$  ceramic, low ESR capacitor at the input and output of these devices should be used. The manufacturer's datasheets should always be referred to when selecting capacitors for these devices and the typical recommended values, types and dielectrics adhered to.

# MXT641T-AT/MXT641T-AB 1.0

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## 10.4.1 SINGLE SUPPLY OPERATION

When designing a PCB for an application using a single LDO, extra care should be taken to ensure short, low inductance traces between the supply and the touch controller supply input pins. Ideally, tracking for the individual supplies should be arranged in a star configuration, with the LDO at the junction of the star. This will ensure that supply current variations or noise in one supply rail will have minimum effect on the other supplies. In applications where a ground plane is not practical, this same star layout should also apply to the power supply ground returns.

Only regulators with a 300 mA or greater rating can be used in a single-supply design.

Refer to the following application note for more information on routing with a single LDO:

- Application Note: MXTAN0208 – *Design Guide for PCB Layouts for maXTouch Touch Controllers*

## 10.4.2 MULTIPLE VOLTAGE REGULATOR SUPPLY

The AVdd supply stability is critical for the device because this supply interacts directly with the analog front end. If noise problems exist when using a single LDO regulator, Microchip recommends that AVdd is supplied by a regulator that is separate from the digital supply. This reduces the amount of noise injected into the sensitive, low signal level parts of the design.

## 10.5 Analog I/O

In general, tracking for the analog I/O signals from the device should be kept as short as possible. These normally go to a connector which interfaces directly to the touchscreen.

Ensure that adequate ground-planes are used. An analog ground plane should be used in addition to a digital one. Care should be taken to ensure that both ground planes are kept separate and are connected together only at the point of entry for the power to the PCB. This is usually at the input connector.

## 10.6 Component Placement and Tracking

It is important to orient all devices so that the tracking for important signals (such as power and clocks) are kept as short as possible.

### 10.6.1 DIGITAL SIGNALS

In general, when tracking digital signals, it is advisable to avoid sharp directional changes on sensitive signal tracks (such as analog I/O) and any clock or crystal tracking.

A good ground return path for all signals should be provided, where possible, to ensure that there are no discontinuities.

## 10.7 EMC and Other Observations

The following recommendations are not mandatory, but may help in situations where particularly difficult EMC or other problems are present:

- Try to keep as many signals as possible on the inside layers of the board. If suitable ground flood fills are used on the top and bottom layers, these will provide a good level of screening for noisy signals, both into and out of the PCB.
- Ensure that the on-board regulators have sufficient tracking around and underneath the devices to act as a heatsink. This heatsink will normally be connected to the 0 V or ground supply pin. Increasing the width of the copper tracking to any of the device pins will aid in removing heat. There should be no solder mask over the copper track underneath the body of the regulators.
- Ensure that the decoupling capacitors, especially high capacity ceramic type, have the requisite low ESR, ESL and good stability/temperature properties. Refer to the regulator manufacturer's datasheet for more information.



## 11.0 GETTING STARTED WITH MXT641T-AT/MXT641T-AB

### 11.1 Establishing Contact

#### 11.1.1 COMMUNICATION WITH THE HOST

The host can use any of the following interfaces to communicate with the device (See [Section 7.0 “Host Communications”](#)):

- I<sup>2</sup>C interface (see [Section 8.0 “I2C Communications”](#))
- SPI interface (see [Section 9.0 “SPI Communications”](#))

#### 11.1.2 POWER-UP SEQUENCE

On power-up, the  $\overline{\text{CHG}}$  line goes low to indicate that there is new data to be read from the device. If the  $\overline{\text{CHG}}$  line does not go low, there is a problem with the device.

Once the  $\overline{\text{CHG}}$  line goes low, the host should attempt to read the first 7 bytes of memory from location 0x00 to establish that the device is present and running following power-up.

A checksum check is performed on the configuration settings held in the non-volatile memory. If the checksum does not match a stored copy of the last checksum, then this indicates that the settings have become corrupted. This is signaled to the host by setting the configuration error bit in the message data for the Command Processor T6 object.

### 11.2 Using the Object Protocol

The device has an object-based protocol that is used to communicate with the device. Typical communication includes configuring the device, sending commands to the device, and receiving messages from the device.

The host must perform the following initialization so that it can communicate with the device:

1. Read the start positions of all the objects in the device from the Object Table and build up a list of these addresses.
2. Use the Object Table to calculate the report IDs so that messages from the device can be correctly interpreted.

#### 11.2.1 CLASSES OF OBJECTS

The mXT641T-AT contains the following classes of objects:

- **Debug objects** – provide a raw data output method for development and testing.
- **General objects** – required for global configuration, transmitting messages and receiving commands.
- **Touch objects** – operate on measured signals from the touch sensor and report touch data.
- **Signal processing objects** – process data from other objects (typically signal filtering operations).
- **Support objects** – provide additional functionality on the device.

#### 11.2.2 OBJECT INSTANCES

**TABLE 11-1: OBJECTS ON THE MXT641T-AT**

Object	Description	Number of Instances	Usage
<b>Debug Objects</b>			
Diagnostic Debug T37	Allows access to diagnostic debug data to aid development.	1	Debug commands only. No configuration/tuning necessary. Not for use in production.
<b>General Objects</b>			
Message Processor T5	Handles the transmission of messages. This object holds a message in its memory space for the host to read.	1	No configuration necessary.
Command Processor T6	Performs a command when written to. Commands include reset, calibrate and backup settings.	1	No configuration necessary.

# MXT641T-AT/MXT641T-AB 1.0

**TABLE 11-1: OBJECTS ON THE MXT641T-AT (CONTINUED)**

Object	Description	Number of Instances	Usage
Power Configuration T7	Controls the sleep mode of the device. Power consumption can be lowered by controlling the acquisition frequency and the sleep time between acquisitions.	1	Must be configured before use.
Acquisition Configuration T8	Controls how the device takes each capacitive measurement.	1	Must be configured before use.
<b>Touch Objects</b>			
Key Array T15	Creates a rectangular array of keys. A Key Array T15 object reports simple on/off touch information.	2	Enable and configure as required.
Multiple Touch Touchscreen T100	Creates a Touchscreen that supports the tracking of more than one touch.	1	Enable and configure as required.
<b>Signal Processing Objects</b>			
One-touch Gesture Processor T24	Operates on the data from a Touchscreen object. A One-touch Gesture Processor T24 converts touches into one-touch finger gestures (for example, taps, double taps and drags).	1	Enable and configure as required.
Two-touch Gesture Processor T27	Operates on the data from a One-touch Gesture Processor T24 object. A Two-touch Gesture Processor T27 converts touches into two-touch finger gestures (for example, pinches, stretches and rotates).	1	Enable and configure as required.
Grip Suppression T40	Suppresses false detections caused, for example, by the user gripping the edge of the touchscreen.	1	Enable and configure as required.
Touch Suppression T42	Suppresses false detections caused by unintentional large touches by the user.	1	Enable and configure as required.
Passive Stylus T47	Processes passive stylus input.	1	Enable and configure as required.
Shieldless T56	Allows a sensor to use true single-layer co-planar construction.	1	Enable and configure as required.
Lens Bending T65	Compensates for lens deformation (lens bending) by attempting to eliminate the disturbance signal from the reported deltas.	3	Enable and configure as required.
Noise Suppression T72	Performs various noise reduction techniques during touchscreen signal acquisition.	1	Enable and configure as required.
Glove Detection T78	Allows for the reporting of glove touches.	1	Enable and configure as required.
Retransmission Compensation T80	Limits the negative effects on touch signals caused by poor device coupling to ground.	1	Enable and configure as required.
Gesture Processor T84	Object not supported in this firmware version		
Self Capacitance Noise Suppression T108	Suppresses the effects of external noise within the context of self capacitance touch measurements.	1	Enable and configure as required.
Self Capacitance Grip Suppression T112	Allows touches to be reported from the self capacitance measurements while the device is being gripped.	2	Enable and configure as required.

**TABLE 11-1: OBJECTS ON THE MXT641T-AT (CONTINUED)**

Object	Description	Number of Instances	Usage
<b>Support Objects</b>			
Communications Configuration T18	Configures additional communications behavior for the device.	1	Check and configure as necessary.
GPIO Configuration T19	Allows the host controller to configure and use the general purpose I/O pins on the device.	1	Enable and configure as required.
Self Test T25	Configures and performs self-test routines to find faults on a touch sensor.	1	Configure as required for pin test commands.
User Data T38	Provides a data storage area for user data.	1	Configure as required.
Message Count T44	Provides a count of pending messages.	1	Read-only object.
CTE Configuration T46	Controls the capacitive touch engine for the device.	1	Must be configured.
Timer T61	Provides control of a timer.	6	Enable and configure as required.
Serial Data Command T68	Provides an interface for the host driver to deliver various data sets to the device.	1	Enable and configure as required.
Dynamic Configuration Controller T70	Allows rules to be defined that respond to system events.	20	Enable and configure as required.
Dynamic Configuration Container T71	Allows the storage of user configuration on the device that can be selected at runtime based on rules defined in the Dynamic Configuration Controller T70 object.	1	Configure if Dynamic Configuration Controller T70 is in use.
CTE Scan Configuration T77	Configures enhanced X line scanning features.	1	Enable and configure as required.
Touch Event Trigger T79	Configures touch triggers for use with the event handler.	3	Enable and configure as required.
Touchscreen Hover Configuration T101	Object not supported in this firmware version		
Auxiliary Touch Configuration T104	Allows the setting of self capacitance gain and thresholds for a particular measurement to generate auxiliary touch data for use by other objects.	1	Enable and configure if using self capacitance measurements
Self Capacitance Global Configuration T109	Provides configuration for a self capacitance measurements employed on the device.	1	Check and configure as required (if using self capacitance measurements).
Self Capacitance Tuning Parameters T110	Provides configuration space for a generic set of settings for self capacitance measurements.	9	Use under the guidance of Microchip field engineers only.
Self Capacitance Configuration T111	Provides configuration for self capacitance measurements employed on the device.	3	Check and configure as required (if using self capacitance measurements).

# MXT641T-AT/MXT641T-AB 1.0

TABLE 11-1: OBJECTS ON THE MXT641T-AT (CONTINUED)

Object	Description	Number of Instances	Usage
Self Capacitance Measurement Configuration T113	Configures self capacitance measurements to generate data for use by other objects.	1	Enable and configure as required.
Data Container T117	Provides a mechanism for retrieving specific data held in the device's internal memory.	6	Read-only object. No configuration necessary.
Data Container Controller T118	Provides direct access to internal data in memory for use with the Data Container T117 objects.	1	Enable and configure as required.

## 11.2.3 CONFIGURING AND TUNING THE DEVICE

The objects are designed such that a default value of zero in their fields is a “safe” value that typically disables functionality. The objects must be configured before use and the settings written to the non-volatile memory using the Command Processor T6 object.

Perform the following actions for each object:

1. Enable the object, if the object requires it.
2. Configure the fields in the object, as required.
3. Enable reporting, if the object supports messages, to receive messages from the object.

## 11.3 Writing to the Device

The following mechanisms can be used to write to the device:

- Using an I<sup>2</sup>C write operation (see [Section 8.2 “Writing To the Device”](#)).
- Using the SPI write operation (see [Section 9.3 “Write Operation and Responses”](#)).

Communication with the device is achieved by writing to the appropriate object:

- To send a command to the device, an appropriate command is written to the Command Processor T6 object.
- To configure the device, a configuration parameter is written to the appropriate object. For example, writing to the Power Configuration T7 configures the power consumption for the device and writing to the touchscreen Multiple Touch Touchscreen T100 object sets up the touchscreen. Some objects are optional and need to be enabled before use.

<b>IMPORTANT!</b>	When the host issues any command within an object that results in a flash write to the device Non-Volatile Memory (NVM), that object should have its CTRL RPTEN bit set to 1, if it has one. This ensures that a message from the object writing to the NVM is generated at the completion of the process and an assertion of the CHG line is executed.  The host must also ensure that the assertion of the $\overline{\text{CHG}}$ line refers to the expected object report ID before asserting the $\overline{\text{RESET}}$ line to perform a reset. Failure to follow this guidance may result in a corruption of device configuration area and the generation of a CFGERR.
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## 11.4 Reading from the Device

Status information is stored in the Message Processor T5 object. This object can be read to receive any status information from the device. The following mechanisms provide an interrupt-style interface for reading messages in the Message Processor T5 object:

- The  $\overline{\text{CHG}}$  line is asserted whenever a new message is available in the Message Processor T5 object (see [Section 8.6 “CHG Line”](#)). See [Section 8.4 “Reading From the Device”](#) for information on the format of the I<sup>2</sup>C read operation.
- When using the SPI interface, two SPI transactions must take place: the first is an SPI Read request which is used to set the address pointer (Address LSByte and MSByte) and to indicate to the slave device how many bytes (Length LSByte and MSByte) the Host wants to read; the second is a response which comes with a payload that actually contains the data that was requested (see [Section 9.4 “Read Operation and Responses”](#)).

# MXT641T-AT/MXT641T-AB 1.0

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Note that the host should always wait to be notified of messages. The host should not poll the device for messages. In particular, when the SPI interface is used, the  $\overline{\text{CHG}}$  line must never be polled. The reason for this is that when polling the Host handling of the  $\overline{\text{CHG}}$  line will be level based instead of falling edge based, as is required.

# MXT641T-AT/MXT641T-AB 1.0

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## 12.0 DEBUGGING AND TUNING

### 12.1 SPI Debug Interface

The SPI Debug Interface is used for tuning and debugging when running the system and allows the development engineer to use Microchip maXTouch Studio to read the real-time raw data. This uses the low-level debug port, accessed via the SPI interface.

The SPI Debug Interface consists of the  $\overline{\text{DBG\_SS}}$ ,  $\text{DBG\_CLK}$ , and  $\text{DBG\_DATA}$  lines. It is recommended that these pins are routed to test points on all designs such that they can be connected to external hardware during system development. These lines should not be connected to power or GND. See [Section 2.3.10 “SPI Debug Interface”](#) for more details.

The SPI Debug Interface is enabled by the Command Processor T6 object and by default will be off.

<b>NOTE</b> The touch controller will take care of the pin configuration. When the $\overline{\text{DBG\_SS}}$ , $\text{DBG\_CLK}$ , and $\text{DBG\_DATA}$ lines are in use for debugging, any alternative function for the pins cannot be used.
---

### 12.2 Object-based Protocol

The device provides a mechanism for obtaining debug data for development and testing purposes by reading data from the Diagnostic Debug T37 object.

<b>NOTE</b> The Diagnostic Debug T37 object is of most use for simple tuning purposes. When debugging a design, it is preferable to use the SPI Debug Interface, as this will have a much higher bandwidth and can provide real-time data.
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### 12.3 Self Test

There is a Self Test T25 object that runs self-test routines in the device to find hardware faults on the sense lines and the electrodes. This object also performs an initial pin fault test on power-up to ensure that there is no X-to-Y short before the high-voltage supply is enabled inside the chip. A high-voltage short on the sense lines would break the device.

## 13.0 SPECIFICATIONS

### 13.1 Absolute Maximum Specifications

Vdd	3.6 V
VddIO	3.6 V
AVdd	3.6 V
Maximum continuous combined pin current, all GPIO $n$ pins	60 mA
Voltage forced onto any pin	-0.3 V to Vdd/VddIO/AVdd + 0.3 V
Configuration parameters maximum writes	10,000
Maximum junction temperature	125°C

**CAUTION!** Stresses beyond those listed under *Absolute Maximum Specifications* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum specification conditions for extended periods may affect device reliability.

### 13.2 Recommended Operating Conditions

Operating temperature	mXT641T-AT: -40°C to +85°C (Grade 3)
	mXT641T-AB: -40°C to +105°C (Grade 2)
Storage temperature	-60°C to +150°C
Vdd	3.3 V $\pm$ 5%
VddIO	1.8 V to 3.3 V
AVdd	3.3 V $\pm$ 5%
XVdd with internal voltage doubler enabled	Vdd to 2 $\times$ Vdd
Temperature slew rate	10°C/min

# MXT641T-AT/MXT641T-AB 1.0

## 13.2.1 DC CHARACTERISTICS

### 13.2.1.1 Analog Voltage Supply – AVdd

Parameter	Min	Typ	Max	Units	Notes
<b>AVdd</b>					
Operating limits	3.14	3.3	3.47	V	
Supply Rise Rate	–	–	0.036	V/ $\mu$ s	For example, for a 3.3 V rail, the voltage must not rise in less than 91 $\mu$ s

### 13.2.1.2 Digital Voltage Supply – Vdd, VddIO

Parameter	Min	Typ	Max	Units	Notes
<b>VddIO</b>					
Operating limits	1.71	3.3	3.47	V	I <sup>2</sup> C
Supply Rise Rate	–	–	0.036	V/ $\mu$ s	For example, for a 3.3 V rail, the voltage must not rise in less than 91 $\mu$ s
<b>Vdd</b>					
Operating limits	3.14	3.3	3.47	V	
Supply Rise Rate	–	–	0.036	V/ $\mu$ s	For example, for a 3.3 V rail, the voltage must not rise in less than 91 $\mu$ s
Supply Fall Rate	–	–	0.05	V/ $\mu$ s	For example, for a 3.3 V rail, the voltage must not fall in less than 66 $\mu$ s

### 13.2.1.3 XVdd Voltage Supply – XVdd

Parameter	Min	Typ	Max	Units	Notes
<b>XVdd</b>					
Operating limits	Vdd	–	2 × Vdd	V	Maximum value with internal voltage doubler

## 13.2.2 POWER SUPPLY RIPPLE AND NOISE

Parameter	Min	Typ	Max	Units	Notes
Vdd	–	–	±50	mV	Across frequency range 1 Hz to 1 MHz
AVdd	–	–	±40	mV	Across frequency range 1 Hz to 1 MHz, with Noise Suppression enabled



## 13.3 Test Configuration

The values listed below were used in the reference unit to validate the interfaces and derive the characterization data provided in the following sections.

**TABLE 13-1: TEST CONFIGURATION**

Object/Parameter	Description/Setting (Numbers in Decimal)
Acquisition Configuration T8	
CHRGTIME	80
MEASALLOW	15
MEASIDLEDEF	2
MEASACTVDEF	2
One-touch Gesture Processor T24	Object Enabled
Two-touch Gesture Processor T27	Object Enabled
Touch Suppression T42	Object Enabled
CTE Configuration T46	
IDLESYNCSPERX	16
ACTVSYNCSPERX	16
Lens Bending T65 Instance 0	Object Enabled
Noise Suppression T72	Object Enabled
Retransmission Compensation T80	Object Enabled
Multiple Touch Touchscreen T100	Object Enabled
XSIZE	30
YSIZE	19
Auxiliary Touch Configuration T104	Object Enabled
Self Capacitance Configuration T111 Instance 0	
INTTIME	100
IDLESYNCSPERL	24
ACTVSYNCSPERL	24
Self Capacitance Configuration T111 Instance 1	
INTTIME	100
IDLESYNCSPERL	64
ACTVSYNCSPERL	64
Self Capacitance Configuration T111 Instance 2	
INTTIME	100
IDLESYNCSPERL	48
ACTVSYNCSPERL	48
Self Capacitance Grip Suppression T112 Instance 0	Object Enabled
Self Capacitance Grip Suppression T112 Instance 1	Object Enabled

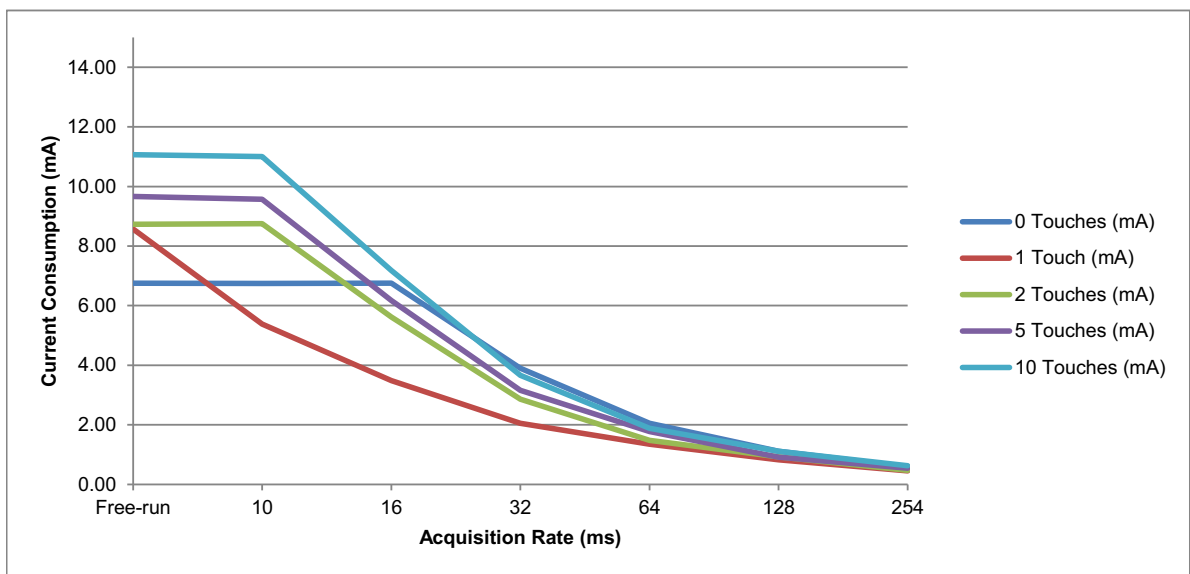
# MXT641T-AT/MXT641T-AB 1.0

## 13.4 Supply Current – I<sup>2</sup>C Interface

**NOTE** The characterization charts show typical values based on the configuration in [Table 13-1](#). Actual power consumption in the user's application will depend on the circumstances of that particular project and will vary from that shown here. Further tuning will be required to achieve an optimal performance.

### 13.4.1 ANALOG SUPPLY

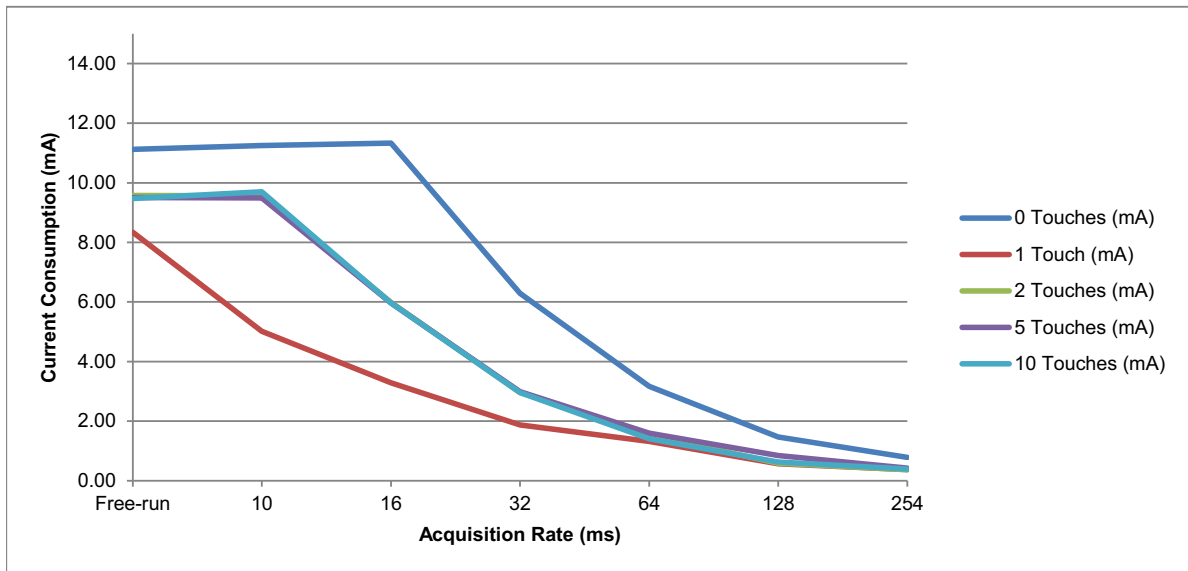
Acquisition Rate (ms)	0 Touches (mA)	1 Touch (mA)	2 Touches (mA)	5 Touches (mA)	10 Touches (mA)
Free-run	6.75	8.57	8.73	9.66	11.07
10	6.74	5.38	8.75	9.57	11.00
16	6.75	3.48	5.62	6.17	7.18
32	3.90	2.05	2.87	3.16	3.66
64	2.05	1.35	1.48	1.77	1.88
128	1.11	0.82	0.92	0.92	1.11
254	0.59	0.46	0.47	0.55	0.63



## 13.4.2 DIGITAL SUPPLY

### 13.4.2.1 Vdd

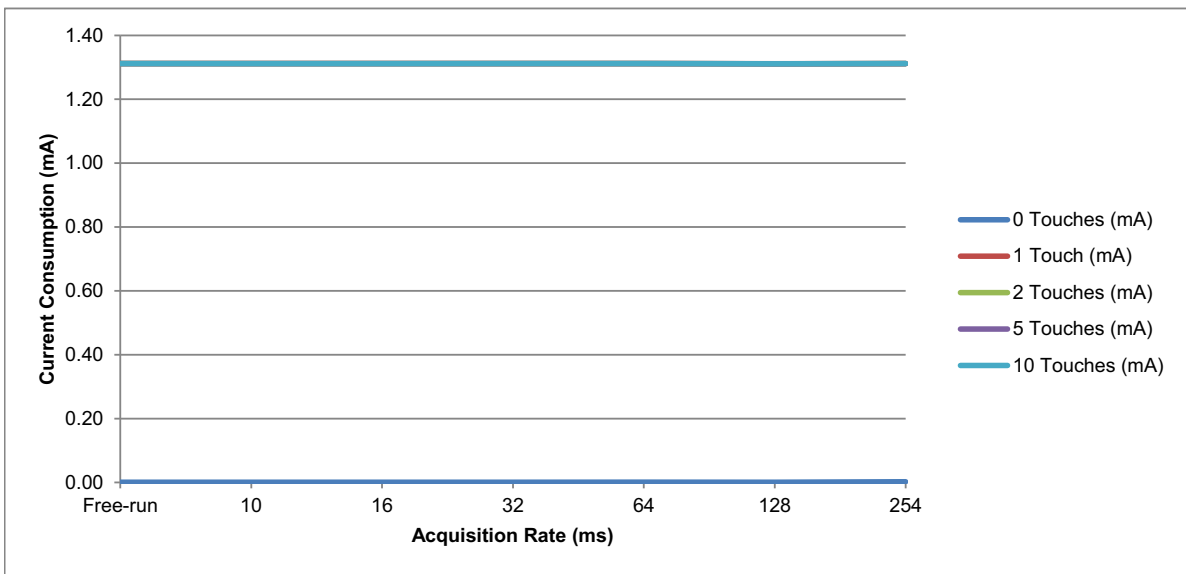
Acquisition Rate (ms)	0 Touches (mA)	1 Touch (mA)	2 Touches (mA)	5 Touches (mA)	10 Touches (mA)
Free-run	11.12	8.34	9.57	9.50	9.47
10	11.25	5.02	9.56	9.49	9.70
16	11.33	3.29	5.98	5.97	5.97
32	6.29	1.88	2.96	2.99	2.96
64	3.17	1.32	1.53	1.60	1.41
128	1.47	0.57	0.59	0.84	0.63
254	0.79	0.38	0.37	0.43	0.39



# MXT641T-AT/MXT641T-AB 1.0

## 13.4.2.2 VddIO

Acquisition Rate (ms)	0 Touches (mA)	1 Touch (mA)	2 Touches (mA)	5 Touches (mA)	10 Touches (mA)
Free-run	0.00	1.31	1.31	1.31	1.31
10	0.00	1.31	1.31	1.31	1.31
16	0.00	1.31	1.31	1.31	1.31
32	0.00	1.31	1.31	1.31	1.31
64	0.00	1.31	1.31	1.31	1.31
128	0.00	1.31	1.31	1.31	1.31
254	0.00	1.31	1.31	1.31	1.31

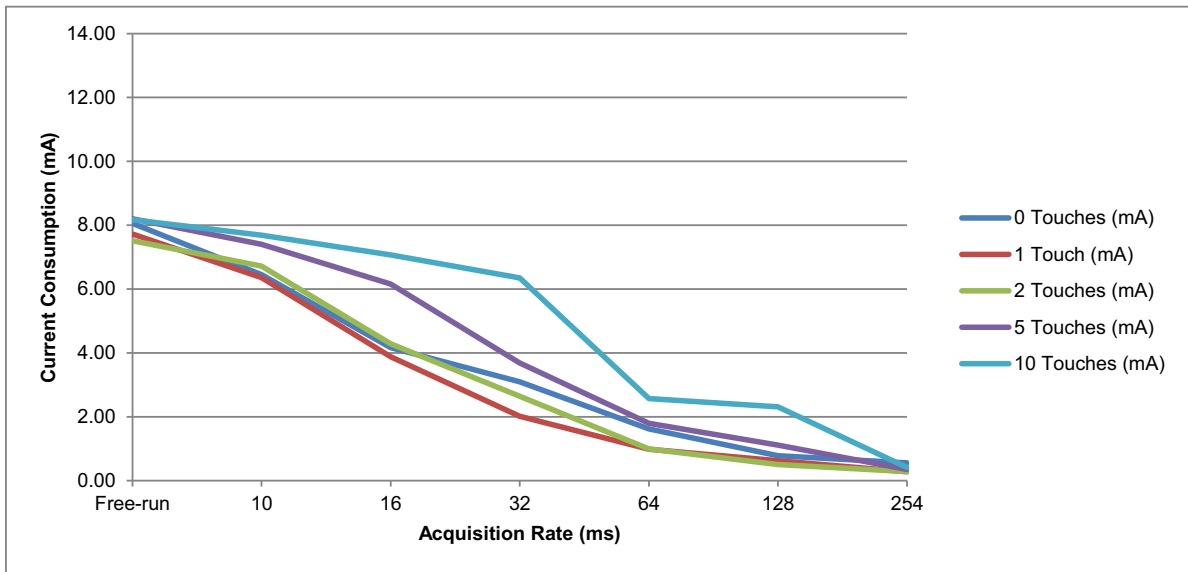


## 13.5 Supply Current – SPI Interface

**NOTE** The characterization charts show typical values based on the configuration in [Table 13-1](#). Actual power consumption in the user's application will depend on the circumstances of that particular project and will vary from that shown here. Further tuning will be required to achieve an optimal performance.

### 13.5.1 ANALOG SUPPLY

Acquisition Rate (ms)	0 Touches (mA)	1 Touch (mA)	2 Touches (mA)	5 Touches (mA)	10 Touches (mA)
Free-run	8.06	7.72	7.51	8.20	8.17
10	6.45	6.36	6.72	7.40	7.69
16	4.16	3.88	4.28	6.16	7.07
32	3.10	2.01	2.65	3.68	6.35
64	1.62	0.98	0.99	1.79	2.57
128	0.78	0.63	0.51	1.11	2.31
254	0.56	0.28	0.28	0.35	0.41

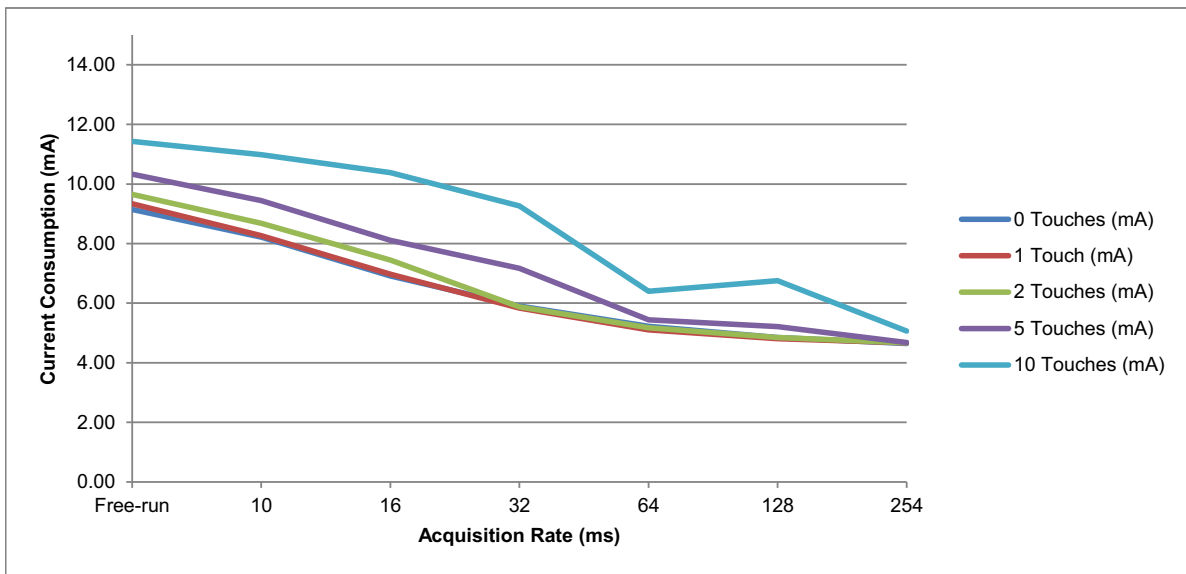


# MXT641T-AT/MXT641T-AB 1.0

## 13.5.2 DIGITAL SUPPLY

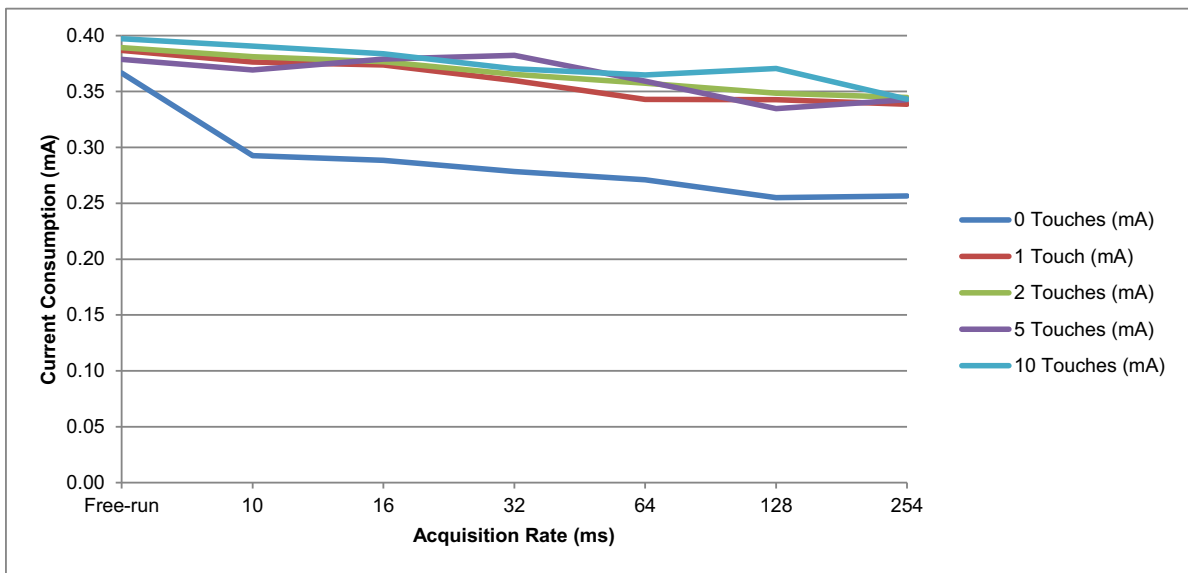
### 13.5.2.1 Vdd

Acquisition Rate (ms)	0 Touches (mA)	1 Touch (mA)	2 Touches (mA)	5 Touches (mA)	10 Touches (mA)
Free-run	9.14	9.34	9.65	10.33	11.43
10	8.22	8.27	8.68	9.45	10.99
16	6.92	6.98	7.44	8.11	10.39
32	5.90	5.84	5.88	7.17	9.27
64	5.22	5.11	5.17	5.44	6.40
128	4.85	4.81	4.85	5.21	6.75
254	4.65	4.67	4.67	4.68	5.06



## 13.5.2.2 VddIO

Acquisition Rate (ms)	0 Touches (mA)	1 Touch (mA)	2 Touches (mA)	5 Touches (mA)	10 Touches (mA)
Free-run	0.37	0.39	0.39	0.38	0.40
10	0.29	0.38	0.38	0.37	0.39
16	0.29	0.37	0.38	0.38	0.38
32	0.28	0.36	0.37	0.38	0.37
64	0.27	0.34	0.36	0.36	0.36
128	0.26	0.34	0.35	0.33	0.37
254	0.26	0.34	0.34	0.34	0.34



## 13.6 Timing Specifications

### 13.6.1 TOUCH LATENCY

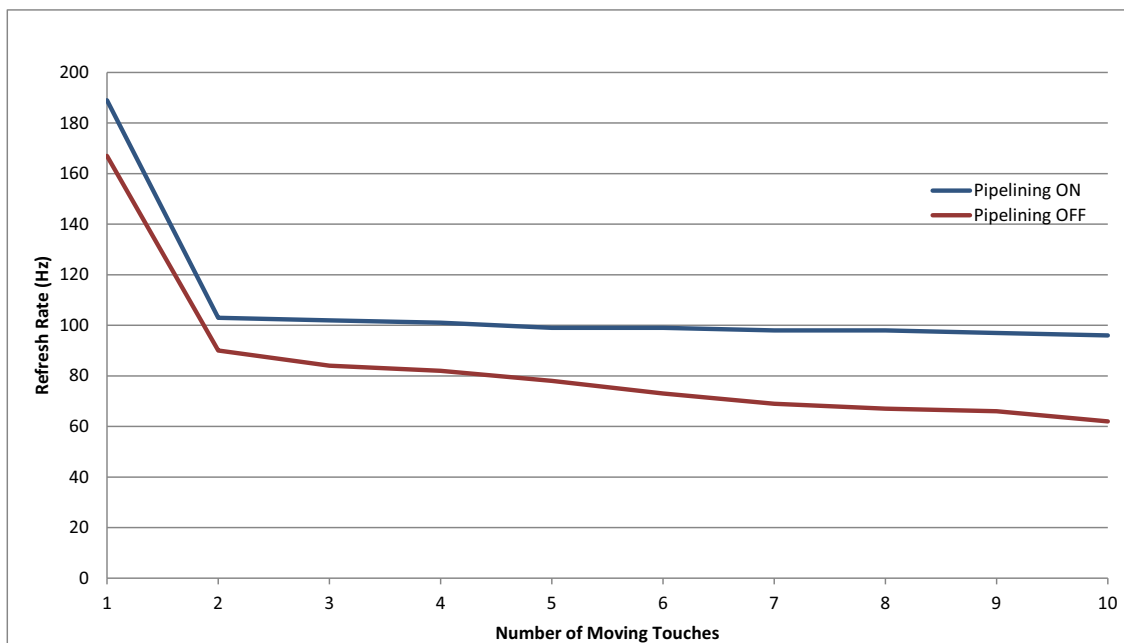
Conditions: XSIZE = 30; YSIZE = 19; CHRGTIME = 60; IDLE/ACTSYNCPERX = 8/10/12; TCHDI = 0, NEXTTCHDI = 0; AMPLHYST = 0; T56 disabled. T = -40°C, 25°C, 85°C, 105°C.

The values were derived using CPK calculations, CPK = 1.66.

Parameter	Min	Typ	Max	Units	Notes
Touch Latency	18.3	26	56.6	ms	Idle/active acquisition interval = 8 ms
	17.8	25.5	56.9	ms	Idle/active acquisition interval = 10 ms
	14.2	27.1	56.9	ms	Idle/active acquisition interval = 12 ms

# MXT641T-AT/MXT641T-AB 1.0

## 13.6.2 SPEED



## 13.6.3 BURST FREQUENCY TOLERANCE

The burst frequency is directly correlated to the system clock. The burst frequency tolerance depends on the tolerance of the system's oscillator (see [Table 13-2](#)).

**TABLE 13-2: OSCILLATOR TOLERANCE – RCOSC32K**

Conditions: T = -40°C, 25°C, 85°C, 105°C

Min Drift	Typ	Max Drift	Notes
-12%	32768 Hz	+7.8%	Minimum/Maximum drift is specified as percentage below/above target frequency

## 13.6.4 RESET TIMINGS

Parameter	Min	Typ	Max	Units	Notes
Power on to CHG line low	80	93	118	ms	Vdd supply for POR VddIO supply for external reset
Hardware reset to $\overline{\text{CHG}}$ line low	80	93	117	ms	
Software reset to CHG line low	93	115	148	ms	

**Note 1:** Any CHG line activity before the power-on or reset period has expired should be ignored by the host. Operation of this signal cannot be guaranteed before the power-on/reset periods have expired.

**2:** If Self Capacitance Global Configuration T109 CMDONRESET (byte 2) = 0 (default), reset timings may be up to 25 ms longer. CMDONRESET should therefore be set to 3 or 5.



## 13.7 Touchscreen Sensor Characteristics

Parameter	Description	
Cm	Mutual capacitance	Typical value is between 0.3 pF and 10 pF on a single node.
Cpx	Mutual capacitance load to X	Microchip recommends a maximum load of 300 pF on each X or Y line. <sup>(1)</sup>
Cpy	Mutual capacitance load to Y	
Cpx	Self capacitance load to X	Microchip recommends a maximum load of 100 pF on each X or Y line. <sup>(1)</sup>
Cpy	Self capacitance load to Y	
$\Delta$ Cpx	Self capacitance imbalance on X	Nominal value is 9.7 pF. Value increases by 1 pF for every 45 pF reduction in Cpx/Cpy (based on 100 pF load)
$\Delta$ Cpy	Self capacitance imbalance on Y	

**Note 1:** Please contact your Microchip representative for advice if you intend to use higher values.

## 13.8 Input/Output Characteristics

Parameter	Description	Min	Typ	Max	Units	Notes
<b>Input (All input pins connected to the VddIO power rail)</b>						
Vil	Low input logic level	-0.3	-	0.3 × VddIO	V	VddIO = 1.8 V to Vdd
Vih	High input logic level	0.7 × VddIO	-	VddIO	V	VddIO = 1.8 V to Vdd
Iil	Input leakage current	-	-	0.5	μA	
$\overline{\text{RESET}}$ pin	Internal pull-up resistor	20	40	60	kΩ	
GPIO pin	Internal pull-up/pull-down resistor					
<b>Output (All output pins connected to the VddIO power rail)</b>						
Vol	Low output voltage	0	-	0.2 × VddIO	V	VddIO = 1.8 V to Vdd Iol = -2 mA
Voh	High output voltage	0.8 × VddIO	-	VddIO	V	VddIO = 1.8 V to Vdd Ioh = 2 mA
GPIO pin	Internal pull-up/pull-down resistor	20	40	60	kΩ	

## 13.9 I<sup>2</sup>C Specification

Parameter	Value
Addresses	0x4A or 0x4B
I <sup>2</sup> C specification <sup>(1)</sup>	Revision 6.0
Maximum bus speed (SCL) <sup>(2)</sup>	3.4 MHz
Standard Mode <sup>(3)</sup>	100 kHz
Fast Mode <sup>(3)</sup>	400 kHz
Fast Mode Plus <sup>(2)</sup>	1 MHz
High Speed Mode <sup>(2)</sup>	3.4 MHz

**Note 1:** More detailed information on I<sup>2</sup>C operation is available from [www.nxp.com/documents/user\\_manual/UM10204.pdf](http://www.nxp.com/documents/user_manual/UM10204.pdf).

**Note 2:** The values of pull-up resistors should be chosen to ensure SCL and SDA rise and fall times meet the I<sup>2</sup>C specification. The value required will depend on the amount of capacitance loading on the lines.

**Note 3:** In systems with heavily laden I<sup>2</sup>C lines, even with minimum pull-up resistor values, bus speed may be limited by capacitive loading to less than the theoretical maximum.

# MXT641T-AT/MXT641T-AB 1.0

## 13.10 SPI Bus Specification

Parameter	Specification
Mode	Mode 3 (CPOL = 1 and CPHA = 1)
Clock idle state	High
Setup on	Leading (falling) edge
Sample on	Trailing (rising) edge
Word size	8-bit
Maximum clock rate	8 MHz

## 13.11 Touch Accuracy and Repeatability

Parameter	Min	Typ	Max	Units	Notes
Linearity (touch only; 5.4 mm electrode pitch)	–	±1	–	mm	8 mm or greater finger
Linearity (touch only; 4.2 mm electrode pitch)	–	±0.5	–	mm	4 mm or greater finger
Accuracy	–	±1	–	mm	
Accuracy at edge	–	±2	–	mm	
Repeatability	–	±0.25	–	%	X axis with 12-bit resolution

## 13.12 Thermal Packaging

### 13.12.1 THERMAL DATA

Parameter	Description	Typ	Unit	Condition	Package
$\theta_{JA}$	Junction to ambient thermal resistance	51.4	°C/W	Still air	100-pin TQFP 14 × 14 × 1 mm
$\theta_{JC}$	Junction to case thermal resistance	9.1	°C/W		100-pin TQFP 14 × 14 × 1 mm

### 13.12.2 JUNCTION TEMPERATURE

The maximum junction temperature allowed on this device is 125°C.

The average junction temperature in °C ( $T_J$ ) for this device can be obtained from the following:

$$T_J = T_A + (P_D \times \theta_{JA})$$

If a cooling device is required, use this equation:

$$T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$$

where:

- $\theta_{JA}$  = package thermal resistance, Junction to ambient (°C/W) (see [Section 13.12.1 “Thermal Data”](#))
- $\theta_{JC}$  = package thermal resistance, Junction to case thermal resistance (°C/W) (see [Section 13.12.1 “Thermal Data”](#))
- $\theta_{HEATSINK}$  = cooling device thermal resistance (°C/W), provided in the cooling device datasheet
- $P_D$  = device power consumption (W)
- $T_A$  is the ambient temperature (°C)

## 13.13 ESD Information

Parameter	Value	Reference standard	Notes
Human Body Model (HBM)	±2000 V	AEC-Q100	
Charge Device Model (CDM)	±500 V	AEC-Q100	Except corner pins
	±750 V	AEC-Q100	Corner pins only

## 13.14 Soldering Profile

Profile Feature	Green Package
Average Ramp-up Rate (217°C to Peak)	3°C/s max
Preheat Temperature 175°C ±25°C	150 – 200°C
Time Maintained Above 217°C	60 – 150 s
Time within 5°C of Actual Peak Temperature	30 s
Peak Temperature Range	260°C
Ramp down Rate	6°C/s max
Time 25°C to Peak Temperature	8 minutes max

## 13.15 Moisture Sensitivity Level (MSL)

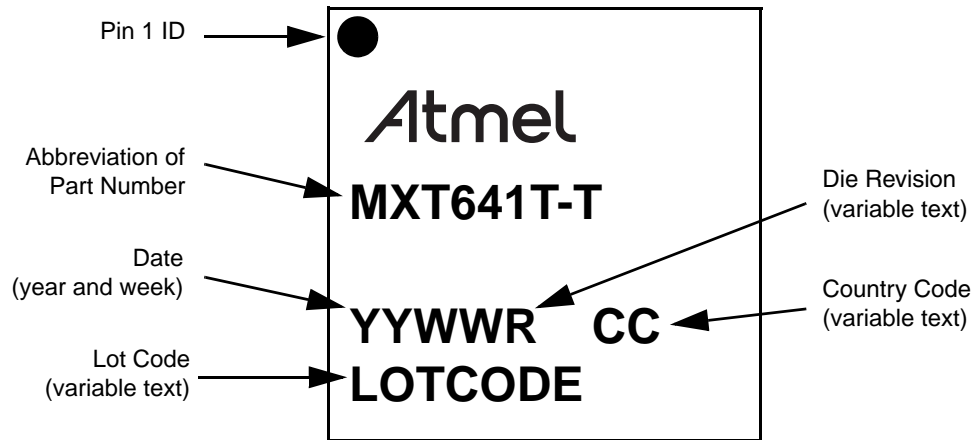
MSL Rating	Package Type(s)	Peak Body Temperature	Specifications
MSL3	QFP	260°C	AEC-Q100

# MXT641T-AT/MXT641T-AB 1.0

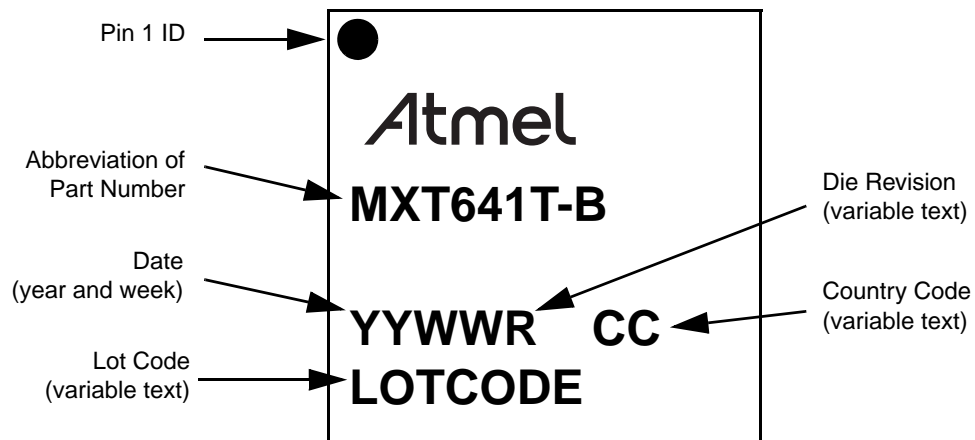
## 14.0 PACKAGING INFORMATION

### 14.1 Package Marking Information

#### 14.1.1 ATMXT641T-AT – 100-PIN TQFP



#### 14.1.2 ATMXT641T-AB – 100-PIN TQFP



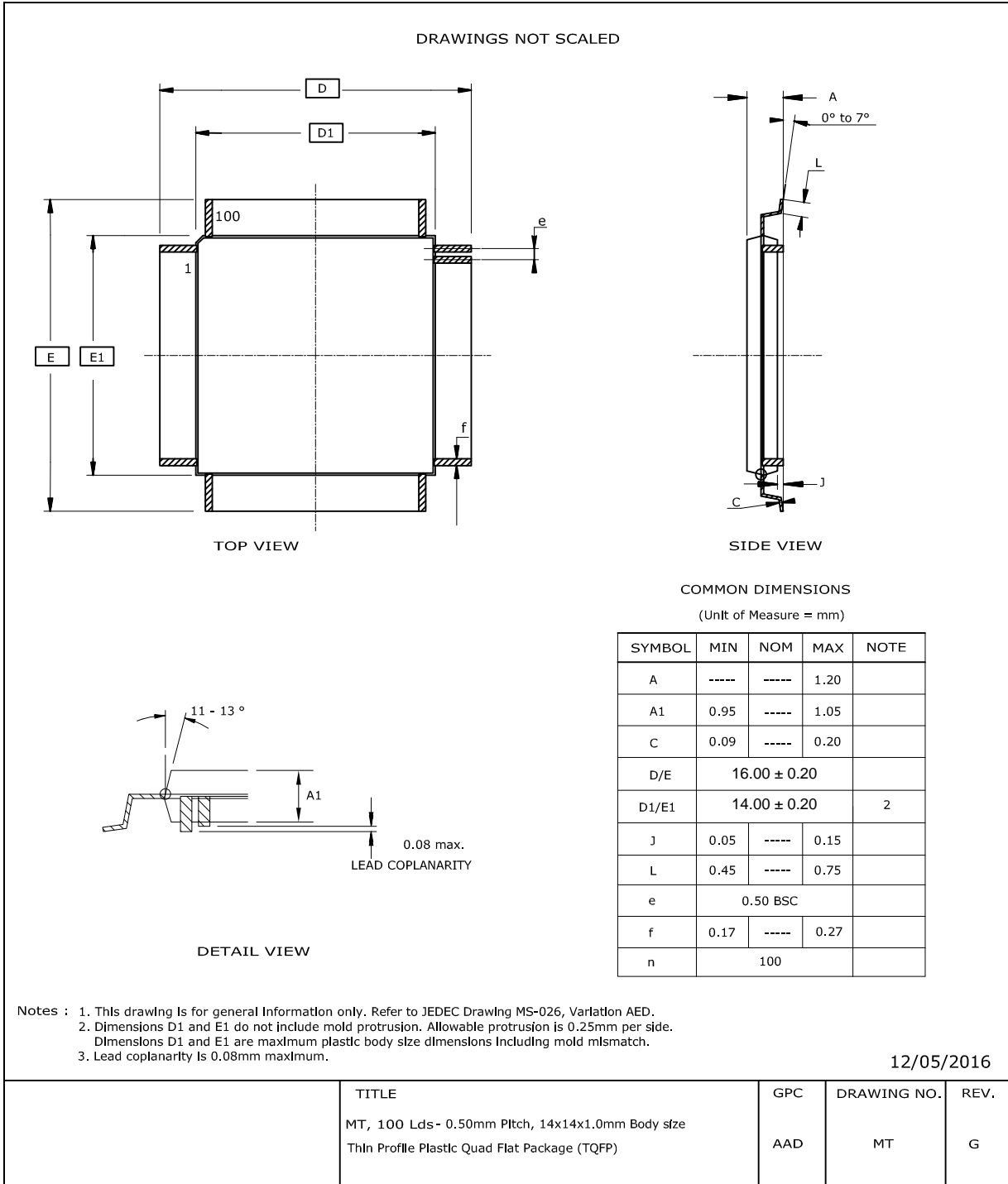
#### 14.1.3 ORDERABLE PART NUMBERS

The product identification system for maXTouch devices is described in "[Product Identification System](#)". That section also lists example part numbers for the mXT641T-AT device.

## 14.2 Package Details

The following section gives the technical details of the package for the device.

### 14.2.1 100-PIN TQFP 14 × 14 × 1 MM



## APPENDIX A: ASSOCIATED DOCUMENTS

<b>NOTE</b> Some of the documents listed below are available under NDA only.
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The following documents are available by contacting your Microchip representative:

### Product Documentation

- Application Note: MXTAN0213 – *Interfacing with maXTouch Touchscreen Controllers*

### Touchscreen design and PCB/FPCB layout guidelines

- Application Note: QTAN0054 – *Getting Started with maXTouch Touchscreen Designs*
- Application Note: MXTAN0208 – *Design Guide for PCB Layouts for maXTouch Touch Controllers*
- Application Note: QTAN0080 – *Touchscreens Sensor Design Guide*

### Configuring the device

- Application Note: QTAN0059 – *Using the maXTouch Self Test Feature*

### Miscellaneous

- Application Note: QTAN0050 – *Using the maXTouch Debug Port*
- Application Note: QTAN0058 – *Rejecting Unintentional Touches with the maXTouch Touchscreen Controllers*
- Application Note: QTAN0061 – *maXTouch Sensitivity Effects for Mobile Devices*

### Tools

- *maXTouch Studio User Guide* (distributed as on-line help with maXTouch Studio)

## APPENDIX B: REVISION HISTORY

### Revision MX (January 2017)

Initial edition for firmware revision 1.0.AA – Atmel Release version

### Revision A (December 2017)

Reformatted edition for firmware revision 1.0.AA – Microchip Release version

This revision incorporates the following updates:

- Updated to Microchip datasheet format:
  - “Pin configuration” moved to start of datasheet
  - “To Our Valued Customers” added
  - Section 14.0 “Packaging Information” updated with new headings. Part numbers moved to “Product Identification System”
  - Associated Documents moved to [Appendix A “Associated Documents”](#)
  - Revision History moved to this appendix
  - Index added
  - “Product Identification System” added
  - “The Microchip Web Site”, “Customer Change Notification Service” and “Customer Support” sections added
  - Front and back covers updated
  - Footnotes incorporated into main text. Cross-reference formats changed.
- Features:
  - Typical touchscreen size updated
  - Automotive Applications section added
  - Touch Sensor Technology section added
  - Panel / cover glass support section replaced by Front Panel Material. Recommended panel thickness for glass revised
  - Advanced Touch Handling section merged into Touch Performance section. Burst Frequency and Scan Speed one finger reporting rate added
  - On-chip Gestures placed in own section
  - Application Interfaces: SPI Debug Interface added
  - Operating Temperature: Updated to show both 85°C and 105°C operating temperatures
  - Design Services section added
  - Other feature points rearranged and reworded slightly
- “Pin configuration”:
  - Table updated to show power rail information. Minor rewording of pin descriptions
- Section 1.0 “Overview of mXT641T-AT/mXT641T-AB”:
  - Touch detection description updated
- Section 2.0 “Schematics”:
  - Schematic drawings modified to show the maximum number of decoupling capacitors required
  - Section 2.3.1 “Power Supply”: New section added
  - Section 2.3.2 “Decoupling capacitors”: Advice on decoupling capacitors modified to recommend maximum number of decoupling capacitors
  - Section 2.3.3 “Pull-up Resistors”: New section added
  - $I^2C$  Interface section removed as unnecessary; information covered elsewhere
  - Section 2.3.10 “SPI Debug Interface”: advice updated with minor rewording. Section heading changed (was *Primary Debug Lines*)
- Section 4.0 “Sensor Layout”:
  - Section 4.1 “Screen Size” added

# MXT641T-AT/MXT641T-AB 1.0

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- [Section 5.0 “Power-up / Reset Requirements”](#):
  - Updated with minor rewording. Recommendation added that design allows host to control power lines. Note concerning device initialization added
  - Checksum information moved to [Section 11.0 “Getting Started with mXT641T-AT/mXT641T-AB”](#)
  - [Section 5.4 “Summary”](#) moved to end
- [Section 6.0 “Detailed Operation”](#):
  - [Section 6.4 “Sensor Acquisition”](#) updated to reflect actual behavior on device
  - [Section 6.7 “Shieldless Support and Display Noise Suppression”](#): Optimal Integration feature added (missing in error)
  - [Section 6.9 “Grip Suppression”](#): Minor rewording of text
  - [Section 6.14 “Adjacent Key Suppression Technology”](#): Text simplified to remove unnecessary information
- [Section 8.0 “I2C Communications”](#):
  - [Section 8.5 “Reading Status Messages with DMA”](#): Footnotes included in main text
- [Section 9.0 “SPI Communications”](#):
  - [Section 9.3 “Write Operation and Responses”](#): Text reworded for clarity
  - [Section 9.6 “Example of a Failed Transaction”](#): Heading changed (was *Example of Failed Protocol*)
- [Section 10.0 “PCB Design Considerations”](#):
  - [Section 10.3.4 “Voltage Pump”](#): Updated to state that EXT CAPn traces should be the same length
  - [Section 10.4 “Voltage Regulators”](#): Additional performance criterion added
  - [Table 10-1](#): Microchip MCP1824S, MAQ5300 and MCP1725 LDOs added
  - I<sup>2</sup>C Line Pull-up Resistor section removed; information duplicated elsewhere
- [Section 11.0 “Getting Started with mXT641T-AT/mXT641T-AB”](#):
  - [Section 11.1.2 “Power-up Sequence”](#): Information and advice corrected. Checksum information added (moved from [Section 5.0 “Power-up / Reset Requirements”](#))
- [Section 13.0 “Specifications”](#):
  - [Section 13.1 “Absolute Maximum Specifications”](#): Maximum junction temperature added
  - [Section 13.2 “Recommended Operating Conditions”](#): Both 85°C and 105°C operating temperatures listed. Cx removed (documented elsewhere)
  - [Section 13.2.1 “DC Characteristics”](#): Tables in sub-sections updated to show rise/fall rates correctly with explanatory notes. Vdd Supply Fall Rate corrected. XVdd Supply Rise Rates removed as not relevant with internal charge pump
  - [Section 13.2.2 “Power Supply Ripple and Noise”](#): Updated to quote single AVdd value
  - [Section 13.4 “Supply Current – I<sup>2</sup>C Interface”](#): Note added to say characterization charts show typical values
  - [Section 13.5 “Supply Current – SPI Interface”](#): Note added to say characterization charts show typical values
  - [Section 13.6.1 “Touch Latency”](#): Range of values updated to reflect both temperature device variants
  - [Section 13.6.4 “Reset Timings”](#): Range of values updated to reflect both temperature device variants
  - [Section 13.7 “Touchscreen Sensor Characteristics”](#) added
  - [Section 13.8 “Input/Output Characteristics”](#): RESET figures now combined with other input pins
  - [Section 13.9 “I2C Specification”](#): Specific resistor values removed
  - [Section 13.13 “ESD Information”](#): Corner and non-corner figures now listed
- [Section 14.0 “Packaging Information”](#):
  - [Section 14.1 “Package Marking Information”](#): Part marking for mXT641T-AB device added
- [Appendix A “Associated Documents”](#):
  - Referenced documents updated
- [“Product Identification System”](#):
  - [“Orderable Part Numbers”](#): mXT641T-AB device added
- mXT641T-AB temperature variant device added and operating temperature information updated throughout
- maXCharger T72 object renamed to Noise Suppression T72
- Self Capacitance maXCharger T108 object renamed to Self Capacitance Noise Suppression T108
- References to restricted documents removed throughout
- References to Atmel Corporation removed or changed to Microchip Technology Inc, where appropriate
- New documentation number assigned



## INDEX

### A

Absolute maximum specifications .....	47
ADDSEL pin .....	23, 24
Adjacent key suppression technology .....	22
AKS. See <i>Adjacent key suppression</i>	
Analog I/O .....	40
Analog voltage supply .....	48
AVdd voltage supply .....	48

### C

Calibration .....	20
Capacitive Touch Engine (CTE) .....	9
Charge time .....	20
Checksum in I <sup>2</sup> C writes .....	24
CHG line .....	12
I <sup>2</sup> C .....	27
mode 0 operation .....	28
mode 1 operation .....	28
SPI .....	30
Clock stretching .....	29
Communications .....	23
communication mode selection .....	23
I <sup>2</sup> C. See <i>I<sup>2</sup>C communications</i>	
SPI. See <i>SPI communications</i>	
Component placement and tracking .....	40
Connection Information see <i>Pinouts</i> .....	3
Customer Change Notification Service .....	68
Customer Notification Service .....	68
Customer Support .....	68

### D

DC characteristics .....	48
Debugging .....	46
object-based protocol .....	46
self test .....	46
SPI Debug Interface .....	13, 46
Decoupling capacitors .....	12, 38
Detailed operation .....	20
Detection integrator .....	20
Device .....	
overview .....	9
Digital filtering .....	21
Digital signals .....	40
Digital voltage supply .....	48
Direct Memory Access .....	25

### E

EMC problems .....	40
ESD information .....	59

### G

Glove detection .....	22
GPIO pins .....	13
Grip suppression .....	21
Ground tracking .....	38

### I

I/O pins .....	12
I <sup>2</sup> C communications .....	24–29
address selection .....	23, 24
ADDSEL pin .....	23, 24
CHG line .....	27
clock stretching .....	29
reading from the device .....	25

reading messages with DMA .....	25
SCL line .....	28
SDA line .....	28
specification .....	57
writes in checksum mode .....	24
writing to the device .....	24
I <sup>2</sup> C interface .....	
SCL line .....	13, 28
SDA line .....	13, 28
Input/Output characteristics .....	57
Internet Address .....	68

### J

Junction temperature .....	58
----------------------------	----

### L

Lens bending .....	21
--------------------	----

### M

Microchip Internet Web Site .....	68
MISO line .....	30
Moisture sensitivity level (msl) .....	59
MOSI line .....	30
Multiple function pins .....	13
Mutual capacitance measurements .....	9

### N

Noise suppression .....	21
display .....	21

### O

Object-based protocol .....	46
Operational modes .....	20
Oscillator tolerance specification .....	56
Overview of the mXT641T-AT .....	9

### P

PCB cleanliness .....	38
PCB design .....	38
analog I/O .....	40
component placement and tracking .....	40
decoupling capacitors .....	38
digital signals .....	40
EMC problems .....	40
ground tracking .....	38
PCB cleanliness .....	38
power supply .....	38
supply rails .....	38
voltage pump .....	38
voltage regulator .....	39
Pinouts .....	3
Power supply .....	
I/O pins .....	12
PCB design .....	38
Power supply ripple and noise .....	48
Power-up/reset .....	17
Initialization .....	19
power-on reset (POR) .....	17
VddIO enabled after Vdd .....	18
Pull-up resistors .....	12
<b>R</b>	
RCOsc32K oscillator olerance specification .....	56
Recommended operating conditions .....	47

# MXT641T-AT/MXT641T-AB 1.0

Repeatability .....	58	$\overline{SS}$ line .....	30
Reset timings .....	56	write operation and responses .....	31
Retransmission compensation .....	21	SPI communications .....	30–37
<b>S</b>		specification .....	58
Schematic .....	10	SPI Debug Interface .....	13, 46
CHG line .....	12	$\overline{SPI\_READ\_OK}$ .....	35
decoupling capacitors .....	12	$\overline{SS}$ line .....	30
GPIO pins .....	13	Stylus support .....	22
I <sup>2</sup> C interface .....	13	Supply rails .....	38
pull-up resistors .....	12	<b>T</b>	
voltage pump .....	12	Test configuration specification .....	49
SCK line .....	30	Thermal data .....	58
SCL line .....	28	Timing specifications .....	55
SCLLine .....	13, 28	Touch accuracy .....	58
Screen size .....	15	Touch detection .....	9, 20
SDA line .....	13, 28	Touchscreen sensor characteristics .....	57
Self capacitance measurements .....	9	Tuning .....	46
Self test .....	46	<b>U</b>	
Sensor acquisition .....	20	Unintentional touch suppression .....	22
Shieldless support .....	21	<b>V</b>	
Soldering profile .....	59	Vdd voltage supply .....	48
Specifications .....	47–59	VddCore supply .....	12
absolute maximum specifications .....	47	VddIO voltage supply .....	48
analog voltage supply .....	48	Voltage pump .....	12, 38
DC characteristics .....	48	Voltage regulator .....	39
digital voltage supply .....	48	multiple supply operation .....	40
ESD information .....	59	single supply operation .....	40
I <sup>2</sup> C specification .....	57	<b>W</b>	
input/output characteristics .....	57	WWW Address .....	68
junction temperature .....	58	<b>X</b>	
moisture sensitivity level (msl) .....	59	XVdd voltage supply .....	48
power supply ripple and noise .....	48		
RCOsc32K oscillator tolerance .....	56		
recommended operating conditions .....	47		
repeatability .....	58		
reset timings .....	56		
soldering profile .....	59		
SPI bus specification .....	58		
test configuration .....	49		
thermal data .....	58		
timing specifications .....	55		
touch accuracy .....	58		
touchscreen sensor characteristics .....	57		
XVdd voltage supply .....	48		
SPI Communications			
SPI protocol opcodes .....	31		
CHG line .....	30		
communications protocol .....	30		
failed protocol .....	37		
general operations .....	36		
MISO line .....	30		
MOSI line .....	30		
operation .....	30		
read operation and responses .....	34		
SCK line .....	30		
SPI mode 3 .....	30		
SPI transaction header .....	31		
SPI_INVALID_CRC .....	37		
SPI_INVALID_REQ .....	36		
SPI_READ_FAIL .....	36		
spi_read_ok .....	35		
SPI_READ_REQ .....	34		
SPI_WRITE_FAIL .....	33		
SPI_WRITE_OK .....	33		
SPI_WRITE_REQ .....	32		

# MXT641T-AT/MXT641T-AB 1.0

## PRODUCT IDENTIFICATION SYSTEM

The table below gives details on the product identification system for maXTouch devices. See [“Orderable Part Numbers”](#) below for example part numbers for the mXT641T-AT/mXT641T-AB.

To order or obtain information, for example on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-XXX	[X]	[XX]	[X]	[XXX]
Device	Package	Temperature Range	Sample Type	Tape and Reel Option	Pattern
Device:	Base device name				
Package:	A	=	QFP (Plastic Quad Flatpack)		
	CCU	=	UFBGA (Ultra Thin Fine-pitch Ball Grid Array)		
	C2U	=	UFBGA (Ultra Thin Fine-pitch Ball Grid Array)		
	NHU	=	UFBGA (Ultra Thin Fine-pitch Ball Grid Array)		
	C4U	=	X1FBGA (Extra Thin Fine-pitch Ball Grid Array)		
	MAU	=	XQFN (Super Thin Quad Flat No Lead Sawn)		
	MA5U	=	XQFN (Super Thin Quad Flat No Lead Sawn)		
	UU	=	WLCSP (Wafer Level Chip Scale Package)		
Temperature Range:	<i>Blank</i>	=	-40°C to +85°C (Grade 3)		
	T	=	-40°C to +85°C (Grade 3)		
	B	=	-40°C to +105°C (Grade 2)		
Sample Type:	<i>Blank</i>	=	Release Sample		
	ES	=	Pre-release (Engineering) Sample		
Tape and Reel Option:	<i>Blank</i>	=	Standard Packaging (Tube or Tray)		
	R	=	Tape and Reel <sup>(1)</sup>		
Pattern:	QTP, SQTP, Code or Special Requirements (Blank Otherwise)				

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. See [“Orderable Part Numbers”](#) below or check with your Microchip Sales Office for package availability with the Tape and Reel option.

## Orderable Part Numbers

Orderable Part Number	Firmware Revision	Description
ATMXT641T-AT (Supplied in trays)	1.0.AA	100-pin TQFP 14 x 14 x 1 mm, RoHS compliant Operating temperature range -40°C to +85°C (Grade 3)
ATMXT641T-ATR (Supplied in tape and reel)		
ATMXT641T-AB (Supplied in trays)	1.0.AA	100-pin TQFP 14 x 14 x 1 mm, RoHS compliant Operating temperature range -40°C to +105°C (Grade 2)
ATMXT641T-ABR (Supplied in tape and reel)		

# MXT641T-AT/MXT641T-AB 1.0

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