BGS110MN20

SP10T Diversity Antenna Switch with MIPI RFFE Interface

Data Sheet

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Power Management & Multimarket

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Revision History

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Page	**Subjects (major changes since last revision)**
01	NDA disclaimer removed

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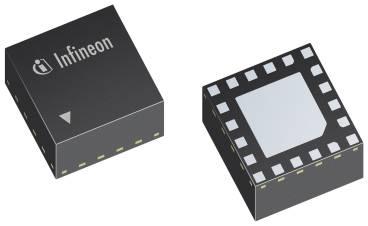
SP10T Diversity Antenna Switch

1 Features



- Suitable for multi-mode WCDMA / LTE diversity applications
- Ultra-low insertion loss and harmonics generation
- 10 high-linearity, interchangeable RX ports
- 0.1 to 2.7 GHz coverage
- High port-to-port-isolation
- Direct to battery supply enabled by large supply voltage range from 2.5 V to 5.5 V
- Integrated MIPI RFFE interface supporting 1.2 and 1.8 V bus voltage
- Software programmable MIPI RFFE USID
- No decoupling capacitors required if no DC applied on RF lines
- Small form factor 2.3 mm x 2.3 mm
- 1 kV HBM ESD protection
- RoHS and WEEE compliant package

RoHS HAL

2 Product Description

The BGS110MN20 is a Single Pole Ten Throw (SP10T) Diversity Switch Module optimized for wireless applications up to 2.7 GHz. It is a perfect solution for multi-mode handsets based on quadband GSM, WCDMA and LTE. The switch module configuration is shown in Fig. 1. The module comes in a miniature TSNP package and comprises of a high power CMOS SP10T switch with integrated MIPI RFFE interface.

No external DC blocking capacitors are required in typical applications as long as no DC is applied to any RF port.

Table 1: Ordering Information

Type	Package	Marking
BGS110MN20	PG-TSNP-20-1	1AM2

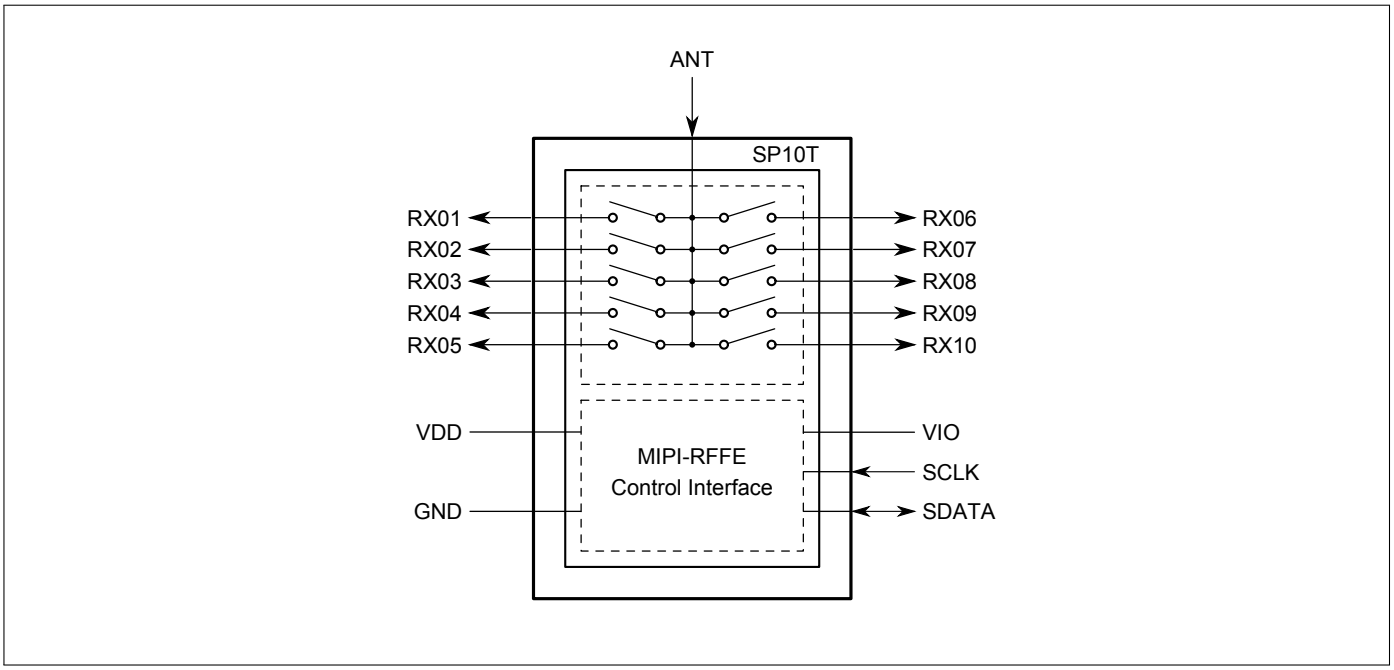


Figure 1: BGS110MN20 block diagram

3 Maximum Ratings

Attention: stresses above the maximum ratings listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings. Exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 2: Maximum Ratings, Table I at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency range[1]	f	0.1	–	–	GHz	
Supply voltage[2]	V_{DD}	-0.5	–	6.0	V	–
Junction temperature[2]	T_j	–	–	125	°C	–
Storage temperature range[3]	T_{STG}	-55	–	150	°C	–
RF input power at all RX ports[2]	P_{RF_RX}	–	–	32	dBm	CW, all ports terminated with 50 Ohm
ESD capability, CDM [3][4]	$V_{ESD_{CDM}}$	−500	–	+500	V	All pins
ESD capability, HBM [3][5]	$V_{ESD_{HBM}}$	−1	–	+1	kV	Digital, digital versus RF
		−1	–	+1	kV	RF
ESD capability, system level[3][6]	$V_{ESD_{ANT}}$	−8	–	+8	kV	ANT versus system GND, with 27 nH shunt inductor

[1] Switch has no highpass response. There is also a DC connection between switched paths. The DC voltage at RF ports V_{RFDC} has to be 0V.
[2] Guaranteed by design.
[3] Guaranteed by characterization.
[4] Field-Induced Charged-Device Model JESD22-C101. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.
[5] Human Body Model ANSI/ESDA/JEDEC JS-001-2012 (R = 1.5 kΩ, C = 100 pF).
[6] IEC 61000-4-2 (R = 330 Ω, C = 150 pF), contact discharge.

Table 3: Maximum Ratings, Table II at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum DC-voltage on RF ports and RF ground[1)]	V_{RFDC}	0	–	0	V	No DC voltages allowed on RF ports
RFFE supply voltage[1)]	V_{IO}	-0.5	–	3.6	V	–
RFFE control voltage levels[1)]	V_{SCLK}, V_{SDATA}	-0.7	–	V_{IO}+0.7	V	–

[1)] Guaranteed by design.

Table 4: Thermal Resistance at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance junction - soldering point[1)]	R_{thJS}	–	54	–	K/W	–

[1)] Guaranteed by design.

4 Operation Ranges

Table 5: Operation Ranges

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ambient temperature	T_A	-30	25	85	°C	–
Supply voltage[1)]	V_{DD}	2.5	3.5	5.5	V	–
Supply current[2)]	I_{DD}	–	80	200	µA	–
Supply current in user low power mode[2)]	I_{LP}	-	0.6	1	µA	–
Supply current in shutdown state[1)]	I_{SD}	-	0.5	1	µA	V_{DD}=0V
RFFE supply voltage[1)]	V_{IO}	1.1	1.8	1.95	V	–
RFFE input high voltage[2)3)]	V_{IH}	0.7*V_{IO}	–	V_{IO}	V	–
RFFE input low voltage[2)3)]	V_{IL}	0	–	0.3*V_{IO}	V	–
RFFE output high voltage[2)3)]	V_{OH}	0.8*V_{IO}	–	V_{IO}	V	–
RFFE output low voltage[2)3)]	V_{OL}	0	–	0.2*V_{IO}	V	–
RFFE control input capacitance[4)]	C_{Ctrl}	–	–	2	pF	–
RFFE supply current[2)]	I_{VIO}	–	15	–	µA	Idle state

[1)] Guaranteed by characterization.
[2)] Guaranteed by test.
[3)] SCLK and SDATA
[4)] Guaranteed by design.

Table 6: RF Input Power

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RX ports (50Ω)[1)]	P_{RF_RX}	–	–	27	dBm	T_A = -30 °C...+85 °C

[1)] Guaranteed by characterization.

5 RF Characteristics

Table 7: RF Characteristics at T_A = −30... + 85°C, P_{IN} = 0 *dBm*, V_{DD} = 2.5...5.5 *V*, Z_0=50Ω, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion Loss[3)]						
RX01-04, RX07-10	IL	–	0.30	0.45	dB	0.1 to 1.0 GHz [1)]
		–	0.40	0.60	dB	1.0 to 2.0 GHz [2)]
		–	0.50	0.80	dB	2.0 to 2.7 GHz [2)]
Insertion Loss[3)]						
RX05, RX06	IL	–	0.30	0.45	dB	0.1 to 1.0 GHz [1)]
		–	0.40	0.65	dB	1.0 to 2.0 GHz [2)]
		–	0.60	0.85	dB	2.0 to 2.7 GHz [2)]
Return Loss[3)]						
RX01-10	RL	18	25	–	dB	0.1 to 1.0 GHz [2)]
		12	20	–	dB	1.0 to 2.0 GHz [1)]
		10	16	–	dB	2.0 to 2.7 GHz [2)]
Isolation (ANT-RX)[3)]						
RX01-10	ISO	28	40	–	dB	0.1 to 1.0 GHz [1)]
		22	35	–	dB	1.0 to 2.0 GHz [2)]
		19	30	–	dB	2.0 to 2.7 GHz [2)]
Intermodulation Distortion (UMTS Band 1, Band 5)[2)3)]						
2nd order intermodulation	IMD2 low	–	-105	-95	dBm	IMT, US Cell (see Tab. 8)
3rd order intermodulation	IMD3	–	-110	-100	dBm	IMT, US Cell (see Tab. 9)
2nd order intermodulation	IMD2 high	–	-110	-100	dBm	IMT, US Cell (see Tab. 8)
Harmonic Generation (UMTS Band 1, Band 5)[2)3)]						
H2	P_{Harm}	80	90	–	dBc	25 dBm, 50Ω, CW mode
H3	P_{Harm}	80	90	–	dBc	25 dBm, 50Ω, CW mode

[1)] Guaranteed by test.
[2)] Guaranteed by characterization.
[3)] On application board with application circuit according to Fig. 8

Table 8: IMD2 Testcases

Band	CW tone 1 (MHz)	CW tone 1 (dBm)	CW tone 2 (MHz)	CW tone 2 (dBm)
IMT	1950	20	190 (IMD2 low)	-15
			4090 (IMD2 high)	
US Cell	835	20	45 (IMD2 low)	-15
			1715 (IMD2 high)	

Table 9: IMD3 Testcases

Band	CW tone 1 (MHz)	CW tone 1 (dBm)	CW tone 2 (MHz)	CW tone 2 (dBm)
IMT	1950	20	1760	-15
US Cell	835	20	790	-15

Table 10: Switching Time at T_A = -30 °C...+85 °C, P_{IN} = 0 *dBm*, Supply Voltage = 2.5 V...5.5 V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switching Time						
MIPI to RF time[1)]	t_{INT}	–	1.5	2	µs	50 % last SCLK falling edge to 90 % ON, see Fig. 2
Power up settling time[1)]	t_{PUP}	–	10	25	µs	After power down mode

[1)] Guaranteed by characterization.

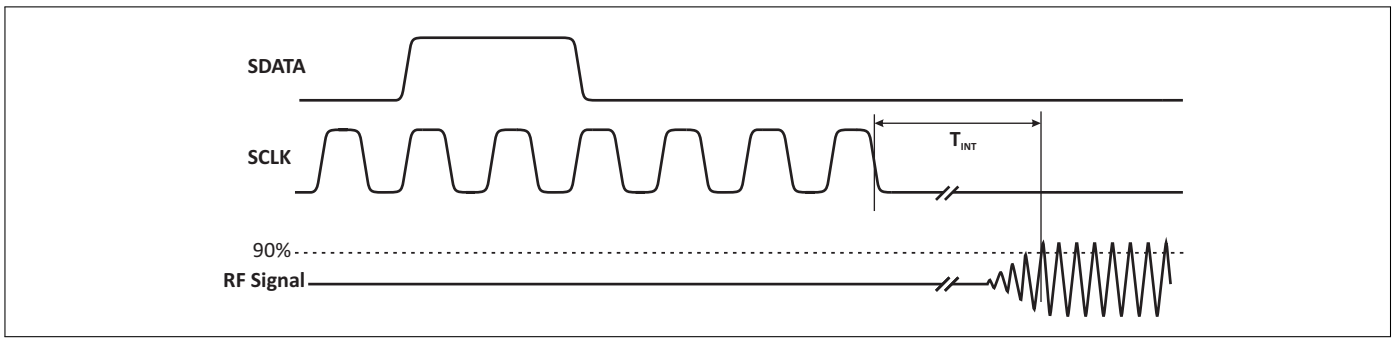


Figure 2: MIPI to RF Time

6 MIPI RFFE Specification

Supported MIPI Functions

The MIPI RFFE interface supports following functions:

- Register write command sequence
- Register read command sequence
- Register 0 write command sequence
- Programmable USID
- Trigger function

All sequences are implemented according to the 'MIPI Alliance Specification for RF Front-End Control Interface' document version 1.10 - 26. July 2011. By default the device goes into low power mode after power on.

Table 11: Register Mapping

Register Address	Register Name	Data Bits	Function	Default	Broadcast Support	Trigger Support	R/W
0x0000	REGISTER_0	7:0	MODE_CTRL	00000000	No	Yes	R/W
0x001C	PM_TRIG	7:6	PWR_MODE	10	Yes	No	R/W
		5	TRIGGER_MASK_2	0	No	No	
		4	TRIGGER_MASK_1	0	No	No	
		3	TRIGGER_MASK_0	0	No	No	
		2	TRIGGER_2	0	Yes	No	
		1	TRIGGER_1	0	Yes	No	
		0	TRIGGER_0	0	Yes	No	
0x001D	PRODUCT_ID	7:0	PRODUCT_ID	10000101	No	No	R
0x001E	MANUFACTURER_ID	7:0	MANUFACTURER_ID [7:0]	00011010	No	No	R
0x001F	MAN_USID	7:6	SPARE	00	No	No	R/W
		5:4	MANUFACTURER_ID [9:8]	01			
		3:0	USID	1010			
0x001B	GROUP_SID	7:4	RESERVED	0	No	No	R/W
		3:0	GROUP_SID	0			

Table 12: MIPI RFFE Operating Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLK Frequency	FSCLK	0.032	–	26	MHz	Full speed[2)]
		0.032	–	13	MHz	Half speed[2)]
SCLK Period	TSCLK	0.038	–	32	µs	Full speed
		0.077	–	32	µs	Half speed
SCLK Low Period	TSCLKIL	11.25	–	–	ns	Full speed, see Fig. 3
		24	–	–	ns	Half speed, see Fig. 3
SCLK High Period	TSCLKIH	11.25	–	–	ns	Full speed, see Fig. 3
		24	–	–	ns	Half speed, see Fig. 3
SDATA Setup Time	TS	1	–	–	ns	Full speed, see Fig. 4
		2	–	–	ns	Half speed, see Fig. 4
SDATA Hold Time	TH	5	–	–	ns	Full speed, see Fig. 4
		5	–	–	ns	Half speed, see Fig. 4
SDATA Release Time	TSDATAZ	–	–	10	ns	Full speed, see Fig. 5
		–	–	18	ns	Half speed, see Fig. 5
Time for Data Output	TD	–	–	10.25	ns	Full speed, see Fig. 6
		–	–	22	ns	Half speed, see Fig. 6
SDATA Rise/Fall Time	TSDATAOTR	2.1	–	6.5	ns	Full speed, see Fig. 6
		2.1	–	10	ns	Half speed, see Fig. 6
VIO Rise Time	TVIO-R	10	–	450	µs	See Fig. 7
VIO Reset Time	TVIO-RST	10	–	–	µs	See Fig. 7
Reset Delay Time	TSIGOL	0.12	–	–	µs	See Fig. 7

[1)] Guaranteed by design unless otherwise specified.
[2)] Guaranteed by characterization.

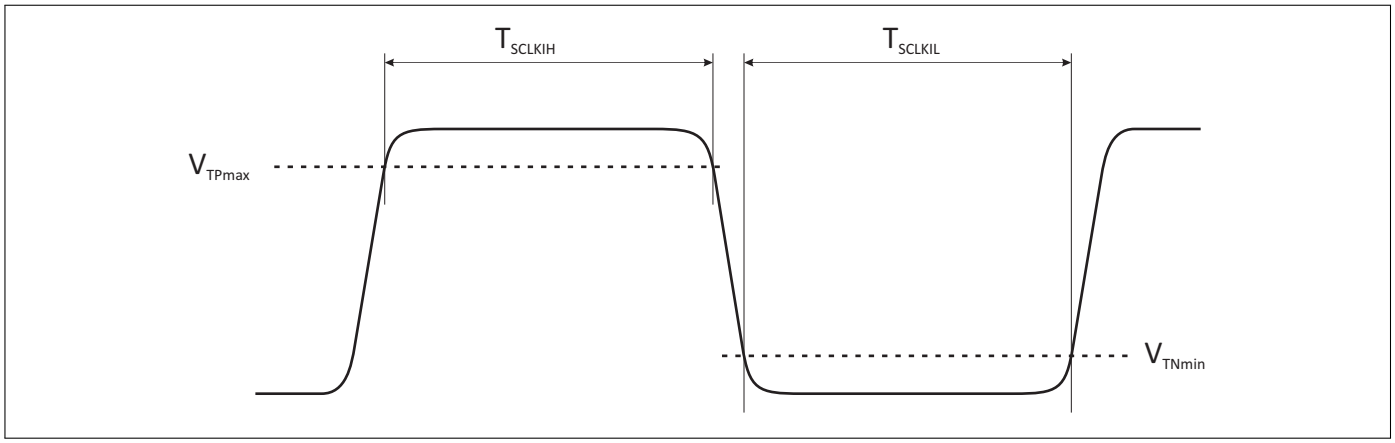


Figure 3: Received clock signal constraints

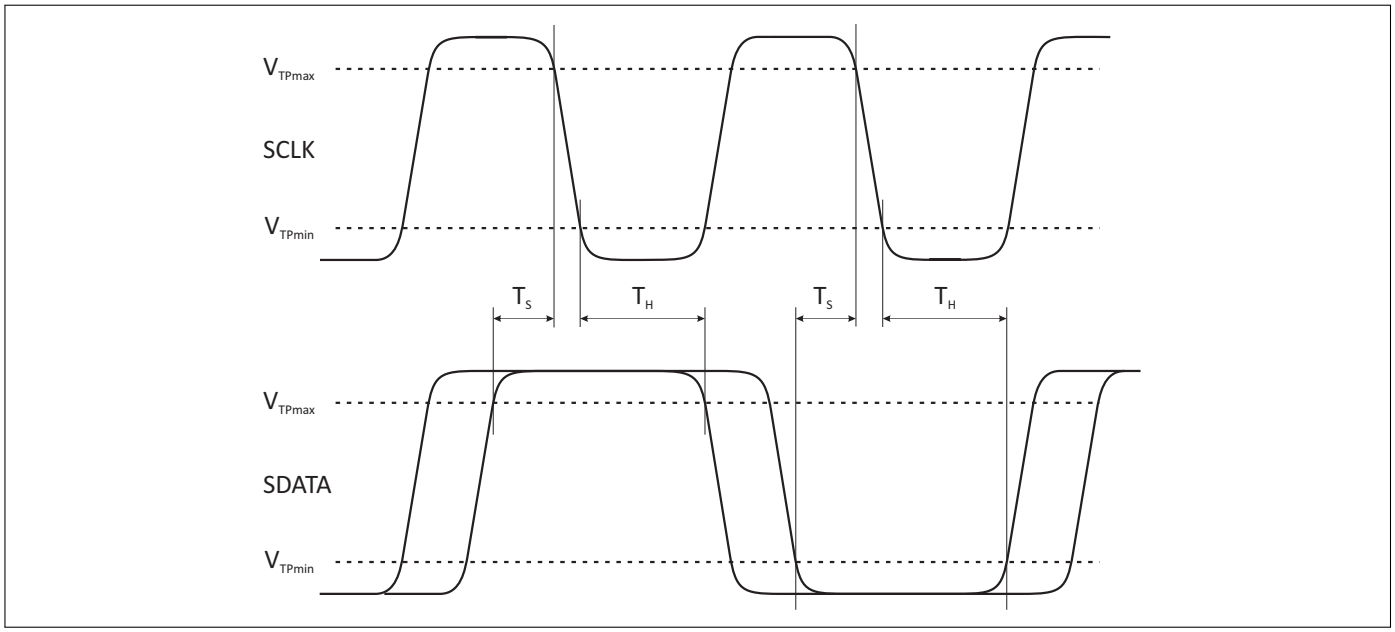


Figure 4: Bus active data receiver timing requirements

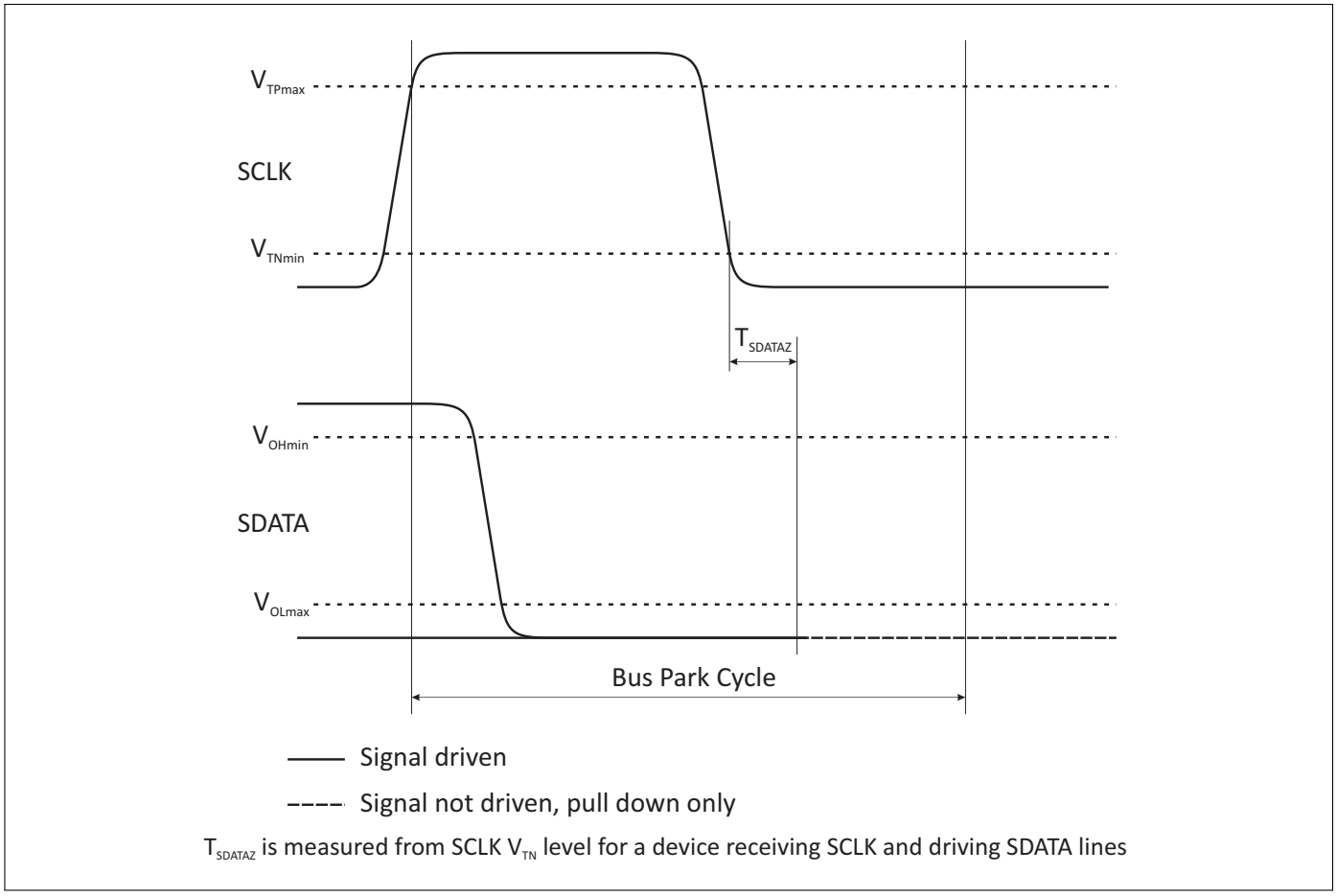


Figure 5: Bus park cycle timing

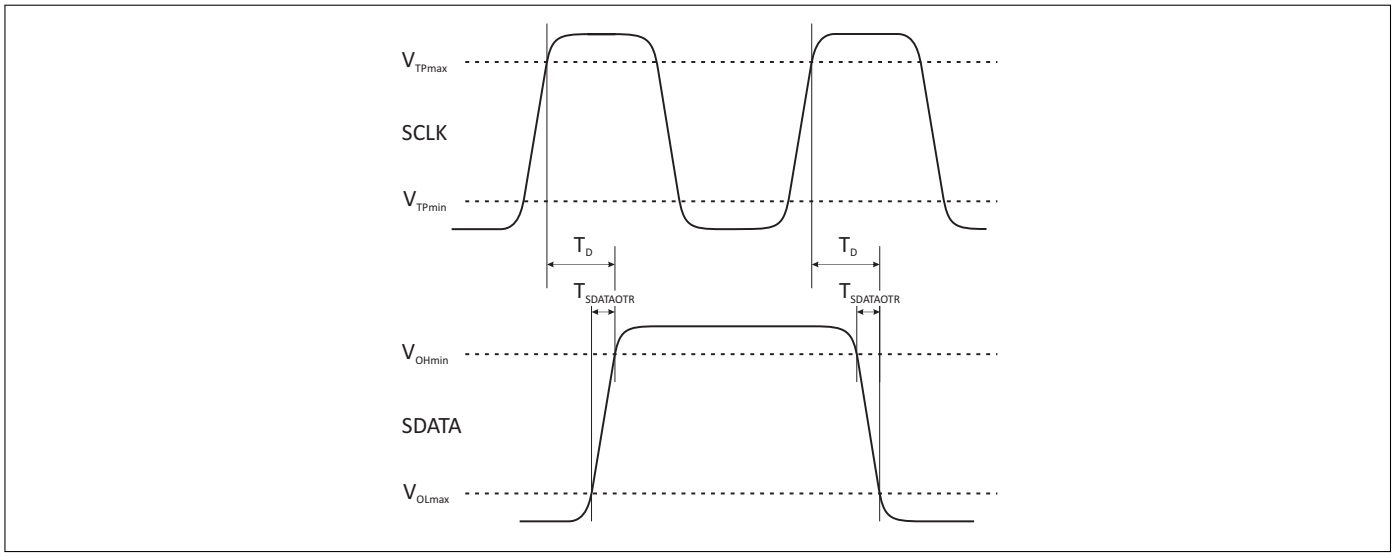


Figure 6: Bus active data transmission timing specification

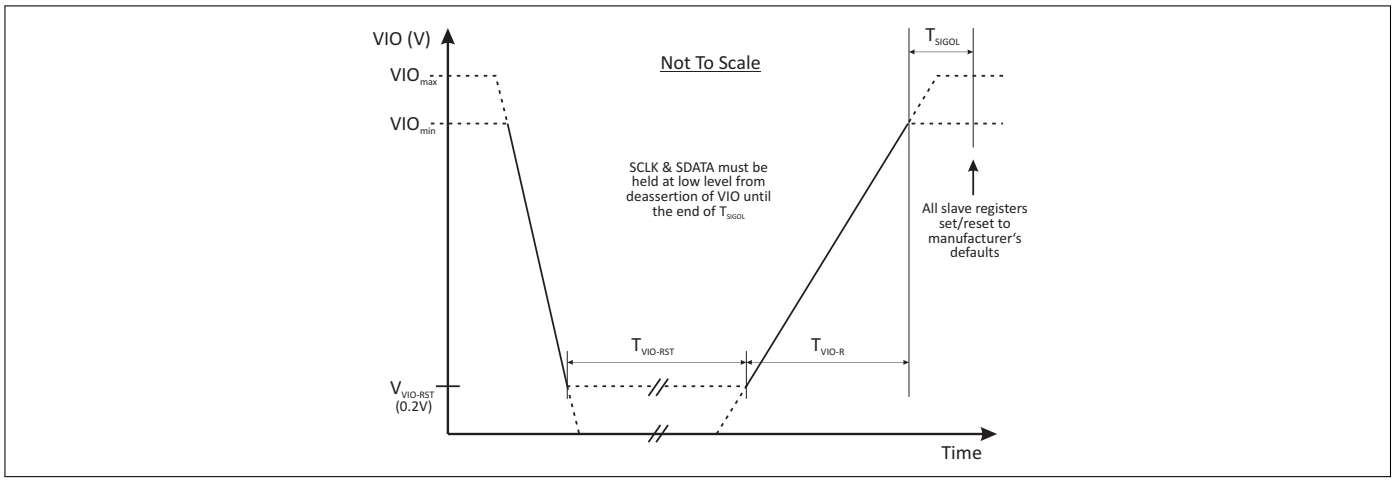


Figure 7: Requirements for VIO-initiated reset

Table 13: Modes of Operation (Truth Table)

		REGISTER_0 Bits							
State	**Mode**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	Isolation	x	0	0	0	0	0	0	0
2	RX01	x	0	0	0	0	0	1	0
3	RX02	x	0	0	0	1	0	1	0
4	RX03	x	0	0	0	1	1	1	0
5	RX04	x	0	0	0	1	0	1	1
6	RX05	x	0	0	0	0	0	0	1
7	RX06	x	0	0	0	1	0	0	1
8	RX07	x	0	0	0	0	1	1	0
9	RX08	x	0	0	0	0	1	0	0
10	RX09	x	0	0	0	1	1	0	0
11	RX10	x	0	0	0	1	0	0	0

7 Pin Definition and Package Outline

Table 14: Pin Configuration

No.	Name	Pin Type	Buffer Type	Function
0	GND	GND		RF ground; die pad
1	NC			Not connected
2	RX10	I/O		RX port 10
3	RX09	I/O		RX port 9
4	RX08	I/O		RX port 8
5	RX07	I/O		RX port 7
6	RX06	I/O		RX port 6
7	GND	GND		RF ground
8	GND	GND		RF ground
9	ANT	I/O		Antenna port
10	GND	GND		RF ground
11	RX05	I/O		RX port 5
12	RX04	I/O		RX port 4
13	RX03	I/O		RX port 3
14	RX02	I/O		RX port 2
15	RX01	I/O		RX port 1
16	GND	GND		RF ground
17	VDD	PWR		V_{DD} supply
18	VIO	PWR		MIPI RFFE supply
19	SDATA	I/O		MIPI RFFE data
20	SCLK	I		MIPI RFFE clock

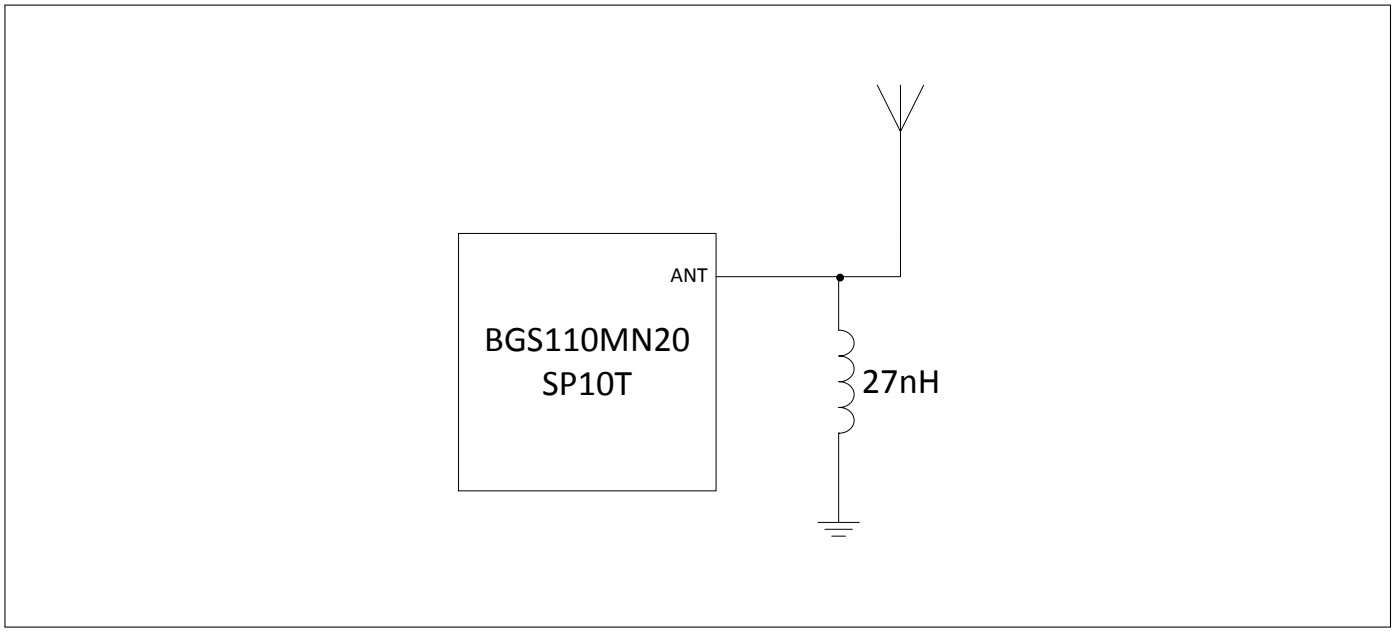


Figure 8: Application circuit

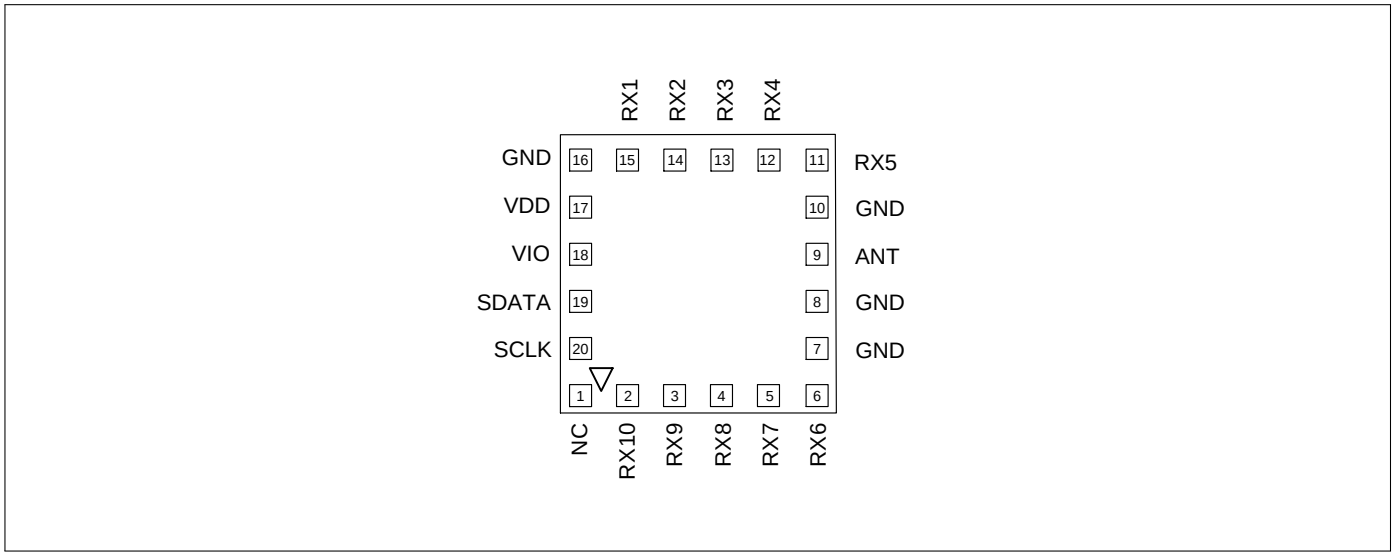


Figure 9: Pin configuration (top view)

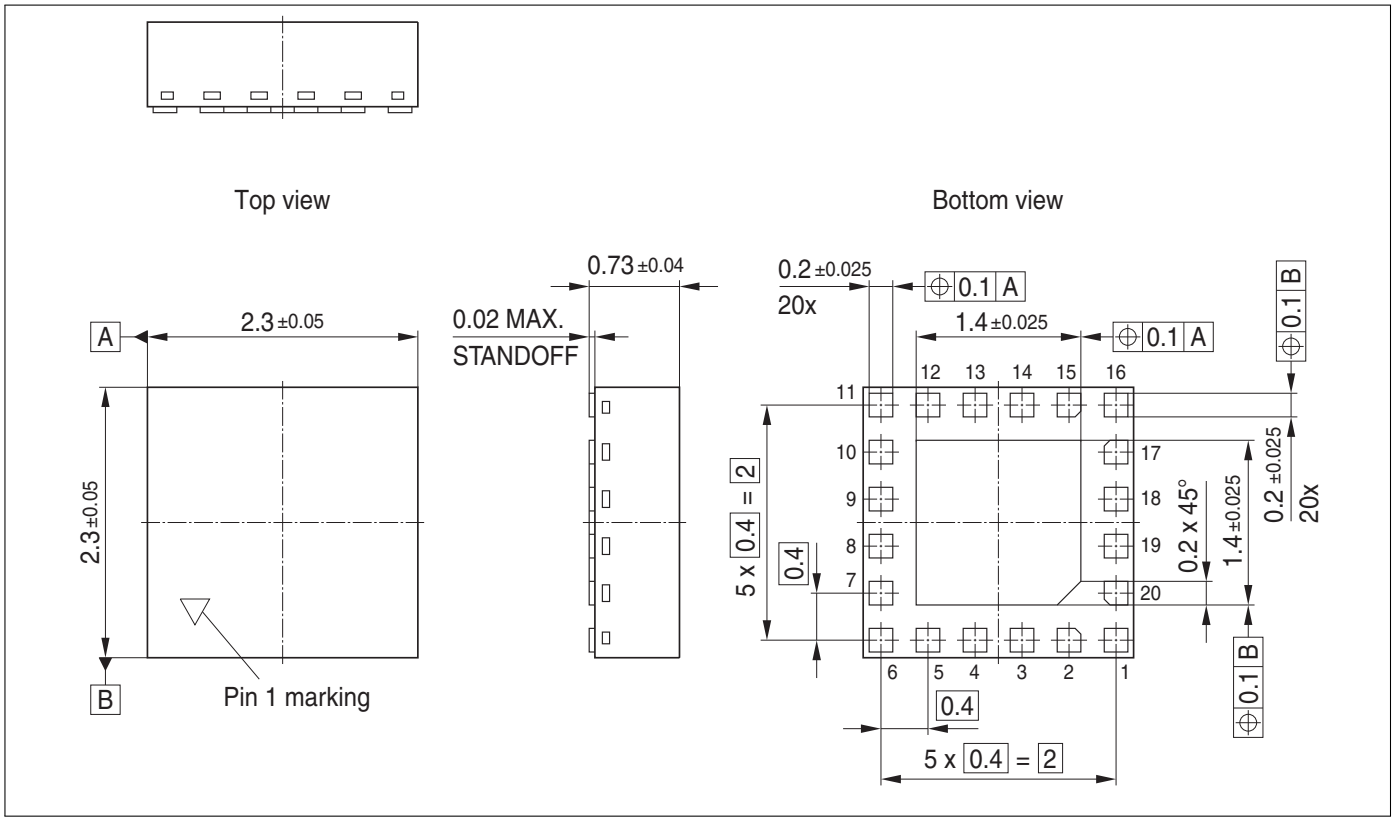


Figure 10: Package outline

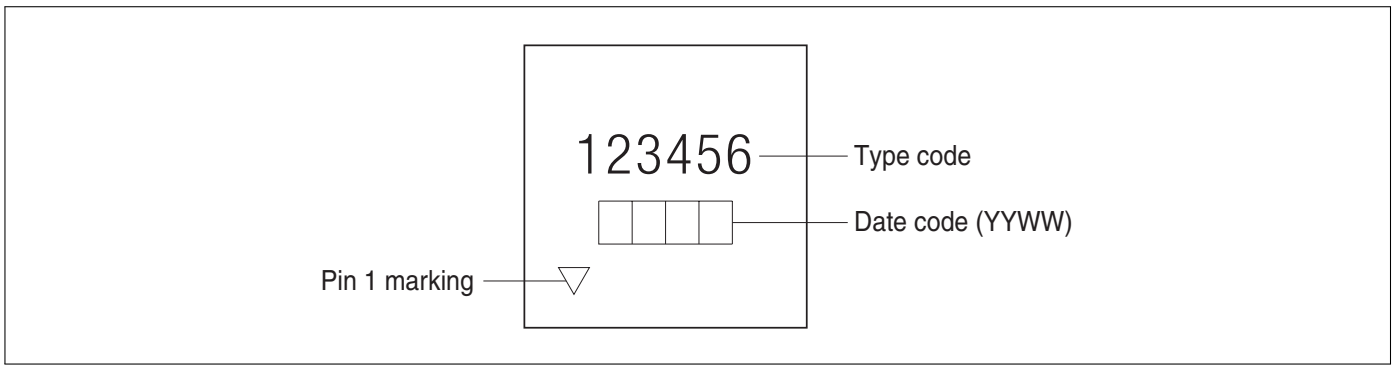


Figure 11: Marking

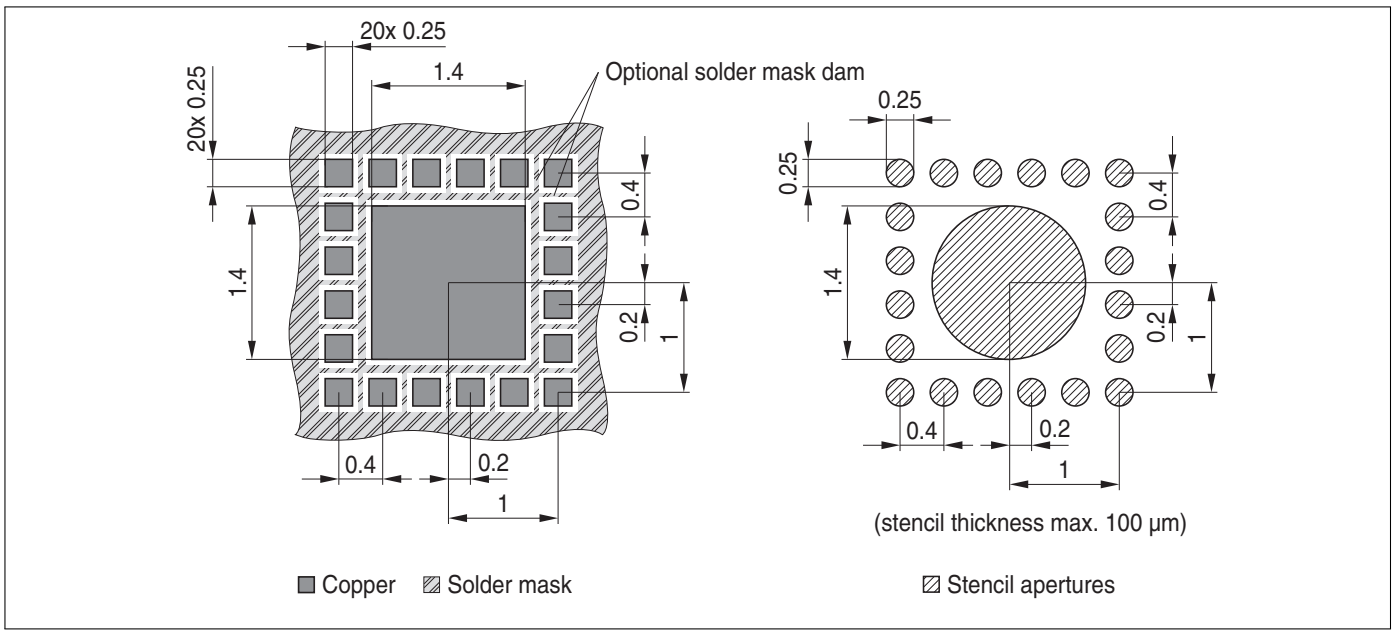


Figure 12: Land pattern and stencil mask

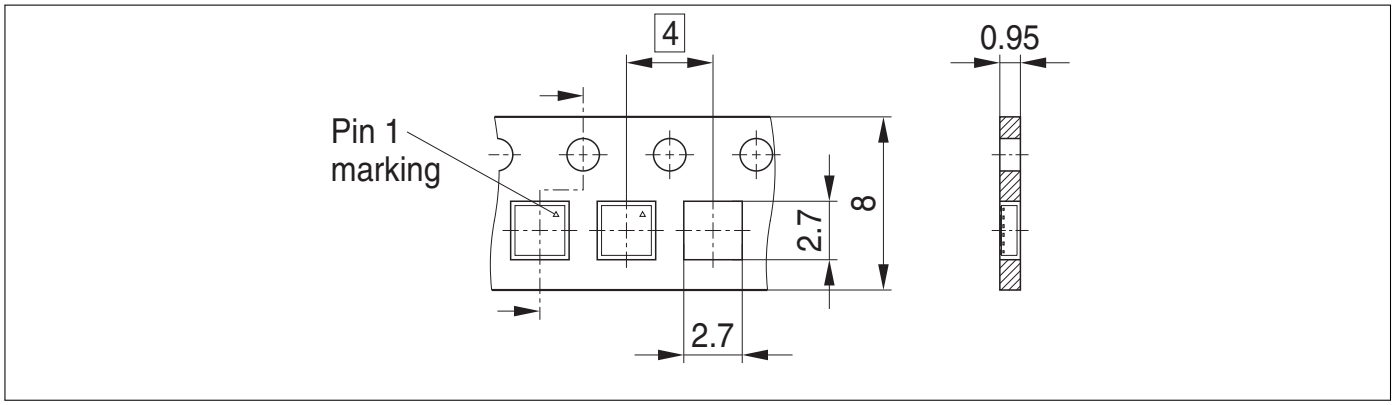


Figure 13: Tape dimensions

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