

Features

■ VOLTAGE OFFSET: ±100uV (MAX)

■ WIDE COMMON MODE VOLTAGE:-0.3V to +36V

■ SUPPLY VOLTAGE: 2.7V to +36V

■ ACCURACY and ZERO-DRIFT PERFORMANCE

♦ ±1% Gain Error (Max over temperature)

♦ 0.5µV/°C Offset Drift (Max)

♦ 10ppm/°C Gain Drift (Max)

■ TWO GAIN OPTIONS for VOLTAGE OUTPUT

◆ TP199A1T: 50V/V

◆ TP199A2T: 100V/V

■ LOW SUPPLY CURRENT: 120uA (TYP)

■ Rail-to-Rail Output

■ PACKAGE: SC70-6

■ Industrial –40°C to 125°C Operation Range

■ ESD Rating: Robust 3KV – HBM, 2KV – CDM

 Higher performance Drop-In Compatible With INA213, INA214, INA199, NCS199 Products

Applications

■ CURRENT SENSING (High-Side/Low-Side)

■ BATTERY CHARGERS

■ POWER MANAGEMENT

CELL PHONE CHARGER

■ ELECTRICAL CIGIRATE

■ WIRELESS CHARGER

■ TELECOM EQUIPMENT

Description

The TP199 series of zero-drift, bi-directional current sense amplifier can sense voltage drops across shunts at common-mode voltages from -0.3V to 36V, independent of the supply voltage. Two fixed gains are available: 50V/V, and 100V/V. The low offset of the zero-drift architecture enables current sensing with maximum drops across the shunt as low as **10mV** full-scale.

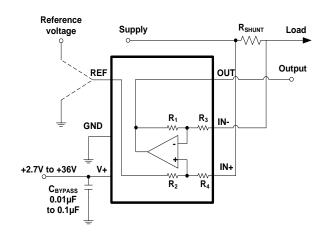
TP199 devices operate from a single +2.7V to 36V power supply, with drawing a typical of 120uA of supply current. All versions are specified from -40°C +125°C, and offered in SC70-6 packages.

GAIN OPTIONS TABLE

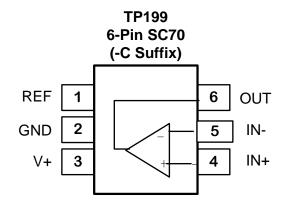
PRODUCT	GAIN	R3 and R4	R1 and R2
TP199A1T	50	20kΩ	1ΜΩ
TP199A2T	100	10kΩ	1ΜΩ

$$V_{OUT} = (I_{LOAD} \times R_{SHUNT})GAIN + V_{REF}$$

Application schematic



Pin Configuration





Order Information

Model Name	Order Number	Gain	Package	Transport Media, Quantity	Package Marking
TP199	TP199A1T-CR	50V/V	6-Pin SC70	Tape and Reel, 3,000	9A1
17199	TP199A2T-CR	100V/V	6-Pin SC70	Tape and Reel, 3,000	9A2

Absolute Maximum Ratings Note 1

Supply Voltage:	42.0V	Current at Supply Pins	±60mA
Input Voltage	GND- 0.3 to 42V	Operating Temperature Range40°	'C to 125°C
Input Current: +IN, -IN Note 3	±5mA	Maximum Junction Temperature	150°C
Output Current: OUT	±35mA	Storage Temperature Range –65°	C to 150°C
		Lead Temperature (Soldering, 10 sec)	260°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The op amp supplies must be established simultaneously, with, or before, the application of any input signals.

Note 3: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500mV beyond the power supply, the input current should be limited to less than 10mA.

Note 4: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
НВМ	Human Body Model ESD	MIL-STD-883H Method 3015.8	±3	kV
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	±2	kV

Thermal Resistance

Package Type	θ_{JA}	θ _{JC}	Unit
6-Pin SC70	227	80	°C/W



Electrical Characteristics

The specifications are at TA = 25°C, VSENSE = VIN+ - VIN-, VS = 5 V, VIN+ = 12V, and VREF = VS / 2, unless otherwise noted

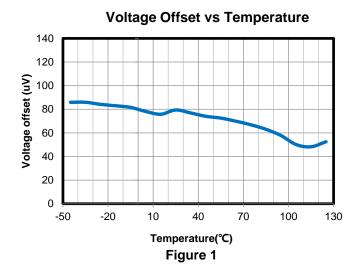
Symbol	Parameter	Conditions	Min	Тур	Max	Unit	
INPUT							
Vos	Input Offset Voltage	VSENSE = 0 mV		±5	±100	uV	
V _{os} TC	Input Offset Voltage Drift	VSENSE = 0 mV, -40°C to 125°C		0.1	0.5	μV/°C	
V _{CM}	Common-mode Input Range	-40°C to 125°C	-0.3		36	V	
CMRR	Common Mode Rejection Ratio	VIN+ = 5~26 V, VSENSE = 0 mV, -40°C to 125°C	95	120		dB	
I _B	Input Bias Current	VSENSE = 0 mV		35		uA	
los	Input Offset Current	VSENSE = 0 mV		0.4		uA	
PSRR	Power Supply Rejection Ratio	Vs = +2.7~18V, VIN+ = +18V, VSENSE = 0 mV		±1		uV/V	
NOISE RTINote	e 5						
e _n	Input Voltage Noise Density	f = 1kHz		30		nV/√Hz	
OUTPUT							
G	Gain	TP199A1T		50		V/V	
G		TP199A2T		100		V/V	
EG	Gain Error	VSENSE = -5~5mV, -40°C to 125°C		±0.1%	±1%		
EG TC	Gain Error Vs Temperature	-40°C to 125°C		3	10	ppm	
C_{LOAD}	Maxim capacitive load	No oscillation		1		nF	
V _{OH}	Output Swing from Supply Rail	R_{LOAD} = 10kΩ to REF, -40°C to 125°C		0.02	0.05	V	
V _{OL}	Output Swing from Supply Rail	R_{LOAD} = 10kΩ to REF, -40°C to 125°C		0.01	0.05	V	
FREQUENCY RESPONSE							
DW	Dan dwidth	CLOAD = 10pF, TP199A1T		48		kHz	
BW	Bandwidth	CLOAD = 10pF, TP199A2T		30		kHz	
SR	Slew Rate			0.6		V/µs	
POWER SUPPLY							
V+	Supply Voltage		2.7		36	V	
ΙQ	Quiescent Current	VSENSE = 0 mV		120	145	μΑ	
TEMPERATURE RANGE							
	Specified range		-40		125	°C	
	Operating range		-55		150	°C	

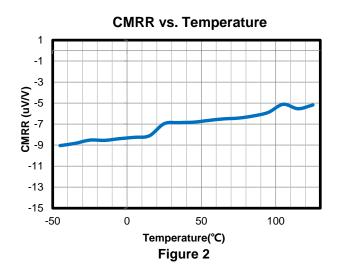
Note 5: RTI = referred to input

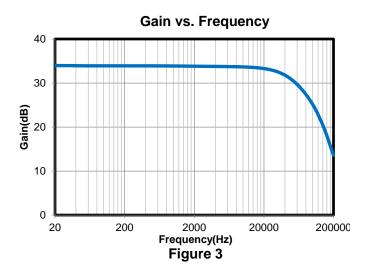


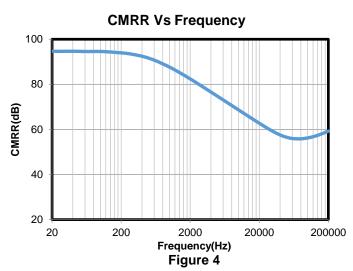
Typical Performance Characteristics

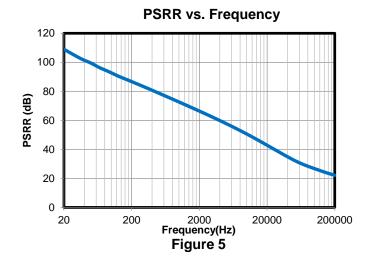
The TP199A1T is used for characteristics at TA = 25°C, VS = 5V, VIN+ =12V, and VREF=VS/2, unless otherwise noted



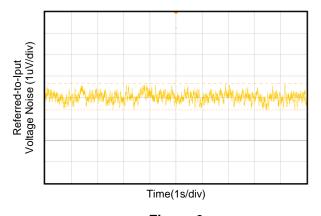








0.1-Hz to 10Hz Voltage Noise (Referred-to-Input)



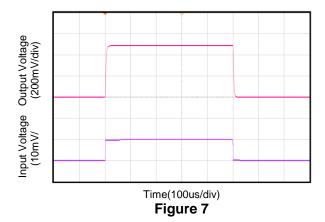
Fiaure 6



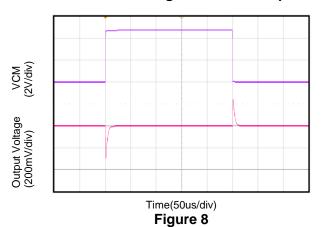
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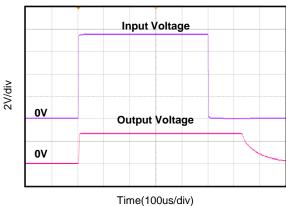
Step response (10-mVpp Input Step)



Common-Mode Voltage Transient Response



Noninverting Differential Input Overload



ime(100us/div Figure 9

Inverting Differential Input Overload

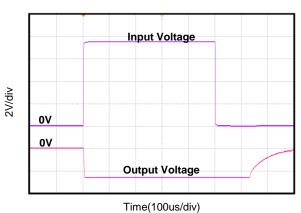


Figure 10

Start-up Response

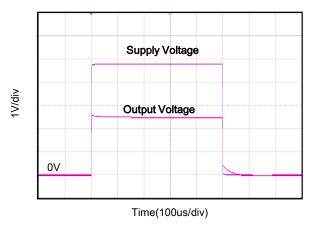


Figure 11

Brownout Recovery

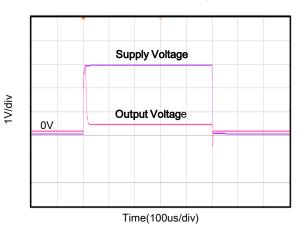
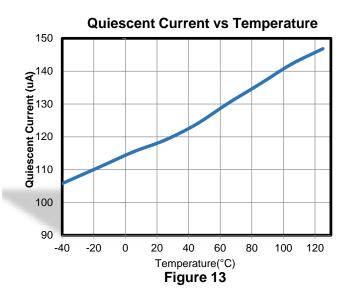


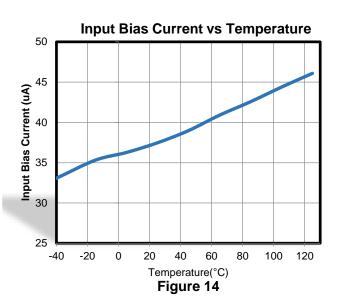
Figure 12

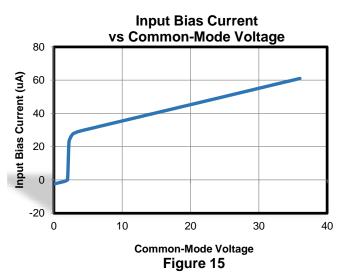


Typical Performance Characteristics

The TP199A1T is used for characteristics at TA = 25°C, VS = 5V, VIN+ =12V, and VREF=VS/2, unless otherwise noted







Pin Functions

IN-: Inverting Input of the Amplifier.

IN+: Non-Inverting Input of Amplifier.

OUT: Amplifier Output. The voltage range extends to within mV

of each supply rail.

REF: Reference voltage

V+: Positive Power Supply. Typically, the voltage is from 2.7V to 36V. A bypass capacitor of 0.1µF as close to the part as possible should be used between power supply pin and ground pin.

GND: Negative Power Supply.

Operation Overview

The TP199 family is 36V, common-mode, zero-drift topology, current-sensing amplifiers that can be used in both low-side and high-side configurations. These specially-designed, current-sensing amplifiers are able to accurately measure voltages developed across current-sensing resistors on common-mode voltages that far exceed the supply voltage powering the device. Current can be

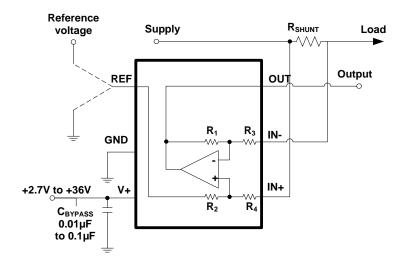


measured on input voltage rails as high as 36 V while the device can be powered from supply voltages as low as 2.7 V.

The zero-drift topology enables high-precision measurements with maximum input offset voltages as low as 60 μ V with a maximum temperature contribution of 0.5 μ V/°C over the full temperature range of –40°C to 125°C.

Applications Information

Application schematic



Above figure shows the basic connections of the TP199. The input pins, IN+ and IN-, should be connected as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistor.

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

Selecting RSHUNT

The zero-drift offset performance of the TP199 offers several benefits. Most often, the primary advantage of the low offset characteristic enables lower full-scale drops across the shunt. For example, nonzero-drift current shunt monitors typically require a full-scale range of 100 mV.

The TP199 family gives equivalent accuracy at a full-scale range on the order of 10 mV. This accuracy reduces shunt dissipation by an order of magnitude with many additional benefits.

Alternatively, there are applications that must measure current over a wide dynamic range that can take advantage of the low offset on the low end of the measurement. Most often, these applications can use the lower gains of the TP199 to accommodate larger shunt drops on the upper end of the scale. For instance, an TP199A1T operating on a 3.3-V supply could easily handle a full-scale shunt drop of 60 mV, with only 100 uV of offset.

REF Input Impedance Effects

As with any difference amplifier, the TP199 family common-mode rejection ratio is affected by any impedance present at the REF input. This concern is not a problem when the REF pin is connected directly to most references or power supplies. When using resistive dividers from the power supply or a reference voltage, the REF pin should be buffered by an op amp.

Power Supply Recommendation

The input circuitry of the TP199 can accurately measure beyond its power-supply voltage, V+. For example, the V+ power



supply can be 5 V, whereas the load power-supply voltage can be as high as 36 V. However, the output voltage range of the OUT pin is limited by the voltages on the power-supply pin. Note also that the TP199 can withstand the full input signal range up to 36 V at the input pins, regardless of whether the device has power applied or not.

Input Capacitance

To ensure better performance about TP199, recommend to add 100nF capacitance between IN+ with GND and it should be close to the IN+ pin in PCB layout.

Proper Board Layout

To ensure optimum performance at the PCB level, care must be taken in the design of the board layout. To avoid leakage currents, the surface of the board should be kept clean and free of moisture. Coating the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board.

Keeping supply traces short and properly bypassing the power supplies minimizes power supply disturbances due to output current variation, such as when driving an ac signal into a heavy load. Bypass capacitors should be connected as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at least 5mm from supply lines to minimize coupling.

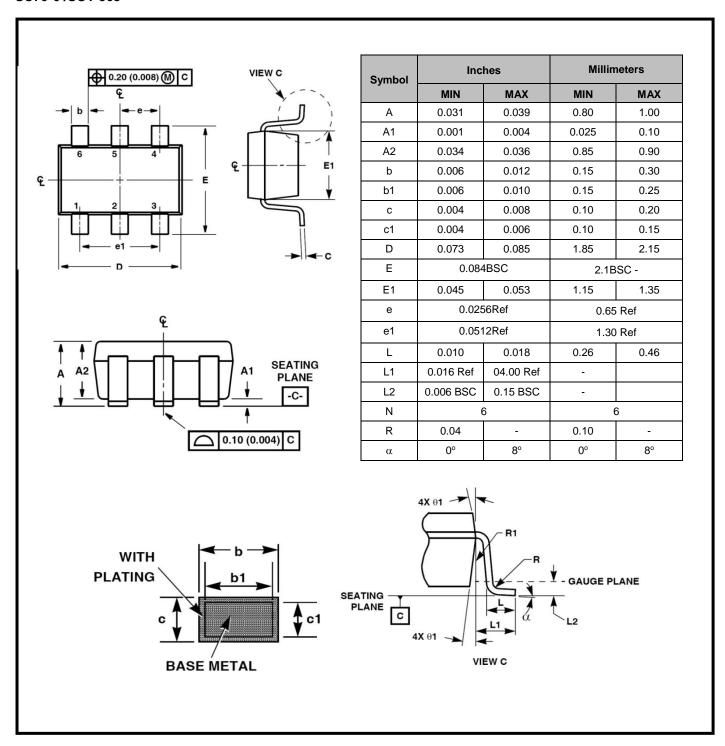
A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so heat sources warm both ends equally. Input signal paths should contain matching numbers and types of components, where possible to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Matching components should be located in close proximity and should be oriented in the same manner. Ensure leads are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

The use of a ground plane is highly recommended. A ground plane reduces EMI noise and also helps to maintain a constant temperature across the circuit board.



Package Outline Dimensions

SC70-6 /SOT-363



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