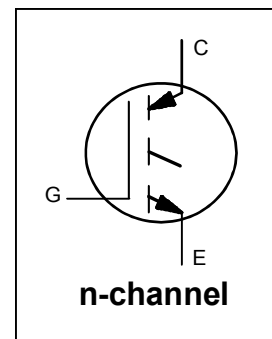


$V_{CES} = 1200V$ $I_{C(Nominal)} = 35A$ $T_{J(max)} = 175^{\circ}C$ $V_{CE(on)} \text{ typ} = 1.9V @ I_C = 35A$
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**Applications**

- Medium Power Drives
- UPS
- HEV Inverter
- Welding
- Induction Heating

<b>G</b>	<b>C</b>	<b>E</b>
Gate	Collector	Emitter

Features	Benefits
Low $V_{CE(ON)}$ and switching Losses	High efficiency in a wide range of applications and switching frequencies
Square RBSOA and Maximum Junction Temperature $175^{\circ}C$	Improved Reliability due to rugged hard switching performance and higher power capability
Positive $V_{CE(ON)}$ Temperature Coefficient	Excellent current sharing in parallel operation

Base part number	Package Type	Standard Pack		Orderable part number
		Form	Quantity	
IRG7CH50K10EF	Die on Film	Wafer	1	IRG7CH50K10EF

**Mechanical Parameter**

Die Size	6.557 x 6.557	mm <sup>2</sup>
Minimum Street Width	75	μm
Emitter Pad Size (Included Gate Pad)	See Die Drawing	mm <sup>2</sup>
Gate Pad Size	1.0053 x 0.7035	
Area Total / Active	43 x 28.02	
Thickness	140	μm
Wafer Size	200	mm
Notch Position	0	Degrees
Maximum-Possible Chips per Wafer	623 pcs.	
Passivation Front side	Silicon Nitride	
Front Metal	Al, Si (4μm)	
Backside Metal	Al (1kA°), Ti (1kA°), Ni (4kA°), Ag (6kA°)	
Die Bond	Electrically conductive epoxy or solder	
Reject Ink Dot Size	0.25 mm diameter minimum	

**Maximum Ratings**

	Parameter	Max.	Units
$V_{CE}$	Collector-Emitter Voltage, $T_J=25^\circ\text{C}$	1200	V
$I_C$	DC Collector Current	①	A
$I_{LM}$	Clamped Inductive Load Current ④	140	A
$V_{GE}$	Gate Emitter Voltage	$\pm 30$	V
$T_J, T_{STG}$	Operating Junction and Storage Temperature	-40 to +175	$^\circ\text{C}$

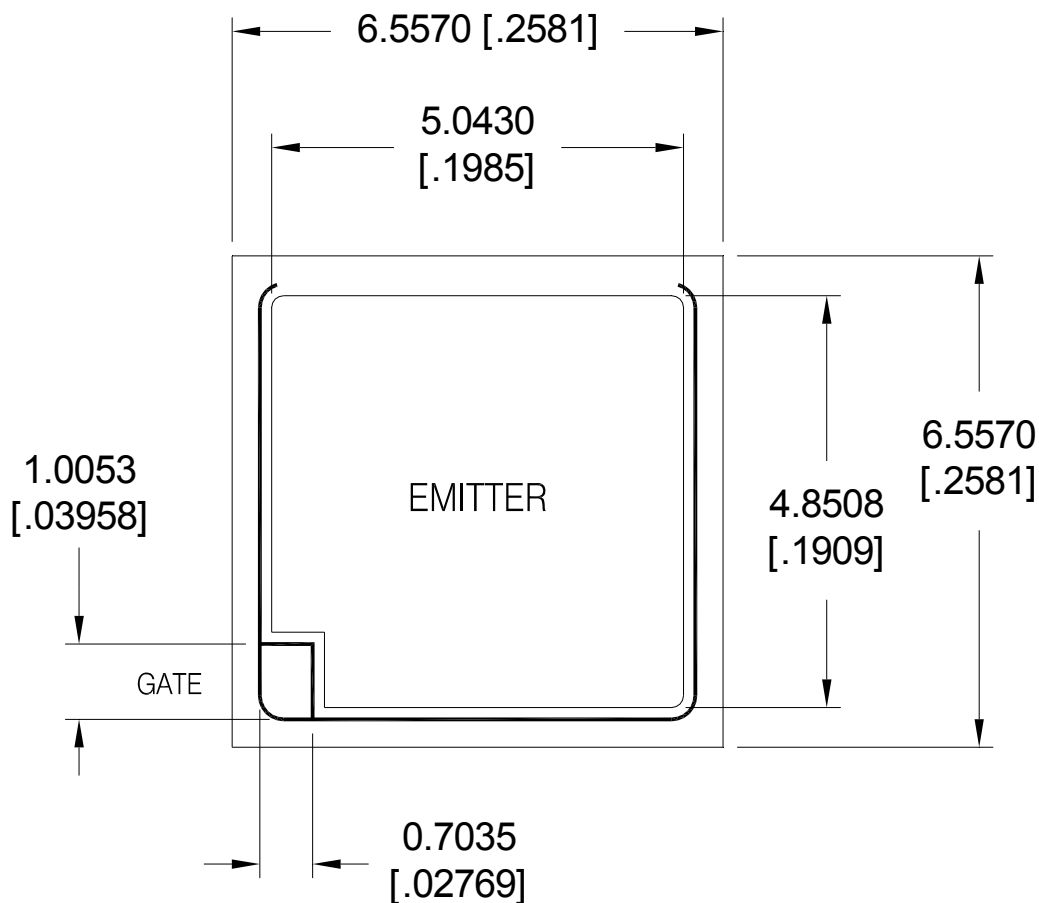
**Static Characteristics (Tested on wafers) .  $T_J=25^\circ\text{C}$** 

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	$V_{GE} = 0\text{V}, I_C = 250\mu\text{A}$ ⑤
$V_{CE(sat)}$	Collector-to-Emitter Saturated Voltage	—	1.95	2.2	V	$V_{GE} = 15\text{V}, I_C = 25\text{A}, T_J = 25^\circ\text{C}$
$V_{GE(th)}$	Gate-Emitter Threshold Voltage	5.0	—	7.5		$I_C = 1.7\text{mA}, V_{GE} = V_{CE}$
$I_{CES}$	Zero Gate Voltage Collector Current	—	1.0	25		$V_{CE} = 1200\text{V}, V_{GE} = 0\text{V}$
$I_{GES}$	Gate Emitter Leakage Current	—	—	$\pm 100$	nA	$V_{CE} = 0\text{V}, V_{GE} = \pm 30\text{V}$

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{CE(sat)}$	Collector-to-Emitter Saturated Voltage	—	1.9	2.3	V	$V_{GE} = 15\text{V}, I_C = 35\text{A}, T_J = 25^\circ\text{C}$
		—	2.5	—		$V_{GE} = 15\text{V}, I_C = 35\text{A}, T_J = 175^\circ\text{C}$
SCSOA	Short Circuit Safe Operating Area	10	—	—	$\mu\text{s}$	$V_{GE}=15\text{V}, V_{CC}=600\text{V},$ ② $R_G=10\Omega, V_P \leq 1200\text{V}, T_J=150^\circ\text{C}$
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				$T_J = 175^\circ\text{C}, I_C = 140\text{A}$ $V_{CC} = 960\text{V}, V_P \leq 1200\text{V}$ $R_g = 10\Omega, V_{GE} = +20\text{V to } 0\text{V}$
$C_{iss}$	Input Capacitance	—	4120	—	pF	$V_{GE} = 0\text{V}$
$C_{oss}$	Output Capacitance	—	160	—		$V_{CE} = 30\text{V}$
$C_{rss}$	Reverse Transfer Capacitance	—	100	—		$f = 1.0\text{MHz}$
$Q_g$	Total Gate Charge (turn-on)	—	170	—	nC	$I_C = 35\text{A}$ ⑥
$Q_{ge}$	Gate-to-Emitter Charge (turn-on)	—	40	—		$V_{GE} = 15\text{V}$
$Q_{gc}$	Gate-to-Collector Charge (turn-on)	—	80	—		$V_{CC} = 600\text{V}$

	Parameter	Min.	Typ.	Max.	Units	Conditions ③
$t_{d(on)}$	Turn-On delay time	—	50	—	ns	$I_C = 35\text{A}, V_{CC} = 600\text{V}$ $R_G = 10\Omega, V_{GE}=15\text{V}, L=200\mu\text{H}$ $T_J = 25^\circ\text{C}$
$t_r$	Rise time	—	80	—		
$t_{d(off)}$	Turn-Off delay time	—	280	—		
$t_f$	Fall time	—	30	—		$I_C = 35\text{A}, V_{CC} = 600\text{V}$ $R_G = 10\Omega, V_{GE}=15\text{V}, L= 200\mu\text{H}$ $T_J = 175^\circ\text{C}$
$t_{d(on)}$	Turn-On delay time	—	50	—		
$t_r$	Rise time	—	70	—		
$t_{d(off)}$	Turn-Off delay time	—	340	—		
$t_f$	Fall time	—	295	—		

# Die Drawing



### NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: INCHES
3. DIE WIDTH AND LENGTH TOLERANCE: -0.0508 [.002]
4. DIE THICKNESS = 0.140 [.0055]

REFERENCE: IRG7CH50K10B

### Notes:

- ① The current in the application is limited by  $T_{JMax}$  and the thermal properties of the assembly.
- ② Not subject to production test- Verified by design / characterization.
- ③ Values influenced by parasitic L and C in measurement.
- ④  $V_{CC} = 80\% (V_{CES})$ ,  $V_{GE} = 20V$ ,  $L = 25\mu H$ ,  $R_G = 10\Omega$ .
- ⑤ Refer to AN-1086 for guidelines for measuring  $V_{(BR)CES}$  safely
- ⑥ Die Level Characterization.

### Additional Testing and Screening

For Customers requiring product supplied as Known Good Die (KGD) or requiring specific die level testing, please contact your local IR Sales.

### Shipping

Sawn Wafer on Film. Please contact your local IR sales office for non– standard shipping options

### Handling

- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Product must be handled only in a class 10,000 or better-designated clean room environment.
- Singulated die are not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected tip should be used.

### Wafer/Die Storage

- Proper storage conditions are necessary to prevent product contamination and/or degradation after shipment.
- Note: To reduce the risk of contamination or degradation, it is recommended that product not being used in the assembly process be returned to their original containers and resealed with a vacuum seal process.
- Sawn wafers on a film frame are intended for immediate use and have a limited shelf life.

### Further Information

For further information please contact your local IR Sales office or email your enquiry to <http://die.irf.com>

Data and specifications subject to change without notice.  
This product has been designed and qualified for Industrial market.  
Qualification Standards can be found on IR's Web site.

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**IOR** Rectifier

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Visit us at [www.irf.com](http://www.irf.com) for sales contact information.

单击下面可查看定价，库存，交付和生命周期等信息

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