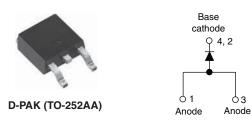
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Schottky Rectifier, 5.5 A



PRODUCT SUMMARY			
Package	D-PAK (TO-252AA)		
I _{F(AV)}	5.5 A		
V _R	100 V		
V_F at I_F	See Electrical table		
I _{RM}	4 mA at 125 °C		
T _J max.	150 °C		
Diode variation	Single die		
E _{AS}	6 mJ		

FEATURES

- Popular D-PAK outline
- Small foot print, surface mountable
- Low forward voltage drop
- High frequency operation
- Guard ring for enhanced ruggedness and long term reliability
- Meets MSL level 1, per J-STD-020, LF maximum peak of 260 °C
- Material categorization: For definitions of compliance please see <u>www.vishay.com/doc?99912</u>

DESCRIPTION

The VS-50WQ10FNPbF surface mount Schottky rectifier has been designed for applications requiring low forward drop and small foot prints on PC board. Typical applications are in disk drives, switching power supplies, converters, freewheeling diodes, battery charging, and reverse battery protection.

MAJOR RATINGS AND CHARACTERISTICS					
SYMBOL	CHARACTERISTICS	VALUES	UNITS		
I _{F(AV)}	Rectangular waveform	5.5	А		
V _{RRM}		100	V		
I _{FSM}	t _p = 5 μs sine	330	А		
V _F	5 A _{pk} , T _J = 125 °C	0.63	V		
TJ	Range	- 40 to 150	°C		

VOLTAGE RATINGS				
PARAMETER	SYMBOL	VS-50WQ10FNPbF	UNITS	
Maximum DC reverse voltage	V _R	100	V	
Maximum working peak reverse voltage	V _{RWM}	100	v	

ABSOLUTE MAXIMUM RATINGS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average forward current See fig. 5	I _{F(AV)}	50 % duty cycle at T_C = 135 °C, rectangular waveform		5.5	
Maximum peak one cycle non-repetitive surge current I _{FSM} See fig. 7	5 µs sine or 3 µs rect. pulse	Following any rated load condition and with rated V _{RRM} applied	330	A	
	10 ms sine or 6 ms rect. pulse		110		
Non-repetitive avalanche energy	E _{AS}	T _J = 25 °C, I _{AS} = 0.5 A, L = 40 mH		6.0	mJ
Repetitive avalanche current	I _{AR}	Current decaying linearly to zero in 1 μ s Frequency limited by T _J maximum V _A = 1.5 x V _R typical 0.5		0.5	А

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COMPLIANT



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ELECTRICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS VAL		VALUES	UNITS
Maximum forward voltage drop See fig. 1	V _{FM} ⁽¹⁾	5 A	T _J = 25 °C	0.77	
		10 A		0.91	V
		5 A	T _J = 125 °C	0.63	
		10 A		0.74	
Maximum reverse leakage current	um reverse leakage current	T _J = 25 °C	$V_{B} = Rated V_{B}$	1	mA
See fig. 2	'RM \''	T _J = 125 °C	VR - Haleu VR	4	
Threshold voltage	V _{F(TO)}	$T_{\rm J} = T_{\rm J}$ maximum $\frac{0.47}{21.46}$		0.47	V
Forward slope resistance	r _t			mΩ	
Typical junction capacitance	CT	$V_{\rm R}$ = 5 $V_{\rm DC}$ (test signal range 100 kHz to 1 MHz), 25 °C 183		pF	
Typical series inductance	L _S	Measured lead to lead 5 mm from package body 5.0 r		nH	

Note

 $^{(1)}\,$ Pulse width < 300 µs, duty cycle < 2 %

THERMAL - MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction and storage temperature range	T _J ⁽¹⁾ , T _{Stg}		- 40 to 150	°C
Maximum thermal resistance, junction to case	R _{thJC}	DC operation See fig. 4	3.0	°C/W
Approximate weight			0.3	g
Approximate weight			0.01	oz.
Marking device		Case style D-PAK (similar to TO-252AA) 50WQ10FN		10FN

Note

 $^{(1)} \quad \frac{dP_{tot}}{dT_J} < \frac{1}{R_{thJA}} \quad \text{thermal runaway condition for a diode on its own heatsink}$



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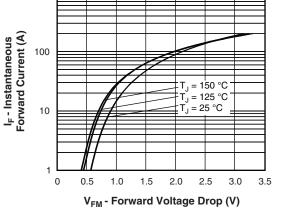


Fig. 1 - Maximum Forward Voltage Drop Characteristics

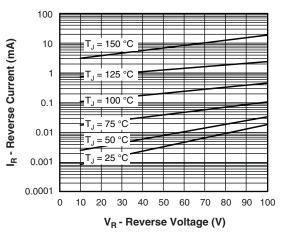


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

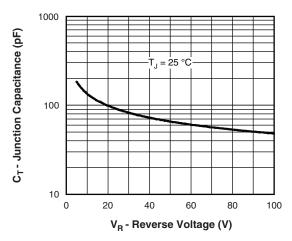
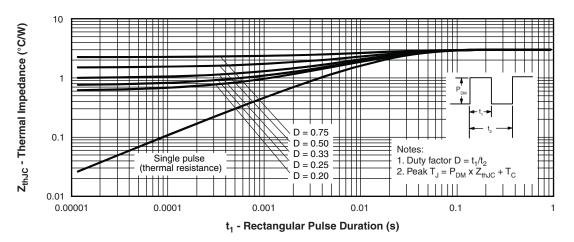


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage





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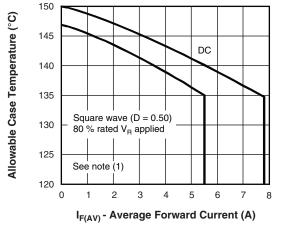
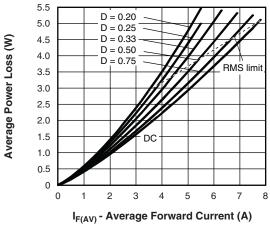


Fig. 5 - Maximum Allowable Case Temperature vs. Average Forward Current





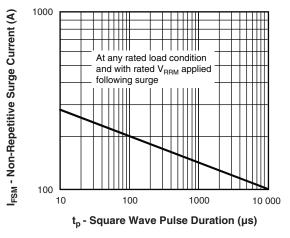


Fig. 7 - Maximum Non-Repetitive Surge Current

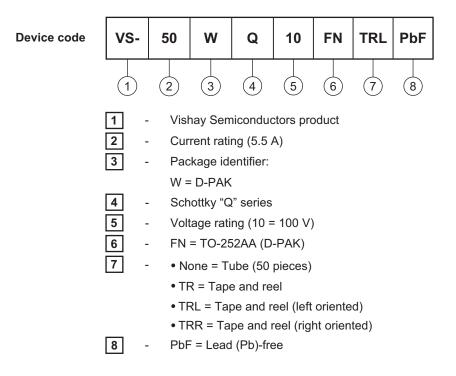
Note

- ⁽¹⁾ Formula used: $T_C = T_J (Pd + Pd_{REV}) \times R_{thJC}$;
- $\begin{array}{l} \mathsf{Pd} = \mathsf{Forward} \ \mathsf{power} \ \mathsf{loss} = \mathsf{I}_{\mathsf{F}(\mathsf{AV})} \ x \ \mathsf{V}_{\mathsf{FM}} \ \mathsf{at} \ (\mathsf{I}_{\mathsf{F}(\mathsf{AV})}/\mathsf{D}) \ (\mathsf{see fig. 6}); \\ \mathsf{Pd}_{\mathsf{REV}} = \mathsf{Inverse} \ \mathsf{power} \ \mathsf{loss} = \mathsf{V}_{\mathsf{R1}} \ x \ \mathsf{I}_{\mathsf{R}} \ (\mathsf{1} \mathsf{D}); \ \mathsf{I}_{\mathsf{R}} \ \mathsf{at} \ \mathsf{V}_{\mathsf{R1}} = \mathsf{80} \ \% \ \mathsf{rated} \ \mathsf{V}_{\mathsf{R}} \end{array}$

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LINKS TO RELATED DOCUMENTS			
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Part marking information	www.vishay.com/doc?95059		
Packaging information	www.vishay.com/doc?95033		
SPICE model	www.vishay.com/doc?95549		



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