REFERENCE DESIGN

IRAUDAMP7D

25W-500W Scalable Output Power Class D Audio Power Amplifier Reference Design Using the IRS2092 Protected Digital Audio Driver

By

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CAUTION:

International Rectifier suggests the following guidelines for safe operation and handling of IRAUDAMP7D Demo Board:

- **Always wear safety glasses whenever operating Demo Board**
- **Avoid personal contact with exposed metal surfaces when operating Demo Board**
- **Turn off Demo Board when placing or removing measurement probes**

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Introduction

The IRAUDAMP7D reference design is a two-channel Class D audio power amplifier that features output power scalability. The IRAUDAMP7D offers selectable half-bridge (stereo) and full-bridge (bridged) modes.

This reference design demonstrates how to use the IRS2092 Class D audio driver IC, along with IR's digital audio dual MOSFETs, such as IRFI4024H-117P, IRFI4019H-117P, IRFI4212H-117P and IRFI4020H-117P, on a single layer PCB. The design shows how to implement peripheral circuits on an optimum PCB layout using a single sided board.

The resulting design requires a small heatsink for normal operation (one-eighth of continuous rated power). The reference design provides all the required housekeeping power supplies and protections.

Unless otherwise noted, this user's manual is based on 150V model, IRAUDAMP7D-150,.

Other output power versions can be configured by replacing components given in the component selection of Table 5 on page 36

Applications

- AV receivers
- Home theater systems
- Mini component stereos
- Powered speakers
- Sub-woofers
- Musical Instrument amplifiers
- Automotive after market amplifiers

Features

Table 1 IRAUDAMP7D Specification Table Series

Notes:

- **All the power ratings are at clipping power (THD+N = 1 %). To estimate power ratings at THD+N=10%, multiply them by 1.33**
- **See Table 5 on page 36 for the complete listing of components table.**

Specifications

General Test Conditions for IRAUDAMP7D-150 (unless otherwise noted) Notes / Conditions

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Audio Performance

Thermal Performance (T_A=25 °C)

Physical Specifications

Test Setup

Connector Description

Switches Descriptions

Indicator Description

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Test Procedures

Test Setup:

- 1. On the unit under test (UUT), set switch S1 to OFF and S300 to Stereo positions.
- 2. Connect 4 Ω -200 W dummy loads to output connectors, SPKR1A and SPKR1B, as shown on Fig 1.
- 3. Set up a dual power supply ±50V with 5A current limit
- 4. Turn OFF the dual power supply before connecting to UUT.
- 5. Connect the dual power supply to CNN1, as shown in Fig 1.

Power up:

- 6. Turn ON the dual power supply. The ±B supplies must be applied and removed at the same time.
- 7. The red LEDs (Protections) turn ON immediately and stay on as long as S1 is in OFF position. Blue LEDs stay OFF.
- 8. Quiescent current for the positive and negative supplies must be less than 50mA, while S1 is in OFF position. Under this condition, IRS2092 is in shutdown mode.
- 9. Slide S1 to ON position; after one second delay, the two blue LEDs turn ON and the red LEDs turns off. The two blue LEDs indicate that PWM oscillation is present. This transition delay time is controlled by CSD pin of IRS2092, capacitor CP3
- 10. Under the normal operating condition with no input signal applied, quiescent current for the positive supply must be less than 50 mA; the negative supply current must be less than 100 mA.

Switching Frequency Test:

11. With an oscilloscope, monitor switching waveform at test points VS1 of VS2 and L1B of CH2. Self oscillating frequency must be 400 kHz \pm 25kHz. Note: The self-oscillating switching frequency is pre-calibrated to 400kHz by the value of R11. To change switching frequency, change the resistances of R11A and R11B for CH1 and CH2 respectively.

Audio Functionality Tests:

- 12. Set the signal generator to 1kHz, 20 m V_{RMS} output.
- 13. Connect audio signal generators to RCA1A and RCA1B.
- 14. Sweep the audio signal voltage from 15 mV_{RMS} to 1 V_{RMS}.
- 15. Monitor the output signals at SPK1A/B with an oscilloscope. Waveform must be a non distorted sinusoidal signal.
- 16. Observe 1 V_{RMS} input generates output voltage of 36 V_{RMS} . The ratio, R8/(R7+R2), determines the voltage gain of IRAUDAMP7D.
- 17. Set switch S300 to Bridged position.
- 18. Observe that voltage gain doubles.

Test Setup using Audio Precision (Ap):

- 19. Use unbalance-floating signal generator outputs.
- 20. Use balanced inputs taken across output terminals, SPKR1A and SPKR1B.
- 21. Connect Ap frame ground to GND in terminal CNN1.
- 22. Place AES-17 filter for all the testing except frequency response.
- 23. Use signal voltage sweep range from 15 mV_{RMS} to 1 V_{RMS}.
- 24. Run Ap test programs for all subsequent tests as shown in Fig 2- Fig 13 below.

Test Results

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Efficiency

Figs 14-19 show efficiency characteristics of the IRAUDAMP7D. The high efficiency is achieved by following major factors:

- 1) Low conduction loss due to the dual FETs offering low $R_{DS(ON)}$
- 2) Low switching loss due to the dual FETs offering low input capacitance for fast rise and fall times
- 3) Secure dead-time provided by the IRS2092, avoiding cross-conduction

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Thermal Considerations

With this high efficiency, the IRAUDAMP7D design can handle one-eighth of the continuous rated power, which is generally considered to be a normal operating condition for safety standards, without additional heatsink or forced air-cooling.

Power Supply Rejection Ratio (PSRR)

The IRAUDAMP7D obtains good power supply rejection ratio of -65 dB at 1kHz shown in Fig 20. With this high PSRR, IRAUDAMP7D accepts any power supply topology as far as the supply voltages fit in the min and max range.

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Short Circuit Protection Response

Figs 21-23 show over current protection reaction time of the IRAUDAMP7D in a short circuit event. As soon as the IRS2092 detects over current condition, it shuts down PWM. After one second, the IRS2092 tries to resume the PWM. If the short circuit persists, the IRS2092 repeats try and fail sequences until the short circuit is removed.

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Actual Reaction Time

IRAUDAMP7D Overview

The IRAUDAMP7D features a self-oscillating type PWM modulator for the lowest component count, highest performance and robust design. This topology represents an analog version of a second-order sigma-delta modulation having a Class D switching stage inside the loop. The

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benefit of the sigma-delta modulation, in comparison to the carrier-signal based modulation, is that all the error in the audible frequency range is shifted to the inaudible upper-frequency range by nature of its operation. Also, sigma-delta modulation allows a designer to apply a sufficient amount of error correction.

The IRAUDAMP7D self-oscillating topology consists of following essential functional blocks.

- Front-end integrator
- PWM comparator
- Level shifters
- Gate drivers and MOSFETs
- Output LPF

Integrator

Referring to Fig 24 below, the input operational amplifier of the IRS2092 forms a front-end secondorder integrator with R7, C4, C6, and R11. The integrator that receives a rectangular feedback signal from the PWM output via R8 and audio input signal via R7 generates quadratic carrier signal in COMP pin. The analog input signal shifts the average value of the quadratic waveform such that the duty cycle varies according to the instantaneous voltage of the analog input signal.

PWM Comparator

The carrier signal in COMP pin is converted to PWM signal by an internal comparator that has threshold at middle point between VAA and VSS. The comparator has no hysteresis in its input threshold.

Level Shifters

The internal input level-shifter transfers the PWM signal down to the low-side gate driver section. The gate driver section has another level-shifter that level shifts up the high-side gate signal to the high-side gate driver section.

Gate Drivers and MOSFETs

The received PWM signal is sent to the dead-time generation block where a programmable amount of dead time is added into the PWM signal between the two gate output signals of LO and HO to prevent potential cross conduction across the output power MOSFETs. The high-side levelshifter shifts up the high-side gate drive signal out of the dead-time block.

The IRS2092 drives two MOSFETs, high- and low-sides, in the power stage providing the amplified PWM waveform.

Output LPF

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The amplified PWM output is reconstructed back to analog signal by the output LC LPF. Demodulation LC low-pass filter (LPF) formed by L1 and C12, filters out the Class D switching carrier signal leaving the audio output at the speaker load. A single stage output filter can be used with switching frequencies of 400 kHz and greater; a design with a lower switching frequency may require an additional stage of LPF.

Functional Descriptions

IRS2092 Gate Driver IC

The IRAUDAMP7D uses IRS2092, a high-voltage (up to 200 V), high-speed power MOSFET driver with internal dead-time and protection functions specifically designed for Class D audio amplifier applications. These functions include OCP and UVP. The IRS2092 integrates bidirectional over current protection for both high-side and low-side MOSFETs. The dead-time can be selected for optimized performance according to the size of the MOSFET, minimizing deadtime while preventing shoot-through. As a result, there is no gate-timing adjustment required externally. Selectable dead-time through the DT pin voltage is an easy and reliable function which requires only two external resistors, R26 and R27 as shown on Fig 25 below.

The IRS2092 offers the following functions.

PWM modulator

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- Dead-time insertion
- Over current protection
- Under voltage protection
- Level shifters

Refer to IRS2092 datasheet and AN-1138 for more details.

Self-Oscillating Frequency

Self-oscillating frequency is determined by the total delay time along the control loop of the system; the propagation delay of the IRS2092, the MOSFETs switching speed, the time-constant of front-end integrator (R7, R8, R11, C4, C6, C7). Variations in +B and –B supply voltages also affect the self-oscillating frequency.

The self-oscillating frequency changes with the duty ratio. The frequency is highest at idling. It drops as duty cycle varies away from 50%.

Adjustments of Self-Oscillating Frequency

Use R11 to set different self-oscillating frequencies. The PWM switching frequency in this type of self-oscillating switching scheme greatly impacts the audio performance, both in absolute

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frequency and frequency relative to the other channels. In the absolute terms, at higher frequencies distortion due to switching-time becomes significant, while at lower frequencies, the bandwidth of the amplifier suffers. In relative terms, interference between channels is most significant if the relative frequency difference is within the audible range.

Normally, when adjusting the self-oscillating frequency of the different channels, it is suggested to either match the frequencies accurately, or have them separated by at least 25kHz. Under the normal operating condition with no audio input signal, the switching-frequency is set around 400kHz in the IRAUDAMP7D**.**

Selectable Dead-time

The dead-time of the IRS2092 is set based on the voltage applied to the DT pin. Fig 26 lists the suggested component value for each programmable dead-time between 25 and 105 ns. All the IRAUDAMP7D models use DT2 (45ns) dead-time.

Protection System Overview

The IRS2092 integrates over current protection (OCP) inside the IC. The rest of the protections, such as over-voltage protection (OVP), under-voltage protection (UVP), speaker DC offset

protection (DCP) and over temperature protection (OTP), are realized externally to the IRS2092 (Fig 27).

In the event that any of these external fault conditions are detected, the external shutdown circuit will disable the output by pulling down CSD pins, turning on red LEDs, and turning off blue LEDs (Fig 28). If the fault condition persists, the protection circuit stays in shutdown until the fault is removed. Once the fault is cleared, the blue LEDs turn on and red LEDs turn off.

Over-Current Protection (OCP) Low-Side Current Sensing

The low-side current sensing feature protects the low side MOSFET from an overload condition in negative load current by measuring drain-to-source voltage across $R_{DS(ON)}$ during its on state. OCP shuts down the switching operation if the drain-to-source voltage exceeds a preset trip level.

The voltage setting on the OCSET pin programs the threshold for low-side over-current sensing. When the VS voltage during low-side conduction gets higher than the OCSET voltage, the IRS2092 turns off outputs and pulls CSD down to -VSS.

High-Side Current Sensing

The high-side current sensing protects the high side MOSFET from an overload condition in positive load current by measuring drain-to-source voltage across $R_{DS(ON)}$ during its on state. OCP shuts down the switching operation if the drain-to-source voltage exceeds a preset trip level.

High-side over-current sensing monitors drain-to-source voltage of the high-side MOSFET while it is in the on state through the CSH and VS pins. The CSH pin detects the drain voltage with reference to the VS pin, which is the source of the high-side MOSFET. In contrast to the low-side current sensing, the threshold of CSH pin to trigger OC protection is internally fixed at 1.2V. An external resistive divider R19, R18 and R17 are used to program a threshold as shown in Fig 26. An external reverse blocking diode D4 is required to block high voltage feeding into the CSH pin during low-side conduction. By subtracting a forward voltage drop of 0.6V at D4, the minimum threshold which can be set for the high-side is 0.6V across the drain-to-source.

Table 2 Actual OCP table setting thresholds

Over-Voltage Protection (OVP)

OVP is provided externally to the IRS2092. OVP shuts down the amplifier if the bus voltage between GND and +B exceeds 75V. The threshold is determined by a Zener diode Z100. OVP

protects the board from harmful excessive supply voltages, such as due to bus pumping at very low frequency continuous output in stereo mode.

Under-Voltage Protection (UVP)

UVP is provided externally to the IRS2092. UVP prevents unwanted audible noise output from unstable PWM operation during power up and down. UVP shuts down the amplifier if the bus voltage between GND and +B falls below a voltage set by Zener diode Z101.

Speaker DC-Voltage Protection (DCP)

DCP protects speakers against DC output current feeding to its voice coil. DC offset detection detects abnormal DC offset and shuts down PWM. If this abnormal condition is caused by a MOSFET failure because one of the high-side or low-side MOSFETs short circuited and remained in the on state, the power supply needs to be cut off in order to protect the speakers. Output DC offset greater than ±4V triggers DCP.

Offset Null (DC Offset) Adjustment

The IRAUDAMP7D requires no output-offset adjustment. DC offsets are tested to be less than ±20 mV.

Over-Temperature Protection (OTP)

A NTC resistor, TH100 in Fig 25, is placed in close proximity to two dual MOSFETs on a heatsink to monitor heatsink temperature. If the heatsink temperature rises above 100 \degree C, the OTP shuts down both channels by pulling down CSD pins of the IRS2092. OTP recovers once the temperature has cooled down.

ON-OFF Switch

OFF position of S1 forces the IRAUDAMP7D to stay in shutdown mode by pulling down the CSD pin. During the shutdown mode the output MOSFETs are kept off.

Click and POP Noise Reduction

Thanks to the click and pop elimination function built into the IRS2092, IRAUDAMP7D does not use any additional components for this function.

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Power Supply Requirements

For convenience, the IRAUDAMP7D has all the necessary housekeeping power supplies onboard and only requires a pair of symmetric power supplies. Power supply voltage depends on the model and is shown in the power selection in Table 1.

House Keeping Power Supply

The internally-generated housekeeping power supplies include ±5.6V for analog signal processing, and $+12V$ supply (V_{cc}) referred to negative supply rail -B for MOSFET gate drive. The VAA and VSS supplying floating input section are fed from +B and -B power stage bus supplies via R117 and R118, respectively. Gate driver section of IRS2092 uses VCC to drive gates of MOSFETs. The V_{CC} is referenced to $-B$ (negative power supply). D3 and CP6 form a bootstrap floating supply for the HO gate driver.

Bus Pumping

When the IRAUDAMP7D is running in the stereo mode, bus pumping effect takes place with low frequency high output. Since the energy flowing in the Class D switching stage is bi-directional, there is a period where the Class D amplifier feeds energy back to the power supply. The majority of the energy flowing back to the supply is from the energy stored in the inductor in the output LPF. Usually, the power supply has no way to absorb the energy coming back from the load. Consequently the bus voltage is pumped up, creating bus voltage fluctuations.

Following conditions make bus pumping worse:

- 1. Lower output frequencies (bus-pumping duration is longer per half cycle)
- 2. Higher power output voltage and/or lower load impedance (more energy transfers between supplies)
- 3. Smaller bus capacitance (the same energy will cause a larger voltage increase)

The OVP protects IRAUDAMP7D from failure in case of excessive bus pumping. One of the easiest counter measures of bus pumping is to drive both of the channels in a stereo configuration out-of-phase so that one channel consumes the energy flow from the other and does not return it to the power supply. Bus voltage detection monitors only +B supply, assuming the bus pumping on the supplies is symmetric in +B and -B supplies.

There is no bus pumping effect in full bridge mode.

Bridged Configuration

By selecting S300 to Bridged position, the IRAUDAMP7D realizes full bridge mode, also known as bridge-tied-load, or BTL configuration. Full bridge operation is achieved by feeding out-of-phase audio input signals to the two input channels as shown in the Fig 30 below.

In bridged mode, IRAUDAMP7D receives audio input signal from channel A only. The on-board inverter feed out-of-phase signal to Channel B. The speaker output must be connected between (+) of Channel A and (+) of Channel B in bridged mode.

In bridged mode, nominal load impedance is $8 Ω$. (See power table in Table 1)

Load Impedance

Each channel is optimized for a 4 Ω speaker load in half bridge and 8 Ω load in full bridge.

Output Filter Selection

Since the output filter is not included in the control loop of the IRAUDAMP7D, the control loop has no ability to compensate performance deterioration caused by the output filter. Therefore, it is necessary to understand what characteristics are preferable when designing the output filter.

- 1) The DC resistance of the inductor should be minimized to 20 m Ω or less.
- 2) The linearity of the output inductor and capacitor should be high with output current and voltage.

Fig 31 demonstrates THD performance difference with various inductors.

Input Signal and Gain Setting

A proper input signal is an analog signal ranging from 20Hz to 20kHz with up to 3 V_{RMS} amplitude with a source impedance of no more than 600 Ω. Input signal with frequencies from 30kHz to 60kHz may cause LC resonance in the output LPF, causing a large reactive current flowing through the switching stage, especially with greater than 8 Ω load impedances, and the LC resonance can activate OCP.

The IRAUDAMP7D has an RC network called Zobel network (R30 and C13) to damp the resonance and prevent peaking frequency response with light loading impedance. (Fig 32) The Zobel network is not thermally rated to handle continuous supersonic frequencies above 20kHz. These supersonic input frequencies can be filtered out by adding R2 and C2 as shown on main schematic Fig 33 and Fig 34. This RC filter works also as an input RF filter to prevent potential radio frequency interferences.

Gain Setting

The ratio of resistors R8/R2 in Fig 23 sets voltage gain. The IRAUDAMP7D has no on board volume control. To change the voltage gain, change the input resistor term R2. Changing R8 affects PWM control loop design and may result poor audio performance.

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IRAUDAMP7D-150 Fabrication Materials

Table 3 IRAUDAMP7D-150 Electrical Bill of Materials

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Table 4 IRAUDAMP7D Mechanical Bill of Materials

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Table 5 IRAUDAMP7D Models Differential Table

IRAUDAMP7D Hardware

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IRAUDAMP7D PCB Specifications

PCB:

- 1. Single Layers SMT PCB with through holes
- 2. 1/16 thickness
- 3. 2/0 OZ Cu
- 4. FR4 material
- 5. 10 mil lines and spaces
- 6. Solder Mask to be Green enamel EMP110 DBG (CARAPACE) or Enthone Endplate DSR-3241or equivalent.
- 7. Top Silk Screen to be white epoxy non conductive per IPC–RB 276 Standard.
- 8. All exposed copper must finished with TIN-LEAD Sn 60 or 63 for 100u inches thick.
- 9. Tolerance of PCB size shall be 0.010 –0.000 inches
- 10. Tolerance of all Holes is -.000 + 0.003"
- 11. PCB acceptance criteria as defined for class II PCB'S standards.

Gerber Files Apertures Description:

All Gerber files stored in the attached CD-ROM were generated from Protel Altium Designer Altium Designer 6. Each file name extension means the following:

- 1. .gbl Bottom copper, bottom side
- 2. .gto Top silk screen
- 3. .gbs Bottom Solder Mask
- 4. .gko Keep Out,
- 5. .gm1 Mechanical
- 6. .gd1 Drill Drawing
- 7. .gg1 Drill locations
- 8. .txt CNC data
- 9. .apr Apertures data

Additional files for assembly that may not be related with Gerber files:

- 10. .pcb PCB file
- 11. .bom Bill of materials
- 12. .cpl Components locations
- 13. .sch Schematic
- 14. .csv Pick and Place Components
- 15. .net Net List
- 16. .bak Back up files
- 17. .lib PCB libraries

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Revision changes descriptions

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105 *Data and specifications subject to change without notice. 09/03/2008*

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