MP6517B

Single-Phase, BLDC, Motor Driver with Integrated Hall Sensor in a TSOT23-6 Package

The Future of Analog IC Technology

DESCRIPTION

The MP6517B is a single-phase, brushless, DC motor drivers with integrated power MOSFETs and a Hall effect sensor. The MP6517B drives single-phase brushless DC fan motors with up to 2A of output current limit. The IC has a 3.3V to 16V input voltage range and input line reverse voltage protection to save the external diode on the supply line.

The MP6517B controls the rotational speed through the PWM signal on the PWM pin. The MP6517B has a rotational speed detection feature and rotor lock fault indication on FG/RD with an open-drain collector output. The output speed versus the input duty curve can be programmed easily for flexible use. To reduce fan driver audible noise and power loss, the MP6517B features a soft on/off phase transition and automatic phase-lock function of the motor winding BEMF and current.

Full protection features include input over-voltage protection (OVP), under-voltage lockout (UVLO), rotor deadlock protection, thermal shutdown, and input reverse protection.

The MP6517B requires a minimal number of external components to save solution cost. The MP6517B is available in TSOT23-6-L, TSOT23-6-R, TSOT23-6-SL, and TSOT23-6-RSL packages.

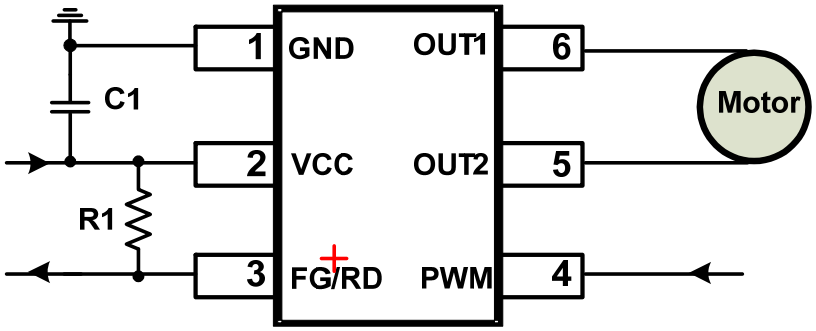
FEATURES

- Embedded Hall Sensor with High Sensitivity
- Wide 3.3V to 16V Operating Input Range
- Up to 2A Programmable Current Limit
- Integrated Power MOSFETs: Total 850mΩ (HS + LS)
- Programmable Speed Curve
- Built-In Adjustable Speed Curve Corner Setting
- Automatic Phase Lock Detection of Winding BEMF and Current Zero-Crossing
- Soft On/Off Phase Transition
- Rotational Speed Indicator (FG) Signal
- 12kHz to 48kHz PWM Input Frequency Range
- Fixed 26kHz Output Switching Frequency
- Input Line Reverse Voltage Protection (RVP)
- Rotor Deadlock (RD) Protection and Automatic Recovery
- Thermal Protection and Automatic Recovery
- Built-In Input OVP, UVLO, and Automatic Recovery
- Available in TSOT23-6-L, TSOT23-6-R, TSOT23-6-SL, and TSOT23-6-RSL Packages

APPLICATIONS

- CPU Fan for Personal Computers or Servers
- Brushless DC Motor

TYPICAL APPLICATION



ORDERING INFORMATION

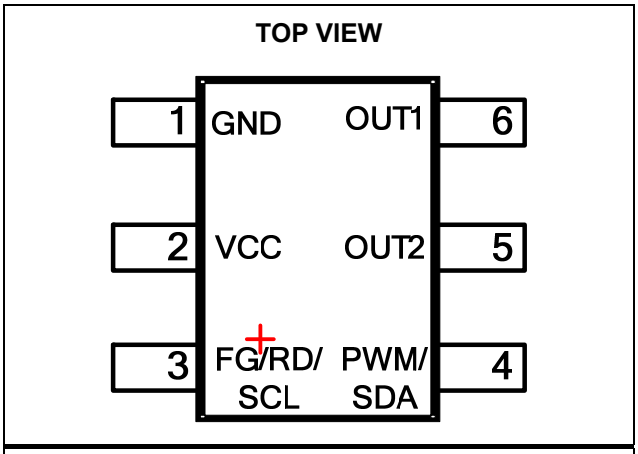
Part Number*	Package	Tape & Reel	Top Marking
MP6517BGJL-xxxx**	TSOT23-6-L	Normal	*See Below*
MP6517BGJR-xxxx**	TSOT23-6-R	**Reverse**	
MP6517BGJS-xxxx**	TSOT23-6-SL	Normal	
MP6517BGJSR-xxxx**	TSOT23-6-RSL	**Reverse**	

* For Tape & Reel, add suffix –Z (e.g. MP6517BGJS–Z)

** “xxxx” is the configuration code identifier.
The four digits of the suffix (xxxx) can be a hexadecimal value between 0 and F.
Please work with an MPS FAE to create this unique number, even if ordering the “0000” code.

Part Number	Top Marking	Bottom Mark	
MP6517BGJL	|BDAY	CLLL	BDA: Product code Y: Year code C: suffix LLL: lot number
MP6517BGJR	|BDAY	CLLL	
MP6517BGJS	BDBY LLL	• •	BDB: Product code Y: Year code C: suffix LLL: lot number
MP6517BGJSR	BDBY LLL	• •	

PACKAGE REFERENCE



Package
TSOT23-6-L
TSOT23-6-R
TSOT23-6-SL
TSOT23-6-RSL

ABSOLUTE MAXIMUM RATINGS (1)

VCC ..... ±19V
VCC(≤1ms) 22V
FG/RD, $V_{OUT1/2}$ ..... -0.3V to 19.3V
FG/RD, $V_{OUT1/2}$(≤1ms) ..... -0.3V to 22.3V
All other pins ..... -0.3V to +6.5V
Continuous power dissipation (T_A = +25°C) (2) 1.25W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -60°C to 150°C

Recommended Operating Conditions (3)

Supply voltage (VCC) 3.3V to16V
Operating junction temp. (T_J) ....-40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-6 ..... 100 ..... 55 ... °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VCC = 12V, T_J = -40°C to 125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input UVLO rising threshold	V_{UVLO}			3		V
Input UVLO hysteresis				0.15		V
Operating supply current	I_{CC}			6.5		mA
Reverse supply current	I_{CCREV}	VCC = -18V			1	mA
PWM input high voltage	V_{PWMH}		1.5			V
PWM input low voltage	V_{PWML}				0.4	V
PWM input frequency	F_{PWM}		12		48	kHz
Min PWM input low-level time (5)			200			ns
PWM input internal pull-up resistance				100		kΩ
HS switch-on resistance	R_{HSON}	I_O = 100mA, including reversed MOSFET		520		mΩ
LS switch-on resistance	R_{LSON}	I_O = 100mA		330		mΩ
Over-current limit protection threshold	I_{OCP}			2.6		A
Output current limit	I_{LMT}	SUCL = 100	-15%	1.36	+15%	A
Internal oscillator frequency	f_{CLK}		-15%	7	+15%	MHz
PWM output frequency	Fs		-15%	26	+15%	kHz
FG output low-level voltage	V_{FG_L}	IFG/RD = 3mA, V_{PULL} = 5V			0.35	V
FG leakage current					1	μA
Soft turn-on angle	θ_{SON_100}	SON_100 = 10000		23.9		°
Soft turn-off angle	θ_{SOFF_100}	SOFF_100 = 11111		45		°
Adjustable delay angle	θe	THETA_E = 0000		0		°
Rotor-lock detection time	T_{RD}			0.6		s
Minimum recommended magnetic field (5)				±1		mT
Thermal shutdown threshold (5)				150		°C
Thermal shutdown hysteresis (5)				25		°C

NOTE:

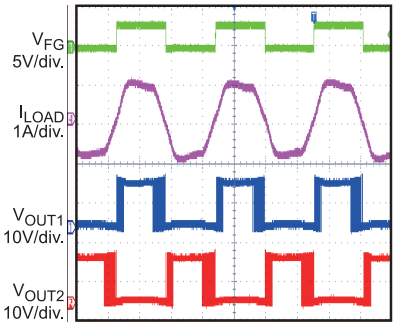
5) Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

VCC = 12V, T_A = 25°C, tested with fan unit, unless otherwise noted.

Typical Waveform, 100% Duty Output

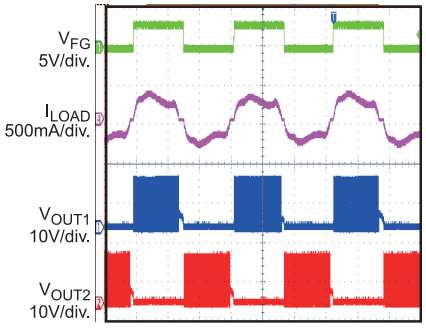
V_{CC}=12V DC, PWM=25kHz, 100% Duty



2ms/div.

Typical Waveform, 50% Duty Output

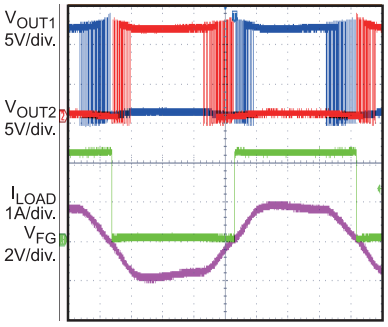
V_{CC}=12V DC, PWM=25kHz, 50% Duty



4ms/div.

Typical Waveform, Switching Soft On & Soft Off

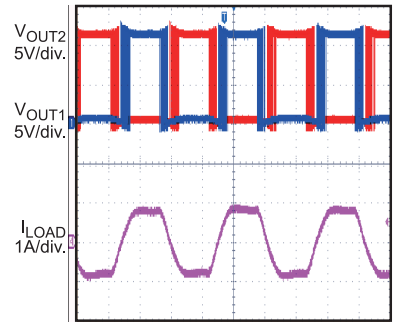
V_{CC}=12V DC, PWM= 5V DC, w/ soft on/off phase transition



800µs/div.

Typical Waveform, Enable Soft On & Soft Off

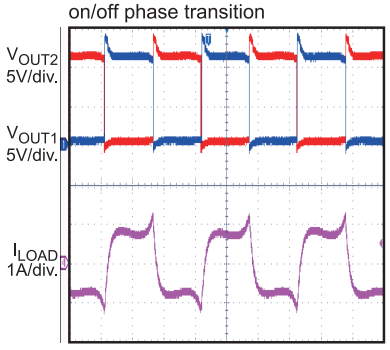
V_{CC}=12V DC, PWM= 5V DC, w/ soft on/off phase transition



2ms/div

Typical Waveform, Disable Soft On & Soft Off

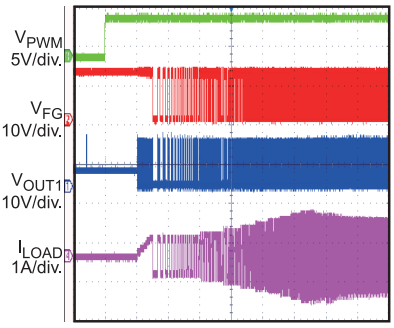
V_{CC}=12V DC, PWM= 5V DC, w/o soft on/off phase transition



2ms/div

Typical Waveform, Start-Up with PWM

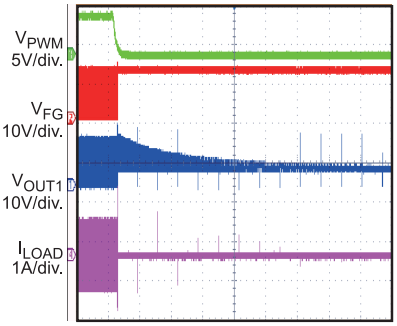
V_{CC}=12V DC, PWM= 0V to 5V DC



400ms/div

Typical Waveform, Shutdown with PWM

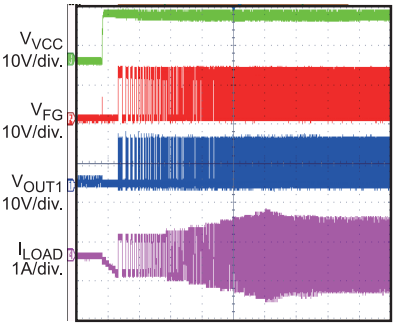
V_{CC}=12V DC, PWM=5V DC to 0V



1s/div

Typical Waveform, Start-Up with VCC

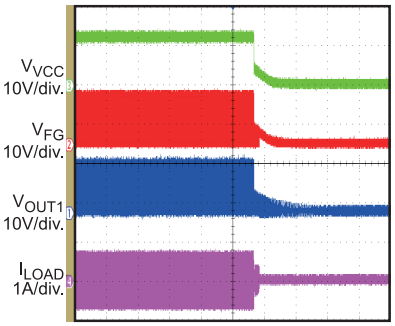
PWM=5V DC, V_{CC}= 0V to 12V DC



400ms/div

Typical Waveform, Shutdown with VCC

PWM=5V DC, V_{CC}=12V DC to 0V



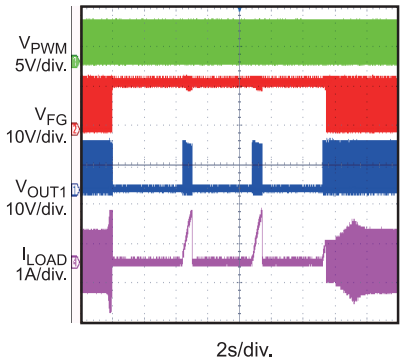
1s/div

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VCC = 12V, T_A = 25°C, tested with fan unit, unless otherwise noted.

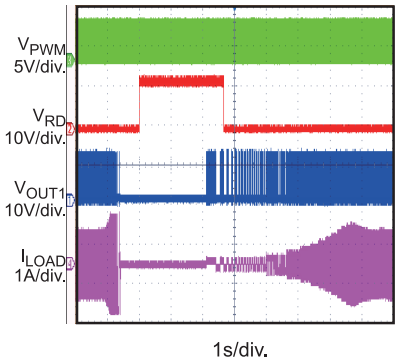
Typical Waveform, Rotor Lock & Release

V_{CC}= 12V DC, PWM=5V DC, Lock Rotor and Releaset



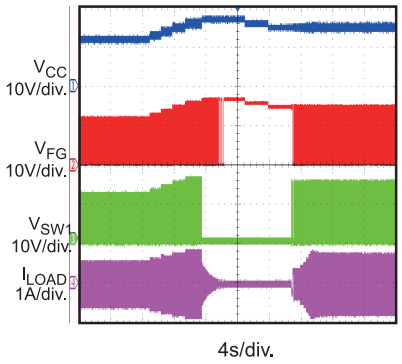
Typical Waveform, Rotor Lock & Release

V_{CC}= 12V DC, PWM=5V DC, Lock Rotor and Release



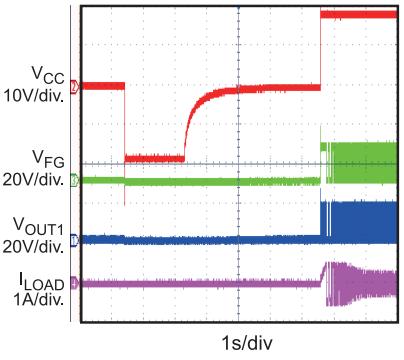
Typical Waveform, Over-Voltage Protection

PWM=25kHz, 100% Duty, V_{CC}=12V DC to 16.5V DC to 14.5V DC, Test with Fan Unit



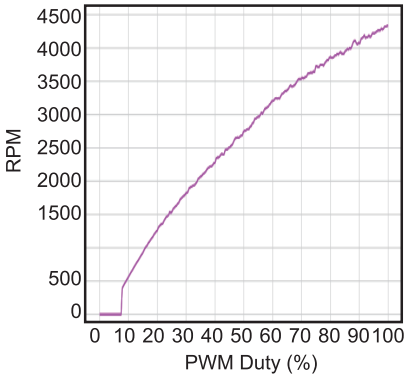
Typical Waveform, VCC Reverse Protection

VIN= 0V to -18V DC to 0V to +18V DC



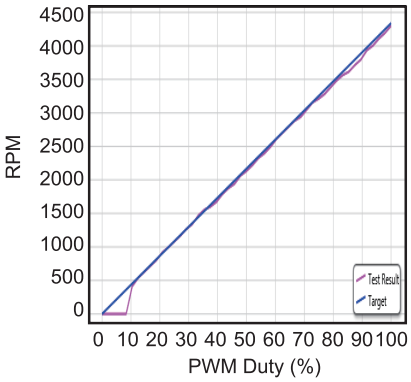
Typical Curve, RPM Output vs. PWM Input Duty

V_{CC}=12V DC, PWM=25kHz, Test with Fan Unit, Default Register Setting



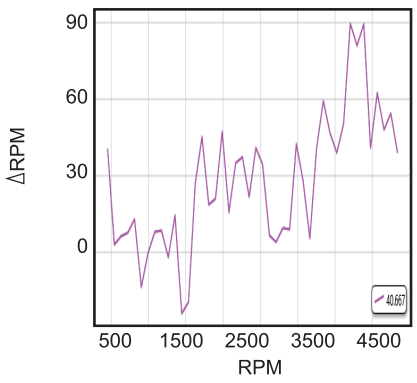
Typical Curve, RPM Output vs. PWM Input Duty

V_{CC}=12V DC, PWM=25kHz, Test with Fan Unit, Optimized Rpm Curve & Programmed by MPS GUI Software



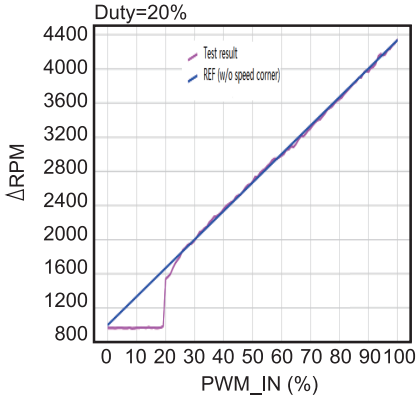
RPM Output Error vs. RPM Target

V_{CC}=12V DC, PWM=25kHz, Test with Fan Unit, Optimized Rpm Curve & Programmed by MPS GUI Software



Typical Curve, RPM Output vs. PWM Input Duty

V_{CC}=12V DC, PWM=25kHz, Optimized Rpm Curve & Programmed by MPS GUI Software, Speed Corner Duty=20%



PIN FUNCTIONS

Pin #	Name	Description
1	GND	**Ground.**
2	VCC	**Input voltage supply.**
3	FG/RD SCL	**Speed indication or rotor lock fault indication output.** This pin functions as I^2C SCL in test mode (TM).
4	PWM SDA	**Rotational speed control PWM input.** PWM 12kHz to 48kHz is recommended in normal operation. PWM is an internal pull-up with 100kΩ of resistance to the internal LDO. This pin functions as I^2C SDA in test mode (TM).
5	OUT2	**Motor driver output 2.** OUT2 is connected to the mid-point of the internal N-channel MOSFET half-bridge.
6	OUT1	**Motor driver output 1.** OUT1 is connected to the mid-point of the internal N-channel MOSFET half-bridge.

BLOCK DIAGRAM

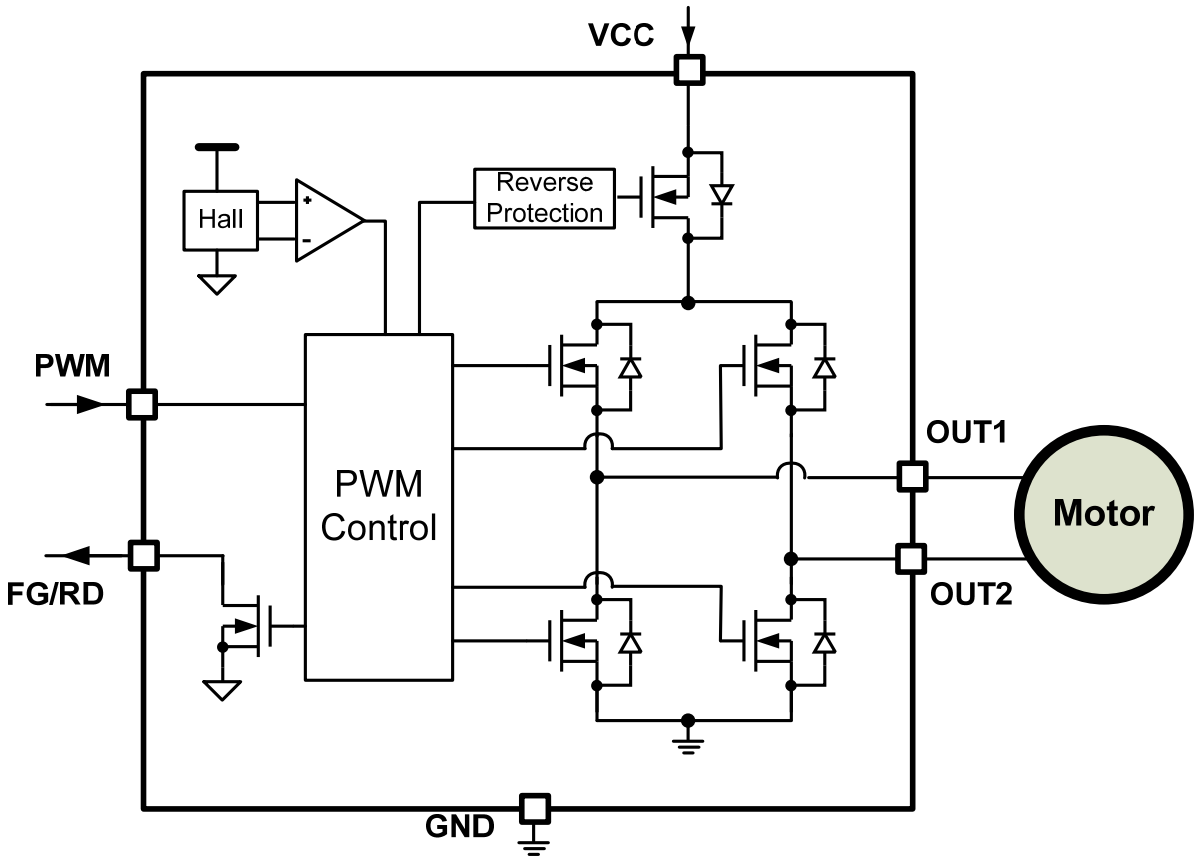


Figure 1: Functional Block Diagram

OPERATION

The MP6517B is a single-phase, brushless, DC motor drivers with integrated power MOSFETs and a Hall effect sensor.

Speed Control

The MP6517B is controlled using a pulse-width modulation (PWM) input interface, which is compatible with industry-standard devices. The IC detects the PWM input signal duty cycle and linearly controls the H-bridge output duty cycle, so the fan speed increases as the input duty cycle increases.

The PWM input accepts a wide input frequency range (12kHz to 48kHz), while the output frequency is kept constant at 26kHz above the audible frequency range.

PWM Output Drive

The IC controls the H-bridge MOSFET switching to reduce speed variation and increase system efficiency (see Figure 2).

When the rotor magnet pole S comes around, the internal Hall sensor outputs high. When the rotor magnet pole N comes around, the internal Hall sensor outputs low. With this H_{A_IN} signal, the H_{A_OUT} signal is generated after the θe delay time, which is set from 0° to 15° through the register THETA_E bits. During the H_{A_OUT} high interval, the OUT2 and OUT1 switching status can be divided to different timing sections.

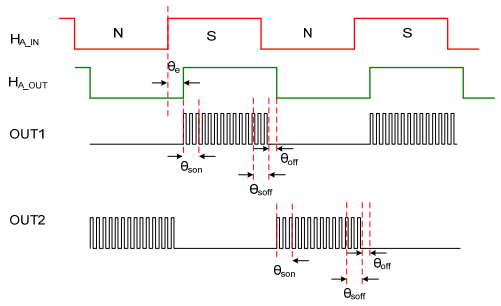


Figure 2: Timing Diagram

Soft Turn-On Section

During this time, OUT1 continues switching, and the duty cycle increases gradually from 0 to the target setting duty cycle in 16 steps max. OUT2 remains low. Determine the duration time from the linear interpolation between the SON_100 and SON_12P5 bits setting value, which is in range of 1.45° to 45° in 32 steps.

Normal PWM Switching Section

During this time, OUT1 continues switching, and the duty cycle is fixed at the target setting duty. OUT2 remains low.

Soft Turn-Off Section

During this time, OUT1 continues switching, and the duty cycle decreases gradually from the target setting duty cycle to 0 in 16 steps max. OUT2 remains low. Determine the duration time from the linear interpolation between the SOFF_100 and SOFF_12P5 bits setting value, which is in range of 1.45° to 45° in 32 steps.

Off Section

During this time, OUT1 remains at high impedance. OUT2 remains low. The time duration is adaptive from 0° to 45°. In steady state, this function block maintains the phase lock of the Hall output falling edge and winding current zero-crossing edge.

For the Hall output low interval, the conducting phase changes, but the switching sequence remains the same.

Minimum Speed and Corner Speed Point

The minimum PWM output duty is determined by the register 00H value when the input PWM duty cycle is lower than the corner duty set by register 14H. By setting register 00H to 0, the fan stops rotating when the PWM input duty is lower than the corner duty. By setting register 00H to a non-zero value, the fan maintains a minimum speed rotation when the PWM input duty is lower than the corner duty (see Figure 3).

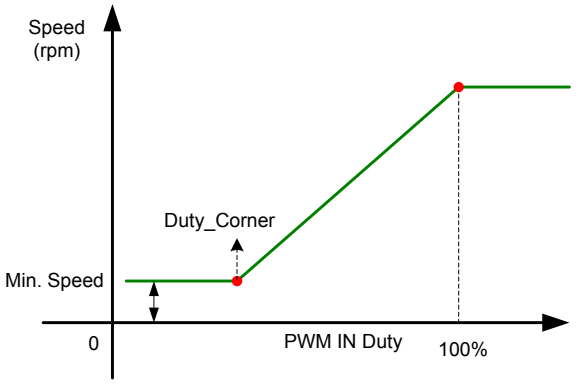


Figure 3: Programmable Speed Curve

Protection Circuits

The MP6517B is fully protected against over-voltage, under-voltage, over-current, over-temperature events and has input reverse protection.

Over-Current Protection (OCP)

The MP6517B protects against internal overload and short circuit by detecting the current flowing through each MOSFET. If the current flowing through any MOSFET exceeds the over-current protection (OCP) threshold after about 1.5μs of blanking time, that MOSFET turns off immediately.

Overload Current Limit

During normal switching, if the current flowing through the high-side MOSFET (HS-FET) of the H-bridge exceeds the threshold set by the register SUCL bits after around 1.5μs of blanking time, the HS-FET turns off immediately. The HS-FET resumes switching in the next switching cycle. The overload current limit is fixed at around 1360mA. To spin up the fan driver softly during start-up, the current limit increases from 0 to the programmed current limit in 16 steps (see Figure 4). Each step limit value lasts for 16 internal Hall cycles. In rotor lock fault cases, the current limit increases with 16 steps with 600ms of detection time.

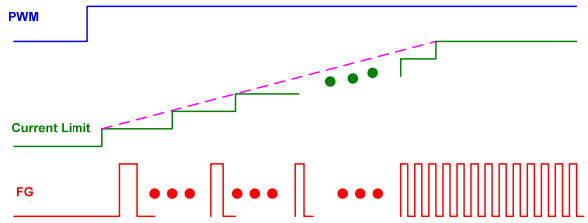


Figure 4: Start-Up Waveforms

Thermal Shutdown

Thermal monitoring is also integrated into the MP6517B. If the die temperature rises above 150°C, the MOSFETs of the switching half-bridge turn off. Once the die temperature has fallen to a safe level, operation resumes automatically.

Under-Voltage Lockout (UVLO)

If at any time VCC falls below the under-voltage lockout (UVLO) threshold voltage, all circuitry in the device is disabled, and the internal logic is reset. Operation resumes when VCC rises above the UVLO threshold.

Rotor Deadlock Protection (RD)

The MP6517B detects the internal Hall signal and outputs a deadlock indication signal to FG/RD if the FGRD bit is set to 11. If the IC cannot see the Hall signal edge change during the 0.6s detection time, all MOSFETs of the H-bridge are turned off. FG/RD is an open-drain output. After 1.8, 2.4, 3, or 3.6s of recovery time (depending on the RLOCK_SEL bit setting), the IC attempts to start up again automatically. FG/RD is pulled low again only after three Hall signal edges are detected after the rotor lock condition is released (see Figure 5).

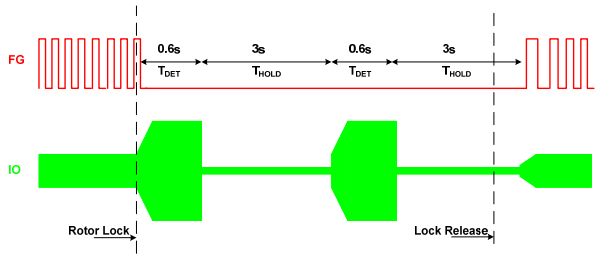


Figure 5: Rotor Deadlock Protection

Rotor Speed Indication (FG)

The MP6517B outputs a Hall detection signal to FG/RD as speed indication. The output signal frequency can be optional for 1x, 0.5x, and 2x the internal Hall sensor output frequency. FG/RD is an open-drain, so it needs a pull-up resistor in the application.

Over-Voltage Protection (OVP)

If VCC exceeds the over-voltage threshold (16.2V), the IC turns off the two HS-FETs and turns on the two low-side MOSFETs (LS-FET) until VCC drops below 15V. Then the IC resumes normal operation.

Input Reverse Connection Protection

If the input line is reverse-connected to VCC and GND, the IC detects the fault condition automatically and shuts down to avoid damage.

Test Mode and Factory Mode

With VCC powered, the IC enters test mode by sourcing 5~10mA of current with an external resistor and negative voltage for around 5ms. In test mode, all function blocks are active, and PWM and FG/RD can be used as the I²C interface to read or write the internal register bits (see Figure 6).

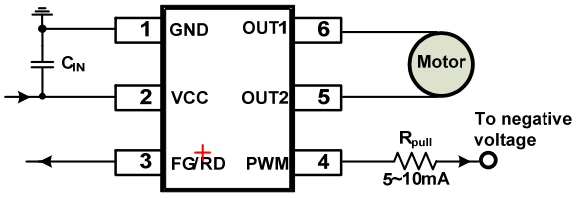


Figure 6: Test Mode Configuration

In test mode, first write the data 28H to the register 11H, and then write the data 04H to the register 10H. In factory mode, all writeable register values can be user-programmed. The IC exits test mode or factory mode when the VCC power is recycled.

I²C Chip Address

After the start condition, the I²C-compatible master sends a 7-bit address followed by an eighth read (1) or write (0) bit. The following bit indicates the register address to or from which the data is written or read (see Figure 7).

1	0	1	0	1	0	1	r/w

Figure 7: I²C Compatible Device Address

REGISTER MAPPING

Add	Type	D7	D6	D5	D4	D3	D2	D1	D0
00H	OTP/REG	PWMO[7:0]							
01H-08H	OTP/REG	PWMO[7:0]							
09H	OTP/REG	PROG[1:0]		PCODE[5:0]					
0AH	OTP/REG	FGRD[1:0]		RPMS[2:0]			SUCL[2:0]		
0BH	OTP/REG	FG	TM	HLL_CALI	SON_12P5[4:0]				
0CH	OTP/REG				SON_100[4:0]				
0DH	OTP/REG		SOFTEN	RD_HL	SOFF_12P5[4:0]				
0EH	OTP/REG				SOFF_100[4:0]				
0FH	OTP/REG		PLLEN	RLOCK_SEL[1:0]		THETA_E[3:0]			
10H	REG	Reserved					FM	Reserved	
11H-13H	REG	Reserved							
14H	OTP/REG	DUTY_CORNER[7:0]							

Register Table 1-9

Addr: 0x00-0x08					
Bit	**Bit Name**	**Access**	**Addr**	**Default**	**Description**
7:0	PWMO	OTP/REG	0x00	00000000	Output duty cycle lookup table. Default is linear mode.
			0x01	00011111	
			0x02	00111111	
			0x03	01011111	
			0x04	01111111	
			0x05	10011111	
			0x06	10111111	
			0x07	11011111	
			0x08	11111111	

Register Table 10

Addr: 0x09				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:6	PROG	OTP/REG	00	Indication of OTP flash. 00: not programmed 01: programmed once 10: programmed twice
5:0	PROC	OTP/REG	000000	The project code of design. Default is 000000.

Register Table 11

Addr: 0x0A				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:6	FGRD	OTP/REG	00	FG or RD output selection. 00: FG 01: 1/2fs*FG 10: 2fs*FG 11: RD
5:3	RPMS	OTP/REG	011	Rotor minimum RPM selection. 000: 50 rpm 001: 100 rpm 010: 200 rpm 011: 400 rpm 100: 800 rpm 101: 1600 rpm 110: 3200 rpm
2:0	SUCL	OTP/REG	100	Start-up current limit. Default is 1360mA. 000: 510mA 111: 2000mA 210mA/step.

Register Table 12

Addr: 0x0B				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7	FG	REG	0	FG signal indication bit (read only).
6	TM	REG	0	Test mode indication (read only). In test mode, turn on all functions except for the OTP flash block. When in POR, if PWM is negative, enter test mode. The TM bit is set to 1. Recycle the power to clear test mode and the TM bit. 0: normal operation 1: test mode
5	HLL_CALI	OTP/REG	0	Hall period calibration enable. 1: enable 0: disable
4:0	SON_12P5	OTP/REG	11111	The electrical angle to turn on the phase transition softly at 12.5% PWM output duty. Default is 11111. 00000: 1.4° 11111: 45°

Register Table 13

Addr: 0x0C				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:5	Reserved			
4:0	SON_100	OTP/REG	10000	The electrical angle to turn on the phase transition softly at 100% PWM output duty. Default is 23.9°. 00000: 1.4° 11111: 45°

Register Table 14

Addr: 0x0D				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7	Reserved			
6	SOFTEN	OTP/REG	1	Soft switching function enable bit. 1: soft function is enabled 0: soft function is disabled
5	RD_HL	OTP/REG	0	RD polarity set when rotor is locked. Default is 0. 0: RD high when locked 1: RD low when locked
4:0	SOFF_12P5	OTP/REG	10000	The electrical angle to turn off the phase transition softly at 12.5% PWM output duty. Default is 23.9°. 00000: 1.4° 11111: 45°

Register Table 15

Addr: 0x0E				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:5	Reserved			
4:0	SOFF_100	OTP/REG	11111	The electrical angle to turn off the phase transition softly at 100% PWM output duty. 00000: 1.4° 11111: 45°

Register Table 16

Addr: 0x0F				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7	Reserved			
6	PLLEN	OTP/REG	1	Load current zero-crossing PLL function enable bit. 1: enable 0: disable
5:4	RLOCK_SEL	OTP/REG	11	Rotor lock off-time to detect time ratio selection. The rotor lock-off timer also determines the OLP retry time. 00: 1:3 (0.6s/1.8s) 01: 1:4 (0.6s/2.4s) 10: 1:5 (0.6s/3.0s) 11: 1:6 (0.6s/3.6s)
3:0	THETA_E	OTP/REG	0000	The electrical angle delay setting bits between the original Hall signal positive edge and output current zero-crossing positive edge. 1° per step. 0000: 0° 1111: 15°

Register Table 17

Addr: 0x10				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:3	Reserved			Write this bit to 00000 during OTP programming.
2	FM	REG	0	Factory mode enable.
1:0	Reserved	REG	00	Write this bit to 00 when not in use.

Register Table 18

Addr: 0x11				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:0				Write 28H to this register first before OTP programming.

Register Table 19-20

Addr: 0x12-0x13				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:0	Reserved			Reserved.

Register Table 21

Addr: 0x14				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:0	DUTY_CORNER	OTP/REG	00000000	Speed corner duty setting point. Output duty cycle keeps the value set by register 00H when the input duty cycle is lower than the duty set by DUTY_CORNER. FFH: 100% 00H: 0%

APPLICATION INFORMATION

Selecting the Input Capacitor

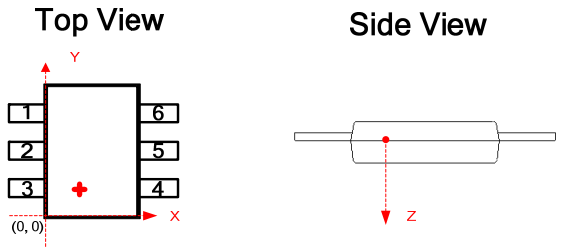
Place an input capacitor (C1) near VCC to keep the input voltage stable and reduce input switching voltage noise and ripple. The input capacitor impedance must be low at the switching frequency. Ceramic capacitors with X7R dielectrics are recommended for their low ESR characteristics. Ensure that the ceramic capacitance is dependent on the voltage rating. The DC bias voltage and value can lose as much as 50% of its capacitance at its rated voltage rating. Leave enough voltage rating margin when selecting the component. For most applications, a 1µF to 10µF ceramic capacitor is sufficient. In some applications, add an additional, large, electrolytic capacitor to absorb inductor energy if needed.

Selecting the PWM Input Resistor

When the input PWM signal rating is >6.5V, which exceeds the PWM voltage rating, a resistor (R2) is needed. The recommended value is 5.1kΩ.

Hall Sensor Position

The Hall sensor cell is located in the lower left corner of the package (see Figure 8).



(X, Y, Z) = (540µm, 508µm, 80µm)
Figure 8: Hall Sensor Position

Input Clamping TVS

To avoid high voltage spikes caused by the energy stored in the motor inductor charges back to the input capacitor side, add a voltage-clamping transient voltage suppressor (TVS) diode. For a 12V case, an 18V/SOD-323 package TVS diode is sufficient. If input connection reserve protection is needed, a unidirectional ZVS diode is recommended (see Section 1 in Figure 9). For small power fans <80mm (<500mA), this is not needed.

Input Snubber

Due to the input capacitor energy charge/discharge during the phase transition soft switching, the input current has switching cycle ringing. If needed, add a 2Ω resistor in series with a 1µF capacitor as an R-C snubber parallel with an input capacitor. This prevents switching cycle ringing efficiently (see Section 2 in Figure 9).

TYPICAL APPLICATION CIRCUIT

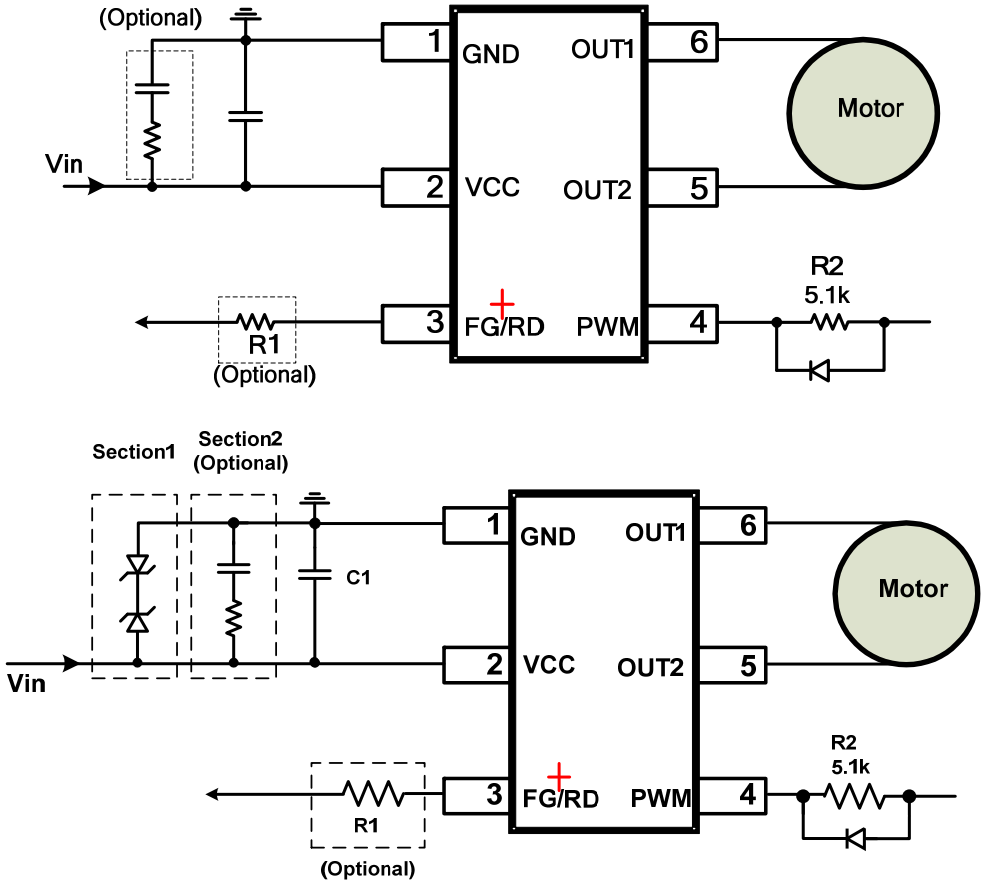
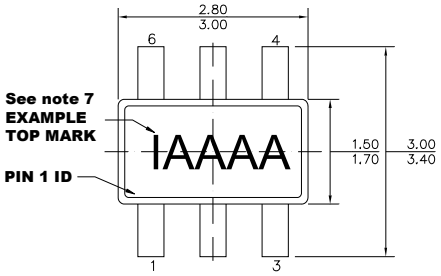


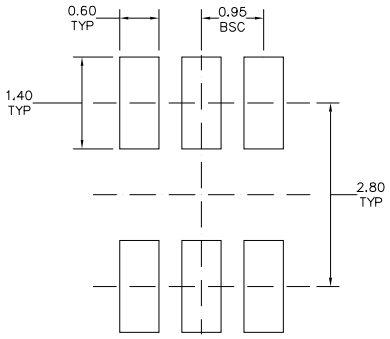
Figure 9: Typical Application Circuit for 12V VCC Input

PACKAGE INFORMATION

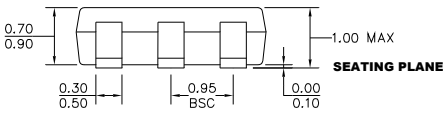
TSOT23-6-L



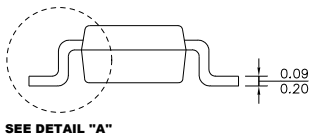
TOP VIEW



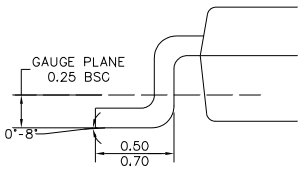
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



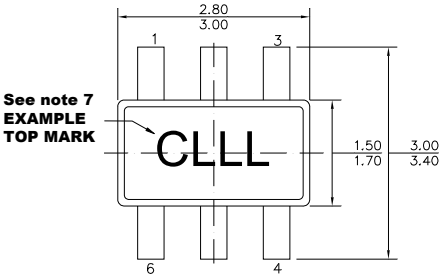
DETAIL "A"

NOTE:

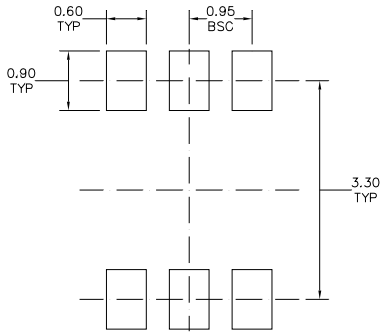
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING REFERENCE TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

PACKAGE INFORMATION *(continued)*

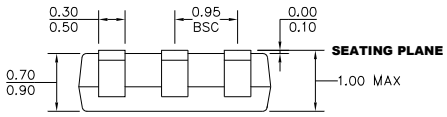
TSOT23-6-R



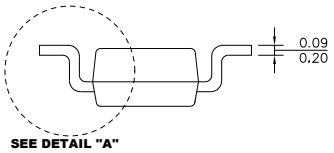
TOP VIEW



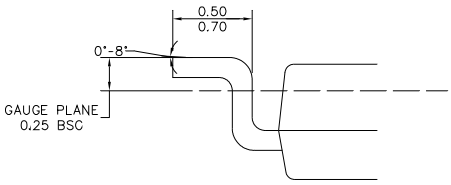
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



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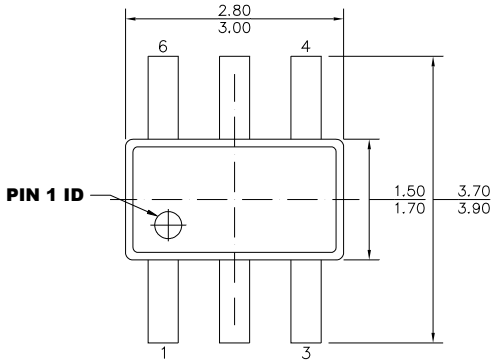
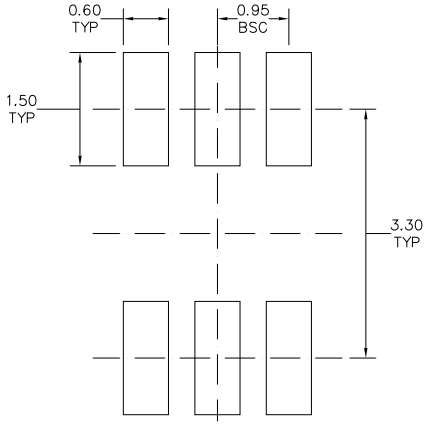
5) DRAWING REFERENCE TO JEDEC MO-193.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS UPPER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

PACKAGE INFORMATION *(continued)*

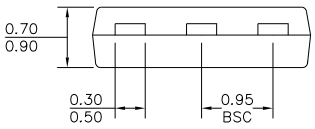
TSOT23-6-SL



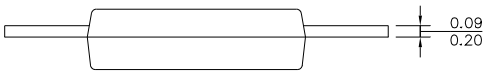
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

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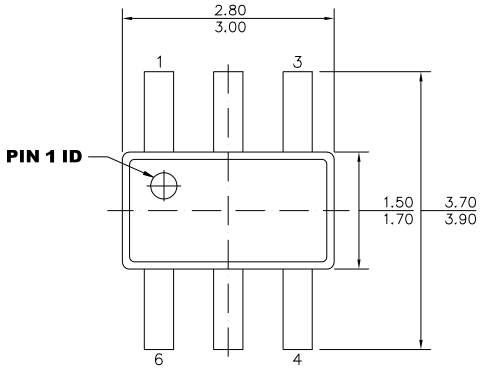
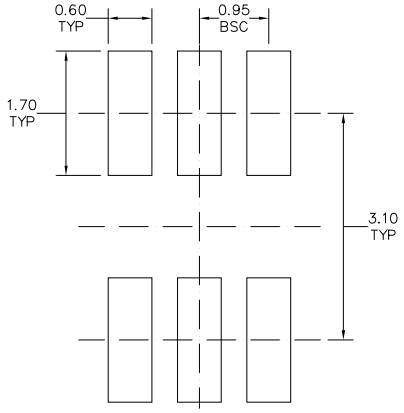
6) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

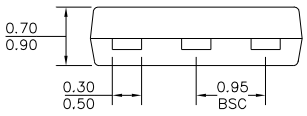
TSOT23-6-RSL



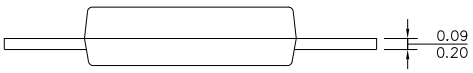
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

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6) DRAWING IS NOT TO SCALE.

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