AT24C128C and AT24C256C

I²C Automotive Temperature Serial EEPROM

128K (16,384 x 8), 256K (32,768 x 8)

DATASHEET

Features

- 2-Wire Serial Interface Compatible with I²C
- Internally Organized 16,384 x 8 (128K), 32,768 x 8 (256K)
- Low-voltage, Medium-voltage and High-voltage Operation
  - Grade 1, V_{CC} = 2.5V to 5.5V
  - Grade 2[1] and 3, V_{CC} = 1.7V to 5.5V
- Extended Temperature Range (Grade 1, 2[1], and 3 as defined in AEC-Q100)
  - Grade 1 Temperature Range: -40°C to 125°C
  - Grade 2 Temperature Range[1]: -40°C to 105°C
  - Grade 3 Temperature Range: -40°C to 85°C
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 400kHz Compatibility
- Write Protect Pin for hardware data protection
- 64 byte Page Write Modes
- Partial Page Writes are Allowed
- Self-timed Write Cycle (5ms max)
- High-reliability
  - Endurance: 1,000,000 Write Cycles
  - Data Retention: 100 Years
- 8-lead JEDEC SOIC, 8-lead TSSOP, and 8-pad UDFN Packages

Note: 1. Contact Sales for Grade 2 Availability

Description

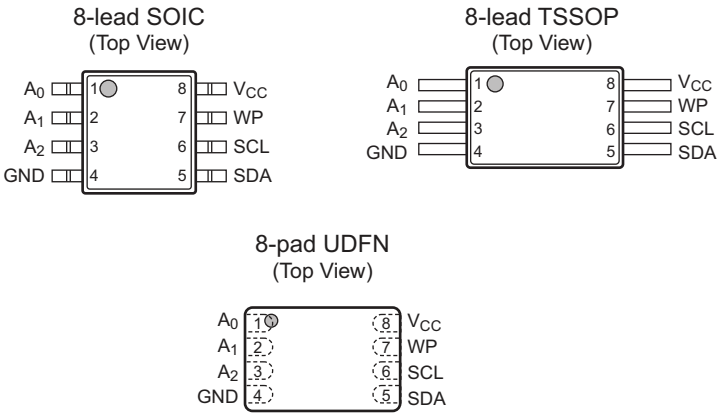
The Atmel® AT24C128C/256C provides 131,072/262,144 bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 16,384/32,768 words of 8 bits each. The device is optimized for use in many automotive applications where low-power and low-voltage operation are essential. AT24C128C/256C is available in space-saving 8-lead JEDEC SOIC, 8-lead TSSOP, and 8-pad UDFN packages and is accessed via a 2-wire serial interface. This device operates from 2.5V to 5.5V for Grade 1 or 1.7V to 5.5V for Grades 2[1] and 3.

Table of Contents

1. Pin Configurations and Pinouts

Figure 1. Pin Configurations

Pin Name	Function
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
A_0 to A_2	Address Inputs
GND	Ground
V_{CC}	Power Supply



Note: Drawings are not to scale.

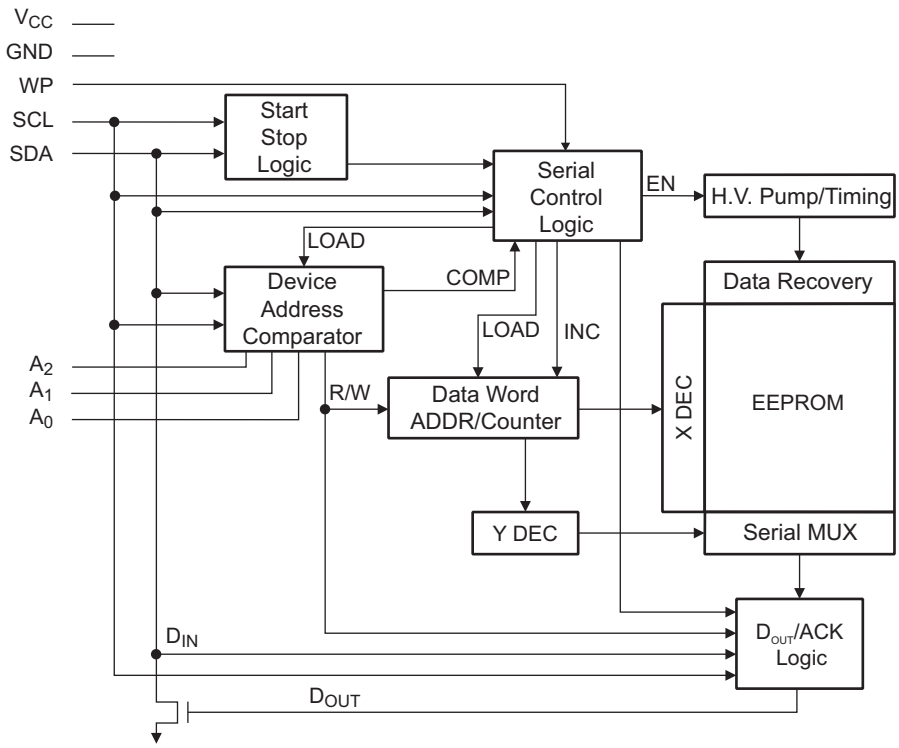
2. Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on any pin with respect to ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0mA

*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3. Block Diagram

Figure 3-1. Block Diagram



4. Pin Description

Serial Clock (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

Serial Data (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

Device Addresses (A_2, A_1, A_0): The A_2, A_1, and A_0 pins are device address inputs that are hardwired or left not connected for hardware compatibility with other Atmel AT24C devices. When the pins are hardwired, as many as eight 128K/256K devices may be addressed on a single bus system (device addressing is discussed in detail in Section 7., Device Addressing). If the pins are left floating, the A_2, A_1, and A_0 pins will be internally pulled down to GND if the capacitive coupling to the circuit board V_{CC} plane is < 3pF. If coupling is > 3pF, Atmel recommends connecting the pin to GND.

Write Protect (WP): AT24C128C/256C has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect pin is connected to V_{CC}, the write protection feature is enabled and operates as shown in the following table.

Table 4-1. Write Protect

WP Pin Status	Part of the Array Protected
At V_{CC}	Full (128K/256K) Array
At GND	Normal Read/Write Operations

5. Memory Organization

AT24C128C/256C, 128K/256KSerial EEPROM: The 128K/256K is internally organized as 256/512 pages of 64 bytes each. Random word addressing requires a 14/15 bit data Word Address.

5.1 Pin Capacitance

Table 5-1. Pin Capacitance[1]

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

5.2 DC Characteristics

Table 5-2. DC Characteristics

Applicable over recommended operating range from: T_{A1} = -40°C to +125°C, V_{CC1} = 2.5V to 5.5V; T_{A2} = -40°C to 105°C, V_{CC2} = 1.7V to 5.5V. (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage	Grade 1		2.5		5.5	V
V_{CC2}		Grade 2[2] and 3		1.7		5.5	
I_{CC}	Supply Current	V_{CC} = 5.0V	Read at 100kHz		0.4	1.0	mA
			Write at 100kHz		2.0	3.0	
I_{SB1}	Standby Current	V_{CC} = 1.7V	V_{IN} = V_{CC} or V_{SS}		0.1	3.0	µA
I_{SB2}		V_{CC} = 2.5V			1.6	4.0	
I_{SB3}		V_{CC} = 5.0V			4.0	6.0	
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}			0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}			0.05	3.0	
V_{IL}	Input Low Level[1]			-0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[1]			V_{CC} x 0.7		V_{CC} + 0.5	
V_{OL1}	Output Low-voltage	V_{CC} = 2.5V	I_{OL} = 3.00mA			0.4	V
V_{OH1}	Output High-voltage		I_{OH} = -1.60mA	V_{CC} – 0.8			
V_{OL2}	Output Low-voltage	V_{CC} = 1.7V	I_{OL} = 0.15mA			0.2	V
V_{OH2}	Output High-voltage		I_{OH} = -100µA	V_{CC} – 0.2			

Notes: 1. V_{IL} min and V_{IH} max are reference only and are not tested.
2. Contact Sales for Grade 2 Availability

5.3 AC Characteristics

Table 5-3. AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +125°C, V_{CC} = +1.7V to +5.5V, CL = 1 TTL Gate and 100pF unless otherwise noted or restricted by grade. Test conditions are listed in Note 3.

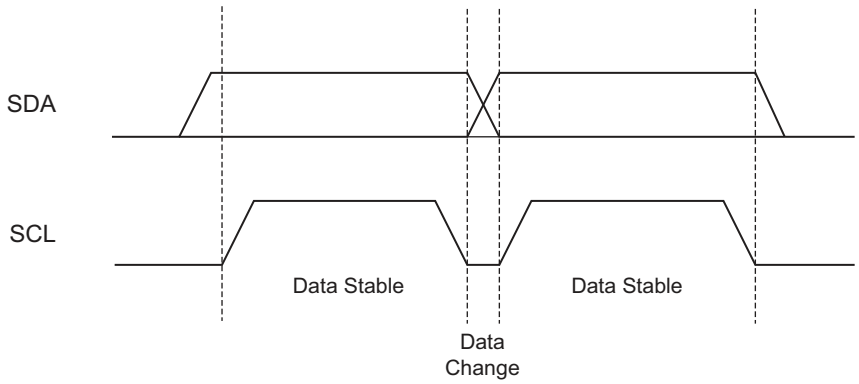
Symbol	Parameter	Min	Max	Units
f_{SCL}	Clock Frequency, SCL		400	kHz
t_{LOW}	Clock Pulse Width Low	1.2		µs
t_{HIGH}	Clock Pulse Width High	0.6		µs
t_I	Noise Suppression Time(1)		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start(2)	1.2		µs
$t_{HD.STA}$	Start Hold Time	0.6		µs
$t_{SU.STA}$	Start Set-up Time	0.6		µs
$t_{HD.DAT}$	Data In Hold Time	0		µs
$t_{SU.DAT}$	Data In Set-up Time	100		ns
t_R	Inputs Rise Time(2)		300	ns
t_F	Inputs Fall Time(2)		300	ns
$t_{SU.STO}$	Stop Set-up Time	0.6		µs
t_{DH}	Data Out Hold Time	50		ns
t_{WR}	Write Cycle Time		5	ms
Endurance(1)	5.0V, 25°C, Page Mode	1,000,000		Write Cycles

Notes:
1. This parameter is characterized and is not 100% tested (T_A = 25°C).
2. This parameter is characterized.
3. AC measurement conditions:
   - RL (connects to V_{CC}): 1.3kΩ (2.5V, 5.5V), 10kΩ (1.7V)
   - Input pulse voltages: 0.3V_{CC} to 0.7V_{CC}
   - Input rise and fall times: ≤ 50ns
   - Input and output timing reference voltages: 0.5 x V_{CC}

6. Device Operation

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a Start or Stop condition as defined below.

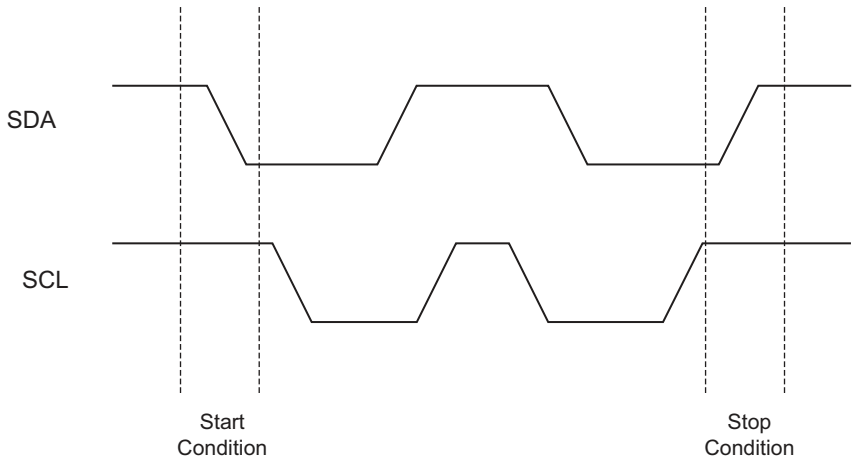
Figure 6-1. Data Validity



Start Condition: A high-to-low transition of SDA with SCL high is a Start condition which must precede any other condition.

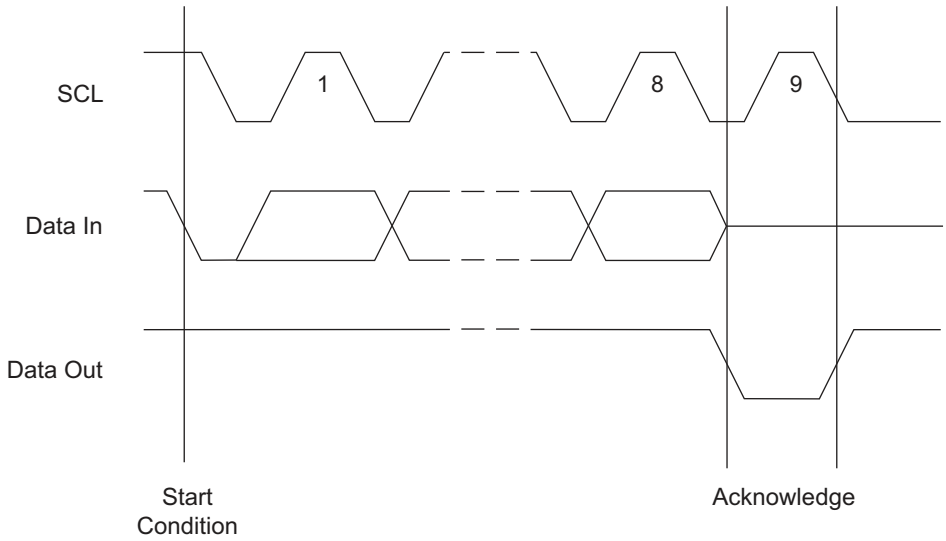
Stop Condition: A low-to-high transition of SDA with SCL high is a Stop condition. After a read sequence, the Stop condition will place the EEPROM in a standby power mode.

Figure 6-2. Start and Stop Definition



Acknowledge: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

Figure 6-3. Output Acknowledge



Standby Mode: The AT24C128C/256C features a low-power standby mode which is enabled:

- Upon power-up.
- After the receipt of the stop bit and the completion of any internal operations.

Memory Reset: After an interruption in protocol, power loss, or system reset, any 2-wire part can be reset by following these steps:

1. Create a Start condition (if possible).
2. Clock nine cycles.
3. Create another Start condition followed by Stop condition as shown in the following figures.

The device should be ready for the next communication after above steps have been completed. In the event that the device is still non-responsive or remains active on the SDA bus, a power cycle must be used to reset the device

Figure 6-4. Memory Reset

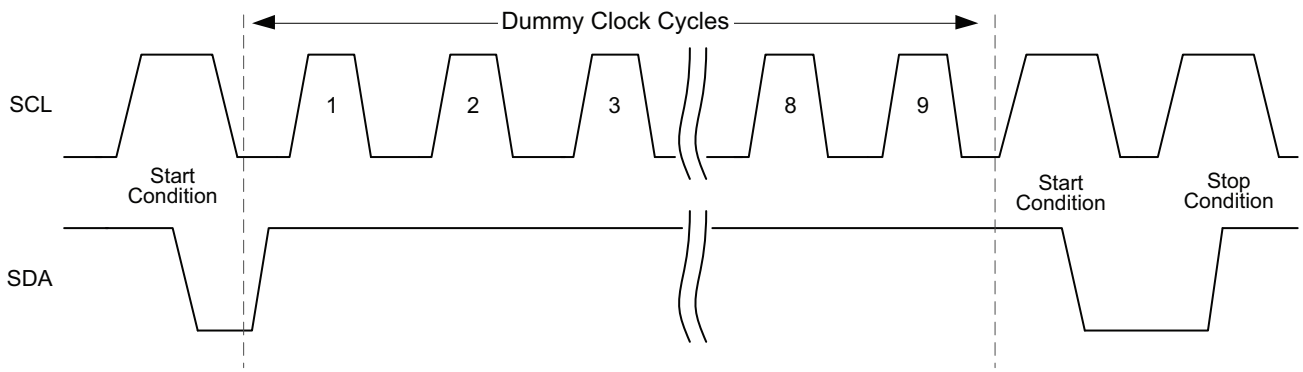


Figure 6-5. Bus Timing

SCL: Serial Clock, SDA: Serial Data I/O

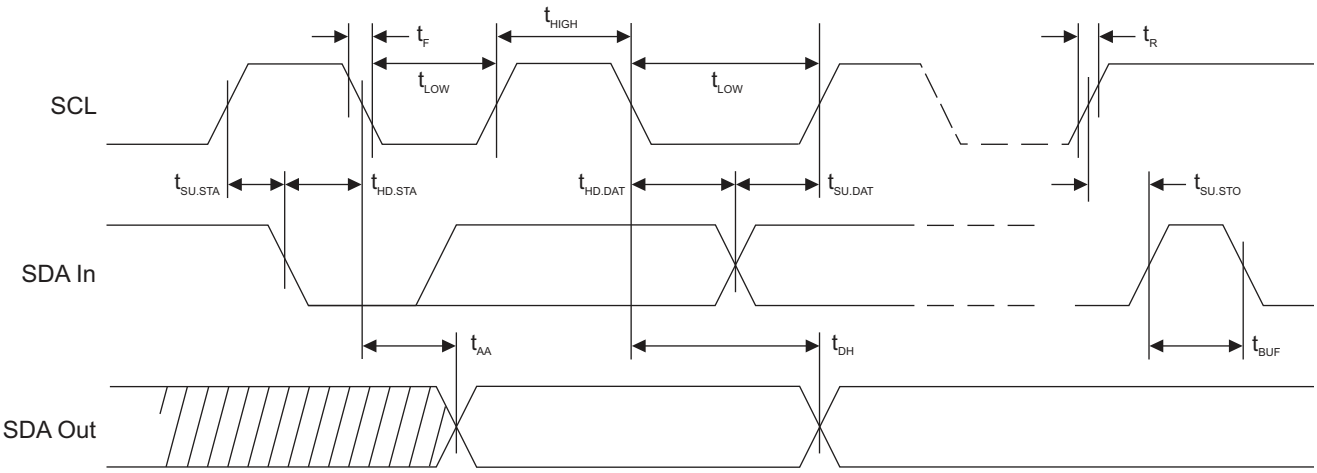
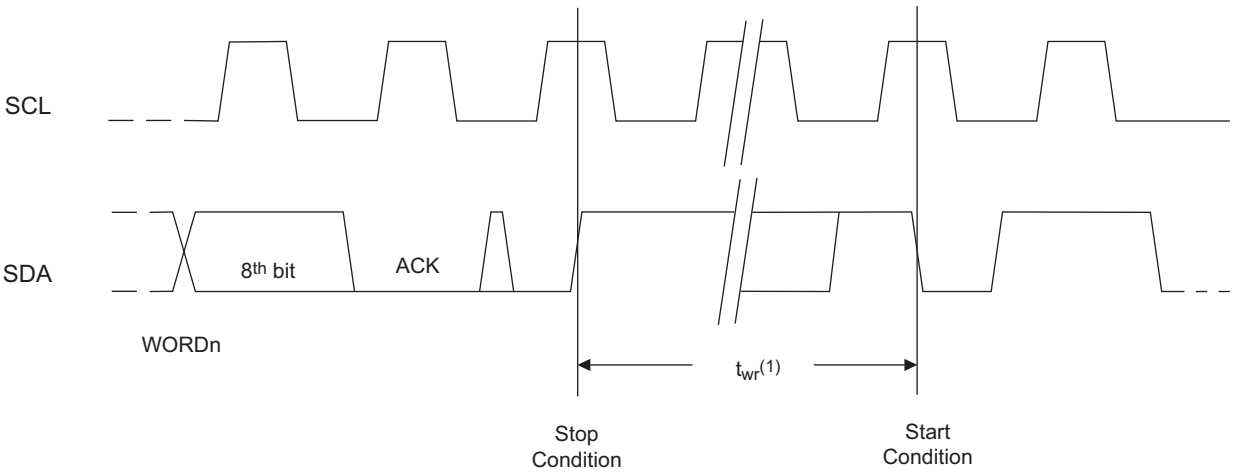


Figure 6-6. Write Cycle Timing

SCL: Serial Clock, SDA: Serial Data I/O



Note: 1. The length of the self timed write cycle, or t_{WR}, is defined as the amount of time from the Stop condition that begins the internal write operation, to the Start condition of the first Device Address byte sent to the device that it subsequently responds to with an ACK.

7. Device Addressing

The 128K/256K EEPROM requires an 8-bit device address word following a start condition to enable the device for a read or write operation.

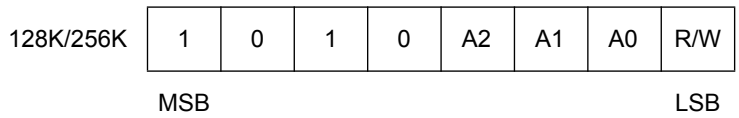
The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

The 128K/256K uses the three device address bits, A_2, A_1, and A_0, to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins. The A_2, A_1, and A_0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the Read/Write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

If the device address meets the requirements listed above, the device will acknowledge with a zero by pulling the SDA signal low. If the comparison is not made, the device will return to a standby state and the SDA signal will float high.

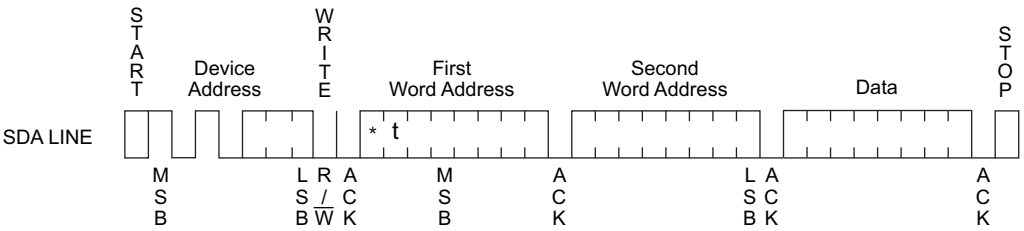
Figure 7-1. Device Address



8. Write Operations

Byte Write: A write operation requires two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this Write Cycle and the EEPROM will not respond until the write is complete.

Figure 8-1. Byte Write



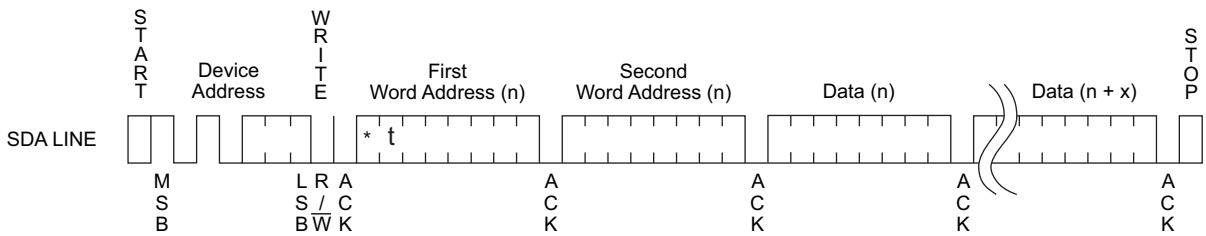
Notes: 1. * = Don't care bit.
2. t = Don't care bit for AT24C128C.

Page Write: The 128K/256K EEPROM is capable of 64 byte page writes.

A Page Write is initiated the same as a Byte Write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to sixty-three more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the Page Write sequence with a stop condition.

The data Word Address lower six bits are internally incremented following the receipt of each data word. The higher data Word Address bits are not incremented, retaining the memory page row location. When the Word Address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than thirty-one data words are transmitted to the EEPROM, the data Word Address will roll-over and previous data will be overwritten.

Figure 8-2. Page Write



Notes: 1. * = Don't care bit.
2. t = Don't care bit for AT24C128C.

Acknowledge Polling: Once the internally timed write cycle has started and the EEPROM inputs are disabled, Acknowledge Polling can be initiated. This involves sending a start condition followed by the device address word. The Read/Write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero, allowing the read or write sequence to continue.

9. Read Operations

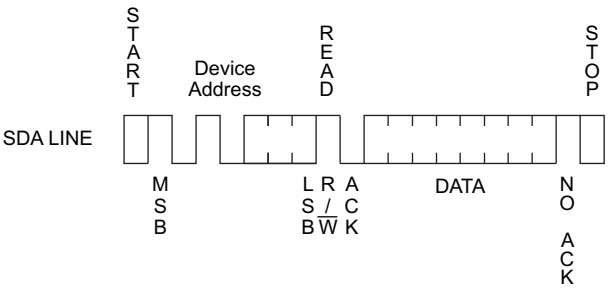
Read operations are initiated the same way as write operations with the exception that the Read/Write select bit in the device address word is set to one. There are three read operations:

- Current Address Read
- Random Address Read
- Sequential Read

Current Address Read: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the device power is maintained. The address roll-over during read is from the last byte of the last memory page to the first byte of the first page. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

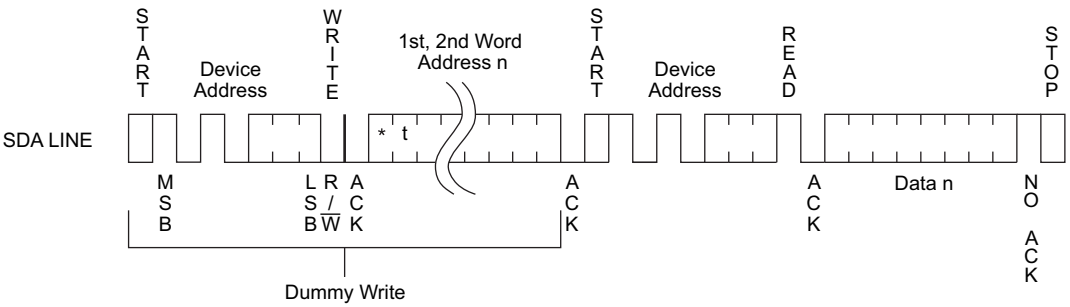
Once the device address with the Read/Write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following Stop condition.

Figure 9-1. Current Address Read



Random Read: A Random Read requires a dummy Byte Write sequence to load in the data Word Address. Once the device address word and data Word Address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the Read/Write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition.

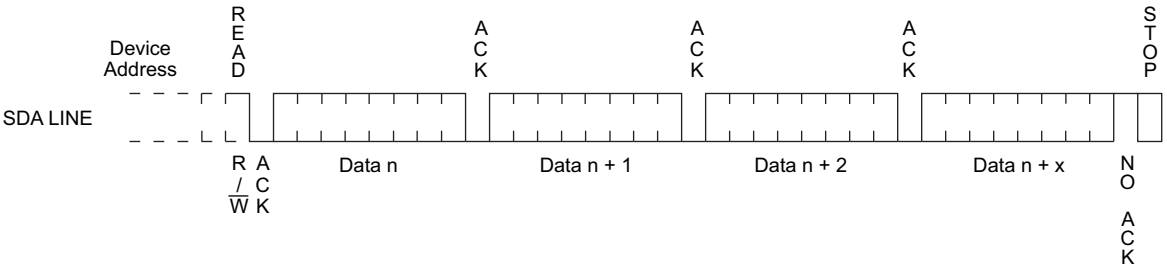
Figure 9-2. Random Read



Notes: 1. * = Don't care bit.
2. t = Don't care bit for AT24C128C.

Sequential Read: Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data Word Address and serially clock out sequential data words. When the memory address limit is reached, the data Word Address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not send an acknowledge (pull the SDA signal low), but does generate the Stop condition.

Figure 9-3. Sequential Read

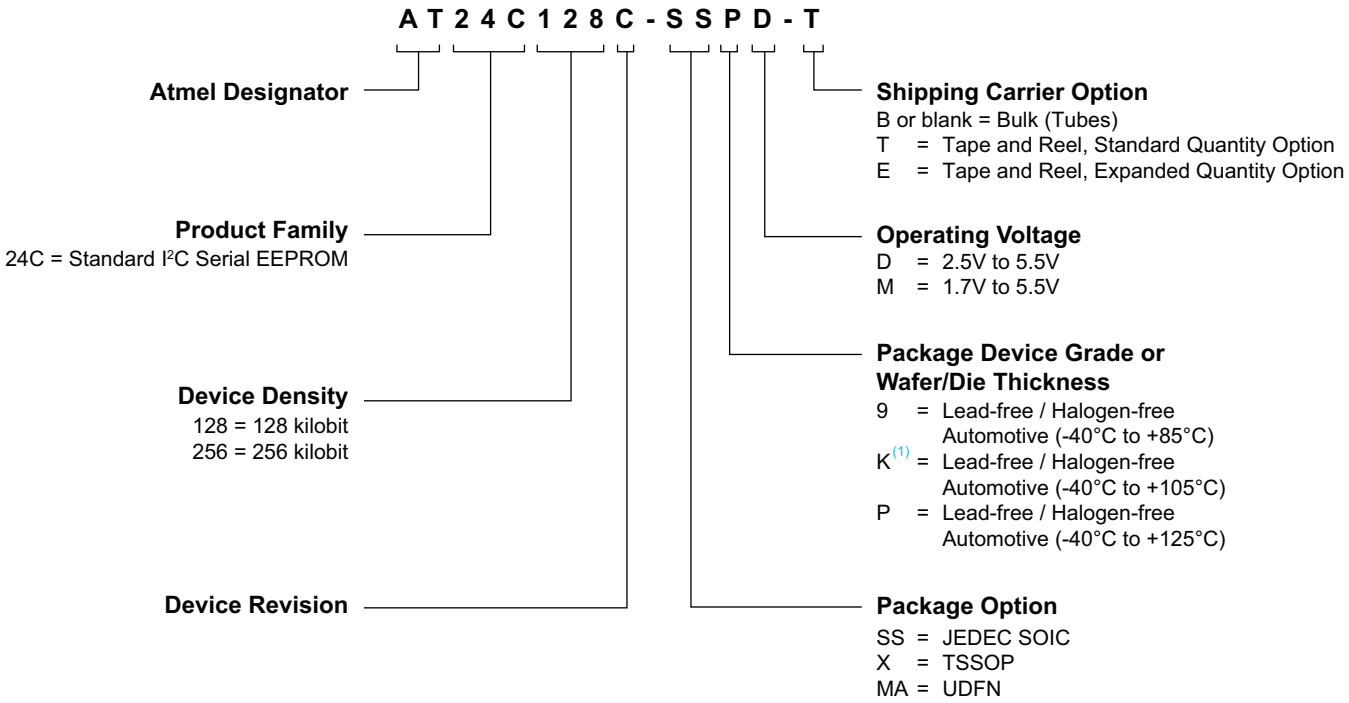


9.1 Power Recommendation

The device internal POR (Power-On Reset) threshold is just below the minimum operating voltage of the device. Power shall rise monotonically from 0.0Vdc to full V_{CC} in less than 1ms. Hold at full V_{CC} for at least 100µs before the first operation. Power shall drop from full V_{CC} to 0.0Vdc in less than 1ms. Power dropping to a non-zero level and then slowly going to zero is *not* recommended. Power shall remain off (0.0Vdc) for 0.5s minimum. Please consult Atmel if your power conditions do not meet the above recommendations.

10. Ordering Information

10.1 Ordering Code Details



Notes: 1. Contact Sales for Grade 2 Availability

10.2 Ordering Code Information

10.2.1 Automotive Grade 1, V_{CC} = 2.5V to 5.5V

Atmel Ordering Code	Lead Finish	Package	Delivery Information		Operation Range
			Form	Quantity	
AT24C128C-SSPD	NiPdAu (Lead-free/Halogen-free)	8S1	Bulk (Tubes)	100 per Tube	Automotive Temperature (-40°C to 125°C)
AT24C128C-SSPD-T			Tape and Reel	4,000 per Reel	
AT24C128C-XPD		8X	Bulk (Tubes)	100 per Tube	
AT24C128C-XPD-T			Tape and Reel	5,000 per Reel	
AT24C128C-MAPD-T		8MA2	Tape and Reel	5,000 per Reel	
AT24C128C-MAPD-E				15,000 per Reel	
AT24C256C-SSPD	NiPdAu (Lead-free/Halogen-free)	8S1	Bulk (Tubes)	100 per Tube	Automotive Temperature (-40°C to 125°C)
AT24C256C-SSPD-T			Tape and Reel	4,000 per Reel	
AT24C256C-XPD		8X	Bulk (Tubes)	100 per Tube	
AT24C256C-XPD-T			Tape and Reel	5,000 per Reel	
AT24C256C-MAPD-T		8MA2	Tape and Reel	5,000 per Reel	
AT24C256C-MAPD-E				15,000 per Reel	

Package Type	
8S1	8-lead, 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8X	8-lead 4.4mm body, Plastic Thin Shrink Small Outline (TSSOP)
8MA2	8-pad, 2.00mm x 3.00mm body, 0.50mm pitch, Ultra Thin, Dual No Lead (UDFN)

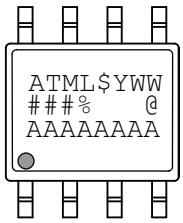
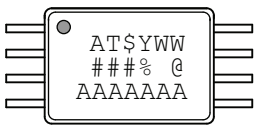
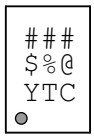
10.2.2 Automotive Grade 3, V_{CC} = 1.7V to 5.5V

Atmel Ordering Code	Lead Finish	Package	Form	Quantity	Operation Range
AT24C128C-SS9M	NiPdAu (Lead-free/Halogen-free)	8S1	Bulk (Tubes)	100 per Tube	Automotive Temperature (-40°C to 85°C)
AT24C128C-SS9M-T			Tape and Reel	4,000 per Reel	
AT24C128C-X9M		8X	Bulk (Tubes)	100 per Tube	
AT24C128C-X9M-T			Tape and Reel	5,000 per Reel	
AT24C128C-MA9M-T		8MA2	Tape and Reel	5,000 per Reel	
AT24C128C-MA9M-E				15,000 per Reel	
AT24C256C-SS9M	NiPdAu (Lead-free/Halogen-free)	8S1	Bulk (Tubes)	100 per Tube	Automotive Temperature (-40°C to 85°C)
AT24C256C-SS9M-T			Tape and Reel	4,000 per Reel	
AT24C256C-X9M		8X	Bulk (Tubes)	100 per Tube	
AT24C256C-X9M-T			Tape and Reel	5,000 per Reel	
AT24C256C-MA9M-T		8MA2	Tape and Reel	5,000 per Reel	
AT24C256C-MA9M-E				15,000 per Reel	

Package Type	
8S1	8-lead, 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8X	8-lead 4.4mm body, Plastic Thin Shrink Small Outline (TSSOP)
8MA2	8-pad, 2.00mm x 3.00mm body, 0.50mm pitch, Ultra Thin, Dual No Lead (UDFN)

10.3 Product Markings

AT24C128C and AT24C256C: Package Marking Information

8-lead SOIC	8-lead TSSOP	8-pad UDFN
		2.0 x 3.0 mm Body 

Note 1: ● *designates pin 1*

Note 2: Package drawings are not to scale

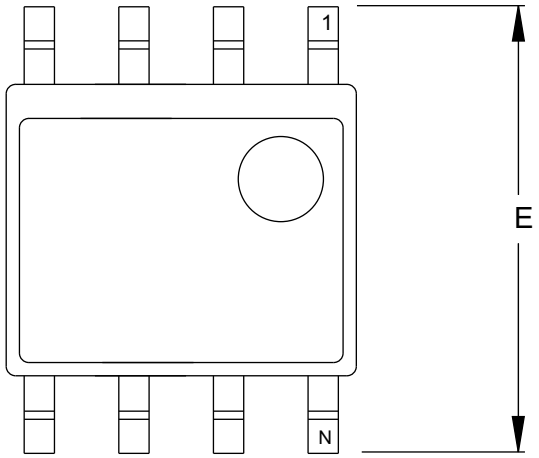
Catalog Number Truncation			
AT24C128C		Truncation Code ###: 2DC	
AT24C256C		Truncation Code ###: 2EC	
Date Codes			**% = Voltages**
Y = Year	M = Month	WW = Work Week of Assembly	D: 2.5V minimum
6: 2016 0: 2020	A: January	02: Week 2	M: 1.7V minimum
7: 2017 1: 2021	B: February	04: Week 4	
8: 2018 2: 2022	...	...	
9: 2019 3: 2023	L: December	52: Week 52	
Country of Assembly	**Lot Number**		**$ = Grade/Lead Finish Material**
@ = Country of Assembly	AAA...A = Atmel Wafer Lot Number		P: Automotive Grade 1/NiPdAu K: Automotive Grade 2/NiPdAu 9: Automotive Grade 3/NiPdAu
Trace Code			**Atmel Truncation**
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ			AT: Atmel ATM: Atmel ATML: Atmel

3/14/2016

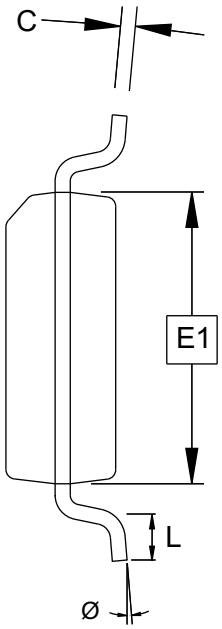
Atmel Package Mark Contact: DL-CSO-Assy_eng@atmel.com	TITLE	DRAWING NO.	REV.
	24C128-256CAM, AT24C128C and AT24C256C Automotive Package Marking Information	24C128-256CAM	C

11. Packaging Information

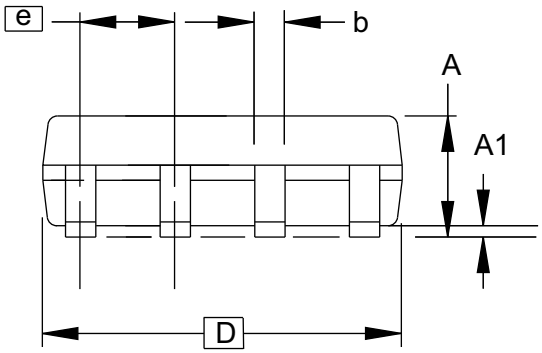
11.1 8S1 — 8-lead JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

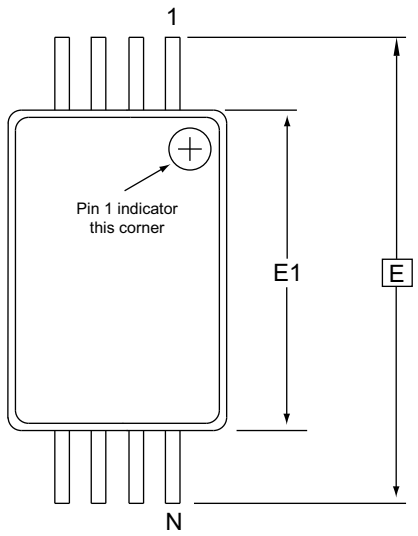
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D		4.90 BSC		
E		6.00 BSC		
E1		3.90 BSC		
e		1.27 BSC		
L	0.40	–	1.27	
Ø	0°	–	8°	

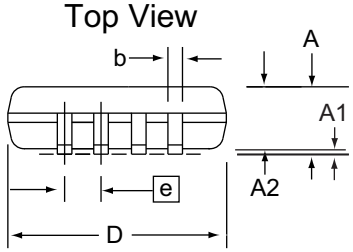
3/6/2015

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**GPC** SWB	**DRAWING NO.** 8S1	**REV.** H

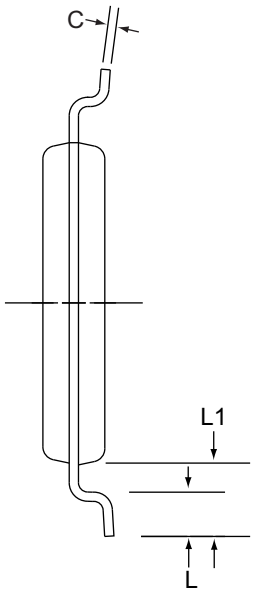
11.2 8X — 8-lead TSSOP



Top View



Side View



End View

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

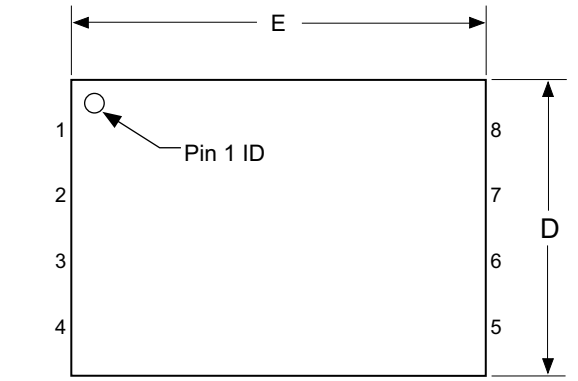
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.20	
A1	0.05	-	0.15	
A2	0.80	1.00	1.05	
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
b	0.19	0.25	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		
C	0.09	-	0.20	

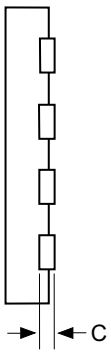
2/27/14

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 8X, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	GPC TNR	DRAWING NO. 8X	REV. E

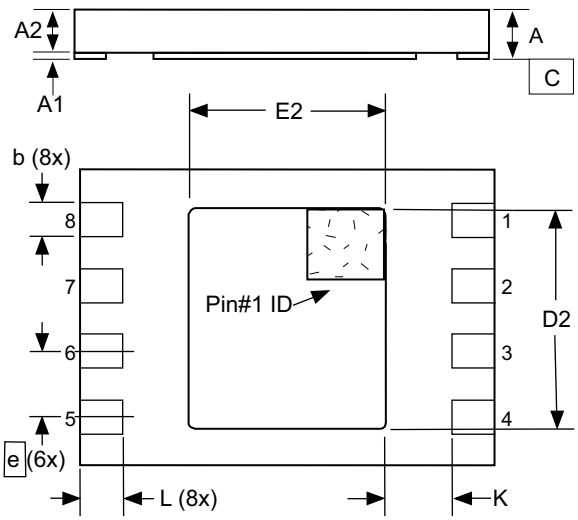
11.3 8MA2 — 8-pad UDFN



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Notes:
1. This drawing is for general information only. Refer to Drawing MO-229, for proper dimensions, tolerances, datums, etc.
2. The Pin #1 ID is a laser-marked feature on Top View.
3. Dimensions b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.
4. The Pin #1 ID on the Bottom View is an orientation feature on the thermal pad.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.50	0.55	0.60	
A1	0.0	0.02	0.05	
A2	-	-	0.55	
D	1.90	2.00	2.10	
D2	1.40	1.50	1.60	
E	2.90	3.00	3.10	
E2	1.20	1.30	1.40	
b	0.18	0.25	0.30	3
C	0.152 REF			
L	0.35	0.40	0.45	
e	0.50 BSC			
K	0.20	-	-	

11/2/15

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 8MA2, 8-pad 2 x 3 x 0.6mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat No-Lead Package (UDFN)	GPC YNZ	DRAWING NO. 8MA2	REV. H

12. Revision History

Doc. Rev.	Date	Comments
8818C	07/2016	Added the Automotive Grade 2 and 3 and UDFN options and table of contents Updated the “Software Reset” section, part marking, 8S1 package drawing, disclaimer page, template and reorganize document.
8818B	10/2012	Removed preliminary status. Updated 8X — TSSOP package drawing and Atmel logos and disclaimer/copy page.
8818A	04/2012	Initial document release

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