

1. Scope

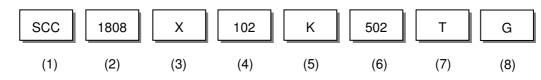
The SCC series X2, X1/Y2 safety capacitors are designed specifically for use in modem, facsimile,

telephone and other electronic equipment.

These parts are compliant to EN60384-14, IEC60384-14, UL60384-14, CSA 60384-1 & CSA 60384-14.

(This product compliant with the RoHS & HF and Pb free.)

2. Parts Number Code



(1)Product

Product Code	
SCC	Safety Approval of MLCC Product

(2)Chip Size

Code	Length×Width	unit : mm(inch)
1808	4.60× 2.00	(.18× .08)
1812	4.60× 3.20	(.18× .12)
2208	5.70× 2.00	(.22× .08)
2211	5.70× 2.80	(.22× .11)
2220	5.70× 5.00	(.22× .20)
2825	7.10× 6.35	(.28× .25)

(3) Temperature Characteristics

Code	Temperature	Temperature	Temperature
	Characteristic	Range	Coefficient
N	NPO	-55°C ~+125°C	30 ppm/° C
Х	X7R	-55℃~+125℃	± 15%

(5)Capacitance Tolerance

Code	Tolerance	Nominal Capacitance
С	± 0.25 pF	Less Than 10 pF
D	± 0.50 pF	(Include 10 pF)
E	± 1.00 pF	_
J	± 5.00 %	More Than 10 pF
К	± 10.0 %	_
М	± 20.0 %	
Q	+10%~+20%	_

(6) Class Level of Capacitors

Code	Class
202	X2
252	X2 (305Vac)
502	X1/Y2
602	X1/Y2 for
	SCC2208N,SCC2211N,SCC2220N Series

(4)	Ca	pac	itaı	nce

(4)Capacitance	unit :pico farads(pF)				
Code	Nominal Capacitance (pF)				
5R0	5.0				
330	33.0				
151	150.0				
102	1,000.0				
103	10,000.0				

X. *If there is a decimal point, it shall be expressed by an* English capital letter R

(7)Tapping

Code	Туре
Т	Tape & Reel
В	Bulk

(8)Special Requirement Code

Code	Туре	
G	Pb free Type	



3. Nominal Capacitance and Tolerance

3.1 Standard Combination of Nominal Capacitance and Tolerance

Class	Characteristic	Toler	ance	Nominal Capacitance
Class	NPO	Less Then 10 pF C (± 0.25 pF)		0.5,1,1.5,2,2.5,3,3.5,4,4.5,5
Ι			D (± 0.50 pF)	5,6,7,8,9,10
			E (± 1.00 pF)	6,7,8,9,10
		More Than 10 pF	J (± 5.00 %)	E-24 series
			K (± 10.0 %)	
Class II	X7R	K (± 10.0 %),	M (± 20.0 %)	E-12 series

3.2 E series(standard Number)

Standard No.	Application Capacitance											
E- 3	1.0			2.2			4.7					
E- 6	1	.0	1	.5	2	.2	3	.3	4	.7	6	.8
E-12	1.0	1.2	1.5	1.8	2.2	2.7	3.3	3.9	4.7	5.6	6.8	8.2
E-24	1.0	1.2	1.5	1.8	2.2	2.7	3.3	3.9	4.7	5.6	6.8	8.2
	1.1	1.3	1.6	2.0	2.4	3.0	3.6	4.3	5.1	6.2	7.5	9.1

4. Operation Temperature Range

Class	Characteristic	Temperature Range	Reference Temp.
Ι	NPO	-55℃ ~ +125℃	25 ℃
Π	X7R	-55℃ ~ +125℃	25°C

5. Storage Condition

Storage Temperature : 5 to 40 $^\circ\mathrm{C}$

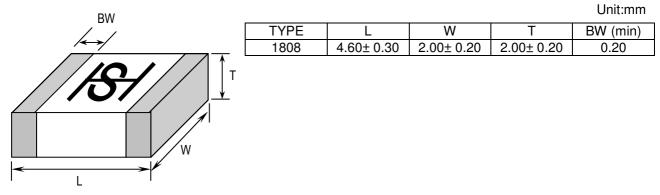
Relative Humidity : 20 to 70 %

Storage Time: 12 months max.

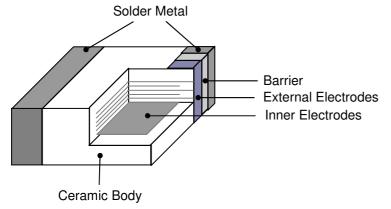


6. Dimensions

6.1 Configuration and Dimension :



6.2 Termination Type :





7. Electronic Nominal Specification

7.1 Safety Standard:

TUV : IEC 60384-14:2013 EN 60384-14:2013 UL :UL 60384-14 CSA 60384-1 & CSA 60384-14

Temperature	Class	Size	Rated	Certificated			•	ince Range	· · ·	
Characteristic	Unace	0.20	Voltage	Certificated		10	10	1 1()2	103
NPO	X2	1808	250 Vrms	TUV/UL	2				1000	
X7R	X2	1808	250 Vrms	TUV/UL			150		2200	
X7R	X2	1812	250 Vrms	TUV/UL			3	30	470	00
X7R	X2	2220	250 Vrms	TUV/UL			150			33000
X7R	X2	2825	250 Vrms	UL				47	/000	5600
NPO	X1/Y2	1808	250 Vrms	TUV/UL	2			330		
X7R	X1/Y2	1808	250 Vrms	TUV/UL			150		1000	
NPO	X1/Y2	1812	250 Vrms	TUV/UL	2			68	0	
X7R	X1/Y2	1812	250 Vrms	TUV/UL			130		1000	
NPO	X1/Y2	2208	250 Vrms	TUV/UL	2			330		
X7R	X1/Y2	2208	250 Vrms	TUV/UL		c	36		1000	
NPO	X1/Y2	2211	250 Vrms	TUV/UL	2			Γ	1000	
X7R	X1/Y2	2211	250 Vrms	TUV/UL			68		2700	
NPO	X1/Y2	2220	250 Vrms	TUV/UL	2				1200	
X7R	X1/Y2	2220	250 Vrms	TUV/UL			100		470	0
X7R	X2	2220	305 Vrms	TUV/UL			150			33000



8. Performance

No.	Ite	m	Spe	cification	Test Condition				
1	Visi	ual	No abnormal exter	rior appearance	Visual Inspection				
2	Dimer	nsion	See Page 3 / Item	6.	Visual Inspection				
3	Capac	itance	Within the specifi	ed tolerance	Char. Frequency Voltage				
4	Q a Dissipatio		More than $30pF : Q \ge 1000$ $30pF \& below: Q \ge 400 + 20C$ (C:pF) Class II (X7R) Maximum : 2.5% (0.025)		$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
5	Insula Resist		Minimum 10,000M	Ω	and placement room temperature for 24±2hr. Applied Voltage: Applied Voltage:500V Charge Time : 60sec.				
6	Voltage		breakdown				Proof No dielectric breakdown or mechanical Applied Voltage: breakdown Y Capacitor :Applied Voltage Y Capacitor :Applied Voltage For 1min. Voltage ramp up rate ≤ 150		Applied Voltage: X Capacitor :Applied Voltage 1075Vdc(4.3Ur) Y Capacitor :Applied Voltage 1500Vac
7	7 Solderability		More than 90% of the terminal surface is to be soldered newly, so metal part does not come out or dissolve		Solder Temperature : $245\pm5^{\circ}$ C Dip Time : 5 ± 0.5 sec. Immersing Speed : $25\pm10\%$ mm/s Solder : Lead Free Solder Flux :Rosin Preheat : At 80~120 °C For 10~30sec.				
8	Resistance	Appear-	No mechanical da	mage shall occur.	Bending shall be applied to the 1.0 mm with				
	to Flexure	ance Capacit-	Characteristic	Cap. Change	1.0 mm/sec. ■ R340				
	of Substrate	ance	Class I (NPO)	≤ ± 5.0% of initial value	C Meter				
			Class II (X7R)	≤ ± 12.5% of initial value	$ - \underbrace{ $				
		Q / tan δ	To satisfy the spec						
		Resistance			Solder the capacitor on P.C. board shown in Fig 1. before testing.				
		Voltage Proof	To satisfy the spec	sified initial value					
9	Robustness of Shear	Appear- ance Capacit-	No indication of peeling shall occur on the terminal electrode. Characteristic Cap. Change		Pull force shall be applied for 10± 1 second. ≦06035N(≒ 0.5 Kg·f) >060310N(≒1.0 Kg·f)				
		ance	Class I (NPO)	≤ ± 5.0% of initial value	N·f				
			Class II (X7R)	≤ ± 12.5% of initial value					
		Q / tan δ	To Satisfy The Spe		Colder the concelter on D.C. he and shows it				
		Insulation Resistance			Solder the capacitor on P.C. board shown in Fig 1. before testing.				
		Voltage Proof	To Satisfy The Spe	ecified Initial Value					



No.	lte	em	Spe	ecification	Test Condition		
10	Resistance To	Appear- ance	No mechanical d	amage shall occur.	Class II capacitor shall be set for 48±4 hours at room temperature after one hour heat		
	Soldering	Capacit-	Characteristic	Cap. Change	treatment at 150 +0/-10 $^{\circ}$ C before initial		
	Heat	ance	Class I (NPO)	$\leq \pm 10\%$ of initial	measure.		
				value	Preheat : At 150± 10℃ For 60~120sec.		
			Class II (X7R)	$\leq \pm 20\%$ of initial	Dip : Solder Temperature of 260±5°C		
		0 / T a a S	To contract the contract	value	Dip Time : 10 ± 1sec. Flux :Rosin		
		Q / Tan δ	To satisfy the spe	ecified initial value	Measure at room temp. after cooling for:		
		Insulation Resistance	More than 1,000	ΩM	Class I : 24 ± 2 Hours Class II : 48 ± 4 Hours		
		Voltage Proof	To Satisfy The Sp	pecified Initial Value			
11	Damp Heat		No mechanical d	amage shall occur.	Test Condition :		
		ance		1	Temperature : 40°C		
	-	Capacit-	Characteristic	Cap. Change	Humidity : 95 %RH		
	State	ance	Class I (NPO)	$\leq \pm 15\%$ of initial	Test Time : 500hr (21days)		
			Class II (X7R)	value ≤ ± 15% of initial	The capacitors with rated voltage(250Vac) applied.		
				value	Measure at room temp. after cooling for:		
		Q	More Than 30pF		Class I :24 ± 2 Hrs		
		Class I	30pF & Below:Q (C:pF)	≧ 275+2.5× C	Class II :48 ± 4 Hrs		
		Tan δ Class II	Maximum 5.0%		Solder The Capacitor On P.C. Board Shown In Fig 2. Before Testing.		
		Insulation	More Than 1,000	ΜΩ			
		Resistance					
		Voltage Proof	To Satisfy The Sp	pecified Initial Value			
12	Endurance	Appear-	No Mechanical	Damage Shall Be	Impulse Voltage		
		ance	Occur		Each individual capacitor shall be subjected		
		Capacit-	Characteristic	Cap. Change	to a 2.5KV(X2) and 5KV(X1/Y2) impulse for three times. Then the capacitors are applied		
		ance	Class I (NPO)	$\leq \pm 20\%$ of initial	to life test.		
			Class II (X7R)	value ≤ ± 20% of initial	(%) Front time T ₁ =1.2µs=1.67T		
				value	100 Time to half-value $T_2=50\mu s$		
		Q	More Than 30pF		90		
		Class I	30pF & Below:Q				
		Tan δ	Maximum 5.0%		50		
		Class II			30		
			Minimum 1,000M	Ω			
		Resistance	To potiofy the one	ecified initial value			
		Voltage Proof	TO Salisty the spe		t t		
		11001					
					Temperature : 125℃		
					Test Time : 1000hrs		
					Applied Voltage :		
					Class X Capacitors :1.25Ur (312.5Vac)		
					Class Y Capacitors :1.70Ur (425Vac)		
					Except that once every hour the voltage shall be increased to 1000Vrms for 0.1s.		
					Shall be increased to 1000 vrms for 0.1S.		
					Additional impulse 2.5KV of Y3 for EN60950 standard.		

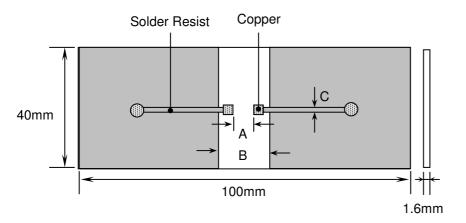


No. Item Specification	Test Condition
13 Passive Flammability Capacitor didn't burnt at a	Ill Volume Sample : 21.56mm ³ Flame exposure time : 5 sec.Max.
14 Active The cheese cloth shall no Flammability a flame	t burn with The capacitors of class each test capacitors applied Ur(250Vac). Then each sample shall be subjected to 20 discharges from a tank capacitor, charge to a voltage that, when discharged, places Ui(2500V) across the capacitor under test. The interval between successive discharges shall be 5s.



Fig.1

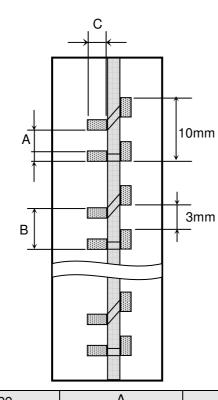
P.C. Board for Bending Strength Test



(referring to IEC384-14 and EN132400)

Material : Glass Epoxy Substrate : Copper (Thickness : 0.035mm) : Solder Resist

Fig.2 Test Substrate



Material : Glass Epoxy Substrate : Copper (Thickness : 0.035mm) : Solder Resist

Thickness : 1.6 mm

Unit:mm

Туре	А	В	С
1206	2.2	5.0	2.0
1808	3.5	7.0	2.5
1812	3.5	7.0	3.7
2208	4.5	8.0	2.5
2211	4.5	8.0	3.0
2220	4.5	8.0	5.6

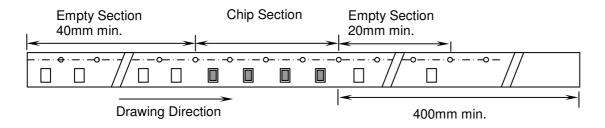


9. Packing

9.1 Bulk Packing

According to customer request.

9.2 Chip Capacitors Tape Packing



9.3 Material And Quantity

Tape		1206	
Material	T≦0.90mm	$0.90mm < T \le 1.25mm$	T>1.25mm
Plastic	4,000 pcs/Reel	3,000 pcs/Reel	2,000 pcs/Reel

Tape	18	08	1812/2208/2211/2220		
Material	$0.9mm < T \leq 1.25mm$	1.25 mm $<$ T \leq 2.0 mm	1.25 mm $<$ T \leq 2.2 mm	T>2.2mm	
Plastic	3000 pcs/Reel	2000 pcs/Reel	1000 pcs/Reel	700 pcs/Reel	

Tape	2825
Material	T>2.6mm
Plastic	400 pcs/Reel

9.4 Cover Tape Reel Off Force

9.4.1 Peel-Off Force

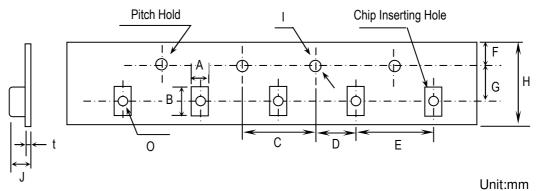
5 g·f \leq Peel-Off Force \leq 70 g·f

9.4.2 Measure Method



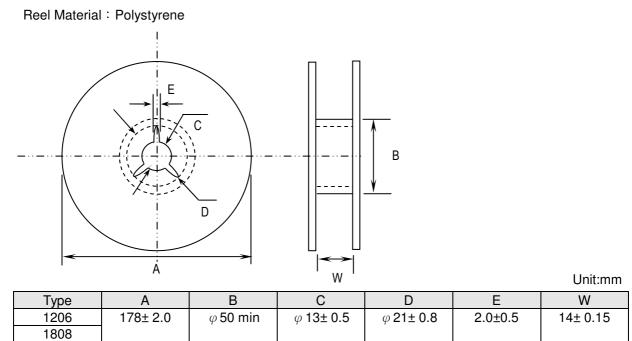


9.5 Plastic Tape



Туре	A	В	С	D	E	F
1206	1.9± 0.2	3.5± 0.2	4.0± 0.1	2.0± 0.05	4.0± 0.1	1.75± 0.1
1808	2.5±0.2	4.9±0.2				
1812	3.6±0.2	4.9±0.2			8.0± 0.1	
2208	2.5±0.2	6.1±0.2				
2211	3.2±0.2	6.1±0.2				
2220	5.4±0.2	6.1±0.2				
2825	6.7±0.2	7.5±0.2			12.0± 0.1	
Туре	G	Н		J	t	0
1206	5.5± 0.05	12.0 ± 0.3	ϕ 1.5+0.1/-0	3.7 max.	0.3 max.	1.0± 0.1
1808						1.5± 0.1
1812						
2208						
2211						
2220						
2825	7.5± 0.10	16.0 ± 0.3			0.35 max.	

9.6 Reel Dimensions





Caution

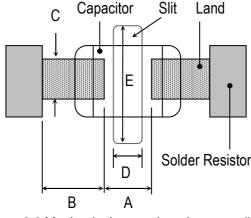
1. Storage

Store the capacitors where the temperature and relative humidity don't exceed 40 °C and 70%RH. We recommend that the capacitors be used within 12 months from the date of manufacturing. Store the products in the original package and do not open the outer wrapped, polyethylene bag, till just before usage. If it is open, seal it as soon as possible or keep it in a desiccant with a desiccation agent.

2. Construction of Board Pattern

Improper circuit layout and pad/land size may cause excessive or not enough solder amount on the PC board. Not enough solder may create weak joint, and excessive solder may increase the potential of mechanical or thermal cracks on the ceramic capacitor. Therefore we recommend the land size to be as shown in the following table:

2.1 Size and recommend land dimensions for reflow soldering.



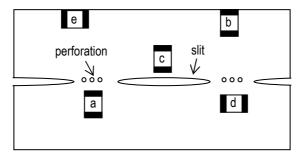
	EIA Code	Chip	(mm)			Land (mm)		
		Γ	W	Α	В	С	D	E
	1808	4.60	2.00	2.8~3.4	1.2~1.4	1.5~1.8	1.0~2.8	3.6~4.1
•	1812	4.60	3.20	2.8~3.4	1.2~1.4	2.3~3.0	1.0~2.8	4.8~5.3
	2208	5.70	2.00	4.0~4.6	1.4~1.6	1.5~1.8	1.0~4.0	3.6~4.1
	2211	5.70	2.80	4.0~4.6	1.4~1.6	2.0~2.6	1.0~4.0	4.4~4.9
	2220	5.70	5.00	4.0~4.6	1.4~1.6	3.5~4.8	1.0~4.0	6.6~7.1
l Ier Resistor								

2.2 Mechanical strength varies according to location of chip capacitors on the P.C. board.

Design layout of components on the PC board such a way to minimize the stress imposed on the components, upon flexure of the boards in depanelization or other processes.

Component layout close to the edge of the board or the "depanelization line" is not recommended.

Susceptibility to stress is in the order of: a>b>c and d>e



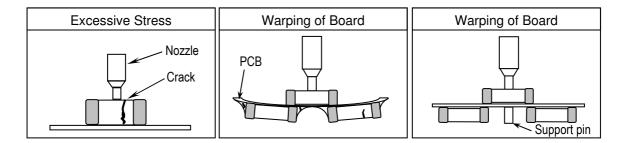


2.3 Layout Recommendation

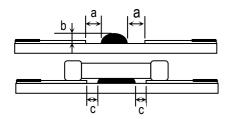
Example	Use of Common Solder Land	Solder With Chassis	Use of Common Solder Land With Other SMD
Need to Avoid	Lead Wire Chip Solder	Chassis \downarrow Excessive Solder \downarrow \downarrow \downarrow \downarrow \downarrow \downarrow \downarrow \downarrow \downarrow \downarrow	Solder Land
Recommendation	Lead Wire Chip Solder Resist Adhesive PCB Solder Land	Solder Resist	Solder Land

3. Mounting

3.1 Sometimes Crack is caused by the impact load due to suction nozzle in pick and place operation. In pick and place operation, if the low dead point is too low, excessive stress is applied to component. This may cause cracks in the ceramic capacitor, therefore it is required to move low dead point of a suction nozzle to the higher level to minimize the board warp age and stress on the components. Nozzle pressure is typically adjusted to 1N to 3N (static load) during the pick and place operation.



3.2 Amount of Adhesive



Example : 0805 & 1206

а	0.2mm min.
b	70 ~ 100 µm
C	Do not touch the solder land

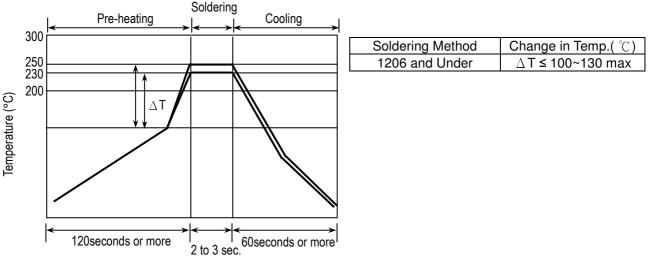


4. Soldering

4.1. Wave Soldering

Most of components are wave soldered with solder at 230 to 250 ℃. Adequate care must be taken to prevent the potential of thermal cracks on the ceramic capacitors. Refer to the soldering methods below for optimum soldering benefits.

Recommend flow soldering temperature Profile



When setting preheat temperatures, that recommend as preheat conditions which can pass the following points for PCB.

- 1) Preheat temperature is too low
 - a. Flux flows to easily
 - b. Possibility of thermal cracks
- 2) Preheat temperature is too high
 - a. Flux deteriorates even when oxide film is removed
 - b. Too large a warp in circuit board
 - c. Loss of reliability in chip and other parts

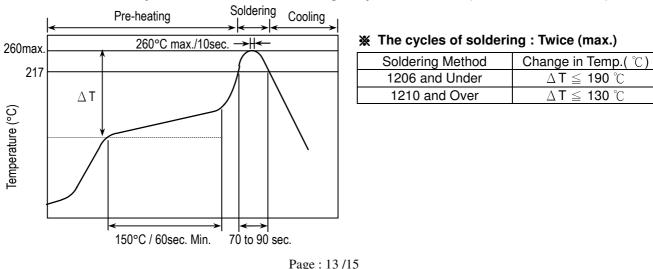
Cooling Condition:

Natural cooling using air is recommended. If the chips are dipped into a solvent for cleaning, the temperature difference (Δ T) must be less than 100°C

4.2 Reflow Soldering

Preheat and gradual increase in temperature to the reflow temperature is recommended to decrease the potential of thermal crack on the components. The recommended heating rate depends on the size of component; however it should not exceed 3°C/Sec.

Recommend reflow profile for Lead-Free soldering temperature Profile (MIL-STD-202G #210F)

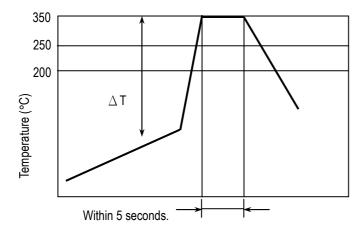


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4.3 Hand Soldering

Sudden heating of the components results in distortion due to a high internal temperature differential, causing cracked chips. When preheating, keep temperature differential Δ T, within the range shown in table. The smaller the Δ T, the less stress on the chip.



Soldering Method	Change in Temp.(°C)
1206 and Under	$\Delta T \leq 150 \ ^{\circ}C$
1210 and Over	∆T ≦ 130 °C

How to Solder Repair by Solder Iron

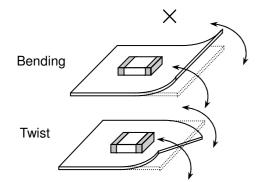
1) Selection of the soldering iron tip

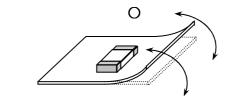
Tip temperature of solder iron various by its type, P.C.board material and solder land size. Higher the tip temperature, quick the operation is .but the heat shock may crack the chip capacitor.

- 2) recommended solder iron condition
 - a.) Preheating Condition : Board and components should be preheated sufficiently at 150 ℃ or over, and soldering should be conducted with soldering iron as boards and components are maintained at sufficient temperatures.
 - b.) Soldering iron power shall not exceed 30 W.
 - c.) Soldering iron tip diameter shall not exceed 3mm.
 - d.) Temperature of iron tip shall not exceed 350 °C and the process should be finished within 5 seconds. (refer to MIL-STD-202G)
 - e.) Do not touch the ceramic dielectric with solder iron other than the terminations. Direct contact of the soldering iron with ceramic dielectric of chip capacitor may cause crack.
 - f.) After soldering ,let the products to cool down gradually in the room temperature.
- ***** The soldering to lose the use of electronic heat gun.

5. Handling after chip mounted

5.1 Please pay attention put the component lateral to the direction in which stress acts.





5.2 Crack will be caused if board is warped due to excessive load by check pin.



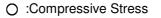
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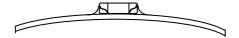


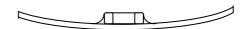
CERTIFIED SAFETY CAPACITORS

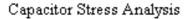
- 5.3 Mechanical stress due to warping and torsion by dividing.
 - (a) Crack occurrence ratio will be increased by manual separation.
 - (b) Crack occurrence ratio will be increased by tensile force , rather than compressive force.

imes :Tensile Stress

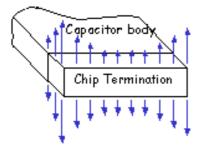


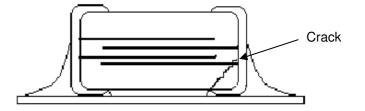






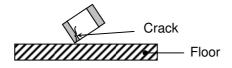




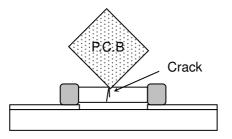


6. Handling of Loose Chip Capacitor

6.1 If dropped the chip capacitor may crack.



6.2 Piling the P.C. board after mounting for storage or handling, the corner of the P.C. board may hit the chip capacitor of another of board to cause crack.



7. Safekeeping condition and period

For safekeeping of the products, we recommend to keep storage temperature +5 ~+40 $^\circ$ C , Humidity 20 ~70%RH and use them within 12 months.



单击下面可查看定价,库存,交付和生命周期等信息

>>Holy Stone(禾伸堂)