

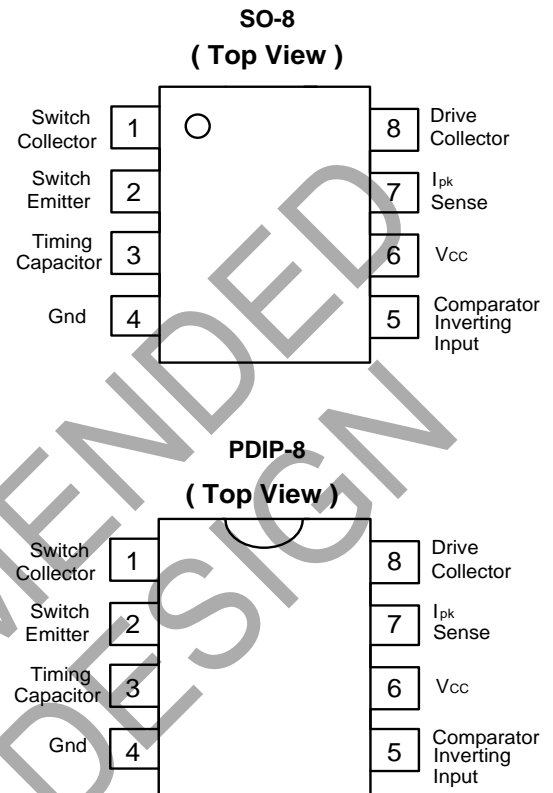
Description

The AP34063 Series is a monolithic control circuit containing the primary functions required for DC-to-DC converters. These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series is specifically designed for incorporating in Step-Down and Step-Up and Voltage-Inverting applications with a minimum number of external components.

Features

- Operation from 3.0V to 40V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.6A
- Output Voltage Adjustable
- Frequency Operation to 100kHz
- Precision 2% Reference
- PDIP-8 and SO-8 Packages
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Pin Assignments

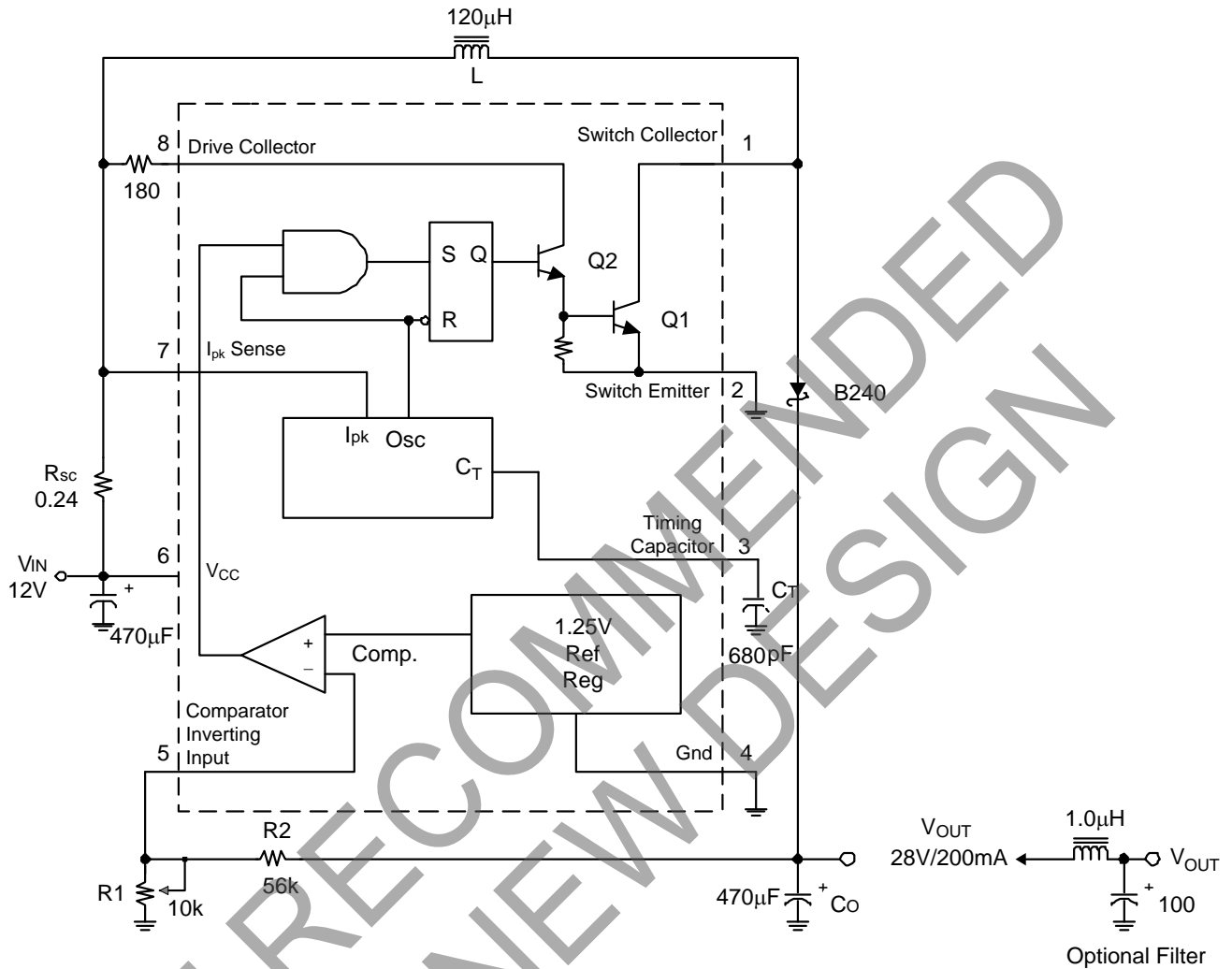


- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

NOT RECOMMENDED FOR NEW DESIGN

Typical Applications Circuit

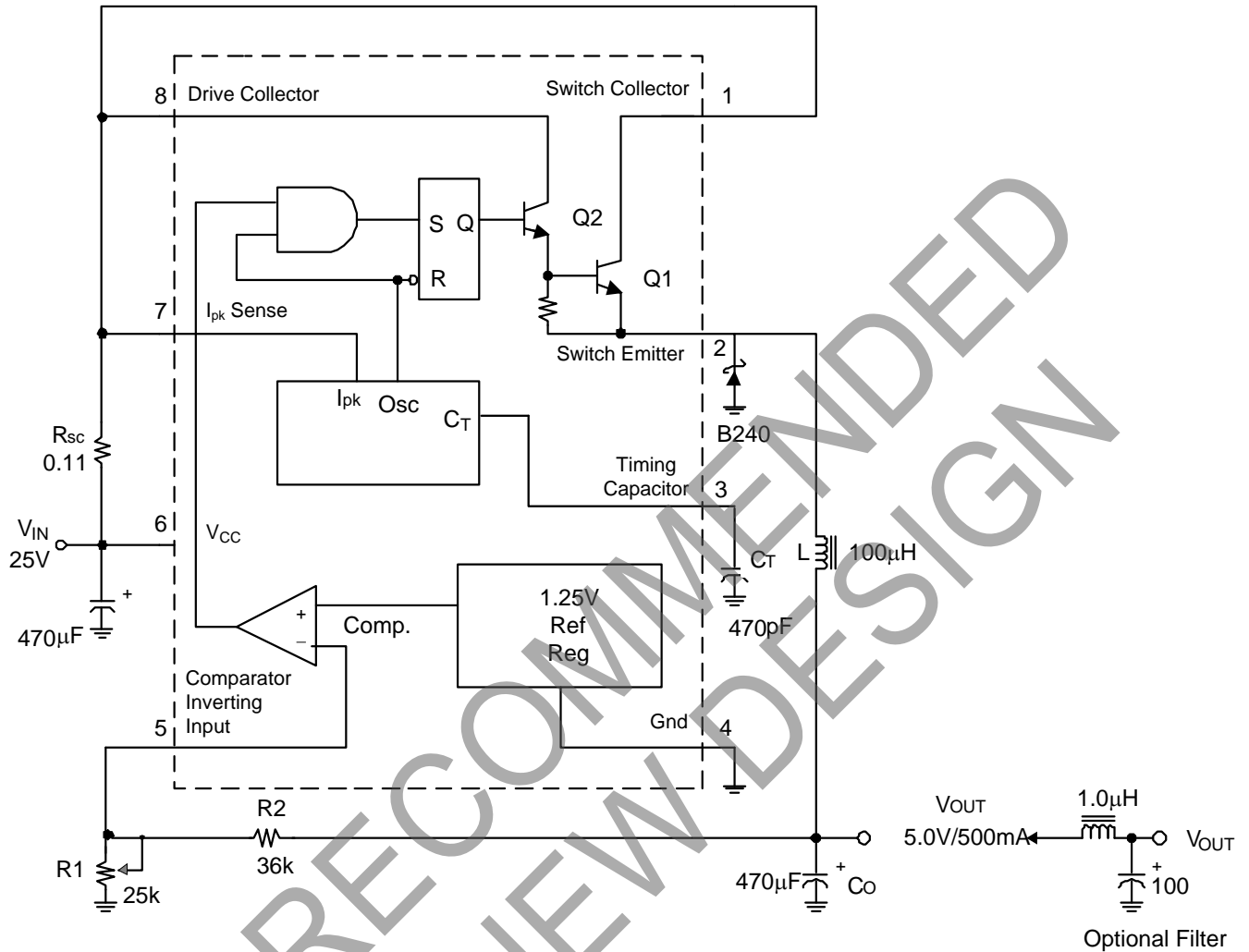
(1) Step-Up Converter



Test	Conditions	Results
Line Regulation	$V_{IN} = 9V \text{ to } 12V, I_O = 200mA$	$20mV = \pm 0.035\%$
Load Regulation	$V_{IN} = 12V, I_O = 50mA \text{ to } 200mA$	$15mV = \pm 0.035\%$
Output Ripple	$V_{IN} = 12V, I_O = 200mA$	$500mV_{PP}$
Efficiency	$V_{IN} = 12V, I_O = 200mA$	80%

Typical Applications Circuit (Cont.)

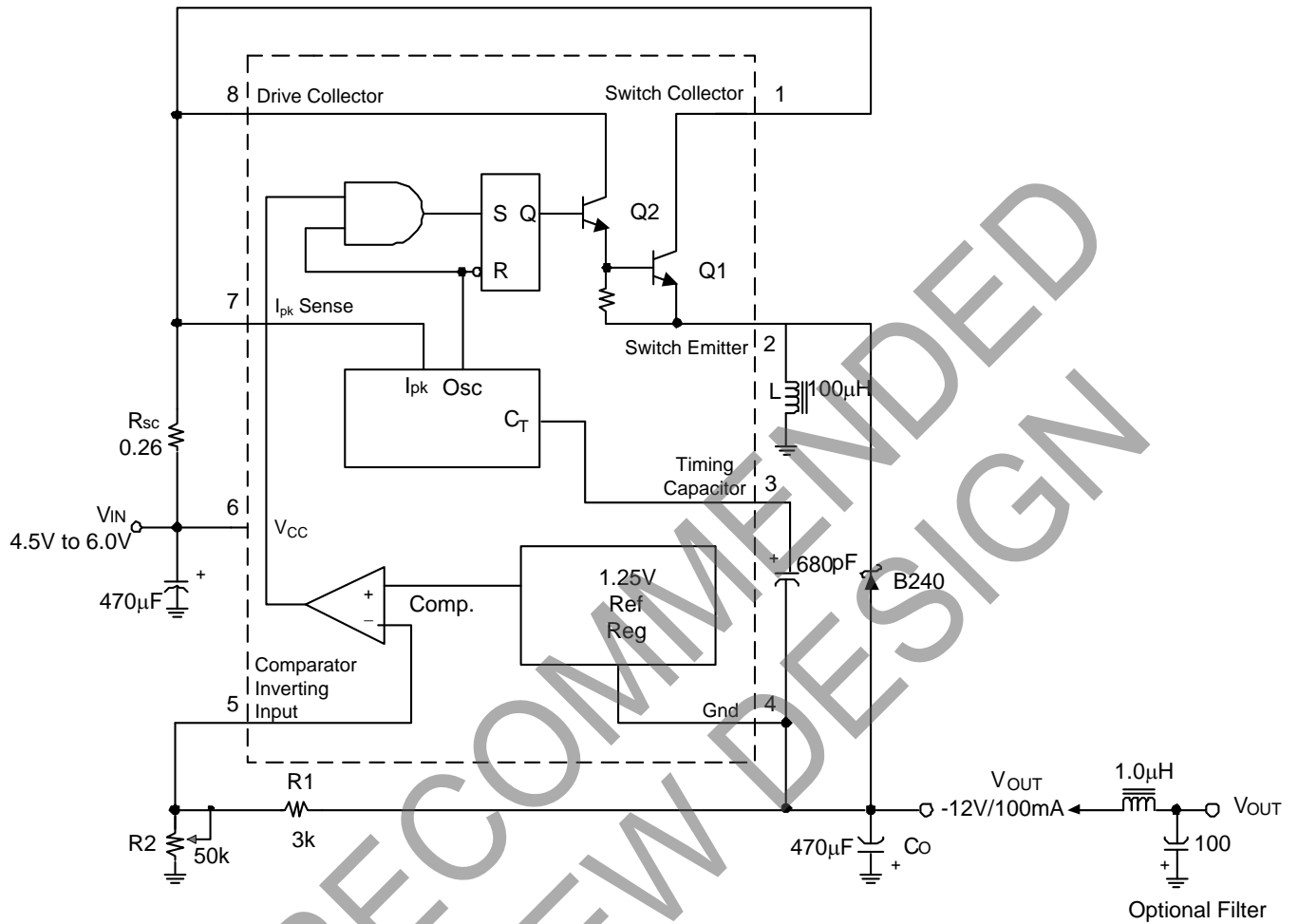
(2) Step-Down Converter



Test	Conditions	Results
Line Regulation	$V_{IN} = 12V \text{ to } 24V, I_O = 500mA$	$20mV = \pm 0.2\%$
Load Regulation	$V_{IN} = 24V, I_O = 50mA \text{ to } 500mA$	$5mV = \pm 0.05\%$
Output Ripple	$V_{IN} = 24V, I_O = 500mA$	$160mV_{PP}$
Efficiency	$V_{IN} = 24V, I_O = 500mA$	82%

Typical Applications Circuit (Cont.)

(3) Voltage Inverting Converter



Test	Conditions	Results
Line Regulation	$V_{IN} = 4.5V \text{ to } 6.0V, I_O = 100mA$	$20mV = \pm 0.08\%$
Load Regulation	$V_{IN} = 5.0V, I_O = 20mA \text{ to } 100mA$	$30mV = \pm 0.12\%$
Output Ripple	$V_{IN} = 5.0V, I_O = 100mA$	$500mV_{PP}$
Efficiency	$V_{IN} = 5.0V, I_O = 100mA$	60%

Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Stresses greater than the 'Absolute Maximum Ratings' specified above, may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.

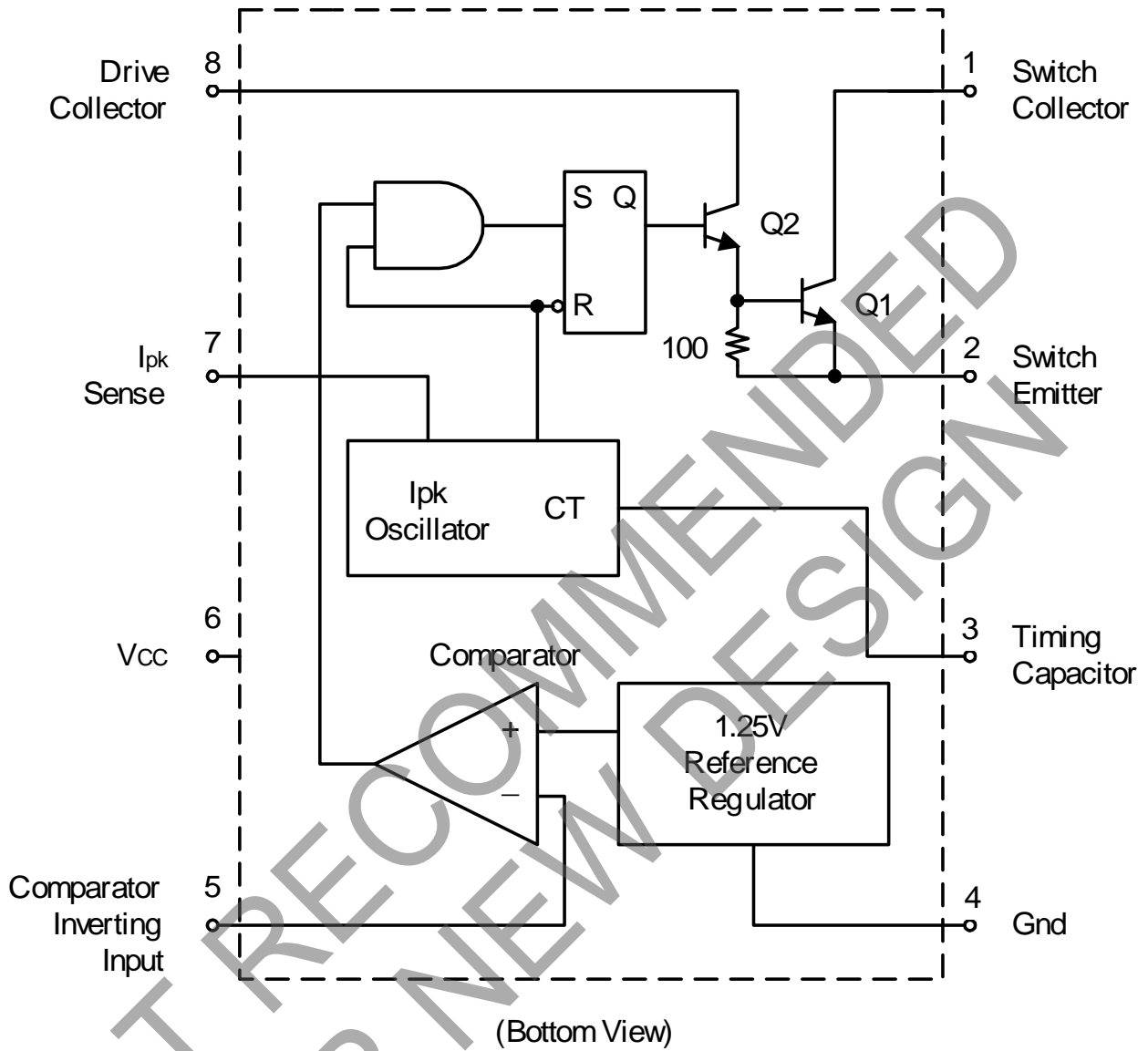
Symbol	Parameter	Value	Unit	
V _{CC}	Power Supply Voltage	40	V	
V _{CIIR}	Comparator Inverting Input Voltage Range	-0.3 to +40	V	
V _{C(SWITCH)}	Switch Collector Voltage	40	V	
V _{E(SWITCH)}	Switch Emitter Voltage (V _{PIN 1} = 40V)	40	V	
V _{CE(SWITCH)}	Switch Collector to Emitter Voltage	40	V	
V _{C(DRIVER)}	Driver Collector Voltage	40	V	
I _{C(DRIVER)}	Driver Collector Current	100	mA	
I _{SW}	Switch Current	1.6	A	
P _D	Power Dissipation (Note 4)	SO-8: T _A = +25°C	600	mW
		PDIP-8: T _A = +25°C	1.25	W
θ _{JA}	Thermal Resistance	SO-8	117	°C/W
		PDIP-8	138	
θ _{JC}		SO-8	19	
		PDIP-8	25	
T _{MJ}	Maximum Junction Temperature (Note 5)	+150	°C	
T _{OP}	Operating Junction Temperature Range	0 to +105	°C	
T _{stg}	Storage Temperature Range	-65 to +150	°C	

Notes: 4. Maximum package power dissipation limits must be observed.
5. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

Electrical Characteristics (V_{CC} = 5.0V, unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	
OSCILLATOR						
f _{OSC}	Frequency (V _{PIN 5} = 0V, C _T = 1.0nF, T _A = +25°C)	24	33	42	kHz	
I _{CHG}	Charge Current (V _{CC} = 5.0V to 40V, T _A = +25°C)	24	30	42	μA	
I _{DISCHG}	Discharge Current (V _{CC} = 5.0V to 40V, T _A = +25°C)	140	200	260	μA	
I _{DISCHG} / I _{CHG}	Discharge to Charge Current Ratio (Pin 7 to V _{CC} , T _A = +25°C)	5.2	6.5	7.5	—	
V _{ipk (SENSE)}	Current Limit Sense Voltage (I _{CHG} = I _{DISCHG} , T _A = +25°C)	300	400	450	mV	
OUTPUT SWITCH						
V _{CE(sat)}	Saturation Voltage, Darlington Connection (I _{SW} = 1.0A, Pins 1, 8 connected)	—	1.0	1.3	V	
V _{CE(sat)}	Saturation Voltage, Darlington Connection (I _{SW} = 1.0A, I _D = 50mA, Forced β ≈ 20)	—	0.45	0.7	V	
h _{FE}	DC Current Gain (I _{SW} = 1.0A, V _{CE} = 5.0V, T _A = +25°C)	50	75	—	—	
I _{C(off)}	Collector Off-State Current (V _{CE} = 40V)	—	0.01	100	μA	
COMPARATOR						
V _{TH}	Threshold Voltage	T _A = +25°C	1.225	1.25	1.275	V
		T _A = 0°C to +70°C	1.21	—	1.29	V
Reg _{LINE}	Threshold Voltage Line Regulation (V _{CC} = 3.0V to 40V)	—	1.4	6.0	mV	
TOTAL DEVICE						
I _{CC}	Supply Current (V _{CC} = 5.0V to 40V, C _T = 1.0nF, Pin 7 = V _{CC} , V _{PIN 5} > V _{TH} , Pin 2 = Gnd, remaining pins open)	—	—	3.5	mA	

Representative Schematic Diagram



Typical Performance Characteristics

Figure 1. $V_{CE(sat)}$ versus I_E

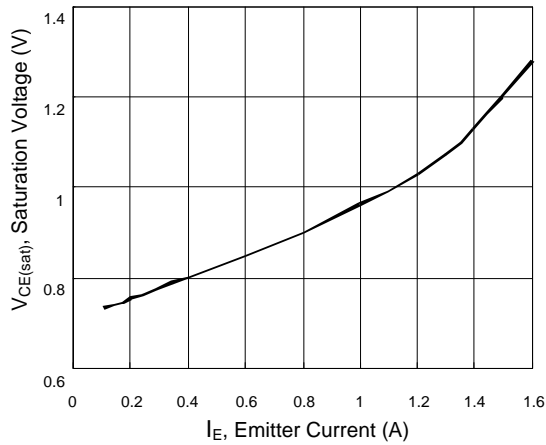


Figure 2. Reference Voltage versus Temp.

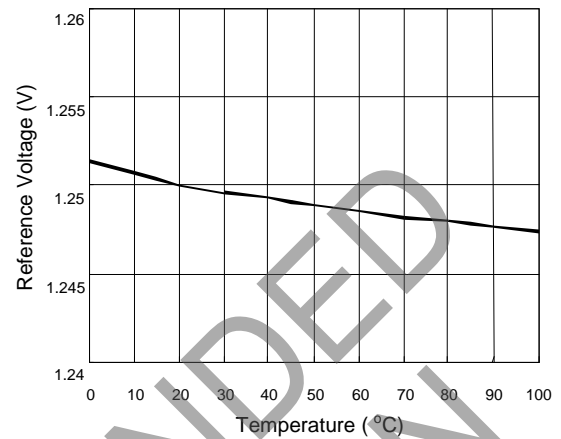


Figure 3. Current Limit Sense Voltage versus Temperature

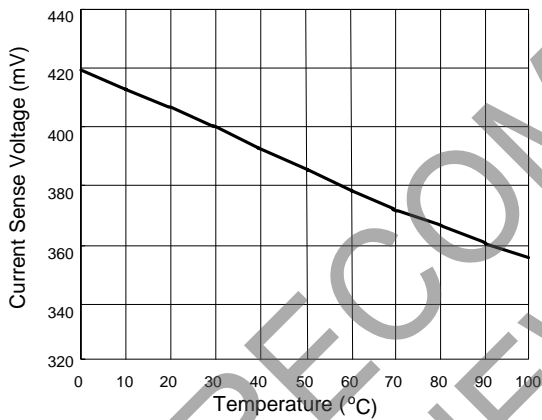


Figure 4. Standby Supply Current versus Supply Voltage

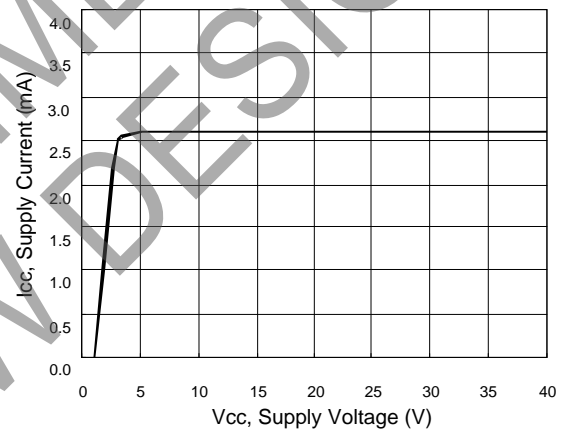


Figure 5. Emitter Follower Configuration Output Saturation Voltage vs. Emitter Current

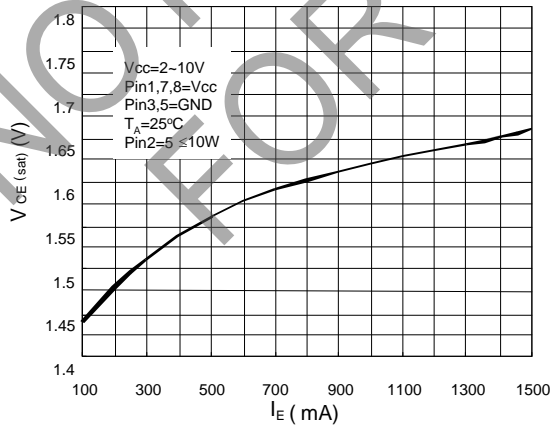
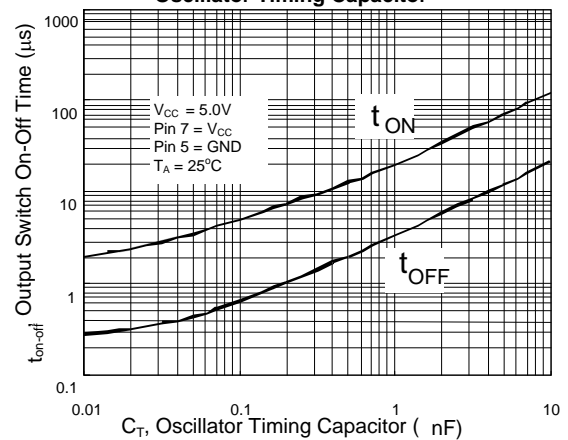


Figure 6. Output Switch On-Off Time versus Oscillator Timing Capacitor



Design Formula Table

Calculation	Step-Up			Step-Down			Voltage-Inverting		
t _{ON} / t _{OFF}	V _{OUT} + V _F - V _{IN(MIN)}			V _{OUT} + V _F			V _{OUT} + V _F		
	V _{IN(MIN)} - V _{SAT}			V _{IN(MIN)} - V _{SAT} - V _{OUT}			V _{IN(MIN)} - V _{SAT}		
(t _{ON} + t _{OFF})	1/f			1/f			1/f		
t _{OFF}	t _{ON} + t _{OFF}			t _{ON} + t _{OFF}			t _{ON} + t _{OFF}		
	t _{ON}	+1		t _{ON}	+1		t _{ON}	+1	
	t _{OFF}			t _{OFF}			t _{OFF}		
t _{ON}	(t _{ON} + t _{OFF}) - t _{OFF}			(t _{ON} + t _{OFF}) - t _{OFF}			(t _{ON} + t _{OFF}) - t _{OFF}		
C _T	4.0 × 10 ⁻⁵ t _{ON}			4.0 × 10 ⁻⁵ t _{ON}			4.0 × 10 ⁻⁵ t _{ON}		
I _{PK} (Switch)	2I _{OUT(MAX)} (t _{ON} / t _{OFF} + 1)			2I _{OUT(MAX)}			2I _{OUT(MAX)} (t _{ON} / t _{OFF} + 1)		
R _{SC}	0.3 / I _{PK} (SWITCH)			0.3 / I _{PK} (SWITCH)			0.3 / I _{PK} (SWITCH)		
L (MIN)	(V _{IN(MIN)} - V _{SAT})		t _{ON(MAX)}	(V _{IN(MIN)} - V _{SAT} - V _{OUT})		t _{ON(MAX)}	(V _{IN(MIN)} - V _{SAT})		t _{ON(MAX)}
	I _{PK} (SWITCH)			I _{PK} (SWITCH)			I _{PK} (SWITCH)		
C _O	9	I _{OUT} t _{ON}		I _{PK} (SWITCH) (t _{ON} + t _{OFF})		9	I _{OUT} t _{ON}		V _{RIPPLE} (pp)
		V _{RIPPLE} (pp)		8V _{RIPPLE} (pp)			V _{RIPPLE} (pp)		

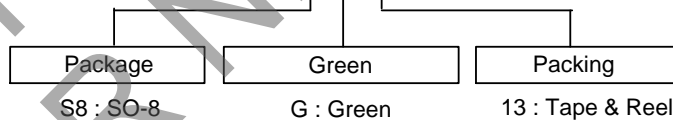
V_{SAT} = Saturation voltage of the output switch.
V_F = Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:

- V_{IN} - Nominal input voltage.
- V_{OUT} - Desired output voltage, |V_{OUT}| = 1.25 (1+R₂/R₁)
- I_{OUT} - Desired output current.
- F_{MIN} - Minimum desired output switching frequency at the selected values of V_{IN} and I_O.
- V_{RIPPLE(pp)} - Desired peak-to-peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

Ordering Information

AP34063 XX X - X

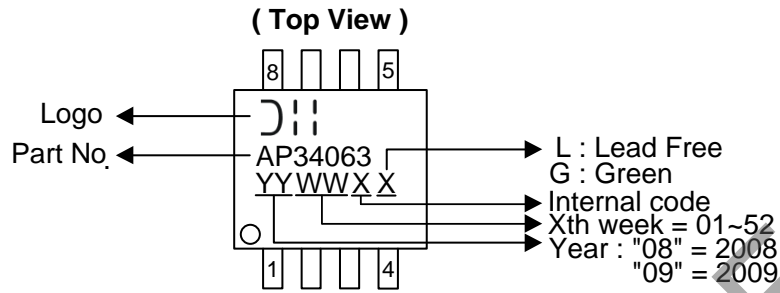


Device	Package Code	Package (Note 7)	Green	Quantity	Part Number Suffix		Status (Note 6)
					Tube	13" Tape and Reel	
AP34063S8G-13	S8	SO-8	Green	2500	NA	-13	In production

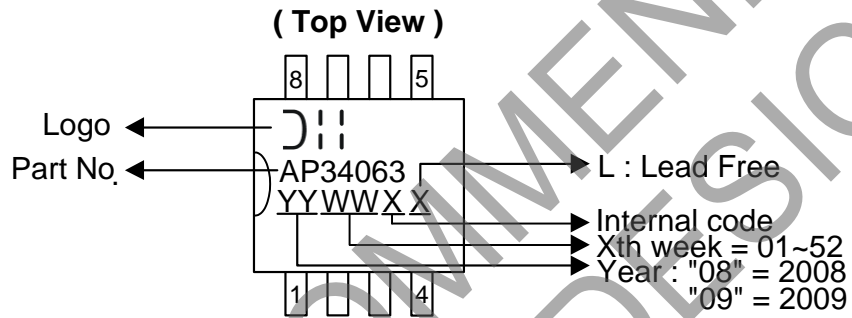
- Notes:
- All Lead-free versions in SO-8 and PDIP-8 are End of Life (EOL) with no replacement.
 - For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information (Note 6)

(1) SO-8



(2) PDIP-8

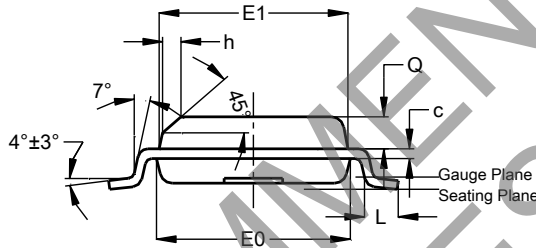
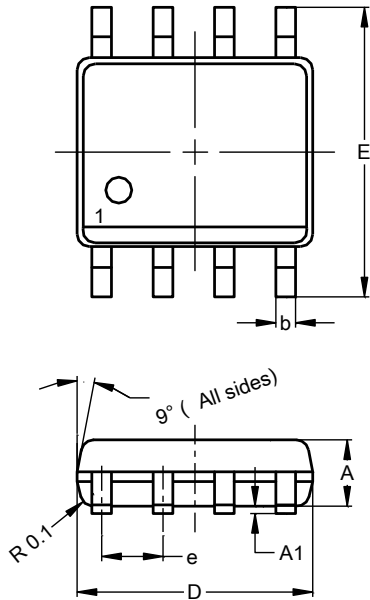


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Package Outline Dimensions (All dimensions in mm.)

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

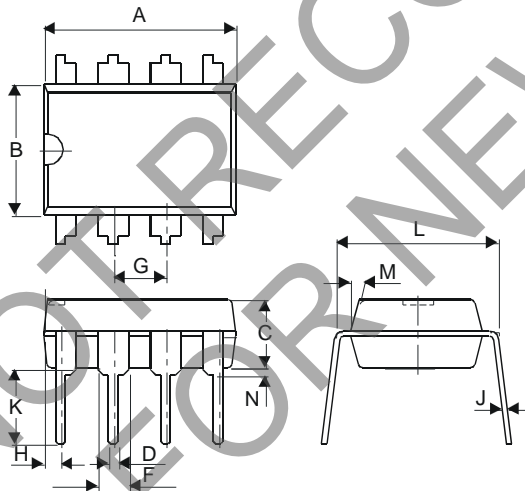
(1) SO-8



SO-8			
Dim	Min	Max	Typ
A	1.40	1.50	1.5
A	0.10	0.20	0.15
b	0.30	0.50	0.40
c	0.15	0.25	0.20
D	.85	4.95	4.90
E	5.90	6.10	6.00
E1	3.80	3.90	3.85
E0	3.85	3.95	3.90
e	--	--	1.27
h	-	--	0.35
L	0.62	0.82	0.72
Q	0.60	0.70	0.65

All Dimensions in mm

(2) PDIP-8



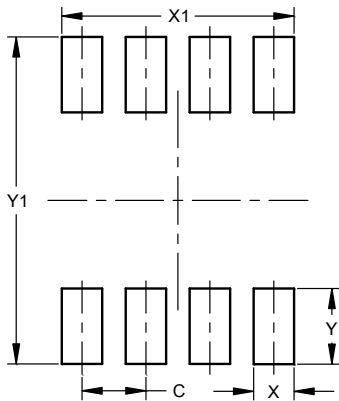
PDIP-8		
Dim	Min	Max
A	9.02	9.53
B	6.15	6.35
C	3.10	3.50
D	0.36	0.56
F	1.40	1.65
G	2.54 typ.	
H	0.71	0.97
J	0.20	0.36
K	2.92	3.81
L	7.62	8.26
M	—	15°
N	0.38 (min)	

All Dimensions in mm

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

(1) SO-8



Dimensions	Value (in mm)
C	1.27
X	0.802
X1	4.612
Y	1.505
Y1	6.50

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