AW9818E 77-Channel LED Driver with I²C Interface

FEATURES

- 77-channel LED or 21 RGB drivers
- 64-level currents setting and breathing individually for each LED
- 4-level IMAX selections: 10/20/30/40 mA
- INTN pin interrupt output, low active
- Compatible I²C Interface, VIO: 1.8V ~ 3.3V
- I²C address: 0x3A/0x3B
- Shutdown mode control: SHDN pin shutdown or software shutdown. Support register reset control and standby mode control
- CLKIO pin can output internal OSC clock(4MHz)or select external input clock
- TQFN4X4-28L package
- Power supply: VDD (2.4V~3.3V) and VBAT (3.4V~5.5V).

APPLICATIONS

- Mobile phones and other hand-held devices
- Gaming device (Keyboard, Mouse etc.)
- LED in white goods application

GENERAL DESCRIPTION

AW9818E is a 77 channels LED driver with I²C interface support. AW9818E uses awinic distinctive Free-Flash™ wisdom dimming technology, each LED can breathing individually with full autonomous or half autonomous mode that reduces serial port communication load of main chipset maximally .

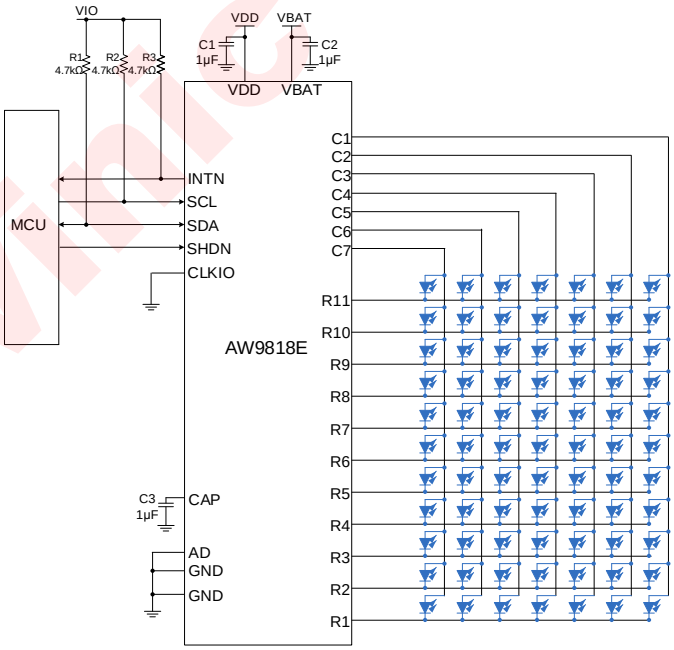
When one breathing complete in AW9818E, INTN pin will trigger an interrupt request. The function is used to synchronize the LED breathing between main chipset and AW9818E.

1.8V I²C interface of 400kHz fast mode is provided, AW9818E supports SHDN pin shutdown or internal soft shutdown function.

AW9818E can configure to output the internal clock (4MHz) or external clock input. AW9818E supports cascading for synchronization of chips.

AW9818E is TQFN4X4-28L package, need two power supply, VDD (2.4V~3.3V) and VBAT (3.4V~5.5V).

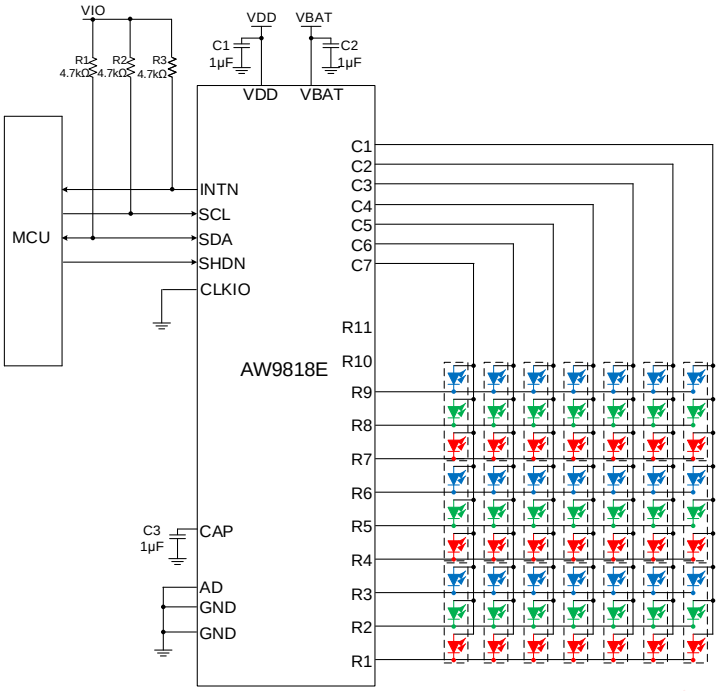
TYPICAL APPLICATION CIRCUIT



LED Configuration Register

LAB7	LAB6	LAB5	LAB4	LAB3	LAB2	LAB1
LAA7	LAA6	LAA5	LAA4	LAA3	LAA2	LAA1
LA97	LA96	LA95	LA94	LA93	LA92	LA91
LA87	LA86	LA85	LA84	LA83	LA82	LA81
LA77	LA76	LA75	LA74	LA73	LA72	LA71
LA67	LA66	LA65	LA64	LA63	LA62	LA61
LA57	LA56	LA55	LA54	LA53	LA52	LA51
LA47	LA46	LA45	LA44	LA43	LA42	LA41
LA37	LA36	LA35	LA34	LA33	LA32	LA31
LA27	LA26	LA25	LA24	LA23	LA22	LA21
LA17	LA16	LA15	LA14	LA13	LA12	LA11

Figure 1 AW9818E LED Application Circuit



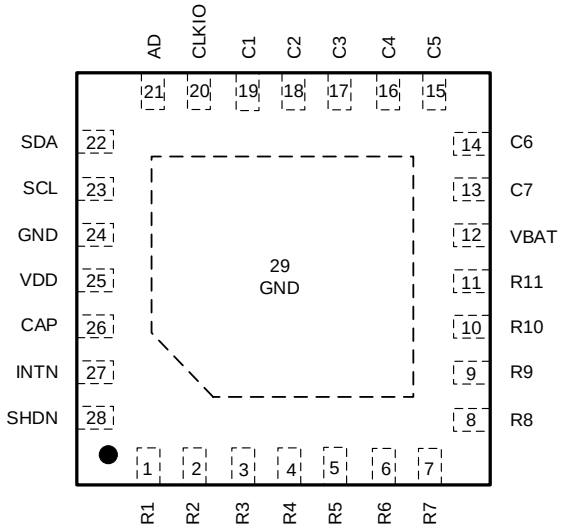
LED Configuration Register

LA97	LA96	LA95	LA94	LA93	LA92	LA91
LA87	LA86	LA85	LA84	LA83	LA82	LA81
LA77	LA76	LA75	LA74	LA73	LA72	LA71
LA67	LA66	LA65	LA64	LA63	LA62	LA61
LA57	LA56	LA55	LA54	LA53	LA52	LA51
LA47	LA46	LA45	LA44	LA43	LA42	LA41
LA37	LA36	LA35	LA34	LA33	LA32	LA31
LA27	LA26	LA25	LA24	LA23	LA22	LA21
LA17	LA16	LA15	LA14	LA13	LA12	LA11

Figure 2 AW9818E RGB Application Circuit

PIN CONFIGURATION AND TOP MARK

AW9818ETQR PIN Configuration
(TOP VIEW)



AW9818ETQR Top Mark
(TOP VIEW)

AW9818 – AW9818ETQR
XXXX – Production Tracing Code

PIN DEFINITION

No.	NAME	DESCRIPTION
1	R1	Row1 LED Cathode Driver Port
2	R2	Row2 LED Cathode Driver Port
3	R3	Row3 LED Cathode Driver Port
4	R4	Row4 LED Cathode Driver Port
5	R5	Row5 LED Cathode Driver Port
6	R6	Row6 LED Cathode Driver Port
7	R7	Row7 LED Cathode Driver Port
8	R8	Row8 LED Cathode Driver Port
9	R9	Row9 LED Cathode Driver Port
10	R10	Row10 LED Cathode Driver Port
11	R11	Row11 LED Cathode Driver Port
12	VBAT	Power Supply V_{BAT}
13	C7	Column7 LED Anode Driver Scan Port
14	C6	Column6 LED Anode Driver Scan Port
15	C5	Column5 LED Anode Driver Scan Port
16	C4	Column4 LED Anode Driver Scan Port
17	C3	Column3 LED Anode Driver Scan Port
18	C2	Column2 LED Anode Driver Scan Port
19	C1	Column1 LED Anode Driver Scan Port
20	CLKIO	Clock Input / Output
21	AD	I^2C Address Select
22	SDA	I^2C Data Bus
23	SCL	I^2C Clock Bus
24	GND	Ground
25	VDD	Power Supply V_{DD}
26	CAP	External Capacity
27	INTN	Interrupt Output, Low Active
28	SHDN	Shutdown Control, Low Active
29	GND	Ground

FUNCTION BLOCK DIAGRAM

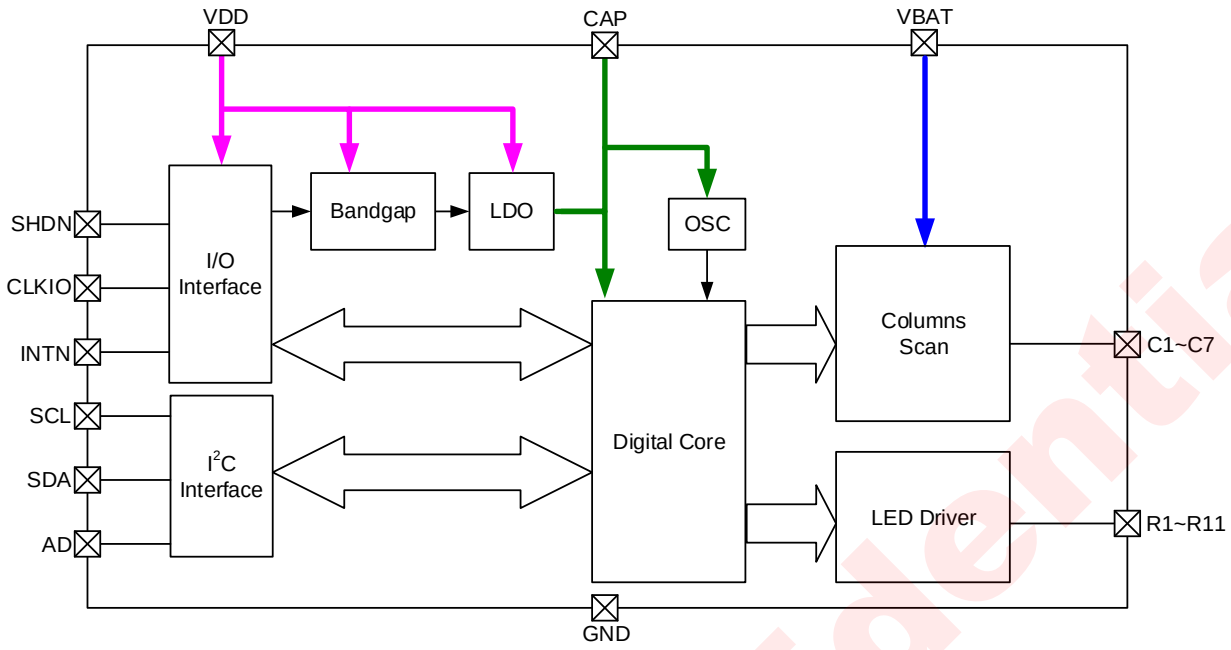
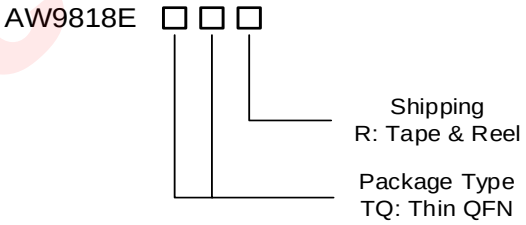


Figure 3 Functional Block Diagram

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	MSL Level	ROHS	Delivery Form
AW9818ETQR	-40°C~85°C	TQFN4X4-28L	AW9818	MSL3	ROHS+HF	6000 units/ Tape and Reel



ABSOLUTE MAXIMUM RATING (NOTE 1)

PARAMETERS	RANGE
Supply voltage range V_{DD}	-0.3V to 3.6V
Supply voltage range V_{BAT}	-0.3V to 5.5V
Voltage on SCL, SDA, SHDN, INTN, CLKIO	-0.3V to V_{DD}
Maximum Power Consumption (PDmax,package@ TA=25°C)	3.2W
Junction-to-ambient thermal resistance θ_{JA}	31°C/W
Maximum Junction temperature T_{JMAX}	125℃
Storage temperature T_{STG}	-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)	260°C
ESD(NOTE 2)	
HBM (human body model)	±2000V
CDM	±1500V
MM	±200V
Latch-Up	
Test Condition: JESD78D	+IT:+100mA -IT:-100mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017.

RECOMMEND WORK CONDITION (VBAT>VDD, T_A=-40°C~85°C)

PARAMETER		TEST CONDITION	RANGE	UNIT
V_{DD}	V_{DD} Input Voltage	T_A=-40°C~85°C	2.4 ~ 3.3	V
V_{BAT}	V_{BAT} Input Voltage	T_A=-40°C~85°C	3.4 ~ 5.5	V

ELECTRICAL CHARACTERISTICS

TA=25°C,VDD=2.8V, VBAT＝4.2V (unless otherwise noted)

SYMBOL	DESCRIPTION	TEST CONDITION	MIN	TYP	MAX	UNIT
Power supply voltage and current						
V_{DD}	IO port input operation voltage	T_A=-40℃~85℃	2.4		3.3	V
V_{BAT}	LED drive input operation voltage	T_A=-40℃~85℃	3.4		5.5	V
I_{VBAT_PD}	V_{BAT} current in shutdown mode	SHDN=GND		6.7	8	μA
I_{VDD_PD}	V_{DD} current in shutdown mode	SHDN=GND		0.1	1	μA
$I_{VBAT\_STANDBY}$	V_{BAT} current in standby mode	SHDN=1.8V		18	36	μA
$I_{VDD\_STANDBY}$	V_{DD} current in standby mode	SHDN=1.8V		75	90	μA
LED Drive						
I_{LED_MAX}	Max current of each LED channel	IMAX[1:0] = 11	37.2	40	42.8	mA
I_{OUT}	Default output current		18	20	22	mA
PMOS Switch						
R_{ON}	PMOS on resistance			1.9	2.05	Ω
OSC						
f_{osc}	OSC clock frequency		3.8	4.3	4.6	MHz
CLKIO Pin						
V_{OH}	Logic output high level	I_{OH} = -2mA	V_{DD}-0.1			V
V_{OL}	Logic output low level	I_{OL} = 7.5mA			0.1	V
V_{IH}	Logic input high level		1.3			V
V_{IL}	Logic input low level				0.4	V
AD Pin						
V_{IH}	Logic input high level		1.3			V
V_{IL}	Logic input low level				0.4	V
SHDN Pin						

SYMBOL	DESCRIPTION	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IH}	Logic input high level		1.3			V
V_{IL}	Logic input low level				0.4	V
$t_{DEGLITCH}$	SHDN deglitch time			5		μs
INTN Pin						
V_{OL}	Logic output low level	I_{OL} = 10 mA			0.1	V
I²C Interface						
V_{OL}	Logic output low level (SDA Pin)	I_{OL} = 10 mA			0.1	V
V_{IH}	Logic input high level		1.3			V
V_{IL}	Logic input low level				0.4	V
$t_{SDA\_DEGLITCH}$	SDA deglitch time			250		ns
$t_{SCL\_DEGLITCH}$	SCL deglitch time			220		ns

I²C INTERFACE TIMING

PARAMETER			MIN	TYP	MAX	UNIT
F_{SCL}	Interface Clock frequency				400	kHz
$T_{DEGLITCH}$	Deglitch time	SCL		200		ns
		SDA		250		ns
$T_{HD:STA}$	(Repeat-start) Start condition hold time		0.6			μs
T_{LOW}	Low level width of SCL		1.3			μs
T_{HIGH}	High level width of SCL		0.6			μs
$T_{SU:STA}$	(Repeat-start) Start condition setup time		0.6			μs
$T_{HD:DAT}$	Data hold time		0			μs
$T_{SU:DAT}$	Data setup time		0.1			μs
T_R	Rising time of SDA and SCL				0.3	μs
T_F	Falling time of SDA and SCL				0.3	μs
$T_{SU:STO}$	Stop condition setup time		0.6			μs
T_{BUF}	Time between start and stop condition		1.3			μs

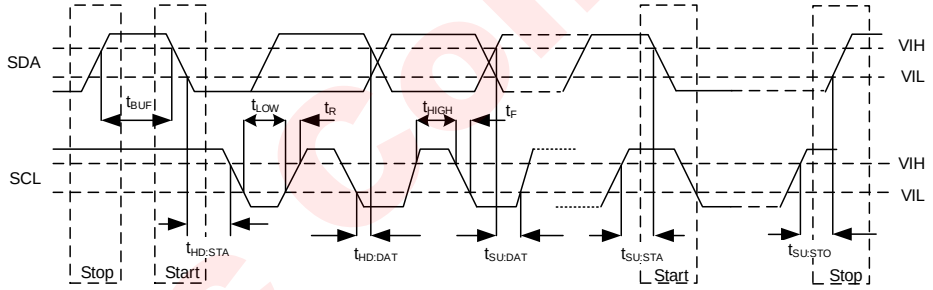


Figure 4 I²C Interface Timing

I²C INTERFACE

AW9818E supports the I²C serial bus and data transmission protocol in fast mode at 400kHz or stand mode at 100kHz. AW9818E operates as a slave on the I²C bus. Connect to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. AW9818E can support different high level (1.8V~3.3V) of this I²C interface.

I²C Start/Stop

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

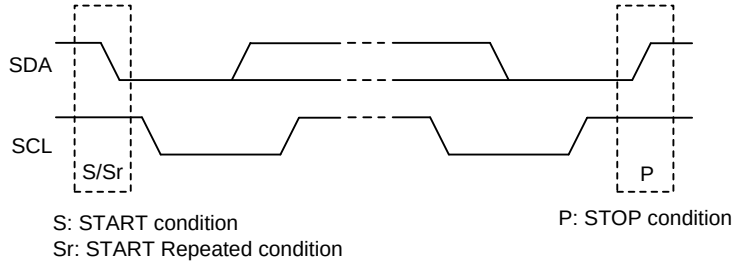


Figure 5 I²C Start/Stop Condition Timing

Data Validation

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

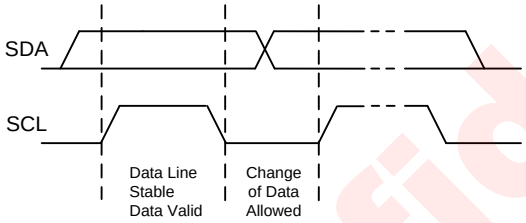


Figure 6 Data Validation Diagram

ACK (Acknowledgement)

ACK means the successful transfer of I²C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

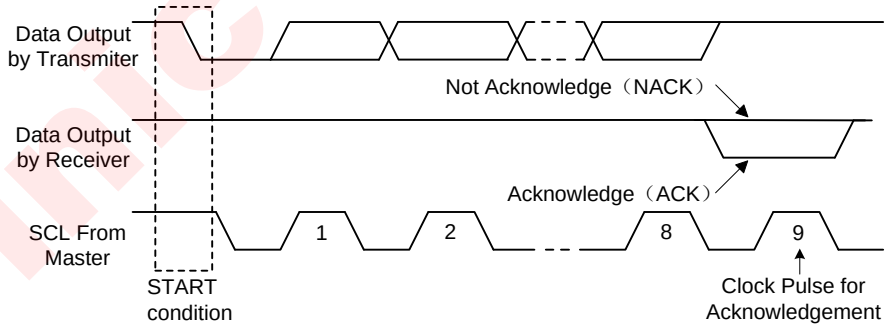


Figure 7 I²C ACK Timing

Device Address

The I²C device address (7-bit, followed by the R/W bit (Read=1/Write=0)) of AW9818E depends on the AD pin status. When AD level is low, the I²C address is 0x3A; when AD level is high, the I²C address is 0x3B.

0	1	1	1	0	1	AD	R/$\overline{W}$

(AD value must be equal to the value of AD pin)

Figure 8 Device Address

Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.

b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master sends data byte to be written to the addressed register

g) Slave sends acknowledge signal

h) If master will send further data bytes the control register address will be incremented by one after acknowledge signal (repeat step f and g)

i) Master generates STOP condition to indicate write cycle end

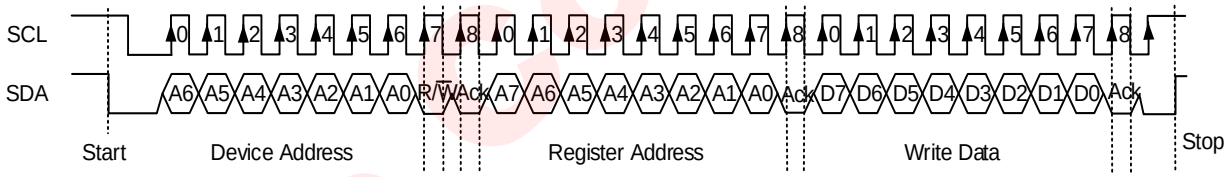


Figure 9 I²C Write Byte Cycle

Read Cycle

In a read cycle, the following steps should be followed:

a) Master device generates START condition

b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master generates STOP condition followed with START condition or REPEAT START condition

g) Master device sends slave address (7-bit) and the data direction bit (R/W = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends data byte from addressed register.

j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.

k) If the master device generates STOP condition, the read cycle is ended.

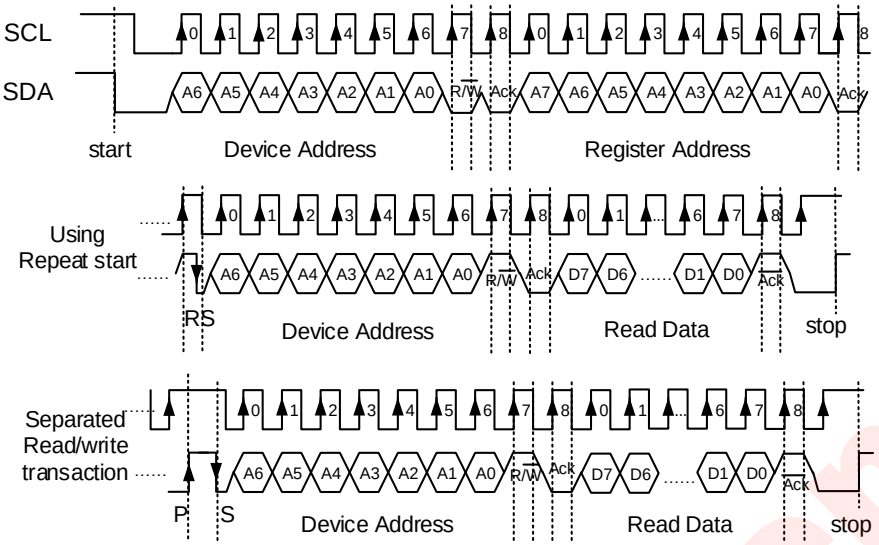


Figure 10 I²C Read Byte Cycle

OPERATING MODE

In AW9818E, there are three work modes available: Shut-down, Standby and Active mode.

Shut-down Mode

AW9818E enters into the shut-down mode when SHDN level is pulled to low. After AW9818E pull SHDN to high level, internal state reset to the default value.

Standby Mode

AW9818E enters into standby mode automatically when pull SHDN to high level in shut-down mode or write 80H to SLEEP register by I²C interface in the active mode. In standby mode, internal data state will not be changed, LED drive is in shut-down state; the I²C interface is accessible, but only configuration registers can be operated.

Active mode

When 00H is written to SLEEP register by I²C interface in standby mode, AW9818E enters into the active mode. In this moment, internal state in AW9818E will be not changed.

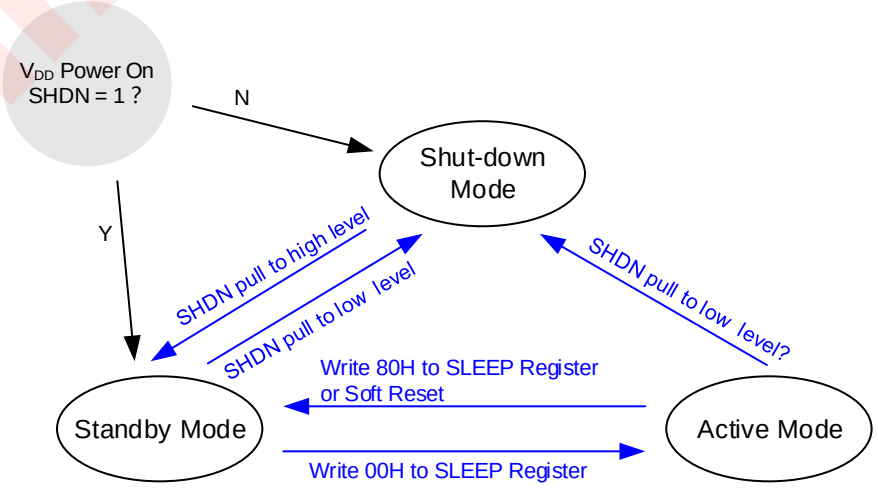


Figure 11 AW9818E operating mode transition

RESET

AW9818E provide three reset modes: Power on reset, SHDN reset and soft reset mode.

Power on reset

When V_{DD} pin is powered on, AW9818E internal circuit will reset automatically. And all state registers will be reset to the default value.

SHDN reset

When SHDN pin is pulled to low level, AW9818E enter into the shut-down mode; AW9818E will enter into the standby mode when pull SHDN to high level in the shut-down mode, reset will be completed automatically.

Soft reset

AW9818E will trigger a soft reset after writing 01H to RSTN register by I^2C interface. After reset, all the registers will be reset to the default value. After the soft reset command is send through the I^2C interface, it takes at least 1ms for chip to acknowledge the new I^2C command.

CLOCK INPUT AND OUTPUT CONTROL

AW9818E use the internal OSC clock (4MHz) as the default.

CLK_IO control bit can be used to select the internal OSC clock output or external clock input. CLK_SEL control bit select the internal OSC clock work or external clock work in clock input state. Clock input or output are both through CLKIO pin.

Permitting the clock input or output, it is expedient to synchronize the breathing time of LED when more AW9818E are cascaded.

INTERRUPT FUNCTION

AW9818E provide the interrupt output to main chipset. The function is used to synchronize the control signal in two different clock domains (main chipset and AW9818E). INTN pin is the open-drain output port, and need the external pull-up resistor (the recommend value is 4.7kΩ).

The interrupt function is available and can be enabled in individual breathing light work mode only. In matrix LED mode, AW9818E will disable the interrupt function automatically.

AW9818E will trigger an interrupt request and INTN pin will be pulled down after LED breathing complete. Reading the corresponding interrupt state bit of LED by I^2C, interrupt will be cleared. 77 LEDs of AW9818E are corresponding to the interrupt state bits in registers INTN_LA1~INTN_LAB.

LED OPERATING MODE

AW9818E support 77 LEDs, and there are two available control mode: Individual LED breathing mode and matrix LED mode. The default control mode is individual LED breathing mode (Configure EN_ARRAY register to select). Using the awinic distinctive Free-Flash™ technology, chipset will scan all columns one by one automatically, to realize 7 columns x 11 rows drive. C1~C7 are column scan ports, the scan frequency is 238Hz. R1~R11 are LED dimming drive ports, which will output different LED drive current when the scan column change.

By configuring the IMAX global register, 77 LEDs will select 10mA, 20mA (default), 30mA or 40mA as the max drive current.

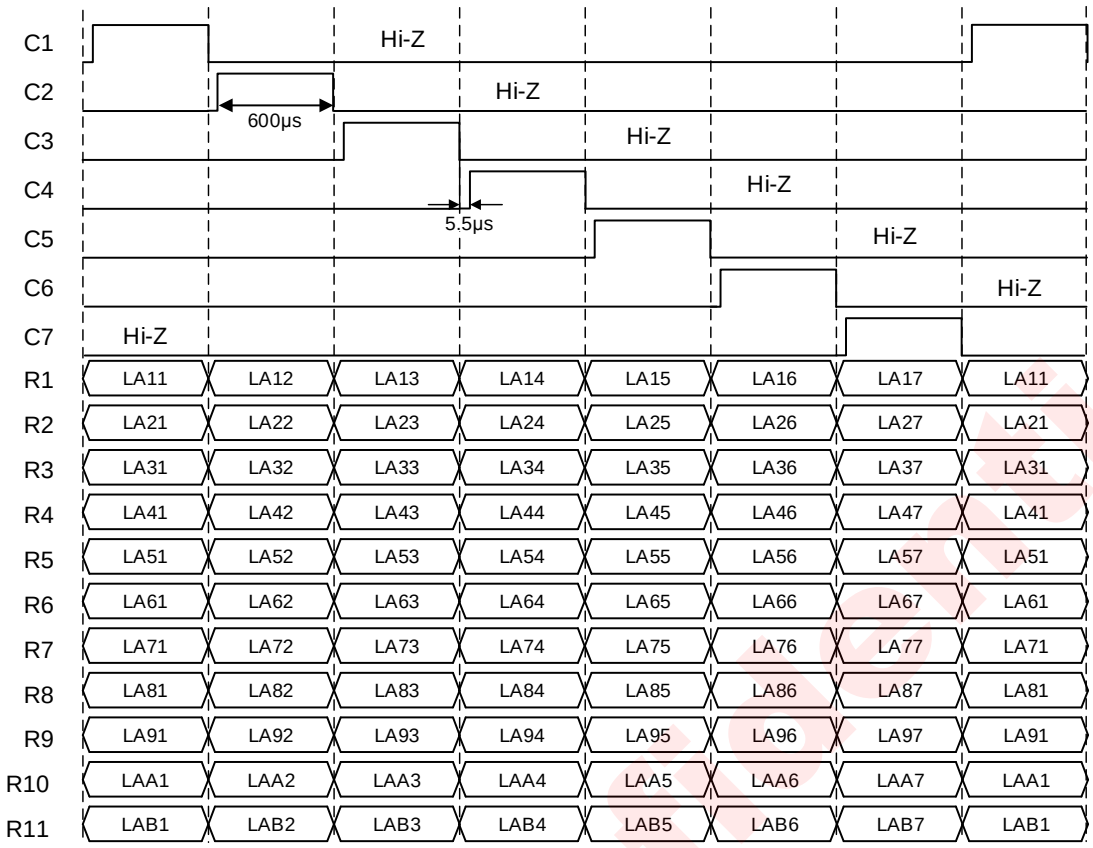


Figure 12 AW9818E LED scan drive operating theory

INDIVIDUAL LED BREATHING CONTROL MODE

AW9818E provide the full autonomous or half autonomous breathing mode to drive LED, the default is half autonomous breathing mode (controlled by FULL_FADE register).

77 LEDs are corresponding to 77 configuration registers (Register address 10H~5CH), each LED can be set the breathing time individually (FDTM configure register) and the max breathing brightness level (DIM configure register). AW9818E can set 64 levels DIM of max breathing brightness. In preselect configuration of the max breathing current, the autonomous breathing drive levels are 64 levels, that is to say, chipset can adjust (0/63)*DIM, (1/63)*DIM, … (63/63)*DIM automatically.

After configured the breathing time and the brightness of each LED, LED will be powered on or off by the corresponding bits in registers LEDONi (60H~6AH). After breathing once, AW9818E will trigger an interrupt request automatically. The main chipset will clear the interrupt when reading the LED corresponding interrupt state register.

When the chipset enter into the active mode first time after power on, AW9818E will write the data of registers 10H~5CH to internal ASP automatically. AW9818E permits to update the LED parameter after the corresponding LED breathing complete (that is to say, data of the configure register can't be changed when LED is breathing). After the data updated, write the UPDATE register, the chipset will write the data of registers 10H~5CH to internal ASP again.

A) Half autonomous breathing mode

Druing half autonomous breathing mode, LED only complete one fade-in or one fade-out. There are four type time: 0s/0.5s/1s/2s to select for fade-in or fade-out. When changing the corresponding trigger bit from '0' to '1' in LEDONi(60H~6AH configure register), LED will fade-in automatically and trigger an

interrupt requeset; When the corresponding trigger bit changed from ‘1‘ to ‘0‘, LED fade-out automatically and trigger interrupt request.

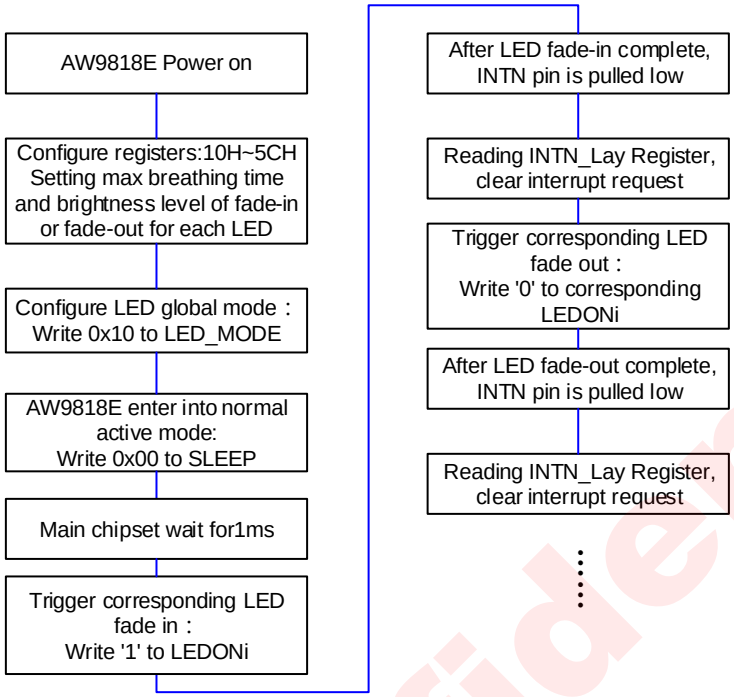


Figure 13 AW9818E LED half autonomous breathing control flow

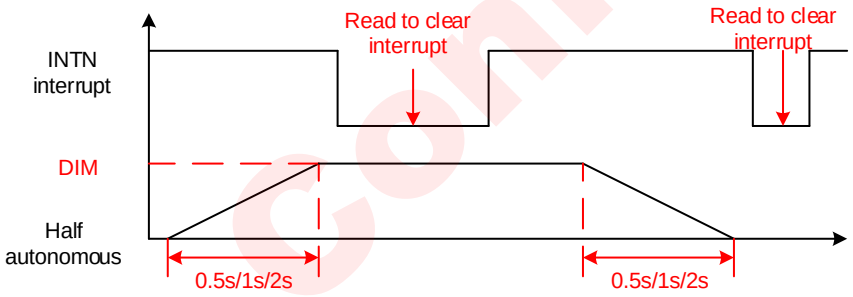


Figure 14 AW9818E LED half autonomous breathing, interrupt trigger and clear

B) Full autonomous breathing mode

Druing full autonomous breathing mode, LED complete one period of fade-in and fade-out. There are four type time: 0s/0.5s/1s/2s to select for an full autonomous breathing period. When changing the corresponding trigger bit from ‘0‘ to ‘1‘ in LEDONi(60H~6AH configuration register), LED will complete an full autonomous breathing automatically and trigger an interrupt requeset. When LED starts the full autonomous breathing, we should set the corresponding trigger bit from ‘1‘ to ‘0‘ for the next full autonomous breathing.

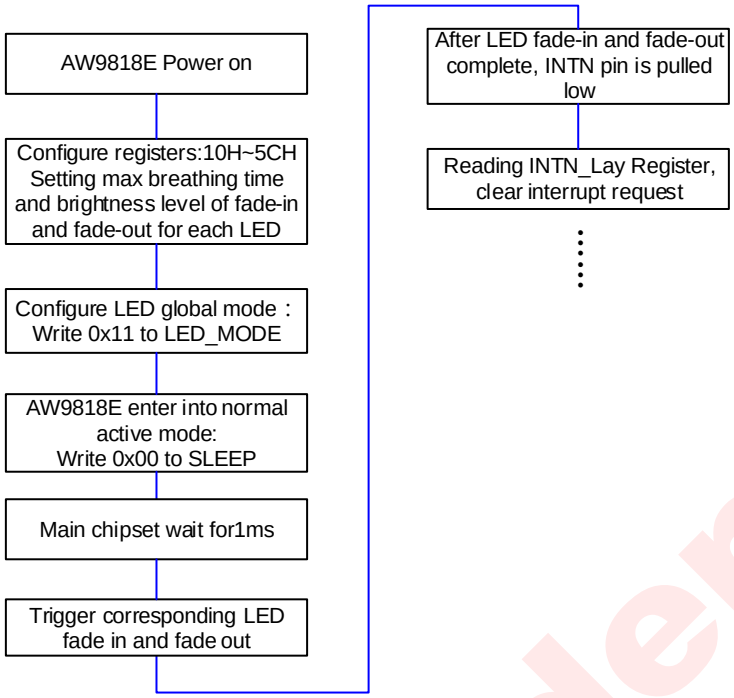


Figure 15 AW9818E LED full autonomous breathing control flow

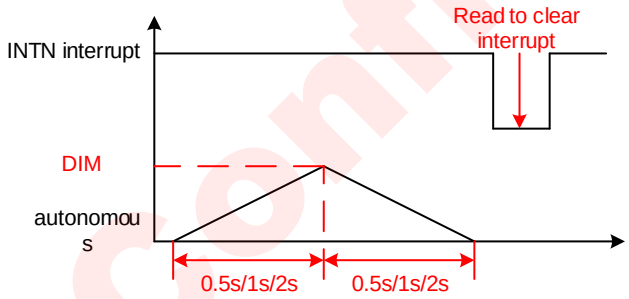


Figure 16 AW9818E LED full autonomous breathing, interrupt trigger and clear

C) Matrix LED mode

AW9818E support 7X11 LED matrix, 77 LEDs are corresponding to 77 configure registers (register address 10H~5CH). Each LED can set the brightness level individually (DIM configure register). AW9818E can display the different brightness effect of static dot matrix. 64 brightness levels are (0/63)*IMAX,(1/63)*IMAX … (63/63)*IMAX.

Dot matrix pattern is set in the standby mode. When AW9818E enter into the active mode first time after power on, the data in registers 10H~5CH will be written to the internal ASP (dedicated processor), and the static pattern will be displayed in the LED matrix. AW9818E permits to update each LED parameter at any time. After data updated, writing the UPDATE register, chipset will write the data in registers 10H~5CH to ASP and the static pattern will be updated in LED matrix.

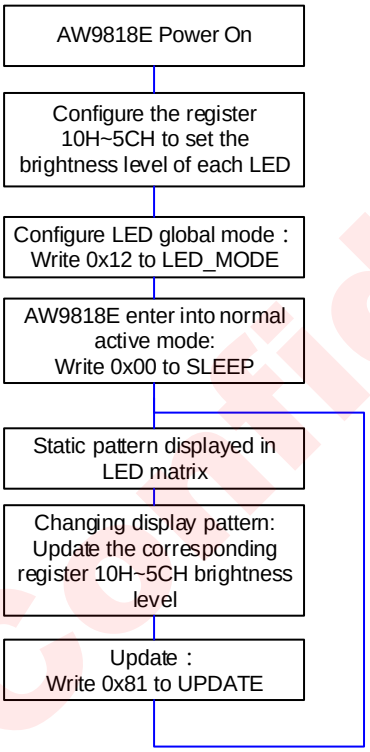


Figure 17 AW9818E LED matrix control flow

REGISTER DESCRIPTION

REGISTER LIST

Address	Name	W/R	Description	Default Value
00H	ID	R	AW9818E chip ID	18H
01H	SLEEP	W/R	Sleep mode control	80H
02H	RSTN	W	Soft reset	00H
03H	LED_MODE	W/R	Global LED mode control	10H
04H	UPDATE	W	Update enable	00H
05H	CLK_SYS	W/R	Clock control	00H
06H ~ 0FH	-	-	-	-
10H	LA11	W	R1/C1 LED corresponding parameter configuration	00H
11H	LA21	W	R2/C1 LED corresponding parameter configuration	00H
12H	LA31	W	R3/C1 LED corresponding parameter configuration	00H
13H	LA41	W	R4/C1 LED corresponding parameter configuration	00H
14H	LA51	W	R5/C1 LED corresponding parameter configuration	00H
15H	LA61	W	R6/C1 LED corresponding parameter configuration	00H
16H	LA71	W	R7/C1 LED corresponding parameter configuration	00H
17H	LA81	W	R8/C1 LED corresponding parameter configuration	00H
18H	LA91	W	R9/C1 LED corresponding parameter configuration	00H
19H	LAA1	W	R10/C1 LED corresponding parameter configuration	00H
1AH	LAB1	W	R11/C1 LED corresponding parameter configuration	00H
1BH	LA12	W	R1/C2 LED corresponding parameter configuration	00H
1CH	LA22	W	R2/C2 LED corresponding parameter configuration	00H
1DH	LA32	W	R3/C2 LED corresponding parameter configuration	00H
1EH	LA42	W	R4/C2 LED corresponding parameter configuration	00H
1FH	LA52	W	R5/C2 LED corresponding parameter configuration	00H
20H	LA62	W	R6/C2 LED corresponding parameter configuration	00H
21H	LA72	W	R7/C2 LED corresponding parameter configuration	00H
22H	LA82	W	R8/C2 LED corresponding parameter configuration	00H
23H	LA92	W	R9/C2 LED corresponding parameter configuration	00H
24H	LAA2	W	R10/C2 LED corresponding parameter configuration	00H
25H	LAB2	W	R11/C2 LED corresponding parameter configuration	00H
26H	LA13	W	R1/C3 LED corresponding parameter configuration	00H
27H	LA23	W	R2/C3 LED corresponding parameter configuration	00H
28H	LA33	W	R3/C3 LED corresponding parameter configuration	00H
29H	LA43	W	R4/C3 LED corresponding parameter configuration	00H
2AH	LA53	W	R5/C3 LED corresponding parameter configuration	00H
2BH	LA63	W	R6/C3 LED corresponding parameter configuration	00H
2CH	LA73	W	R7/C3 LED corresponding parameter configuration	00H
2DH	LA83	W	R8/C3 LED corresponding parameter configuration	00H
2EH	LA93	W	R9/C3 LED corresponding parameter configuration	00H
2FH	LAA3	W	R10/C3 LED corresponding parameter configuration	00H
30H	LAB3	W	R11/C3 LED corresponding parameter configuration	00H
31H	LA14	W	R1/C4 LED corresponding parameter configuration	00H
32H	LA24	W	R2/C4 LED corresponding parameter configuration	00H
33H	LA34	W	R3/C4 LED corresponding parameter configuration	00H
34H	LA44	W	R4/C4 LED corresponding parameter configuration	00H
35H	LA54	W	R5/C4 LED corresponding parameter configuration	00H
36H	LA64	W	R6/C4 LED corresponding parameter configuration	00H
37H	LA74	W	R7/C4 LED corresponding parameter configuration	00H
38H	LA84	W	R8/C4 LED corresponding parameter configuration	00H
39H	LA94	W	R9/C4 LED corresponding parameter configuration	00H
3AH	LAA4	W	R10/C4 LED corresponding parameter configuration	00H
3BH	LAB4	W	R11/C4 LED corresponding parameter configuration	00H

3CH	LA15	W	R1/C5 LED corresponding parameter configuration	00H
3DH	LA25	W	R2/C5 LED corresponding parameter configuration	00H
3EH	LA35	W	R3/C5 LED corresponding parameter configuration	00H
3FH	LA45	W	R4/C5 LED corresponding parameter configuration	00H
40H	LA55	W	R5/C5 LED corresponding parameter configuration	00H
41H	LA65	W	R6/C5 LED corresponding parameter configuration	00H
42H	LA75	W	R7/C5 LED corresponding parameter configuration	00H
43H	LA85	W	R8/C5 LED corresponding parameter configuration	00H
44H	LA95	W	R9/C5 LED corresponding parameter configuration	00H
45H	LAA5	W	R10/C5 LED corresponding parameter configuration	00H
46H	LAB5	W	R11/C5 LED corresponding parameter configuration	00H
47H	LA16	W	R1/C6 LED corresponding parameter configuration	00H
48H	LA26	W	R2/C6 LED corresponding parameter configuration	00H
49H	LA36	W	R3/C6 LED corresponding parameter configuration	00H
4AH	LA46	W	R4/C6 LED corresponding parameter configuration	00H
4BH	LA56	W	R5/C6 LED corresponding parameter configuration	00H
4CH	LA66	W	R6/C6 LED corresponding parameter configuration	00H
4DH	LA76	W	R7/C6 LED corresponding parameter configuration	00H
4EH	LA86	W	R8/C6 LED corresponding parameter configuration	00H
4FH	LA96	W	R9/C6 LED corresponding parameter configuration	00H
50H	LAA6	W	R10/C6 LED corresponding parameter configuration	00H
51H	LAB6	W	R11/C6 LED corresponding parameter configuration	00H
52H	LA17	W	R1/C7 LED corresponding parameter configuration	00H
53H	LA27	W	R2/C7 LED corresponding parameter configuration	00H
54H	LA37	W	R3/C7 LED corresponding parameter configuration	00H
55H	LA77	W	R4/C7 LED corresponding parameter configuration	00H
56H	LA57	W	R5/C7 LED corresponding parameter configuration	00H
57H	LA67	W	R6/C7 LED corresponding parameter configuration	00H
58H	LA77	W	R7/C7 LED corresponding parameter configuration	00H
59H	LA87	W	R8/C7 LED corresponding parameter configuration	00H
5AH	LA97	W	R9/C7 LED corresponding parameter configuration	00H
5BH	LAA7	W	R10/C7 LED corresponding parameter configuration	00H
5CH	LAB7	W	R11/C7 LED corresponding parameter configuration	00H
5DH ~ 5FH	-	-	-	-
60H	LEDON1	W/R	Trigger control of 7 LEDs in R1 row	00H
61H	LEDON2	W/R	Trigger control of 7 LEDs in R2 row	00H
62H	LEDON3	W/R	Trigger control of 7 LEDs in R3 row	00H
63H	LEDON4	W/R	Trigger control of 7 LEDs in R4 row	00H
64H	LEDON5	W/R	Trigger control of 7 LEDs in R5 row	00H
65H	LEDON6	W/R	Trigger control of 7 LEDs in R6 row	00H
66H	LEDON7	W/R	Trigger control of 7 LEDs in R7 row	00H
67H	LEDON8	W/R	Trigger control of 7 LEDs in R8 row	00H
68H	LEDON9	W/R	Trigger control of 7 LEDs in R9 row	00H
69H	LEDONA	W/R	Trigger control of 7 LEDs in R10 row	00H
6AH	LEDONB	W/R	Trigger control of 7 LEDs in R11 row	00H
6BH ~ 6FH	-	-	-	-
70H	INTN_LA1	R	Interrupt state of 7 LEDs in R1 row	00H
71H	INTN_LA2	R	Interrupt state of 7 LEDs in R2 row	00H
72H	INTN_LA3	R	Interrupt state of 7 LEDs in R3 row	00H
73H	INTN_LA4	R	Interrupt state of 7 LEDs in R4 row	00H
74H	INTN_LA5	R	Interrupt state of 7 LEDs in R5 row	00H
75H	INTN_LA6	R	Interrupt state of 7 LEDs in R6 row	00H
76H	INTN_LA7	R	Interrupt state of 7 LEDs in R7 row	00H
77H	INTN_LA8	R	Interrupt state of 7 LEDs in R8 row	00H
78H	INTN_LA9	R	Interrupt state of 7 LEDs in R9 row	00H
79H	INTN_LAA	R	Interrupt state of 7 LEDs in R10 row	00H

7AH	INTN_LAB	R	Interrupt state of 7 LEDs in R11 row	00H

DETAILED REGISTER DESCRIPTION

00H: ID, Chip ID register (Default:18H)

BIT	Name	W/R	Description	Default Value
7:0	ID	R	AW9818E chip ID is 18H	18

01H: SLEEP, Sleep mode control register (Default:80H)

BIT	Name	W/R	Description	Default Value
7	SLEEP	W/R	Sleep mode control bit: 1: Sleep mode 0: Enable, enter into active mode	1
6:0	-	-	-	-

02H: RSTN, Reset control register (Default:00H)

BIT	Name	W/R	Description	Default Value
7:0	SW_RSTN	W	Soft reset control, reset all digital register unit. Write '0x01' to reset.	0

03H: LED_MODE, LED mode control register (Default:10H)

BIT	Name	W/R	Description	Default Value
7:6	-	-	-	-
5:4	IMAX	W/R	LED max drive current selection: 00: 10mA 01: 20mA 10: 30mA 11: 40mA	01
3:2	-	-	-	-
1	EN_ARRAY	W/R	LED matrix mode enable: 0: Control each LED channel individually 1: 77 LEDs compose 7X11 LED matrix	0
0	FULL_FADE	W/R	Breathing mode selection of LED full or half single period: 0: Half single breathing mode 1: Full single breathing mode	0

04H: UPDAT, 77 LEDs parameter update control register (Default:00H)

BIT	Name	W/R	Description	Default Value
7:1	-	-	-	-
0	UPDATE	W	Update data in register 10H~5CH to internal dedicate processor: Write '0x81' to update 7X11 data	0

05H: CLK_SYS, Clock control register (Default:00H)

BIT	Name	W/R	Description	Default Value
7:2	-	-	-	-
1	CLK_IO	W/R	Clock input or output selection: 0: Clock input 1: Clock output, output internal OSC frequency	0
0	CLK_SEL	W/R	Clock source selection: 0: Internal OSC clock frequency 4MHz 1: External clock input	0

10H~5CH: LAyx(y=1~A, x=1~7), LED brightness and breathing time selection register (Default:00H)

<table>
<tr><th>BIT</th><th>Name</th><th>W/R</th><th>Description</th><th>Default Value</th></tr>
<tr><td>7:6</td><td>FDTM</td><td>W</td><td>LED autonomous breathing time setting, Available when EN_ARRAY=10 :
<table>
<tr><td></td><td>FULL_FADE=0</td><td>FULL_FADE=1</td></tr>
<tr><td>00</td><td>No fade-in/fade-out</td><td>No fade-in/fade-out</td></tr>
<tr><td>01</td><td>0.5s</td><td>1s</td></tr>
<tr><td>10</td><td>1s</td><td>2s</td></tr>
<tr><td>11</td><td>2s</td><td>4s</td></tr>
</table></td><td>00</td></tr>
<tr><td>5:0</td><td>DIM</td><td>W</td><td>Control LED drive current, linearity and 64 levels
00H: 0 mA (LED OFF)
01H: (1/63)*IMAX mA
02H: (2/63)*IMAX mA
…
3FH: (63/63)*IMAX mA</td><td>00</td></tr>
</table>

60H~6AH: LEDONi (i=1~B), Row i LED trigger control (Default:00H)

BIT	Name	W/R	Description	Default Value
7	-	-	-	-
6	LEDONi7	W/R	Row i, C7 column trigger control: FULL_FADE=0: 0: LED fade-out trigger 1: LED fade-in trigger FULL_FADE=1: 0: Clear trigger state 1: LED trigger a fade-in and fade-out process	0
5	LEDONi6	W/R	Row i, C6 column trigger control: FULL_FADE=0: 0: LED fade-out trigger 1: LED fade-in trigger FULL_FADE=1: 0: Clear trigger state 1: LED trigger a fade-in and fade-out process	0
4	LEDONi5	W/R	Row i, C5 column trigger control: FULL_FADE=0: 0: LED fade-out trigger 1: LED fade-in trigger FULL_FADE=1: 0: Clear trigger state 1: LED trigger a fade-in and fade-out process	0
3	LEDONi4	W/R	Row i, C4 column trigger control: FULL_FADE=0: 0: LED fade-out trigger 1: LED fade-in trigger FULL_FADE=1: 0: Clear trigger state 1: LED trigger a fade-in and fade-out process	0
2	LEDONi3	W/R	Row i, C3 column trigger control: FULL_FADE=0: 0: LED fade-out trigger 1: LED fade-in trigger FULL_FADE=1: 0: Clear trigger state 1: LED trigger a fade-in and fade-out process	0
1	LEDONi2	W/R	Row i, C2 column trigger control: FULL_FADE=0: 0: LED fade-out trigger 1: LED fade-in trigger FULL_FADE=1: 0: Clear trigger state 1: LED trigger a fade-in and fade-out process	0
0	LEDONi1	W/R	Row i, C1 column trigger control: FULL_FADE=0: 0: LED fade-out trigger 1: LED fade-in trigger FULL_FADE=1: 0: Clear trigger state 1: LED trigger a fade-in and fade-out process	0

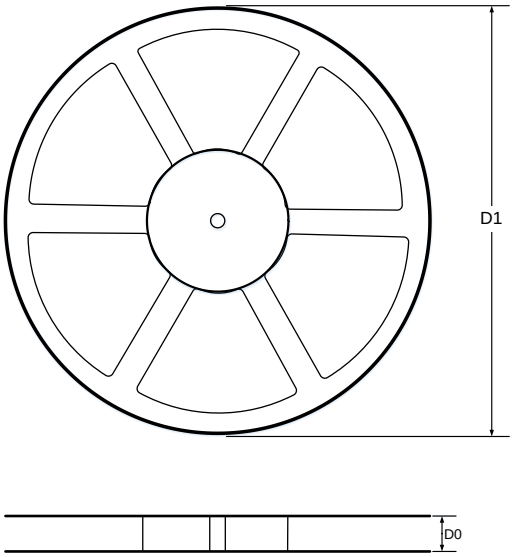
70H~7AH: INTN_LAi (i=1~B), Row i LED interrupt state register (Default:00H)

BIT	Name	W/R	Description	Default Value
7	-	-	-	-
6	INTN_Lay7	R	Row y, column 7 interrupt state: 0: No interrupt 1: Interrupt	0

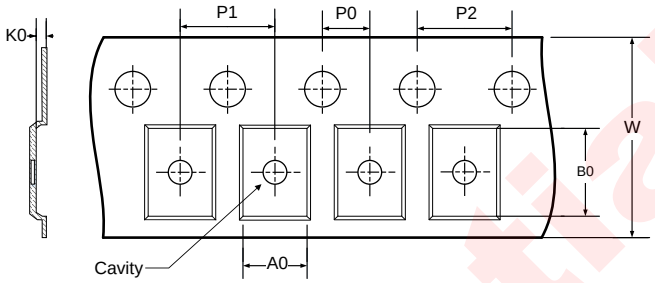
5	INTN_Lay6	R	Row y, column 6 interrupt state: 0: No interrupt 1: Interrupt	0
4	INTN_Lay5	R	Row y, column 5 interrupt state: 0: No interrupt 1: Interrupt	0
3	INTN_LAy4	R	Row y, column 4 interrupt state: 0: No interrupt 1: Interrupt	0
2	INTN_Lay3	R	Row y, column 3 interrupt state: 0: No interrupt 1: Interrupt	0
1	INTN_Lay2	R	Row y, column 2 interrupt state: 0: No interrupt 1: Interrupt	0
0	INTN_Lay1	R	Row y, column 1 interrupt state: 0: No interrupt 1: Interrupt	0

TAPE AND REEL INFORMATION

REEL DIMENSIONS

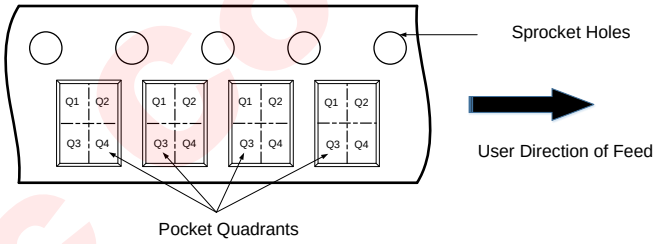


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

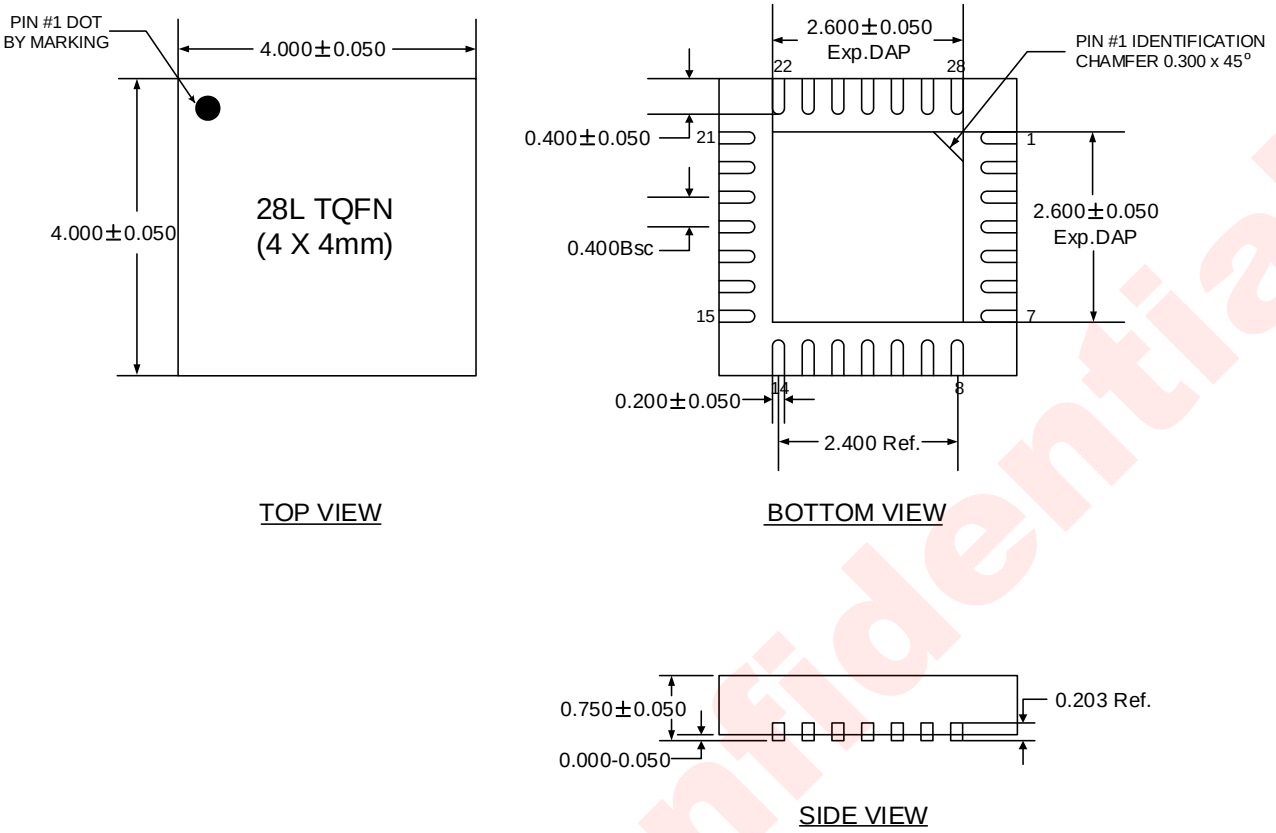
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



All Dimensions are nominal

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	4.3	4.3	1.1	2	8	4	12	Q1

PACKAGE DESCRIPTION

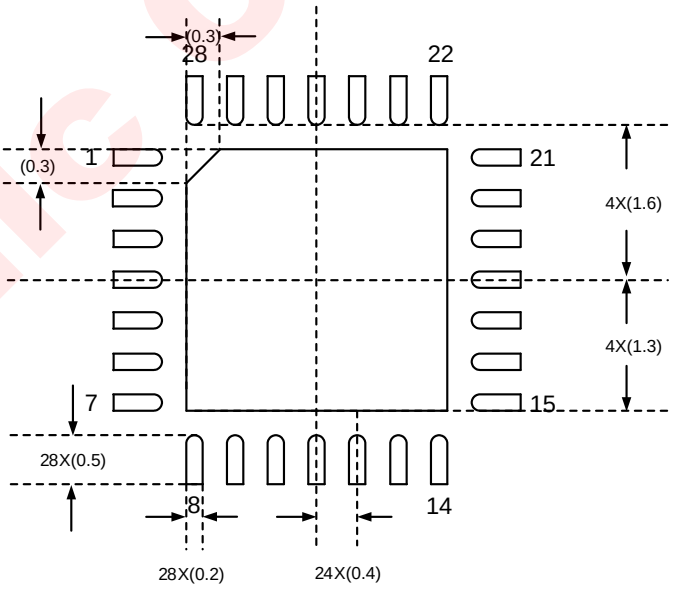


TOP VIEW

BOTTOM VIEW

SIDE VIEW

RECOMMENDED LAND PATTERN



TOP VIEW

REVISION HISTORY

Version	Date	Revision Record
V1.0	Aug. 2018	First officially release
V1.1	Jun. 2019	Modify the software reset description --page12

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