Description

APR3415B is a secondary side Combo IC, which combines an N-Channel MOSFET and a driver circuit designed for synchronous rectification (SR) in DCM operation. It also integrates output voltage detect function for primary side control system.

The N-Channel MOSFET has been optimized for low gate charge, low $R_{DS(ON)}$, fast switching speed and body diode reverse recovery performance.

The synchronous rectification can effectively reduce the secondary side rectifier power dissipation and provide high performance solution. By sensing MOSFET drain-to-source voltage, APR3415B can output ideal drive signal with less external components. It can provide high performance solution for 5V output voltage application.

Same as AP4341, APR3415B detects the output voltage and provides a periodical signal when the output voltage is lower than a certain threshold. By fast response to secondary side voltage, APR3415B can effectively improve the transient performance of primary side control system.

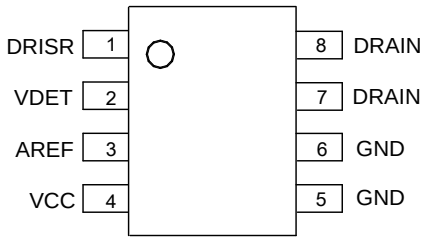
The APR3415B is available in SO-8 (Type CJ) package.

Features

- Synchronous Rectification for DCM Operation Flyback
- Eliminate Resonant Ring Interference
- Fast Detector of Supply Voltages
- Fewest External Components
- **Totally Lead-free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Pin Assignments

(Top View)



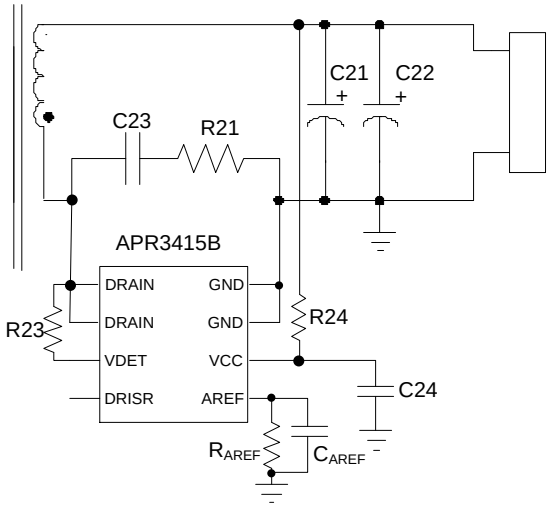
SO-8 (Type CJ)

Applications

- Adapters/Chargers for Cell/Cordless Phones, ADSL Modems, MP3 and Other Portable Apparatus
- Standby and Auxiliary Power Supplies

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

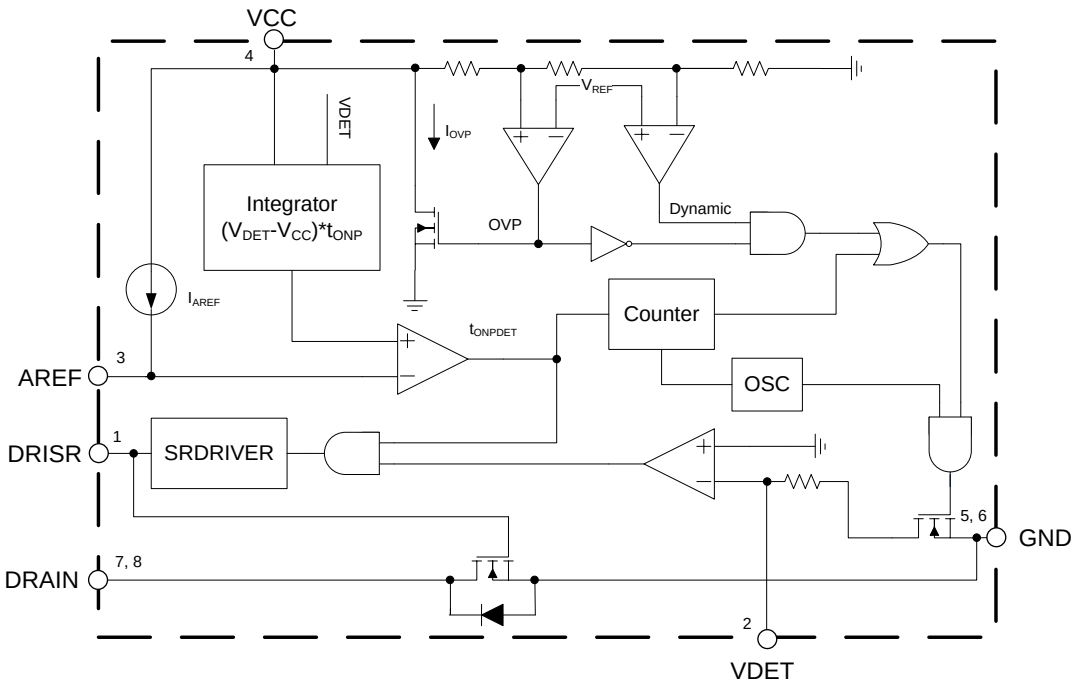
Typical Applications Circuit



Pin Descriptions

Pin Number	Pin Name	Function
1	DRISR	Synchronous rectification MOSFET drive
2	VDET	Synchronous rectification sense input and dynamic function output, connected to DRAIN through a resistor
3	AREF	Program a voltage reference with a resistor from AREF to GND, to enable synchronous rectification MOSFET drive signal
4	VCC	Power supply, connected with system output
5, 6	GND	Source pin of internal MOSFET, connected to Ground
7, 8	DRAIN	Drain pin of internal MOSFET

Functional Block Diagram



Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V_{CC}	Supply Voltage	-0.3 to 7.5	V
V_{DET}, V_{DRAIN}	Voltage at VDET, DRAIN Pin (Note 5)	-2 to 50	V
V_{AREF}, V_{DRISR}	Voltage at AREF, DRISR Pin	-0.3 to 6	V
I_D	Continuous Drain Current	15	A
I_{DM}	Pulsed Drain Current	60	A
P_D	Power Dissipation at T_A=+25ºC	0.7	W
θ_{JA}	Thermal Resistance (Junction to Ambient) (Note 6)	88	ºC/W
θ_{JC}	Thermal Resistance (Junction to Case) (Note 6)	19	ºC/W
T_J	Operating Junction Temperature	+150	ºC
T_{STG}	Storage Temperature	-65 to +150	ºC
T_{LEAD}	Lead Temperature (Soldering, 10 sec)	+300	ºC

Notes: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.

5. VDET pin ESD sensitive, pass 1500V HBM. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch^2 pad layout.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	3.3	5.6	V
T_A	Ambient Temperature	-40	+85	ºC

Electrical Characteristics (@T_A = +25°C, V_{CC} =5V, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage (VCC Pin)						
$I_{STARTUP}$	Startup Current	V_{CC}=$V_{STARTUP}$-0.1V	–	100	150	μA
I_{OP}	Operating Current	VDET pin floating V_{CC}=$V_{TRIGGER}$+20mV	40	100	150	μA
$V_{STARTUP}$	Startup Voltage	–	2.6	3.1	3.4	V
–	UVLO	–	2.3	2.8	3.1	V
Dynamic Output Section/Oscillator Section						
$V_{TRIGGER}$	Internal Trigger Voltage	–	5.15	5.2	5.25	V
–	Duty Cycle	–	4	8	12	%
t_{OSC}	Oscillation Period	V_{CC}=5V	18	30	37.5	μs
$I_{TRIGGER}$	Internal Trigger Current	V_{CC}=$V_{TRIGGER}$, VCC/VDET pin is separately connected to a 20Ω resistor	30	–	42	mA
t_{DIS}	Minimum Period	–	18	30	37.5	ms
V_{DIS}	Discharge Voltage	–	5.27	5.35	5.43	V
I_{DIS}	Discharge Current	V_{CC}=V_{DIS}+0.1V	1.5	3	4.5	mA
V_{DIS}-$V_{TRIGGER}$	Trigger Discharger Gap	–	30	110	–	mV
V_{OVP}	Overshoot Voltage for Discharge	–	5.7	5.8	5.9	V
I_{OVP}	Overshoot Current for Discharge	V_{CC}=V_{OVP}+0.1V, VCC pin is connected to a 20Ω resistor	40	–	100	mA
Synchronous Voltage Detect						
V_{THON}	Gate Turn On Threshold	–	0	–	1	V
V_{THOFF}	Gate Turn Off Threshold	–	-20	-12.5	-5	mV
t_{DON}	Turn On Delay Time	From V_{THON} to V_{DRISR}=1V	–	70	130	ns
t_{DOFF}	Turn Off Propagation Delay Time	From V_{THOFF} to V_{DRISR}=3V	–	100	150	ns
t_{RG}	Gate Turn On Rising Time	From 1V to 3V, C_L=4.7nF	–	50	100	ns
t_{FG}	Gate Turn Off Falling Time	From 3V to 1V, C_L=4.7nF	–	50	100	ns
t_{LEB_S}	Minimum On Time	–	0.9	1.8	2.7	μs
t_{LEB_L}		–	–	–	6.5	
V_{DRISR_HIGH}	Drive Output Voltage	V_{CC}=5V	3.7	–	–	V
V_{S_MIN}	SR Minimum Operating Voltage (Note 7)	–	–	–	4.5	V
t_{OVP_LAST}	Added OVP Discharge Time	–	–	2.0	–	ms
Kqs	(Note 8)	(V_{DET}-V_{CC})*t_{ONP} = 25Vμs	0.325	–	0.515	mA*μs

Notes: 7. Specifies the minimum SR operating voltage of V_{IN_DC}, V_{IN_DC}≥N_{PS}*V_{S_MIN}.
8. Used to specify the value of R_{AREF}.

Electrical Characteristics (@T_A =+25°C, unless otherwise specified.) (continued)

MOSFET Static Characteristics

Parameters	Symbol	Conditions	Min	Typ	Max	Unit
Drain to Source Breakdown Voltage	$V_{DSS(BR)}$	V_{GS}=0V, I_D=0.25mA	50	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=0.25mA	0.5	0.9	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=50V, V_{GS}=0V	–	–	1	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS}=10V, V_{DS}=0V	–	–	±10	μA
Drain to Source On-state Resistance	$R_{DS(ON)}$	V_{GS}=4.5V, I_D=15A	12	17	30	mΩ

MOSFET Dynamic Characteristics

Parameters	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V, f=1MHz	–	1316	–	pF
Output Capacitance	C_{oss}		–	97	–	
Reverse Transfer Capacitance	C_{rss}		–	85	–	
Gate to Source Charge	Q_{gs}	V_{GS}=0V to 10V, V_{DD}=25V, I_D=15A	–	3.2	–	nC
Gate to Drain Charge (Miller Charger)	Q_{gd}		–	5.7	–	
Total Gate Charge	Q_g		–	15.2	–	
Gate Resistance	R_g	–	–	0.85	–	Ω

Output Voltage Detect Function Description

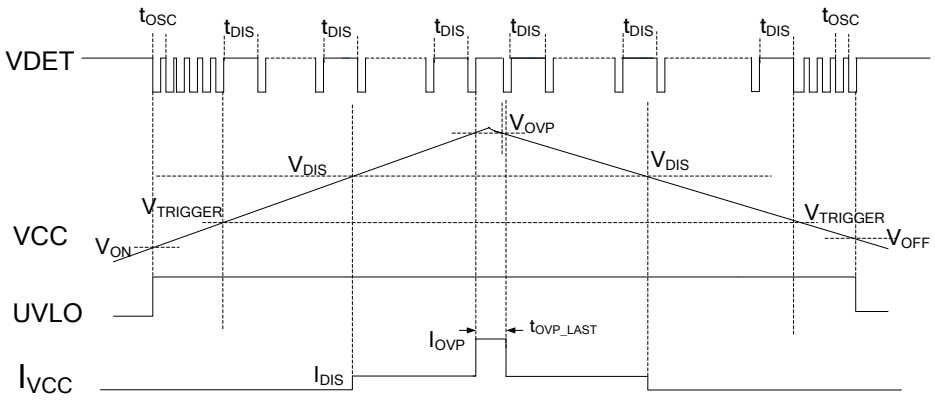


Figure 1. Typical Waveforms of APR3415B

When V_{CC} is beyond power-on voltage (V_{ON}), the APR3415B starts up. The VDET pin asserts a periodical pulse and the oscillation period is t_{OSC}. When V_{CC} is beyond the trigger voltage ($V_{TRIGGER}$), the periodical pulse at VDET pin is discontinued. When V_{CC} is beyond the discharge voltage (V_{DIS}), the discharge circuit will be enabled, and a 3mA current (I_{DIS}) will flow into VCC pin. When V_{CC} is higher than the overshoot voltage (V_{OVP}), the APR3415B will enable a discharge circuit, the discharge current (I_{OVP}) will last t_{OVP_LAST} time. After the t_{OVP_LAST} time, APR3415B will stop the discharge current and detect VCC voltage again. If V_{CC} is still higher than V_{OVP}, the t_{OVP_LAST} time discharge current will be enabled again. Once the OVP discharge current is asserted, the periodical pulse at VDET pin will be disabled.

When the V_{CC} falls below the power-off voltage (V_{OFF}), the APR3415B will shut down.

Operation Description

MOSFET Driver

The operation of the SR is described with timing diagram shown in Figure 2. APR3415B monitors the MOSFET drain-source voltage. When the drain voltage is lower than the turn-on threshold voltage V_{THON}, the IC outputs a positive drive voltage after a turn-on delay time (t_{DON}). The MOSFET will turn on and the current will transfer from the body diode into the MOSFET's channel.

In the process of drain current decreasing linearly toward zero, the drain-source voltage rises synchronically. When it rises over the turn off threshold voltage V_{THOFF}, APR3415B pulls the drive signal down after a turn off delay (t_{DOFF}).

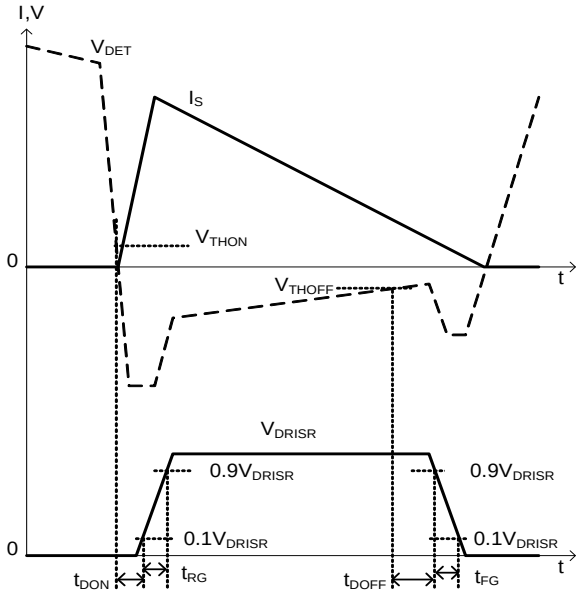


Figure 2. Typical Waveforms of APR3415B

Operation Description (continued)

Minimum On Time

When the controlled MOSFET gate is turned on, some ringing noise is generated. The minimum on-time timer blanks the V_{THOFF} comparator, keeping the controlled MOSFET on for at least the minimum on time. If V_{THOFF} falls below the threshold before minimum on time expires, the MOSFET will keep on until the end of the minimum on time.

The minimum on time is in direct proportion to the $(V_{DET}-V_{CC})*t_{ONP}$. When $(V_{DET}-V_{CC})*t_{ONP}=5V*5\mu s$, the minimum on time is about 1.8µs.

The Value and Meaning of AREF Resistor

Regarding the DCM-operating flyback converter, after the secondary rectifier stops conduction, the primary MOSFET drain-to-source ringing waveform is a result of the resonance of primary inductance and equivalent switch device output capacitance. This ringing waveform probably leads to Synchronous Rectifier error conduction. To avoid this fault occurring, APR3415B has a special function design by means of volt-second product detecting. From the sensed voltage of VDET pin to see, the volt-second product of voltage above VCC at primary switch on time is much higher than the volt-second product of each cycle ringing voltage above V_{CC}. Therefore each time before the synchronous rectifier turns on, the APR3415B judges whether the detected volt-second product of the VDET voltage above V_{CC} is higher than the threshold and then turn on synchronous Rectifier. The purpose of AREF resistor is to determine the volt-second product threshold. The APR3415B has a parameter, Kqs, which converts the R_{AREF} value to volt-second product.

$$Area2 = R_{AREF} * Kqs$$

In general, the Area1 and Area3 values depend on system design and are always fixed after system design freezes. As for Diodes Incorporated's PSR design, the Area1 value changes with primary peak-current value and Area3 value generally stays constant at all conditions. The AREF resistor design must consider the worst case, which is the minimum primary peak-current condition. Because of system design parameter distribution, Area1 and Area3 have moderate tolerance. Area2 must be designed between the middle of Area1 and Area3 to keep enough design margin.

Note: To keep the volt-second product threshold stable, a capacitor is recommended to be paralleled with AREF resistor.

$$Area3 < R_{AREF} * Kqs < Area1$$

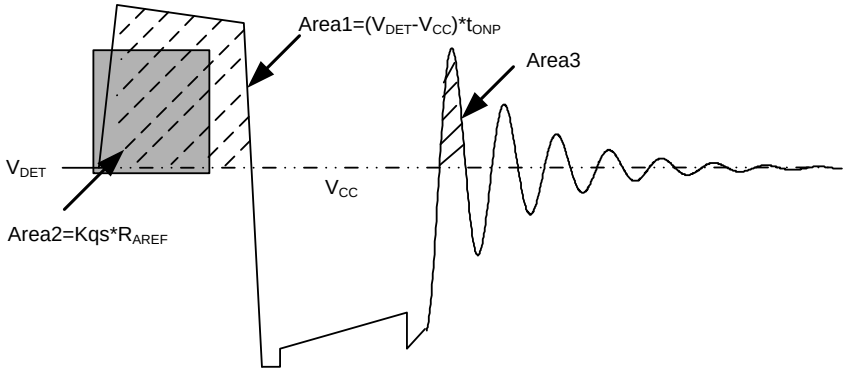


Figure 3. AREF Function

SR Minimum Operating Voltage

APR3415B sets a minimum SR operating voltage by comparing the difference between V_{DET} and the output voltage (V_{CC}). The value of V_{DET}–V_{CC} must be higher than its internal reference, APR3415B then begins to integrate the area of $(V_{DET}–V_{CC})*t_{ONP}$. If not, the area integration does not start, and the SR driver is disabled.

SR Turning off Timing Impact on PSR CV Sampling

As for the synchronous rectification on flyback power systems, SR MOSFET must turn off before the secondary side current decreases to zero in order to avoid reverse-current flow. When SR turns off in advance, the secondary current will flow through the body diode. The SR turn-off time is determined by the V_{THOFF} at a fixed system. When V_{THOFF} is closer to zero, the SR turn-on time becomes longer and body diode conduction time becomes shorter. Because of the different voltage drops between SR MOSFET and body diode, the PSR feedback signal's (V_{FB}) voltage jumps when the SR MOSFET turns off. If the PSR CV sampling time t_{SAMPLE} is too closely behind this voltage jump time, there is either an unstable system operation issue or a lower-output voltage issue.

Operation Description (continued)

To ensure stable system operation, the following equation must be met:

$t_{BODYDIODE} < t_{ONS} - t_{SAMPLE}$

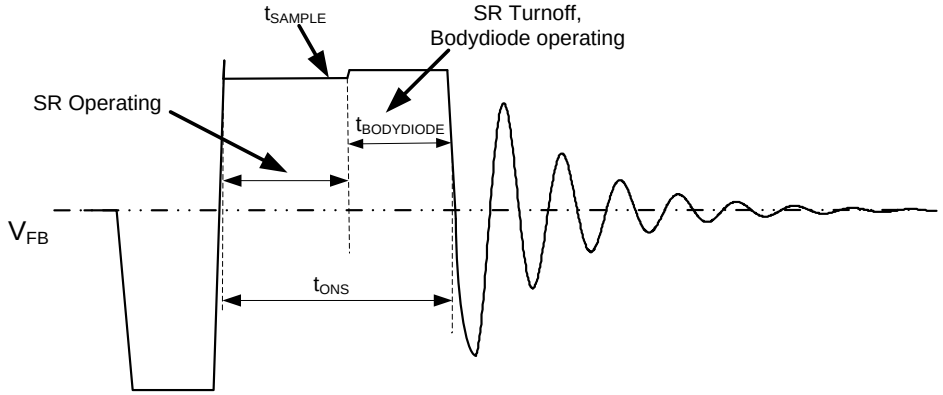


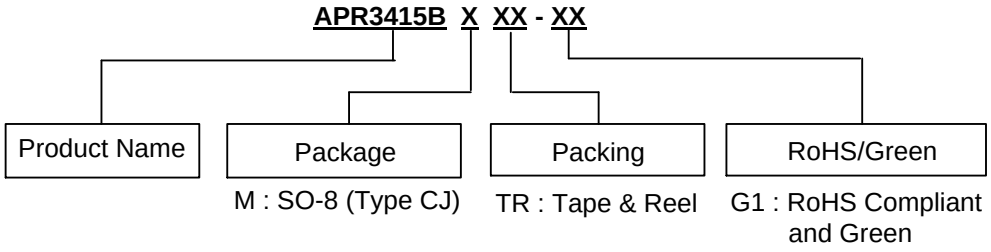
Figure 4. SR Turning off Timing Impact on PSR CV Sampling

Recommended Application Circuit Parameters

The two resistors R23 and R24 are used to pass ESD test. The value of R23 and R24 must be over 20Ω and below 47Ω respectively because of the undershoot performance. The package of R23 and R24 must be at least 0805 and there isn't any trace under these two resistors.

C_{AREF} is recommended to be paralleled with AREF resistor to keep the volt-second product threshold stable. A 20nF C_{AREF} and a 100nF C24 are recommended.

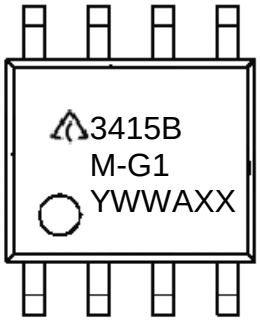
Ordering Information



Package	Temperature Range	Part Number	Marking ID	Packing
SO-8 (Type CJ)	-40 to +85°C	APR3415BMTR-G1	3415BM-G1	4000/Tape & Reel

Marking Information

(Top View)

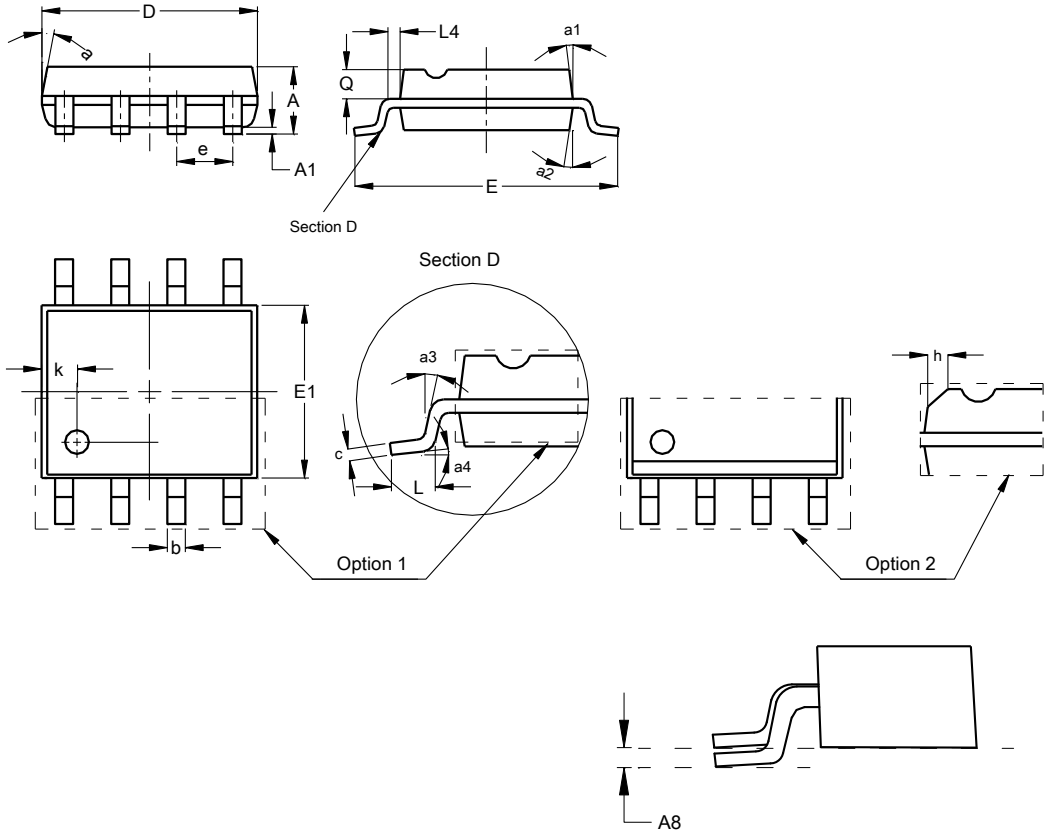


First and Second Lines: Logo and Marking ID
Third Line: Date Code
Y: Year
WW: Work Week of Molding
A: Assembly House Code
XX: 7th and 8th Digits of Batch No.

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8 (Type CJ)



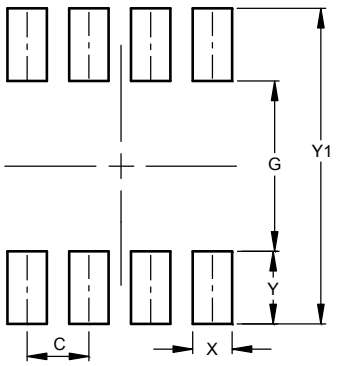
SO-8 (Type CJ)			
Dim	**Min**	**Max**	**Typ**
A	1.350	1.750	--
A1	0.100	0.300	--
b	0.300	0.510	--
c	0.150	0.250	--
D	4.700	5.100	--
E	5.800	6.200	--
E1	3.800	4.000	--
e	--	--	1.27
h	--	--	0.350
k	--	--	1.000
L	0.450	0.820	--
L4	--	--	0.320
a	7°	9°	--
a1	--	--	8°
a2	--	--	8°
a3	0°	8°	--
a4	1°	7°	--
Q	0.600	0.725	--
All Dimensions in mm			

Dimension	Value (in mm)
A8	<0.10

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8 (Type CJ)



Dimensions	Value (in mm)
C	1.270
G	3.900
X	0.650
Y	1.500
Y1	6.900

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