1. Scope

This specification is applies to Multilayer Ceramic Chip Capacitor (MLCC) for use in electric equipment for the voltage is ranging from 100V to 2 KV (not Include).

The MLCC support for Lead-Free wave and reflow soldering, and electrical characteristic and reliability are same as before. **(This product compliant with the RoHS.)**

2. Parts Number Code

HOP	0805	X	222	K	251	T	X
(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)

(1)Product

Product Code	
HOP	**Holystone Open Mode**

(2)Chip Size

Code	Length×Width	unit : mm(inch)
0805	**2.00× 1.25**	**(.079× .049)**

(3)Temperature Characteristics

Code	Temperature Characteristic	Temperature Range	Temperature Coefficient
X	**X7R**	**-55℃~+125℃**	**± 15%**

(4)Capacitance

unit :pico farads(pF)

Code	Nominal Capacitance (pF)
222	**2,200.0**

※. *If there is a decimal point, it shall be expressed by an English capital letter R*

(5)Capacitance Tolerance

Code	Tolerance	Nominal Capacitance
K	**± 10.0 %**	**More Than 10 pF**

(6)Rated Voltage

Code	Rated Voltage (Vdc)
251	**250**

(7)Tapping

Code	Type
T	**Tape & Reel**

(8)Special Requirement Code

Code	Type
X	**Polymer Termination**

3. Nominal Capacitance and Tolerance

3.1 Standard Combination of Nominal Capacitance and Tolerance

Class	Characteristic	Tolerance	Nominal Capacitance
Ⅱ	**X7R**	**K (± 10.0 %)**	**E-3, E-6 series**

3.2 E series(standard Number)

Standard No.	Application Capacitance											
E- 3	1.0				2.2				4.7			
E- 6	1.0		1.5		2.2		3.3		4.7		6.8	
E-12	1.0	1.2	1.5	1.8	2.2	2.7	3.3	3.9	4.7	5.6	6.8	8.2
E-24	1.0	1.2	1.5	1.8	2.2	2.7	3.3	3.9	4.7	5.6	6.8	8.2
	1.1	1.3	1.6	2.0	2.4	3.0	3.6	4.3	5.1	6.2	7.5	9.1

4. Operation Temperature Range

Class	Characteristic	Temperature Range	Reference Temp.
Ⅱ	**X7R**	**-55℃ ~ +125℃**	**25℃**

5. Storage Condition

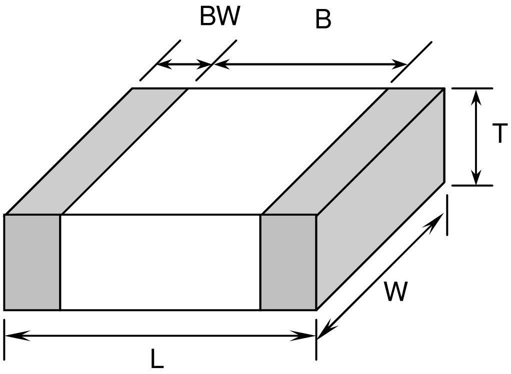
Storage Temperature：5 to 40℃

Relative Humidity：20 to 70 %

Storage Time：12 months max.

6. Dimensions

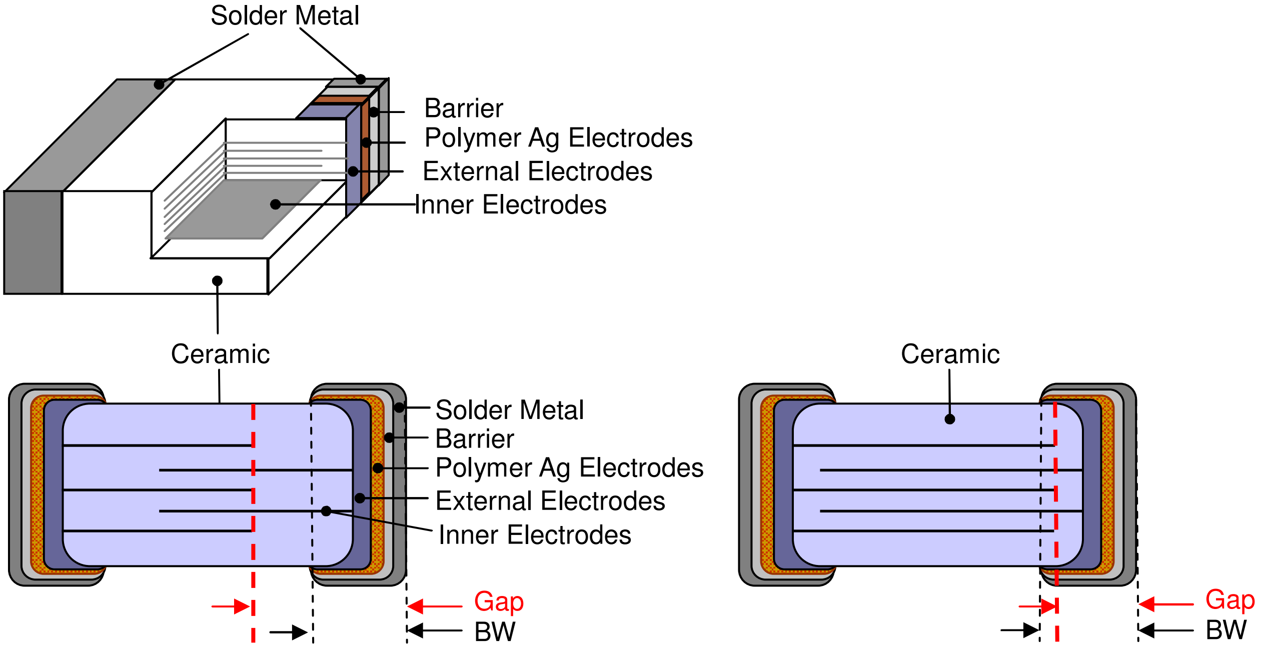
6.1 Configuration and Dimension：



Unit:mm

TYPE	L	W	T	B (min)	BW (min)
0805	2.00± 0.20	1.25± 0.20	0.85± 0.15	0.70	0.20

6.2 Open-Mode Type：

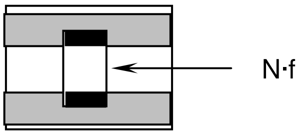
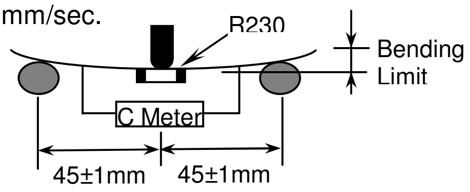


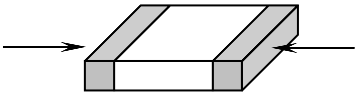
Open-Mode **Standard**

MLCC cracking could result in serious and critical failure modes. The bending crack might occur through two or more inner-electrodes of opposing polarity. Moreover, it will meet short circuit. These short circuits may lead to MLCC overheating and catastrophic failure.

Consequently, **Holy Stone** makes a particular “open-mode” design, which incorporates a “sufficient margin” in the termination structure. With introducing of open-mode design, it can effectively prevent ceramic body cracking and burnout damage during on-board application. “Open-mode design” indeed helps to reduce the risk of big damage and short circuit during on-board. However, we can’t predict the specific types of mechanical or thermal stress, so that we can’t guarantee absolute success.

7. Performance

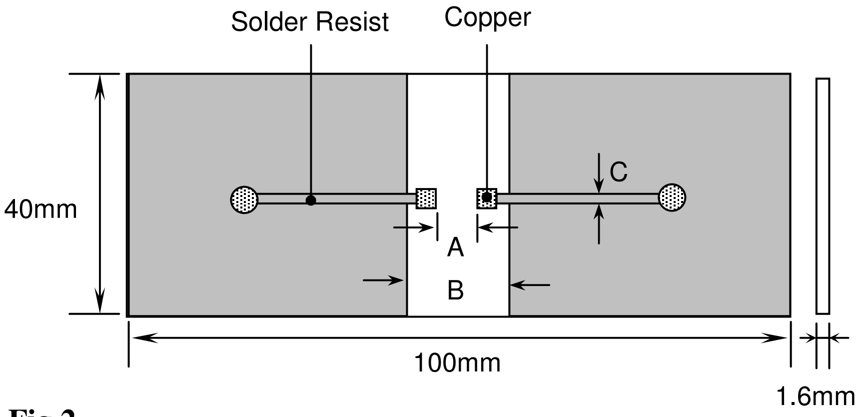
<table>
<tr><th>No.</th><th colspan="2">Item</th><th>Specification</th><th>Test Condition</th></tr>
<tr><td>1</td><td colspan="2">Visual</td><td>No abnormal exterior appearance</td><td>Visual inspection</td></tr>
<tr><td>2</td><td colspan="2">Dimension</td><td>See Page 2</td><td>Visual inspection</td></tr>
<tr><td>3</td><td colspan="2">Insulation Resistance</td><td>10,000MΩ min.</td><td>V≦500V, Rated Voltage
Charge Time：60sec.
Is applied less than 50mA current.</td></tr>
<tr><td>4</td><td>Capacitance</td><td>Class Ⅱ</td><td>Within The Specified Tolerance</td><td rowspan="2">ClassⅡ：<table><tr><th></th><th>Frequency</th><th>Voltage</th></tr><tr><td>X7R</td><td>1KHz±10%</td><td>1.0±0.2Vrms</td></tr></table>Perform a heat temperature at 150±5℃ for 30min. then place room temp. for 24±2hr.</td></tr>
<tr><td>5</td><td>Tan δ</td><td>Class Ⅱ</td><td><table><tr><th>Char.</th><th>Maximum</th></tr><tr><td colspan="2">X7R: 2.5% max.</td></tr></table></td></tr>
<tr><td>6</td><td colspan="2">Withstanding Voltage</td><td>No dielectric breakdown or mechanical breakdown</td><td>V＜500V : 200% Rated Voltage
Voltage ramp up rate≦500v/sec
for 1~5 sec. charge/discharge Current is less than 50mA.
※ Withstanding voltage testing requires immersion of the element in a isolation fluid prevent arcing on the chip surface, at voltage over 1000Vdc.</td></tr>
<tr><td>7</td><td>Temperature Capacitance Coefficient</td><td>Class Ⅱ</td><td><table><tr><th>Char.</th><th>Temp. Range</th><th>Cap. Change(%)</th></tr><tr><td>X7R</td><td>-55℃~+125℃</td><td>± 15%</td></tr></table></td><td>ClassⅡ:
(C2-C1)/C1 × 100%
C1:Capacitance at standard temperature(25℃)
C2: Capacitance at test temperature (T2)</td></tr>
<tr><td>8</td><td colspan="2">Adhesive Strength of Termination</td><td>No indication of peeling shall occur on the terminal electrode.</td><td>Pull force shall be applied for 10± 1 second.
≦0603----5N(≒ 0.5 Kg·f)
＞0603----10N(≒1.0 Kg·f)
 </td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">Resistance to Flexure of Substrate</td><td>Appear-ance</td><td>No mechanical damage shall be occur.</td><td rowspan="2">Bending shall be applied to the 3.0 mm with 1.0 mm/sec.
 </td></tr>
<tr><td>C-Meter</td><td>Capacitance Change<table><tr><th>Char.</th><th>Cap. Change</th></tr><tr><td>X7R</td><td>≦ ± 12.5%</td></tr></table></td></tr>
</table>

<table>
<tr><th>No.</th><th colspan="2">Item</th><th colspan="3">Specification</th><th>Test Condition</th></tr>
<tr><td>10</td><td colspan="2">Solderability</td><td colspan="3">More than 90% of the terminal surface is to be soldered newly, so metal part does not come out or dissolve .
</td><td>Solder Temperature : 245± 5℃
Dip Time : 5 ± 0.5 sec.
Immersing Speed : 25±10% mm/s
Solder : Lead Free Solder
Flux :Rosin
Preheat : At 80~120 ℃ for 10~30sec.</td></tr>
<tr><td rowspan="6">11</td><td rowspan="6">Resistance To Soldering Heat</td><td>Appearance</td><td colspan="3">No mechanical damage shall occur.</td><td rowspan="6">ClassⅡ capacitor shall be set for 48±4 hours at room temperature after one hour heat treatment at 150 +0/-10℃ before initial measure.
Preheat : At 150± 10℃ For 60~120sec.
Dip : Solder Temperature of 260± 5℃
Dip Time : 10 ± 1sec.
Immersing Speed : 25±10% mm/s
Flux :Rosin
Measure at room temperature after cooling for ClassⅡ: 48 ± 4 Hours</td></tr>
<tr><td rowspan="2">Capacitance</td><td colspan="2">Characteristic</td><td>Cap. Change</td></tr>
<tr><td>Class Ⅱ</td><td>X7R</td><td>Within ± 10%</td></tr>
<tr><td>Tan δ ClassⅡ</td><td colspan="3">To satisfy the specified initial value</td></tr>
<tr><td>Insulation Resistance</td><td colspan="3">To satisfy the specified initial value</td></tr>
<tr><td>Withstand Voltage</td><td colspan="3">To satisfy the specified initial value</td></tr>
<tr><td rowspan="5">12</td><td rowspan="5">Tempera-. ture Cycle</td><td>Appearance</td><td colspan="3">No mechanical damage shall occur</td><td rowspan="5">ClassⅡ capacitor shall be set for 48± 4 hours at room temperature after one hour heat treatment at 150 +0/-10 ℃ before initial measure.
Capacitor shall be subjected to five cycles of the temperature cycle as following:
<table><tr><th>Step</th><th>Temp.(℃)</th><th>Time(min)</th></tr><tr><td>1</td><td>Min Rated Temp. +0/-3</td><td>30</td></tr><tr><td>2</td><td>25</td><td>3</td></tr><tr><td>3</td><td>Max Rated Temp. +3/-0</td><td>30</td></tr><tr><td>4</td><td>25</td><td>3</td></tr></table>Measure at room temperature after cooling for ClassⅡ:48 ± 4 Hrs
Solder the capacitor on P.C. board shown in Fig 2. before testing.</td></tr>
<tr><td rowspan="2">Capacitance</td><td colspan="2">Characteristic</td><td>Cap. Change</td></tr>
<tr><td>Class Ⅱ</td><td>X7R</td><td>Within ± 7.5%</td></tr>
<tr><td>Tan δ ClassⅡ</td><td colspan="3">To satisfy the specified initial value</td></tr>
<tr><td>Insulation Resistance</td><td colspan="3">To satisfy the specified initial value</td></tr>
<tr><td rowspan="6">13</td><td rowspan="6">Humidity</td><td>Appearance</td><td colspan="3">No mechanical damage shall occur</td><td rowspan="6">ClassⅡ capacitor shall be set for 48± 4 hours at room temperature after one hour heat treatment at 150+0/-10 ℃ before initial measure.
Temperature : 40± 2℃
Relative Humidity : 90 ~ 95%RH
Test Time : 500 ＋12/－0Hr
Measure at room temperature after cooling for ClassⅡ : 48 ± 4Hrs
Solder the capacitor on P.C. board shown in Fig 2. before testing.</td></tr>
<tr><td rowspan="2">Capacitance</td><td colspan="2">Characteristic</td><td>Cap. Change</td></tr>
<tr><td>Class Ⅱ</td><td>X7R</td><td>Within ± 15%</td></tr>
<tr><td rowspan="2">Tan δ ClassⅡ</td><td colspan="2">Char.</td><td>Maximum</td></tr>
<tr><td colspan="3">X7R: 5.0% max.</td></tr>
<tr><td>Insulation Resistance</td><td colspan="3">1,000MΩ min.</td></tr>
</table>

No.	Item		Specification			Test Condition
14	High Temperature Load (Life Test)	Appearance	No mechanical damage shall occur			Class Ⅱ capacitors applied DC voltage (following table) is applied for one hour at maximum operation temperature ±3℃ then shall be set for 48±4 hours at room temperature and the initial measurement shall be conducted. Applied Voltage : 120%Rated Voltage Test Time : 1000 +12/-0Hr Current Applied : 50 mA Max. Measure at room temperature after cooling for Class Ⅱ : 48 ± 4 Hours
		Capacitance	Characteristic		Cap. Change	
			Class Ⅱ	X7R	Within ± 15%	
		Tan δ Class Ⅱ	Char.	maximum		
			X7R: 5.0% max.			
		Insulation Resistance	1,000MΩ min.			
15	Vibration	Appearance	No mechanical damage shall occur			Solder the capacitor on P.C. Board shown in Fig 2. before testing. Vibrate the capacitor with amplitude of 1.5mm P-P changing the frequencies from 10Hz to 55Hz and back to 10Hz in about 1 min. Repeat this for 2 hours each in 3perpendicular directions.
		Capacitance	Characteristic		Cap. Change	
			Class Ⅱ	X7R	Within ± 7.5%	
		Tan δ Class Ⅱ	To satisfy the specified initial value			
		Insulation Resistance	To satisfy the specified initial value			

Fig.1

P.C. Board for Bending Strength Test



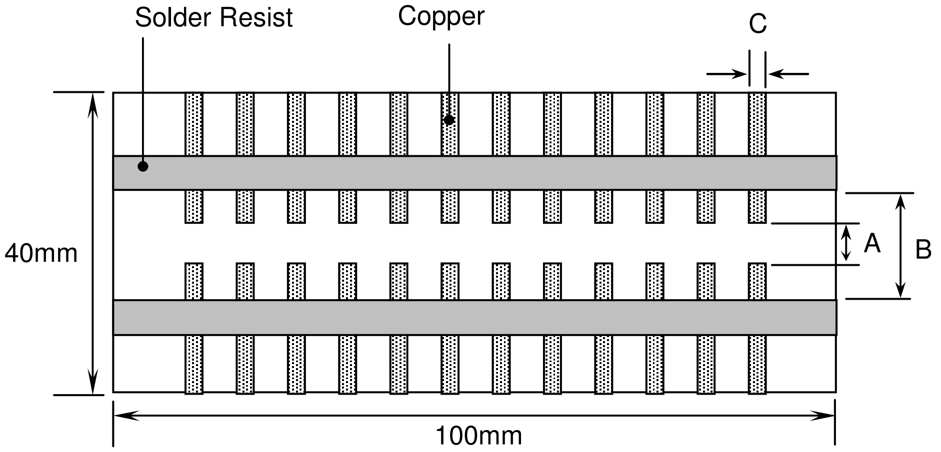
Material : Glass Epoxy Substrate

▨ : Copper (Thickness : 0.035mm)

▢ : Solder Resist

Fig.2

Test Substrate



Material : Glass Epoxy Substrate

▨ : Copper (Thickness : 0.035mm)

▢ : Solder Resist

Thickness : 1.6 mm

Unit:mm

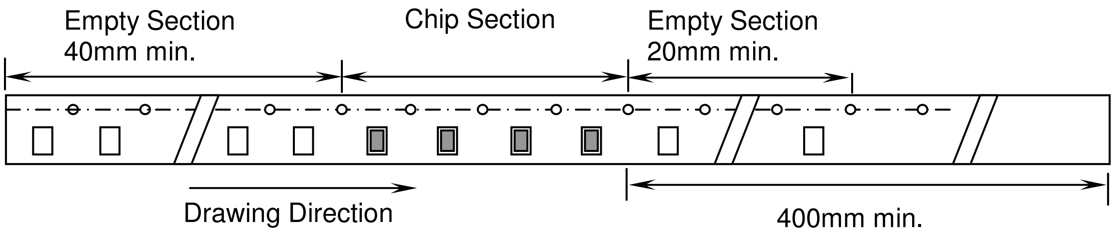
Type	A	B	C
0201	0.2	0.9	0.4
0402	0.5	1.5	0.6
0603	1.0	3.0	1.0
0805	1.2	4.0	1.6
1206	2.2	5.0	2.0
1210	2.2	5.0	2.9
1808	3.5	7.0	2.5
1812	3.5	7.0	3.7
1825	3.5	7.0	6.9
2208	4.5	8.0	2.5
2211	4.5	8.0	3.0
2220	4.5	8.0	5.6
2225	4.5	8.0	7.0

8. Packing

8.1 Bulk Packing

According to customer request.

8.2 Chip Capacitors Tape Packing



8.3 Material And Quantity

Tape Material	0201	0402	0603/0805	
	T≦0.33mm	T≦0.55mm	T≦0.90mm	T＞0.90mm
Paper	15,000 pcs/Reel	10,000 pcs/Reel	4,000 pcs/Reel	NA
Plastic	NA	NA	NA	3,000 pcs/Reel

Tape Material	1206		
	T≦0.90mm	0.90mm＜T≦1.25mm	T＞1.25mm
Paper	4,000 pcs/Reel	NA	NA
Plastic	NA	3,000 pcs/Reel	2,000 pcs/Reel

Tape Material	1808/1210		
	T≦1.25mm	1.25mm＜T≦2.40mm	T＞2.40mm
Paper	NA	NA	NA
Plastic	3000 pcs/Reel	2000 pcs/Reel	500/1,000 pcs/Reel

Tape Material	1812/2211/2220		1825/2225		2208
	T≦2.20mm	T＞2.20mm	T≦2.20mm	T＞2.20mm	T≦2.20mm
Paper	NA	NA	NA	NA	NA
Plastic	1000 pcs/Reel	700 pcs/Reel	700 pcs/Reel	400 pcs/Reel	1000 pcs/Reel

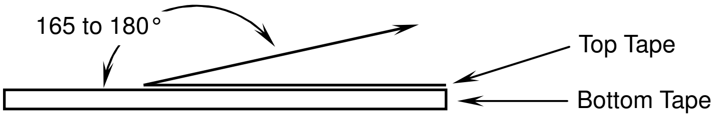
NA：Not Available

8.4 Cover Tape Reel Off Force

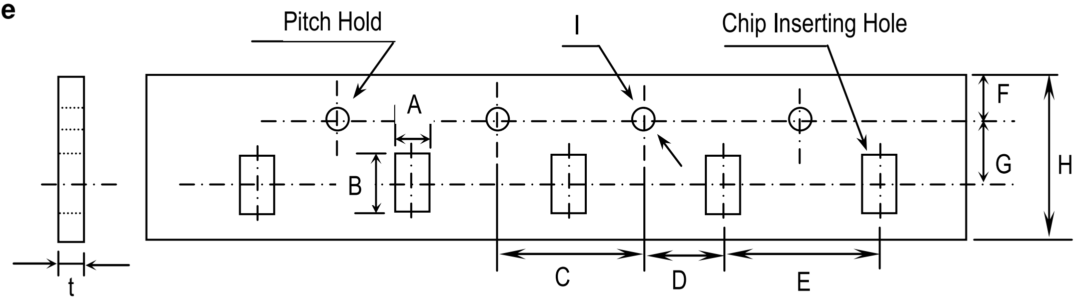
8.4.1 Peel-Off Force

5 g·f ≦Peel-Off Force ≦70 g·f

8.4.2 Measure Method



8.5 Paper Tape

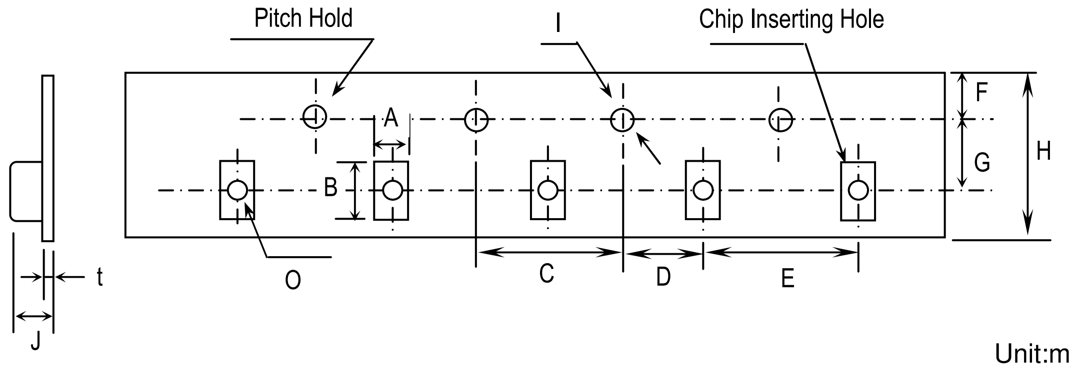


Unit:mm

TYPE	A	B	C	D	E
0201	0.37± 0.1	0.67± 0.1	4.00± 0.1	2.00± 0.05	2.00± 0.1
0402	0.61± 0.1	1.20± 0.1			
0603	1.10± 0.2	1.90± 0.2			4.00± 0.1
0805	1.50± 0.2	2.30± 0.2			
1206	1.90± 0.2	3.50± 0.2			
1210	2.90± 0.2	3.60± 0.2			

TYPE	F	G	H	I	t
0201	1.75± 0.10	3.50± 0.05	8.0± 0.30	φ 1.50 +0.10/-0	1.10 max.
0402					
0603					
0805					
1206					
1210					

8.6 Plastic Tape



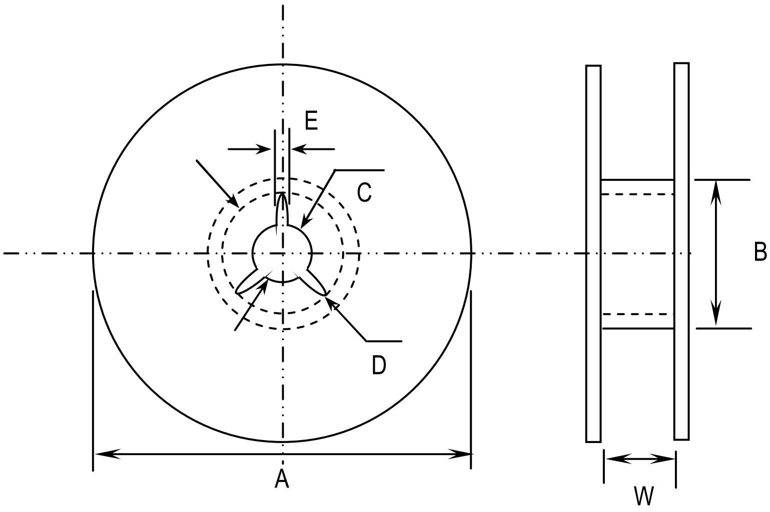
Unit:mm

Type	A	B	C	D	E	F
0805	1.5±0.2	2.3±0.2	4.0± 0.1	2.0± 0.05	4.0± 0.1	1.75± 0.1
1206	1.9±0.2	3.5±0.2				
1210	2.9±0.2	3.6±0.2				
1808	2.5±0.2	4.9±0.2				
1812	3.6±0.2	4.9±0.2			8.0± 0.1	
1825	6.9±0.2	4.9±0.2				
2208	2.5±0.2	6.1±0.2				
2211	3.2±0.2	6.1±0.2				
2220	5.4±0.2	6.1±0.2				
2225	6.9±0.2	6.1±0.2				

Type	G	H	I	J	t	O
0805	3.5± 0.05	8.0± 0.3	φ 1.5+0.1/-0	3.0 max.	0.3 max.	1.0± 0.1
1206						
1210						
1808	5.5± 0.05	12.0 ± 0.3		4.0 max.		1.5± 0.1
1812						
1825						
2208						
2211						
2220						
2225						

8.7 Reel Dimensions

Reel Material：Polystyrene



Unit:mm

Type	A	B	C	D	E	W
0201	φ 382 max	φ 50 min	φ 13± 0.5	φ 21± 0.8	2.0±0.5	10± 0.15
0402						
0603						
0805						
1206						
1210						
1808	φ 178±0.2	φ 60±0.2				13±0.3
1812						
1825						
2208						
2211						
2220						
2225						

Precautionary Notes:

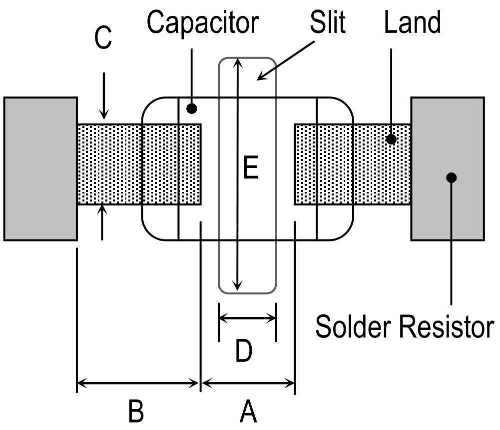
1. Storage

Store the capacitors where the temperature and relative humidity don’t exceed 40℃ and 70%RH. We recommend that the capacitors be used within 12 months from the date of manufacturing. Store the products in the original package and do not open the outer wrapped, polyethylene bag, till just before usage. If it is open, seal it as soon as possible or keep it in a desiccant with a desiccation agent.

2. Construction of Board Pattern

Improper circuit layout and pad/land size may cause excessive or not enough solder amount on the PC board. Not enough solder may create weak joint, and excessive solder may increase the potential of mechanical or thermal cracks on the ceramic capacitor. Therefore we recommend the land size to be as shown in the following table:

2.1 Size and recommend land dimensions for reflow soldering .



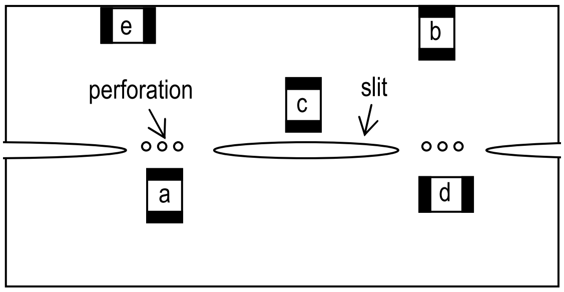
EIA Code	Chip (mm)		Land (mm)				
	L	W	A	B	C	D	E
0201	0.60	0.30	0.2~0.3	0.2~0.4	0.2~0.4	--	--
0402	1.00	0.50	0.3~0.5	0.3~0.5	0.4~0.6	--	--
0603	1.60	0.80	0.4~0.6	0.6~0.7	0.6~0.8	--	--
0805	2.00	1.25	0.7~0.9	0.6~0.8	0.8~1.1	--	--
1206	3.20	1.60	2.2~2.4	0.8~0.9	1.0~1.4	1.0~2.0	3.2~3.7
1210	3.20	2.50	2.2~2.4	1.0~1.2	1.8~2.3	1.0~2.0	4.1~4.6
1808	4.60	2.00	2.8~3.4	1.8~2.0	1.5~1.8	1.0~2.8	3.6~4.1
1812	4.60	3.20	2.8~3.4	1.8~2.0	2.3~3.0	1.0~2.8	4.8~5.3
1825	4.60	6.35	2.8~3.4	1.8~2.0	5.1~5.8	1.0~4.0	7.1~8.3
2208	5.70	2.00	4.0~4.6	2.0~2.2	1.5~1.8	1.0~4.0	3.6~4.1
2211	5.70	2.80	4.0~4.6	2.0~2.2	2.0~2.6	1.0~4.0	4.4~4.9
2220	5.70	5.00	4.0~4.6	2.0~2.2	3.5~4.8	1.0~4.0	6.6~7.1
2225	5.70	6.35	4.0~4.6	2.0~2.2	5.1~5.8	1.0~4.0	7.1~8.3

2.2 Mechanical strength varies according to location of chip capacitors on the P.C. board.

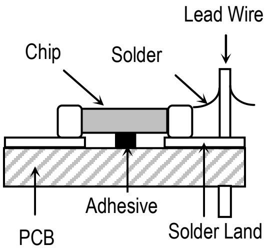
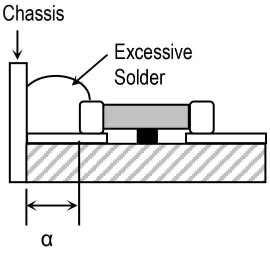
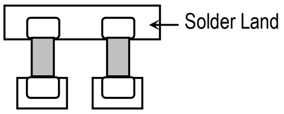
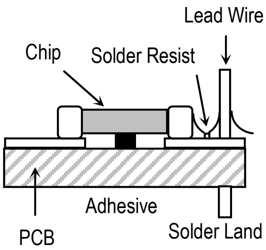
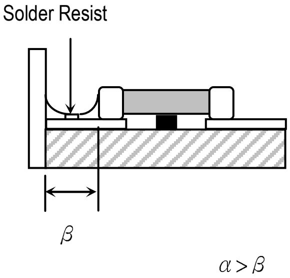
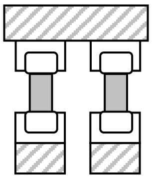
Design layout of components on the PC board such a way to minimize the stress imposed on the components, upon flexure of the boards in depanelization or other processes.

Component layout close to the edge of the board or the “depanelization line” is not recommended.

Susceptibility to stress is in the order of: a>b>c and d>e



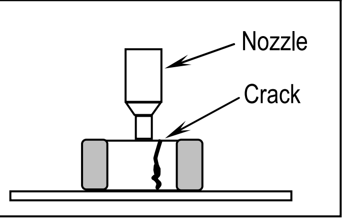
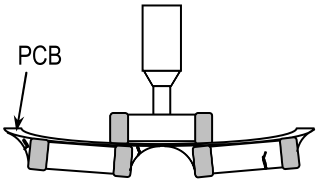
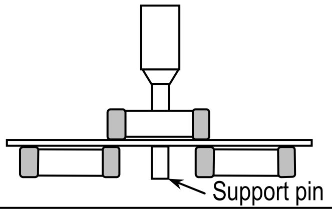
2.3 Layout Recommendation

Example	Use of Common Solder Land	Solder With Chassis	Use of Common Solder Land With Other SMD
Need to Avoid			
Recommendation			

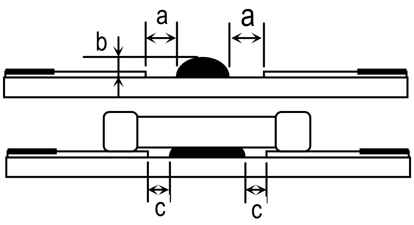
3. Mounting

3.1 Sometimes crack is caused by the impact load due to suction nozzle in pick and place operation.

In pick and place operation, if the low dead point is too low, excessive stress is applied to component. This may cause cracks in the ceramic capacitor, therefore it is required to move low dead point of a suction nozzle to the higher level to minimize the board warp age and stress on the components. Nozzle pressure is typically adjusted to 1N to 3N (static load) during the pick and place operation.

Excessive Stress	Warping of Board	Warping of Board
		

3.2 Amount of Adhesive



Example : 0805 & 1206

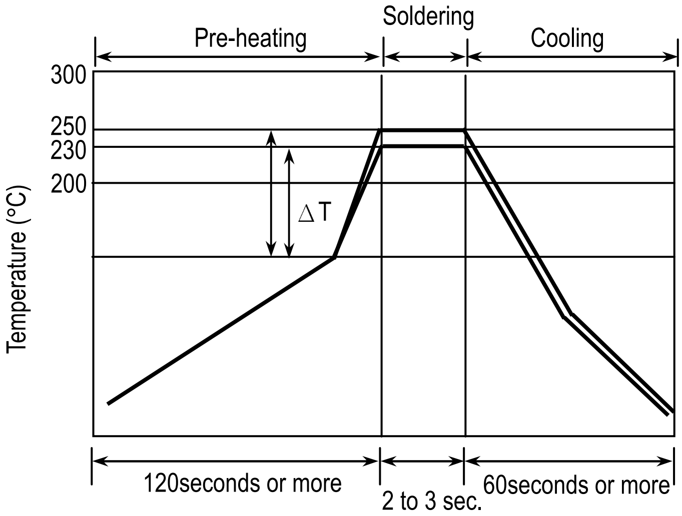
a	0.2mm min.
b	70 ~ 100 μm
c	Do not touch the solder land

4. Soldering

4.1. Wave Soldering

Most of components are wave soldered with solder at 230 to 250℃. Adequate care must be taken to prevent the potential of thermal cracks on the ceramic capacitors. Refer to the soldering methods below for optimum soldering benefits.

Recommend flow soldering temperature Profile



Soldering Method	Change in Temp.(℃)
1206 and Under	ΔT ≤ 100~130 max.

To optimize the result of soldering, proper preheating is essential:

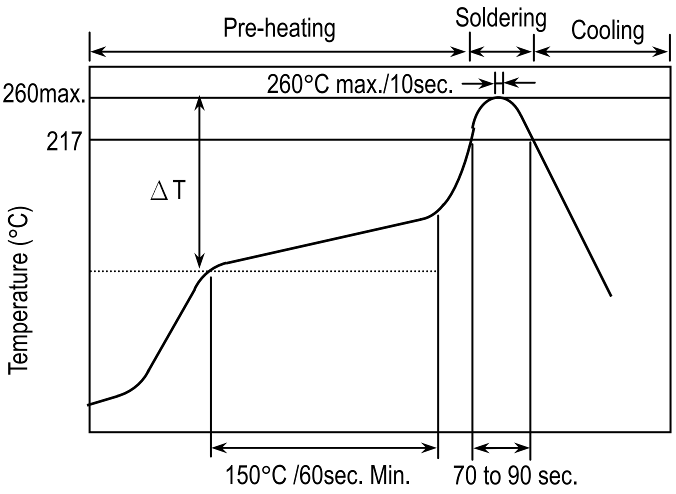
1) Preheat temperature is too low
   a. Flux flows to easily
   b. Possibility of thermal cracks
2) Preheat temperature is too high
   a. Flux deteriorates even when oxide film is removed
   b. Causes warping of circuit board
   c. Loss of reliability in chip and other components

Cooling Condition:
Natural cooling using air is recommended. If the chips are dipped into a solvent for cleaning, the temperature difference (ΔT) between the solvent and the chips must be less than 100℃.

4.2 Reflow Soldering

Preheat and gradual increase in temperature to the reflow temperature is recommended to decrease the potential of thermal crack on the components. The recommended heating rate depends on the size of component, however it should not exceed 3℃/Sec.

Recommend reflow profile for Lead-Free soldering temperature Profile (MIL-STD-202G #210F)

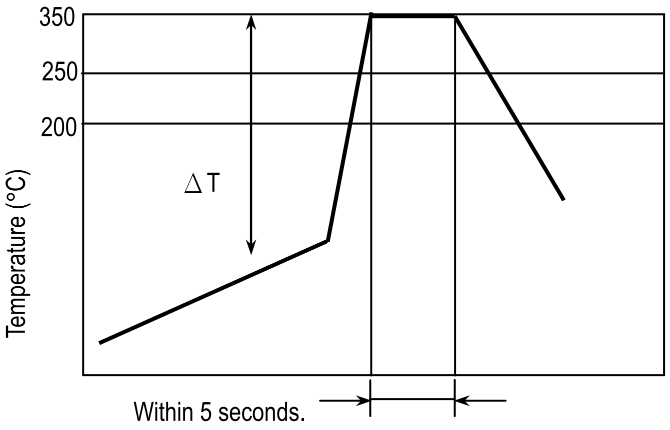


※ The cycles of soldering : Twice (max.)

Soldering Method	Change in Temp.(℃)
1206 and Under	ΔT ≦ 190 ℃
1210 and Over	ΔT ≦ 130 ℃

4.3 Hand Soldering

Sudden temperature change in components, results in a temperature gradient recommended in the following table, and therefore may cause internal thermal cracks in the components. In general a hand soldering method is not recommended unless proper preheating and handling practices have been taken. Care must also be taken not to touch the ceramic body of the capacitor with the tip of solder Iron.



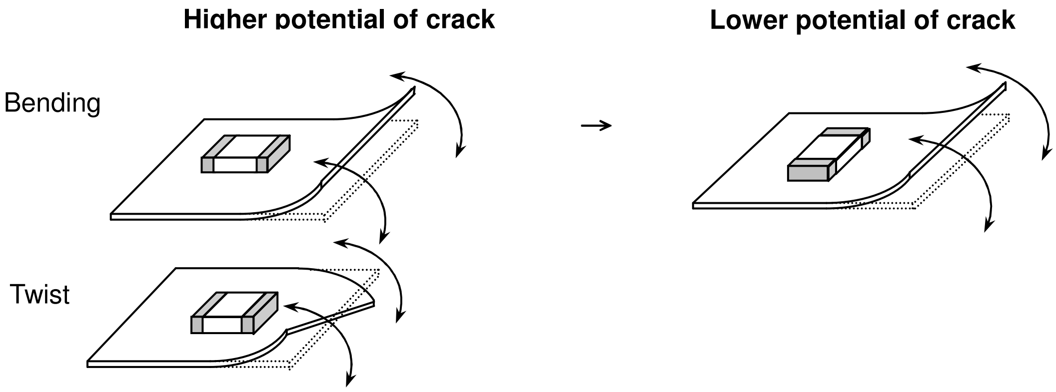
Soldering Method	Change in Temp.(℃)
1206 and Under	ΔT ≦ 190 ℃
1210 and Over	ΔT ≦ 130 ℃

How to Solder Repair by Solder Iron

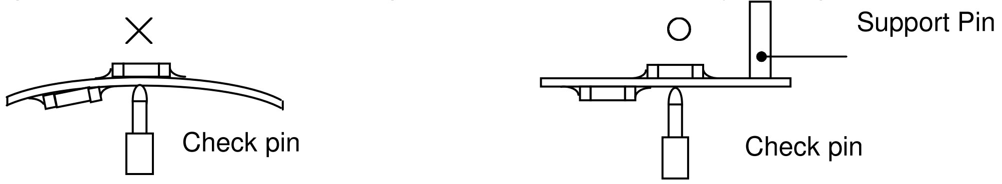
1) Selection of the soldering iron tip
   The required temperature of solder iron for any type of repair depends on the type of the tip, the substrate material, and the solder land size.
2) recommended solder iron condition
   a.) Preheat the substrate to (60℃ to 120℃) on a hot plate. Note that due to the heat loss, the actual setting of the hot plate may have to be higher. (For example 100℃ to 150℃)
   b.) Soldering iron power shall not exceed 30 W.
   c.) Soldering iron tip diameter shall not exceed 3mm.
   d.) Temperature of iron tip shall not exceed 350℃., and the process should be finished within 5 seconds. (refer to MIL-STD-202G)
   f.) Do not touch the ceramic body with the tip of solder iron. Direct contact of the soldering iron tip to ceramic body may cause thermal cracks.
   g.) After soldering operation, let the products cool down gradually in the room temperature.

5. Handling after chip mounted

5.1 Proper handling is recommended, since excessive bending and twist of the board, depends on the orientation of the chip on the board, may induce mechanical stress and cause internal crack in the capacitor.



5.2 There is a potential of crack if board is warped due to excessive load by check pin

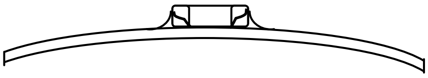


5.3 Mechanical stress due to warping and torsion.

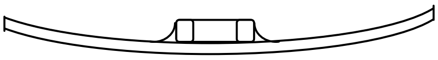
(a) Crack occurrence ratio will be increased by manual separation.

(b) Crack occurrence ratio will be increased by tensile force , rather than compressive force.

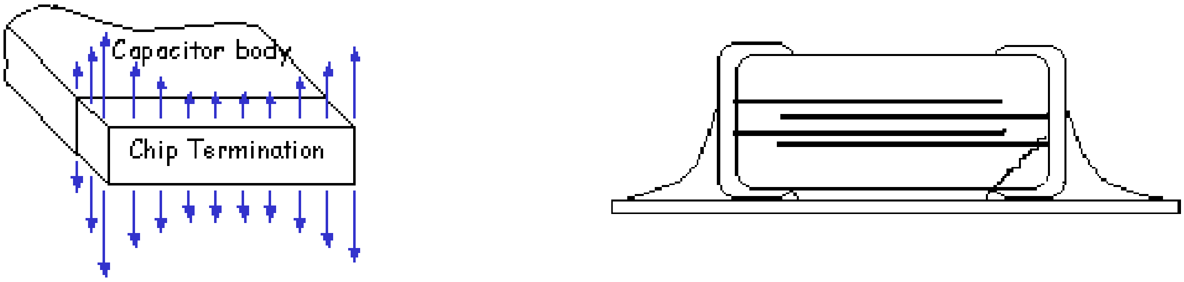
✕ :Tensile Stress



○ :Compressive Stress

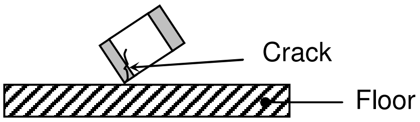


Capacitor Stress Analysis

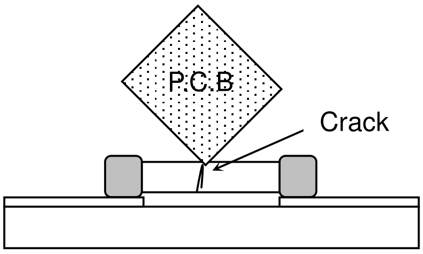


6. Handling of Loose Chip Capacitor

6.1 If dropped the chip capacitor may crack.



6.2 In piling and stacking of the P.C. boards after mounting for storage or handling, the corner of the P.C. board may hit the chip capacitor mounted on another board to cause crack.



7. Safekeeping condition and period

For safekeeping of the products, we recommend to keep the storage temperature between +5 to +40℃ and under humidity of 20 to 70% RH. The shelf life of capacitors is 12 months.