



General Description

The QN3103M3N is the highest performance trench N-Channel MOSFET with extreme high cell density, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The QN3103M3N meet the RoHS and Green Product requirement with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Green Device Available

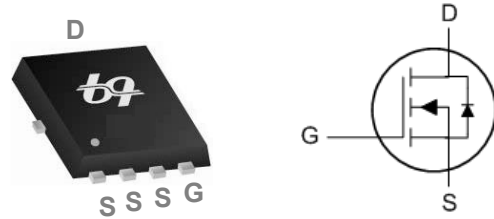
Product Summary

BVDSS	RDSON (VGS=10V)	ID (Tc=25°C)
30V	5.9mΩ	55A

Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

PRPAK 3X3 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	30	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	55	A
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ 10V ¹	34	A
I _D @T _A =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	13	A
I _D @T _A =70°C	Continuous Drain Current, V _{GS} @ 10V ¹	10	A
I _{DM}	Pulsed Drain Current ²	110	A
EAS	Single Pulse Avalanche Energy ³	54	mJ
I _{AS}	Avalanche Current	32.9	A
P _D @T _C =25°C	Total Power Dissipation ⁴	27.7	W
P _D @T _A =25°C	Total Power Dissipation ⁴	1.6	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-Ambient ¹	---	75	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	4.5	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	0.011	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=15A$	---	4.7	5.9	m Ω
		$V_{GS}=4.5V, I_D=10A$	---	6.9	9.0	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	---	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-4.2	---	$\text{mV}/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=24V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=24V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=5V, I_D=10A$	---	20	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	1.3	---	Ω
Q_g	Total Gate Charge (10V)	$V_{DS}=15V, V_{GS}=10V, I_D=10A$	---	15.2	---	nC
$Q_{g4.5V}$	Total Gate Charge (4.5V)	$V_{DS}=15V, V_{GS}=4.5V, I_D=10A$	---	7.7	---	
Q_{gs}	Gate-Source Charge		---	2.2	---	
Q_{gd}	Gate-Drain Charge		---	3.1	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=15V, V_{GS}=10V, R_G=3.3\Omega, I_D=10A$	---	7.0	---	ns
T_r	Rise Time		---	39.0	---	
$T_{d(off)}$	Turn-Off Delay Time		---	15.5	---	
T_f	Fall Time		---	5.8	---	
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	837	---	pF
C_{oss}	Output Capacitance		---	475	---	
C_{rss}	Reverse Transfer Capacitance		---	63	---	

Guaranteed Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy ⁵	$V_{DD}=25V, L=0.1\text{mH}, I_{AS}=24A$	28.8	---	---	mJ

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,6}	$V_G=V_D=0V$, Force Current	---	---	55	A
I_{SM}	Pulsed Source Current ^{2,6}		---	---	110	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1.2	V
trr	Reverse Recovery Time	$I_F=10A, dI/dt=100A/\mu s, T_J=25^\circ\text{C}$	---	28.7	---	nS
Qrr	Reverse Recovery Charge		---	12.3	---	nC

Note :

- The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- The EAS data shows Max. rating. The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1\text{mH}$
- The power dissipation is limited by 150°C junction temperature
- The Min. value is 100% EAS tested guarantee.
- The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

All information provided in this document is subjected to important notice

Typical Characteristics

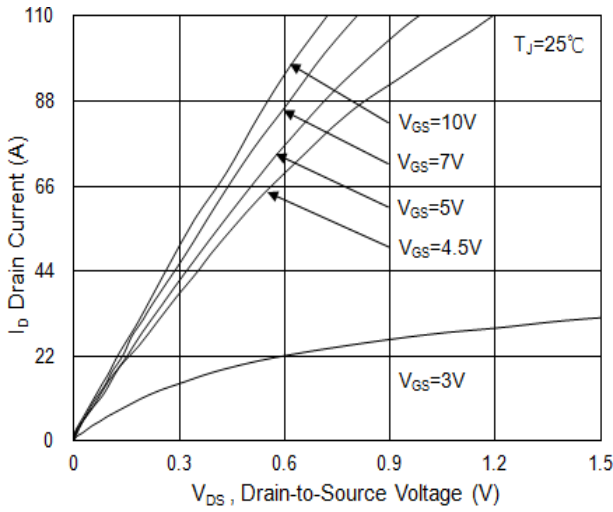


Fig.1 Typical Output Characteristics

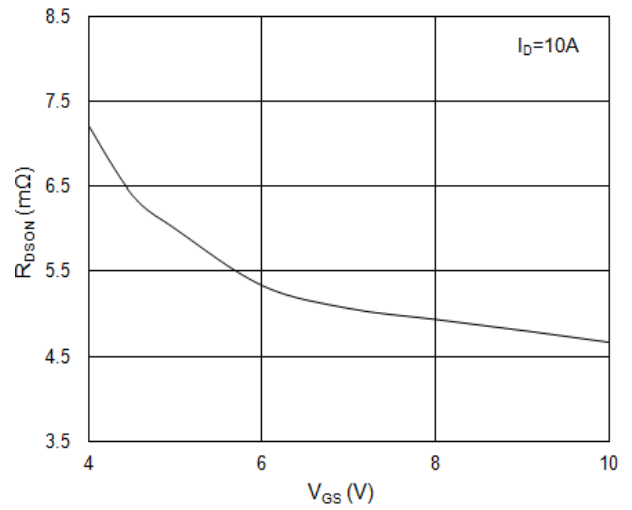


Fig.2 On-Resistance vs. Gate-Source

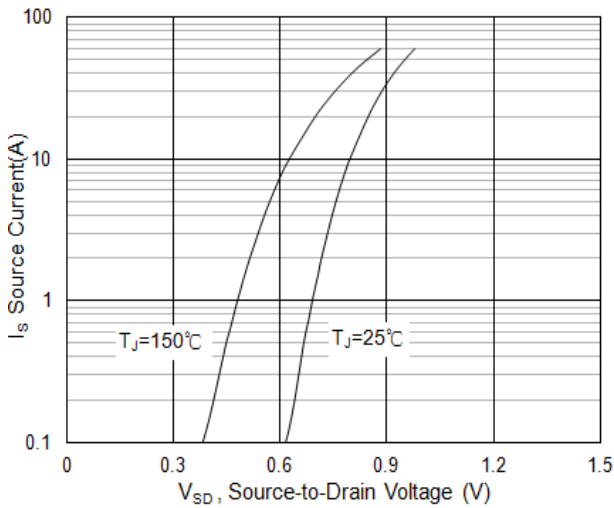


Fig.3 Forward Characteristics of Reverse

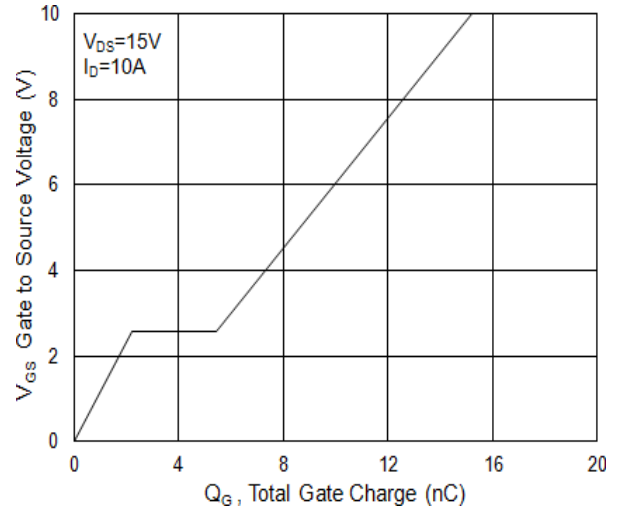


Fig.4 Gate-Charge Characteristics

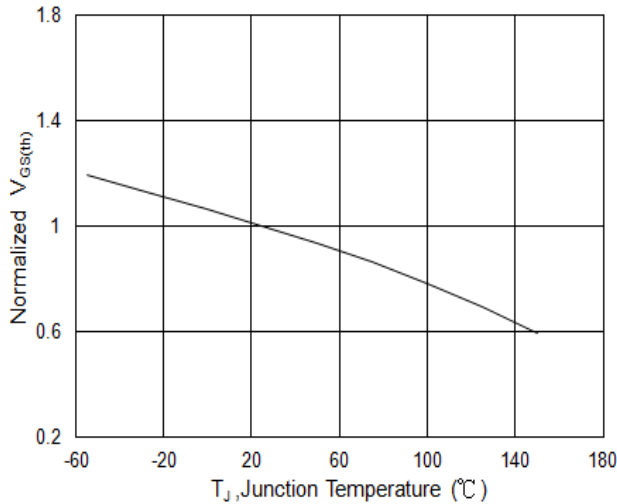


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

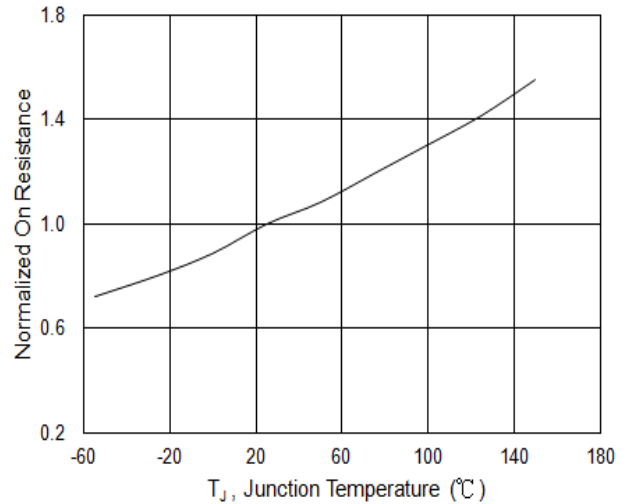


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

N-Channel 30V Fast Switching MOSFET

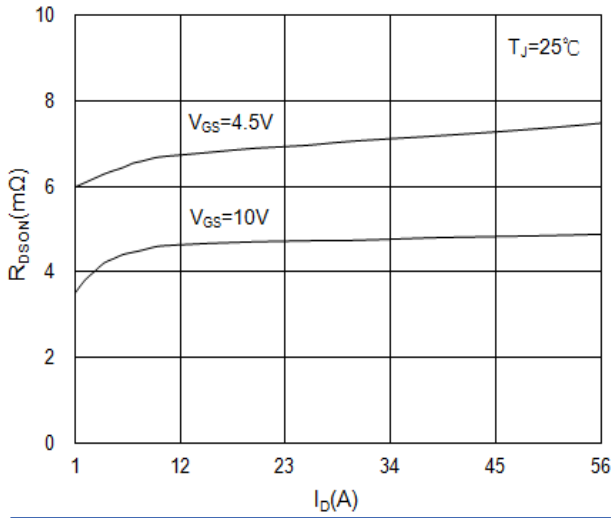


Fig.7 Drain-Source On-State Resistance

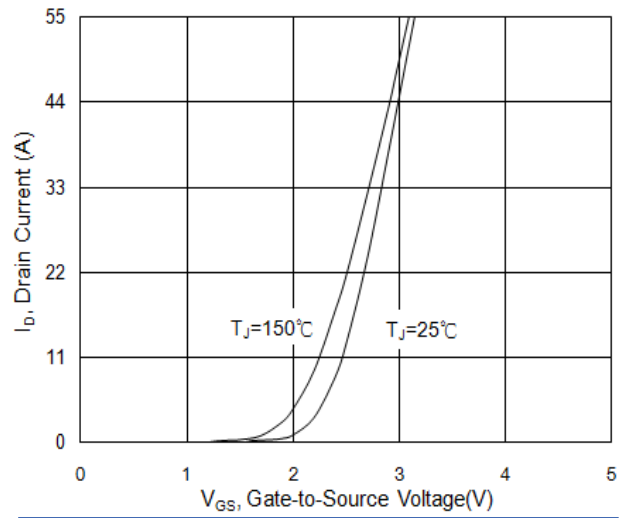


Fig.8 Transfer Characteristics

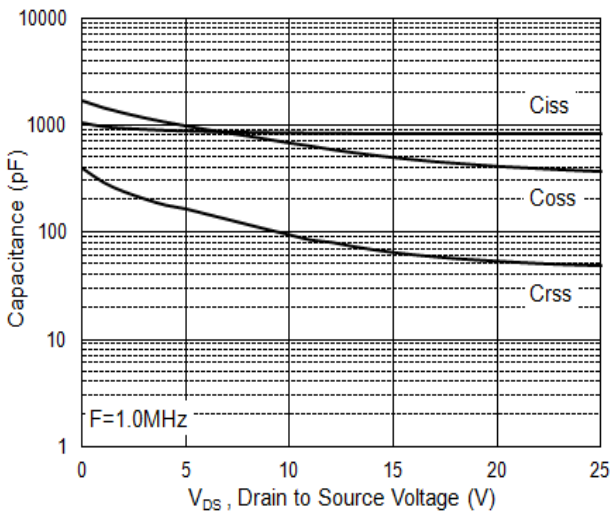


Fig.9 Capacitance

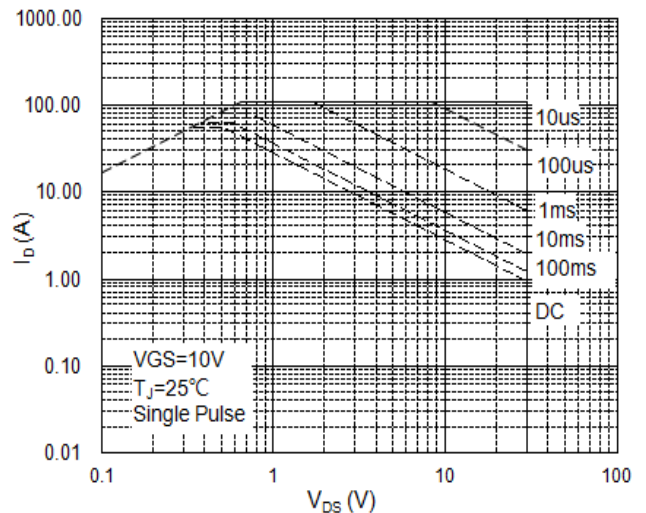


Fig.10 Safe Operating Area

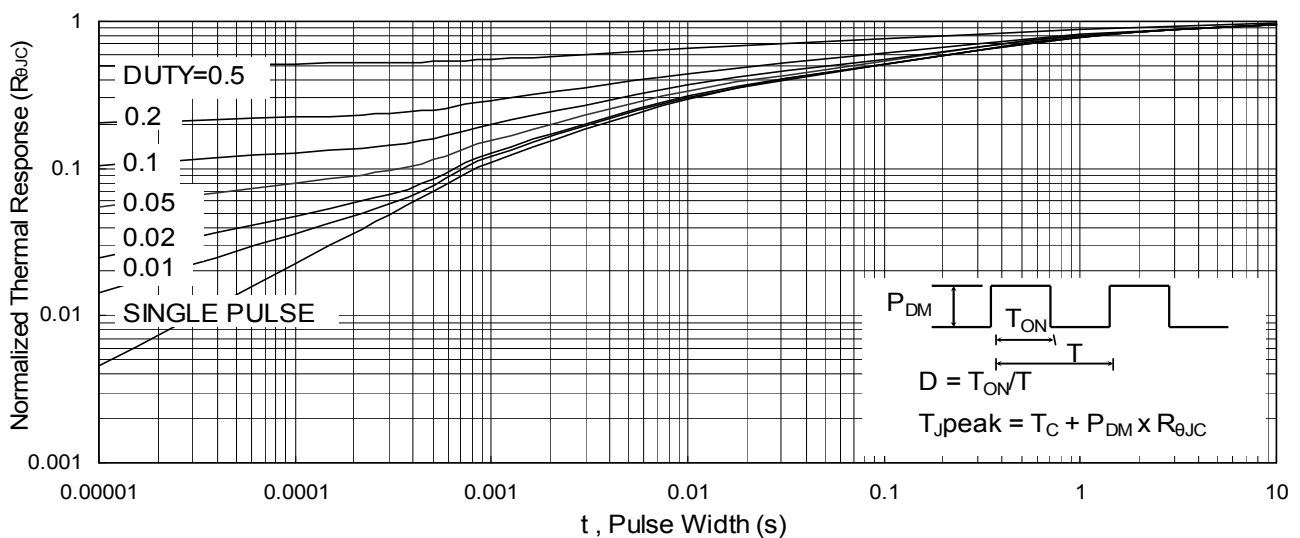
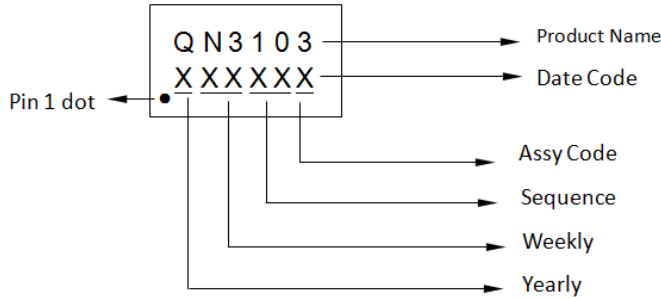
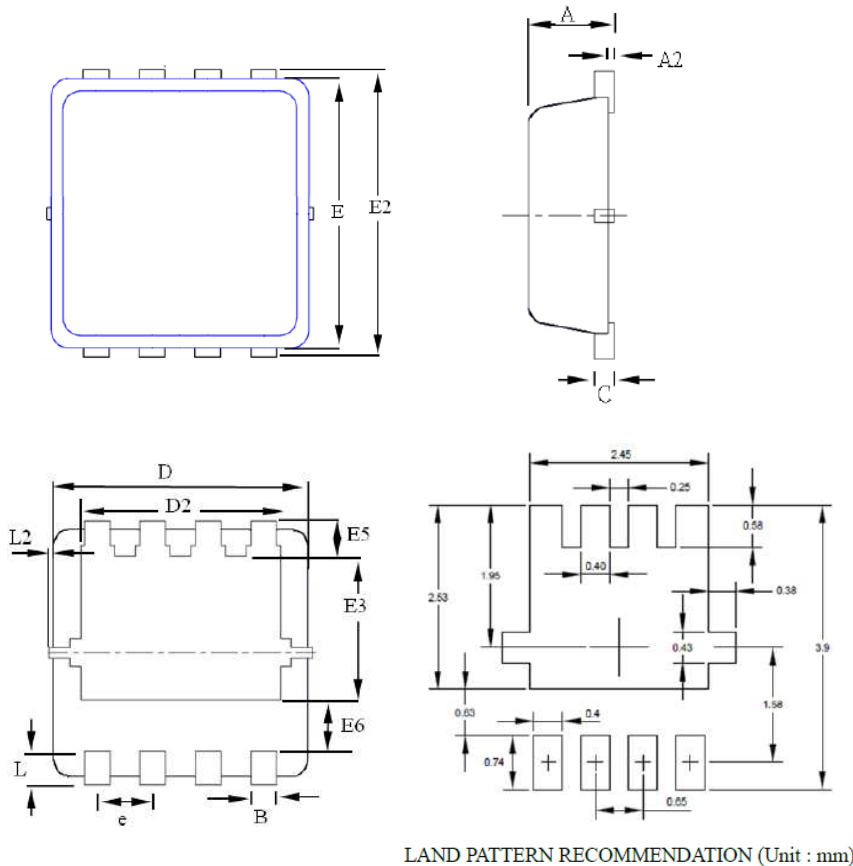


Fig.11 Transient Thermal Impedance

Top Marking



PRPAK3X3 Package Outline Drawing



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.65	0.80	0.90
A2	0.00	--	0.05
B	0.23	0.30	0.40
C	0.10	0.15	0.25
D	2.90	3.00	3.40
D2	1.90	2.35	2.60
E	2.65	3.00	3.20
E2	3.10	3.20	3.50
E3	1.40	1.75	1.98
E5	0.18	0.43	0.48
E6	0.59	0.63	0.79
L	0.25	0.40	0.56
L2	0.00	--	0.15
e	--	0.65	--

Note:

1. ALL DIMENSIONS LISTED ON THE DRAWING MEETING JEDEC STANDARD.
2. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
3. RECOMMENDED LAND PATTERN DESIGN IS ONLY FOR REFERENCE

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