QN6101M6N

N-Channel 60V Fast Switching MOSFET

General Description

The QN6101M6N is the highest performance trench N-Channel MOSFET with extreme high cell density, which provide excellent RDSON and gate charge for most of the synchronous applications.

The QN6101M6N meet the RoHS and Green Product requirement ,with full function reliability approved.

Product Summary

Green RoHS、HF、Pb

BVDSS	RDSON (VGS=10V)	ID (Tc=25℃)
60V	2.8mΩ	111A

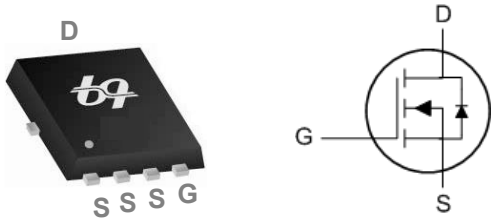
Applications

- Synchronous rectifier for Consumer/Computing /Industry Power Supply

Features

- Advanced high cell density Trench technology
- Green Device Available
- Low Gate drive

PRPAK 5X6 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	111	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ 10V[1]	70	A
I_D@T_A=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	21	A
I_D@T_A=70℃	Continuous Drain Current, V_{GS} @ 10V[1]	17	A
I_{DM}	Pulsed Drain Current[2]	222	A
EAS	Single Pulse Avalanche Energy[3]	132.1	mJ
I_{AS}	Avalanche Current	51.4	A
P_D@T_C=25℃	Total Power Dissipation[4]	62	W
P_D@T_A=25℃	Total Power Dissipation[4]	2.2	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance (> 10S)Junction-Ambient[1]	---	25	℃/W
$R_{\theta JA}$	Thermal Resistance Junction-Ambient[1]	---	55	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	---	2.0	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	60	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=1mA	---	0.04	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V , I_D=20A	---	2.2	2.8	mΩ
		V_{GS}=4.5V , I_D=20A	---	3.1	4.0	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	1.2	---	2.5	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-5.7	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=48V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=48V , V_{GS}=0V , T_J=55℃	---	---	5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=5V , I_D=20A	---	71	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	1.0	---	Ω
Q_g	Total Gate Charge (10V)	V_{DS}=30V , V_{GS}=4.5V , I_D=20A	---	68.0	---	nC
Q_g	Total Gate Charge (4.5V)		---	32.2	---	
Q_{gs}	Gate-Source Charge		---	13.0	---	
Q_{gd}	Gate-Drain Charge		---	9.1	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=30V , V_{GS}=10V , R_G=3Ω I_D=20A	---	14.6	---	ns
T_r	Rise Time		---	33.8	---	
$T_{d(off)}$	Turn-Off Delay Time		---	46.6	---	
T_f	Fall Time		---	10.7	---	
C_{iss}	Input Capacitance	V_{DS}=30V , V_{GS}=0V , f=1MHz	---	4727	---	pF
C_{oss}	Output Capacitance		---	757	---	
C_{rss}	Reverse Transfer Capacitance		---	80	---	

Guaranteed Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy[5]	V_{DD}=50V , L=0.1mH , I_{AS}= 37A	68.45	---	---	mJ

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,6]	V_G=V_D=0V , Force Current	---	---	111	A
I_{SM}	Pulsed Source Current[2,6]		---	---	222	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=1A , T_J=25℃	---	---	1.0	V
trr	Reverse Recovery Time	IF=20A , di/dt=100A/μs , T_J=25℃	---	42	---	nS
Qrr	Reverse Recovery Charge		---	28	---	nC

Note :
1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The EAS data shows Max. rating . The test condition is V_{DD}=50V,V_{GS}=10V,L=0.1mH
4.The power dissipation is limited by 150℃ junction temperature
5.The Min. value is 100% EAS tested guarantee.
6.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

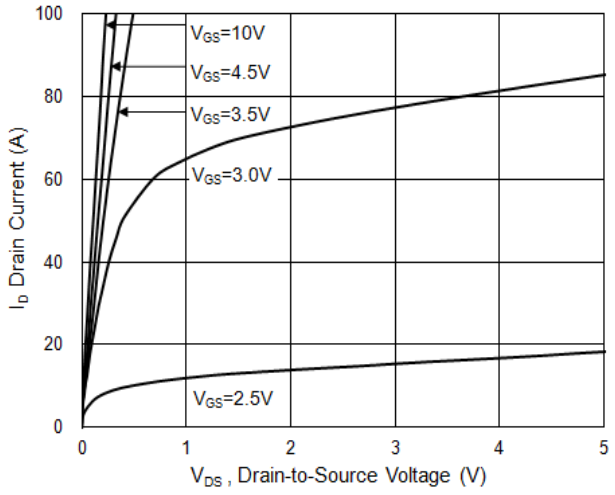


Fig.1 Typical Output Characteristics

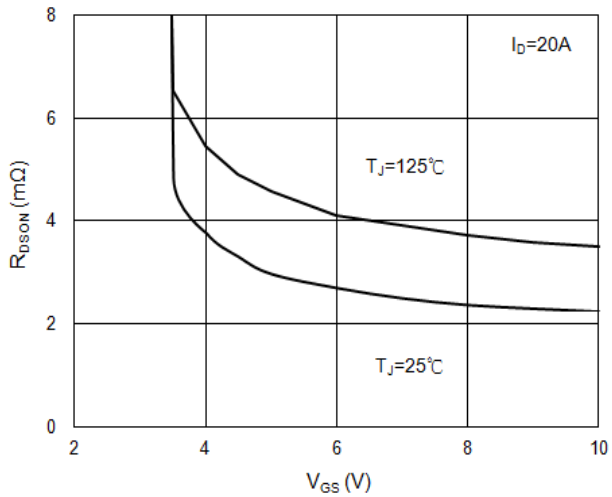


Fig.2 On-Resistance vs. Gate-Source

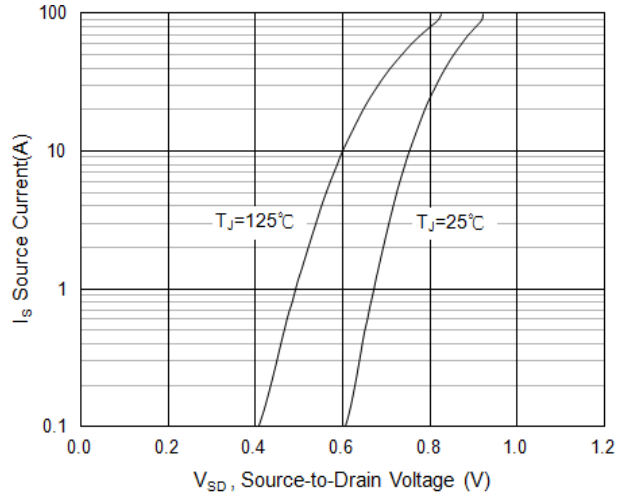


Fig.3 Forward Characteristics of Reverse

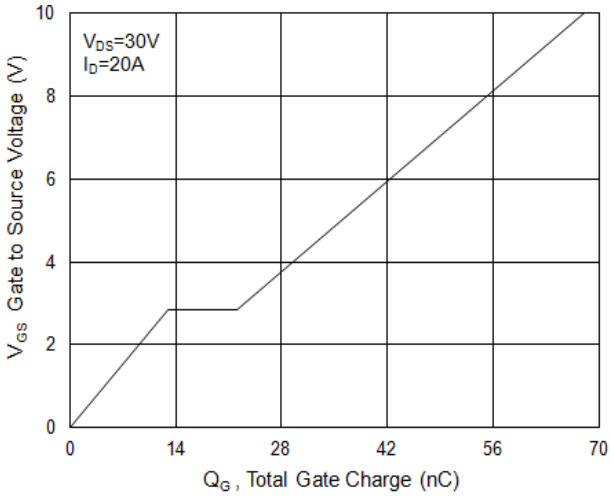


Fig.4 Gate-Charge Characteristics

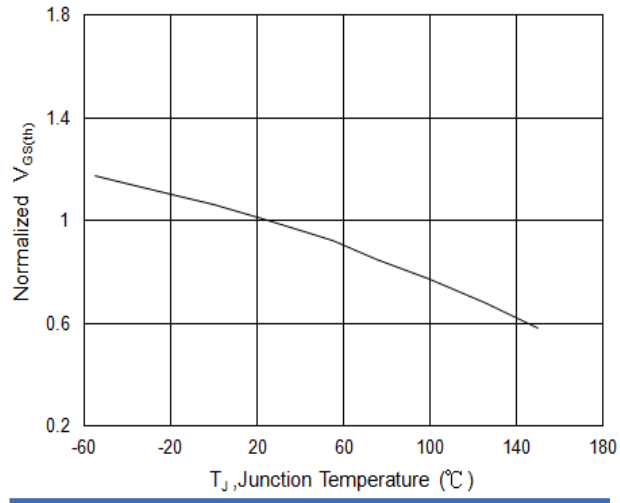


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

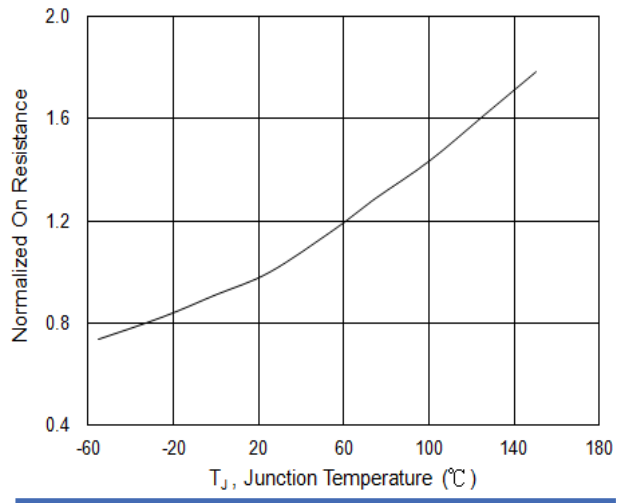


Fig.6 Normalized R_{DSON} vs. T_J

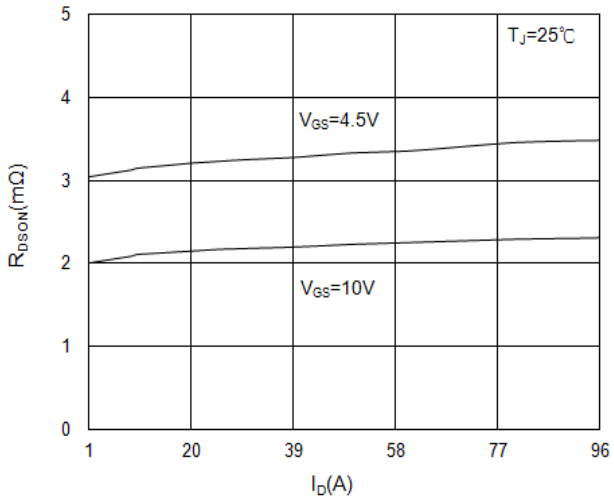


Fig.7 Drain-Source On-State Resistance

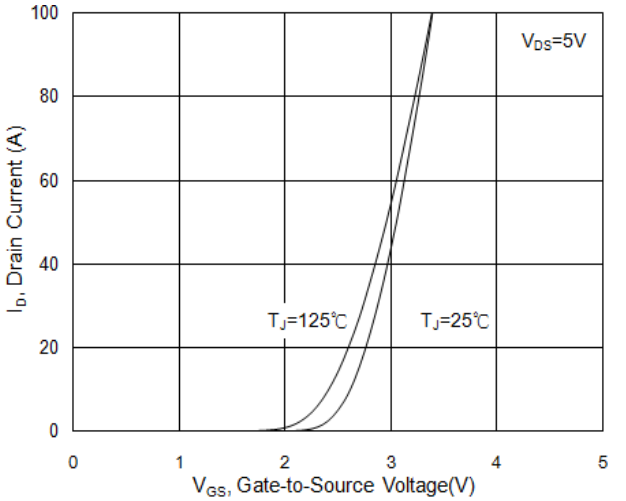


Fig.8 Transfer Characteristics

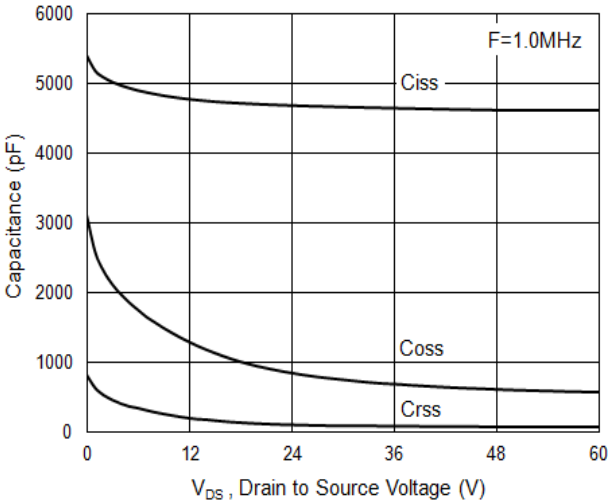


Fig.9 Capacitance

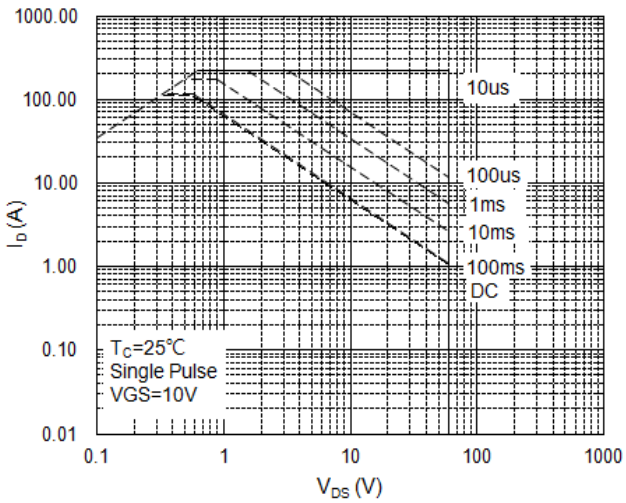


Fig.10 Safe Operating Area

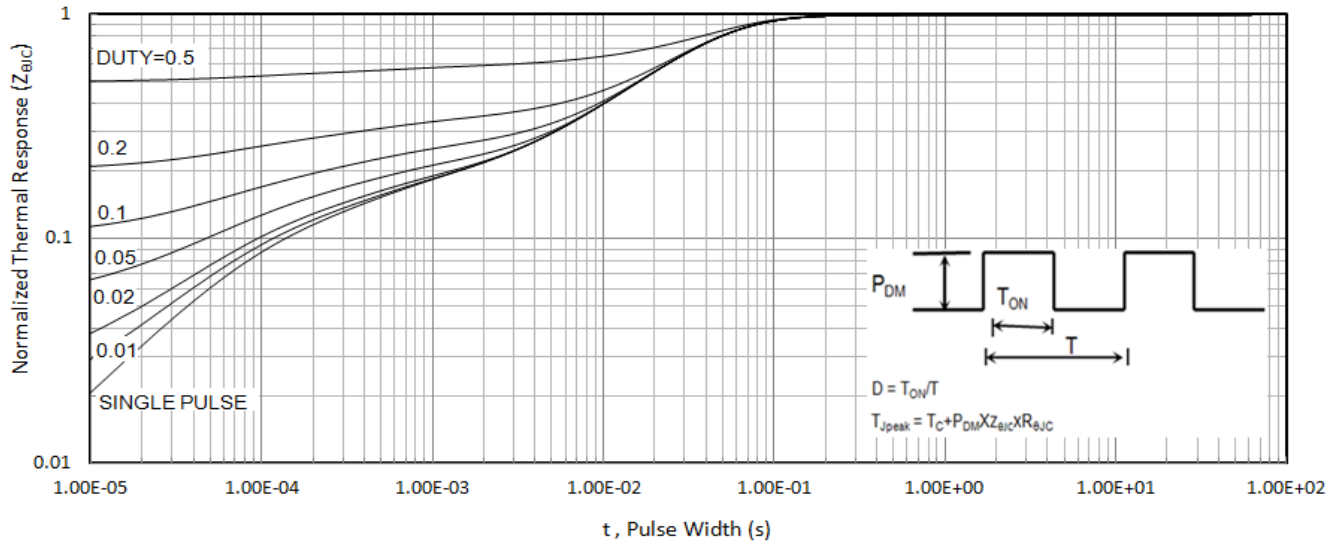
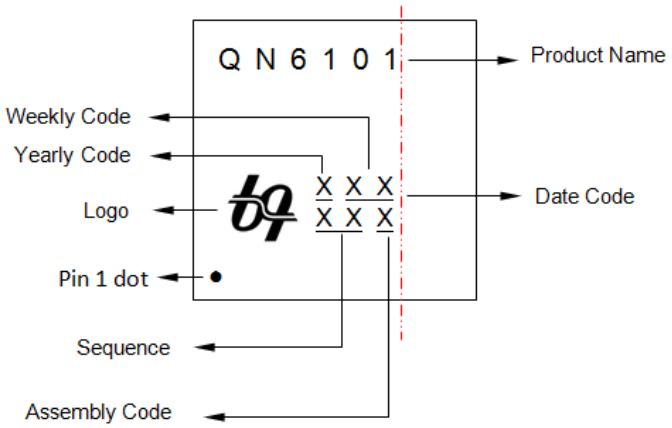
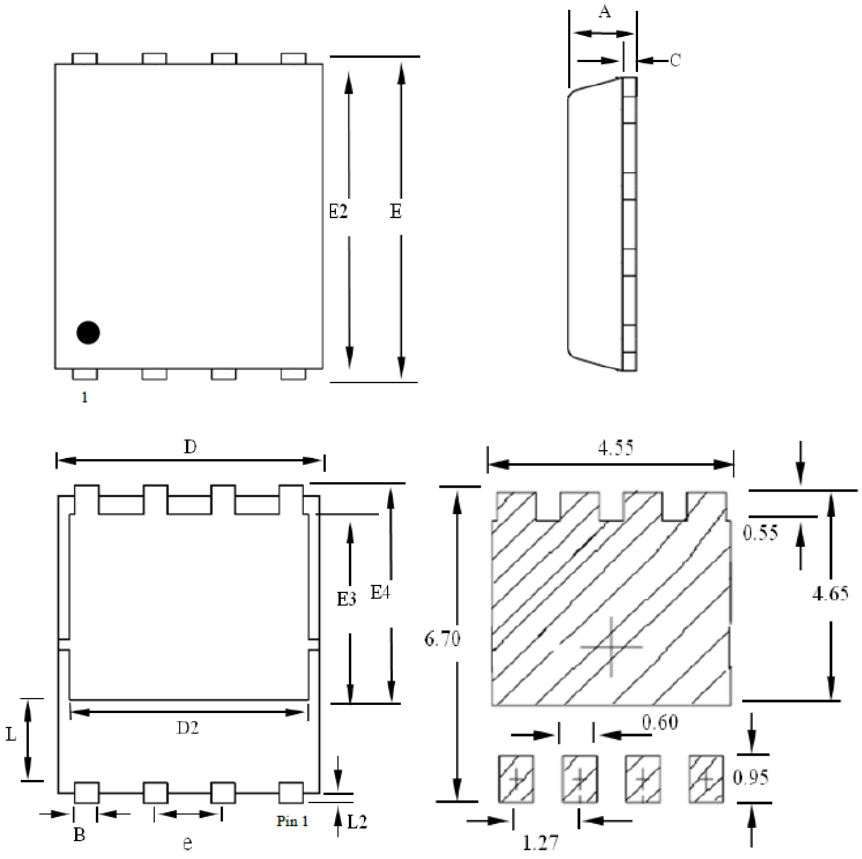


Fig.11 Normalized Maximum Transient Thermal Impedance

Top Marking



PRPAK5X6 Package Outline Drawing



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.90	1.00	1.20
B	0.33	--	0.51
C	0.20	--	0.34
D	4.50	--	5.10
D2	3.60	--	4.22
E	5.90	--	6.13
E2	5.50	--	5.84
E3	3.18	--	4.30
E4	3.69	--	4.39
L	1.10	--	1.39
L2	0.02	--	0.33
e	--	1.27	--

LAND PATTERN RECOMMENDATION (Unit : mm)

Note:
1. ALL DIMENSIONS LISTED ON THE DRAWING MEETING JEDEC STANDARD.
2. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
3. RECOMMENDED LAND PATTERN DESIGN IS ONLY FOR REFERENCE

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