A Highly Integrated USB Audio Single Chip

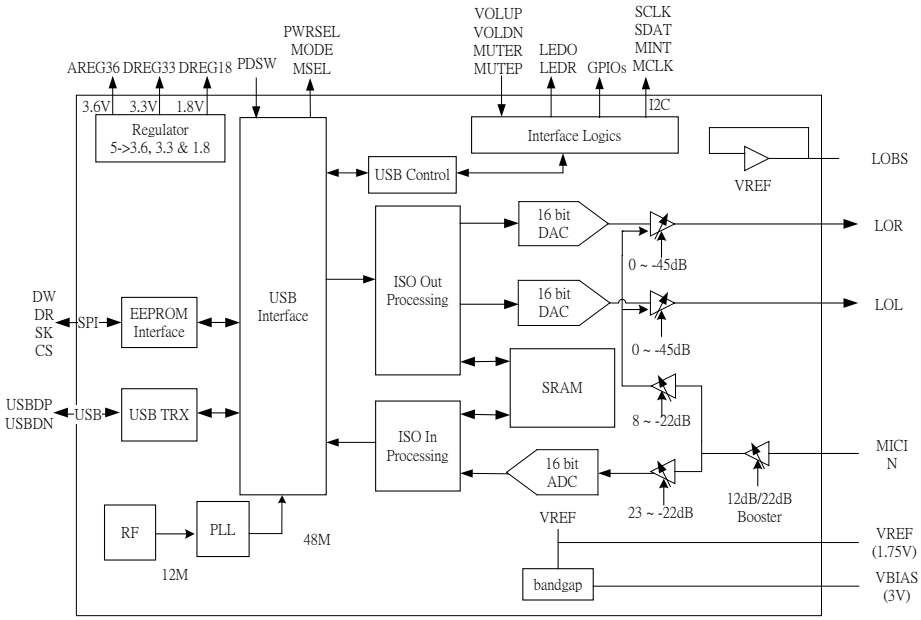
DESCRIPTION

The CM119B is a highly integrated, crystal-free USB audio single chip solution optimized for USB headset, headphone, and dongle applications such as VoIP (Voice over Internet Protocol). All essential analog modules were embedded in the CM119B including dual DAC and earphone driver, ADC, microphone booster, PLL, regulator, and USB transceiver. It also supports 8GPIO pins. In addition, audio adjustment can be easily controlled via specific HID compliant volume control pins. Many features are programmable with jumper pins or external EEPROM. Vendors can customize unique USB VID/PID/Product String/Manufacture String and min/max/initial volumes to EEPROM. The CM119B also comes with an anti-pop noise circuits design and internal oscillator which can operate without an external crystal oscillator.

FEATURES

- Compliant with USB 2.0 Full Speed Operation
- Compliant with USB Audio Device Class Specification v1.0
- Supports USB Suspend/Resume Mode and Remote Wakeup with Volume Control pins
- On-chip oscillator that provides reference sources for PLL and embedded USB transceiver
- Jumper pin for Headset Mode (Playback + Recording) and Speaker/Headphone Mode (Playback Only)
- Jumper pin for Mixer Unit enable/disable under Headset Mode and Power Mode setting
- I2C interface to access internal registers for external MCU and USB host
- USB audio function topology has 2 Input Terminals, 2 Output Terminals, 1 Mixer Unit, 1 Selector Unit, and 3 Feature Units (Headset Mode)
- USB audio function topology has 1 Input Terminal, 1 Output Terminal, and 1 Feature Unit (Speaker Mode)
- Anti-pop noise design for plugged and vice-versa

BLOCK DIAGRAM



Release notes

Revision	Date	Description
1.0	27 Sep 2013	First release

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1 Description and Overview

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2 Ordering information

Product	Package Marking	Package Type	Transport Media	Storage Temperature
CM119B	CM119B	LQFP-48 (7 x 7mm) Green Package	Tray	-45 to 120℃

3 Features

- Compliant with USB 2.0 Full Speed Operation
- Compliant with USB Audio Device Class Specification v1.0
- Supports USB Suspend/Resume Mode and Remote Wakeup with Volume Control pins
- On-chip oscillator that provides reference sources for PLL and embedded USB transceiver
- Jumper pin for Headset Mode (Playback + Recording) and Speaker/Headphone Mode (Playback Only)
- Jumper pin for Operation System Mixer Unit Enable/Disable under Headset Mode
- Jumper pin for Power Mode setting
- USB audio function topology has 2 Input Terminals, 2 Output Terminals, 1 Mixer Unit, 1 Selector Unit, and 3 Feature Units (Headset mode)
- USB audio function topology has 1 Input Terminal, 1 Output Terminal, and 1 Feature Unit (Speaker Mode)
- Anti-pop noise design for device plugged and vice-versa, while A-A path is off
- Supports one Control Endpoint, one Isochronous out Endpoint, one Isochronous in Endpoint, and one Interrupt in Endpoint
- Alternate zero bandwidth setting for releasing playback bandwidth on USB Bus when the device is inactive
- Includes volume up, volume down, and playback mute support USB HID for Host Control Synchronization
- Includes Record Mute Pin with LED Indicator for Record Mute Status
- Includes external EEPROM Interface for Vendor Specific USB VID, PID, Product String, Manufacture String, and max/min/initial volumes
- Supports AES/EBU, IEC60958, S/PDIF Consumer Formats for Stereo PCM Data at S/PDIF Output
- Supports I2C Interface for External MCU Integrated
- Includes Isochronous transfer that uses Adaptive Mode with Internal PLL for Synchronization
- 48K/44.1KHz Sampling Rate for both Playback and Recording
- Soft Mute Function
- Embedded16bit audio DAC with Earphone Phone Buffer
- Embedded16bit ADC input with Microphone Boost
- Embedded power on Reset Block

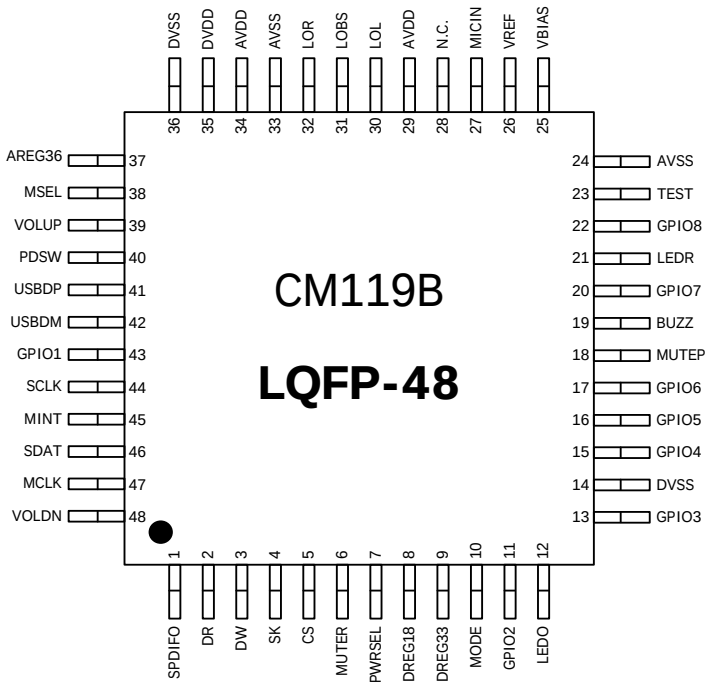
- Embedded 5V to 3.6V/3.3V/1.8V regulators for single external 5V power
- Industrial standard 48-pin LQFP Package
- Optional Hardware SDK tool for third-party software

4 Pin Descriptions

4.1 Pin Assignment (by pin number)

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	SPDIFO	13	GPIO3	25	VBIAS	37	AREG36
2	DR	14	DVSS	26	VREF	38	MSEL
3	DW	15	GPIO4	27	MICIN	39	VOLUP
4	SK	16	GPIO5	28	N.C.	40	PDSW
5	CS	17	GPIO6	29	AVDD	41	USBDP
6	MUTER	18	MUTEP	30	LOL	42	USBDM
7	PWRSEL	19	BUZZ	31	LOBS	43	GPIO1
8	DREG18	20	GPIO7	32	LOR	44	SCLK
9	DREG33	21	LEDR	33	AVSS	45	MINT
10	MODE	22	GPIO8	34	AVDD	46	SDAT
11	GPIO2	23	TEST	35	DVDD	47	MCLK
12	LEDO	24	AVSS	36	DVSS	48	VOLDN

4.2 Pin-out Diagram



4.3 Pin Signal Descriptions

Pin #	Symbol	Type	Description
1	SPDIFO	DO, 8mA, SR	SPDIF Output
2	DR	DIO, 8mA, PD, 5VT	USB Controller Data Read From EEPROM Interface EEPROM Data Output
3	DW	DO, 4mA, SR	USB Controller Data Writes to EEPROM Interface EEPROM Data Input
4	SK	DO, 4mA, SR	EEPROM Interface Clock (100KHz)
5	CS	DO, 4mA, SR	EEPROM Interface Chip Select
6	MUTER	DI, ST, PU	Mute Recording (Edge Trigger with de-Bouncing)
7	PWRSEL	DI, ST	H: Pull Up to 3.3V; L: Pull Down to Ground Speaker Mode H：Self-Powered with 100mA；L：Bus Power with 500mA Headset Mode H：Bus Power with 100mA；L：Bus Power with 500mA
8	DREG18	P	1.8V Regulator Output for Digital Core
9	DREG33	P	3.3V Regulator Output for Digital I/O (driving current 40mA)
10	MODE	DI, ST	H: Pull Up to 3.3V; L: Pull Down to Ground L：Headset Mode: Playback & Recording H：Speaker Mode: Playback Only
11	GPIO2	DIO, 8mA, PD, 5VT	GPIO Pin
12	LEDO	DO, SR, 4mA	LED for Operation; Output H for Power On; Toggling for Data Transmit
13	GPIO3	DIO, 8mA, PD, 5VT	GPIO Pin
14	DVSS	P	Digital Ground
15	GPIO4	DIO, 8mA, PD, 5VT	GPIO Pin
16	GPIO5	DIO, 8mA, PD, 5VT	GPIO Pin
17	GPIO6	DIO, 8mA, PD, 5VT	GPIO Pin
18	MUTEP	DI, ST, PU	Mute Playback (Edge Trigger with de-Bouncing)
19	BUZZ	DO, 8mA, SR	Buzzer Output Pin
20	GPIO7	DIO, 8mA, PD, 5VT	GPIO Pin
21	LEDR	DO, SR, 4mA	LED for Mute Recording Indicator; Outputs H when Recording is Muted
22	GPIO8	DIO, 8mA, PD, 5VT	GPIO Pin
23	TEST	DI, ST, PD	Test Mode Select Pin; Pull Low for Normal Operation
24	AVSS	P	Analog Ground
25	VBIAS	AO	Microphone Bias Voltage Supply (3V)
26	VREF	AO	Connecting to External Decoupling Capacitor for Embedded Bandgap Circuit; 1.75V Output
27	MICIN	AI	Microphone Input, input impedance is 10k Ohm
28	N.C.	--	N.C.
29	AVDD	P	5V Analog Power for Analog Circuit
30	LOL	AO	Line Out Left Channel
31	LOBS	AO	DC 1.75V Output for Line Out Bias
32	LOR	AO	Line Out Right Channel
33	AVSS	P	Analog Ground
34	AVDD	P	5V Analog Power for Analog Circuit
35	DVDD	P	5V Power Supply to Internal Regulator
36	DVSS	P	Digital Grounding
37	AREG36	P	3.6V analog power for analog circuit
38	MSEL	DI, ST	Mixer Enable/Disable Pin H: Pull Up to 3.3V, L: Pull Down to Ground L: Without Mixer

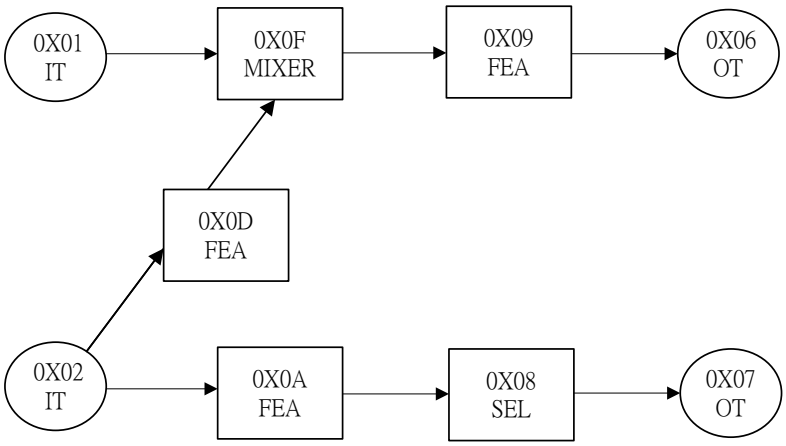
			H: With Mixer (With Default Mute) USB Descriptors are to be change accordingly
39	VOLUP	DI, ST, PU	Volume Up (Edge Trigger with de-Bouncing)
40	PDSW	DO, 4mA , OD	Power Down Switch Control (for PMOS Polarity) 0: Normal Mode, 1: Power Down Mode
41	USBDP	AIO	USB Data D+
42	USBDM	AIO	USB Data D-
43	GPIO1	DIO, 8mA, PD, 5VT	GPIO Pin
44	SCLK	DIO, 8mA, PD, 5VT	External MCU Serial Bus Clock Pin
45	MINT	DO, 4mA, SR	External MCU Interrupt Pin When Register Address 4 ~ 7 has new data, MINT is set Low; after MCU read, MINT is reset to H
46	SDAT	DIO, 8mA, PD, 5VT	External MCU Serial Bus Data Pin
47	MCLK	DO, 4mA, SR	External MCU Clock Pin, Clock Frequency is programmable Default is 1.5 MHz (Options Include 6MHz, 3MHz, and 1.5MHz)
48	VOLDN	DI, ST, PU	Volume Down (Edge Trigger with de-Bouncing)

Note: DI / DO / DIO – Digital Input / Output / Bi-Directional Pin, AI / AO / AIO – Analog Input / Output / Bi-Directional Pin, SR – Slew Rate Control, ST – Schmitt Trigger, PD / PU – Pull Down / Pull Up, 5VT – 5 Volt Tolerant (3.3V Pin), OD – Open Drain, P – Power Supply Pin

5 USB Topology

The CM119B supports headset and speaker topology that can be selected by MODE pin. The topology setting as follows: MODE=0, Headset Topology
MODE=1, Speaker Topology

5.1 Headset Topology



5.1.1 Device Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	12	Total 18 Bytes
1	bDescriptorType	1	01	Device descriptor
2	bcdUSB	2	0110	USB 1.1 compliant
4	bDeviceClass	1	00	Device class specified by interface
5	bDeviceSubClass	1	00	Device subclass specified by interface
6	bDeviceProtocol	1	00	Device protocol specified by interface
7	bMaxPacketSize0	1	8	Endpoint zero Size = 8 bytes
8	idVendor	2	0d8c	Vendor ID
10	idProduct	2	0013	Product ID
12	bcdDevice	2	0100	Device compliant to the Audio Device Class specification version 1.00
14	iManufacturer	1	01	Index of string descriptor that characterizes the manufacturer
15	iProduct	1	02	Index of string descriptor that characterizes the product
16	iSerialNumber	1	00	Index of string descriptor that characterizes the device's serial number
17	bNumConfigurations	1	01	Configurations number = 1

5.1.2 Configuration Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Total 9 Bytes
1	bDescriptorType	1	02	Configuration descriptor
2	wTotalLength	2	XXXX	Total length of data returned for this configuration: Programmable by MSEL and MODE pin
4	bNumInterfaces	1	04	Number of interfaces supported by this configuration: 0: control interface 1: ISO-OUT interface 2: ISO-IN interface 3: INT-IN(HID) interface
5	bConfigurationValue	1	01	Configuration value
6	iConfiguration	1	00	Index of string descriptor that characterizes this configuration

7	bmAttributes	1	80	Bus Power and support Remote Wakeup
8	bMaxPower	2	32	Maximum power consumption of the USB Device: 100mA

5.2 Speaker Topology

5.2.1 Device Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	12	Descriptor length
1	bDescriptorType	1	01	Device descriptor
2	bcdUSB	2	0110	USB 1.1 compliant
4	bDeviceClass	1	00	Device class specified by interface
5	bDeviceSubClass	1	00	Device subclass specified by interface
6	bDeviceProtocol	1	00	Device protocol specified by interface
7	bMaxPacketSize0	1	08	Endpoint zero packet size
8	idVendor	2	0d8c	Vendor ID
10	idProduct	2	0013	Product ID
12	bcdDevice	2	0100	Device release number
14	iManufacturer	1	01	Index of string descriptor that characterizes the manufacturer
15	iProduct	1	02	Index of string descriptor that characterizes the product
16	iSerialNumber	1	00	Index of string descriptor that characterizes the serial number
17	bNumConfigurations	1	01	Number of configuration

5.2.2 Configuration Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	02	Configuration descriptor
2	wTotalLength	2	XXXX	Total length of data returned for this configuration: Programmable by MSEL and MODE pin
4	bNumInterfaces	1	03	Number of interfaces supported by this Configuration: 00: Control 01: ISO-Out 02: INT-IN (HID)
5	bConfigurationValue	1	01	Configuration value
6	iConfiguration	1	00	Index of string descriptor that characterizes this configuration
7	bmAttributes	1	80	Attributes(PWRSEL=0:Bus Powered, 1:SELF Powered)
8	bMaxPower	1	32	Maximum power consumption from bus = 100mA

6 Function Description

6.1 Content Format for EEPROM (93C46)

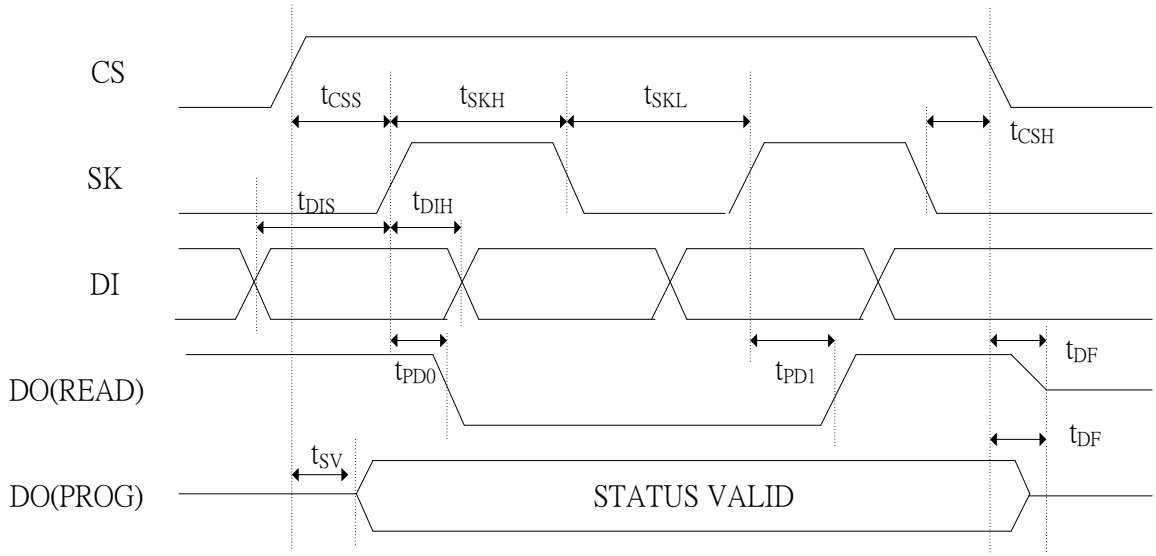
The CM119B integrates USB transceiver, internal oscillator and regulator so that only several passive components are necessary for the USB interface connection. Default USB descriptors are embedded in the CM119B; therefore there is no additional design effort needed for a generic USB operation. For customized product, customer can attach a SPI interface 93C46 EEPROM to override the embedded VID, PID and initial/max/min volume settings. The CM119B automatically detects 93C46 existence and performs the overwrite function during power up.

Each address has 2-byte data, prefix `0x` means hex number

Address(Hex)	Description	
0x00	bit[15:4] Magic Word 0x670X where X = bit 4, 3, 2, 1 bit[3] The value within address 0x2A, 0x2B, 0x32 is valid 1: valid 0: invalid bit[2] reserved, should be 1 bit[1] serial number enable control 1: enable, 0: disable(default) bit[0] reserved, should be 1	
0x01	VID 2-byte	
0x02	PID 2-byte	
0x03	Serial number 1st byte (bit15-bit8, first character)	Serial number length (bit7-bit0)
0x04 ~ 0x09	Serial number 12-byte	
0x0A	Product string 1st byte (bit15-bit8, first character)	Product string length (bit7-bit0) [0x3E->30,0x40->31Char]
0x0B ~ 0x19	Product string 30-byte (default: USB Audio Device)	
0x1A	Manufacturer string 1st byte (bit15-bit8, first character)	Manufacturer string length (bit7-bit0) [0x3E->30,0x40->31Char]
0x1B ~ 0x29	Manufacturer string 30-byte (default: C-Media Electronics Inc.)	
0x2A	bit[15: 9] DAC initial volume (7-bit, default = -10dB) bit[8: 3] ADC initial volume (6-bit, default = 8dB) bit[2] DAC EEPROM MAX/MIN volume valid bit[1] ADC EEPROM MAX/MIN volume valid bit[0] AA EEPROM MAX/MIN volume valid	
0x2B	bit[15:11] AA initial volume (5-bit, default = -7dB) bit[10] Reserved, should be 0 bit[9] Boost mode 0: 22dB 1:12dB (default) bit[8] Reserved, should be 0 bit[7] Total Power Control 1:enable, 0:disable(default) bit[6] Reserved, should be 0 bit[5] MIC High Pass Filter 1:enable(default), 0:disable bit[4] MIC PLL Adjust 1:enable, 0:disable(default) bit[3] MIC BOOST 1:enable (default), 0:disable bit[2] DAC Output Terminal property set to SPK or HP 1: Headset, 0: Speaker(default) bit[1] HID, 1: enable (default), 0: disable bit[0] Remote wakeup, 1:enable, 0:disable(default)	

0x2C	bit[15:0] DAC Minimum Volume (0xD300, DAC-Min.=-37dB, default=-37dB)
0x2D	bit[15:0] DAC Maximum Volume (0x0000, DAC-Max.=0dB, default=0dB)
0x2E	bit[15:0] ADC Minimum Volume(0xEA00, ADC-Min.=-22dB, default=-12dB)
0x2F	bit[15:0] ADC Maximum Volume(0x1700, ADC-Max.=+23dB, default=+23dB)
0x30	bit[15:0] AA Minimum Volume (0xE900, AA-Min.=-23dB, default=-23dB)
0x31	bit[15:0] AA Maximum Volume (0x0800,AA-Max.+8dB, default=+8dB)
0x32	EE_OPTION2 Register bit[3] Reserved, should be 0 bit[2] Reserved, should be 0 bit[1] Reserved, should be 1 bit[0] Reserved, should be 0
~ END	

6.2 EEPROM SPI interface Timing Information



Symbol	Parameter	Test Condition*	Min	Typ	Max	Units
f_{SK}	SK Clock Frequency	2.7V<=Vcc<=5.5V	0	-	200	KHz
t_{SKH}	SK High Time	2.7V<=Vcc<=5.5V	250	-	-	ns
t_{SKL}	SK Low Time	2.7V<=Vcc<=5.5V	250	-	-	ns
t_{CS}	Minimum CS Low Time	2.7V<=Vcc<=5.5V	250	-	-	ns
t_{CSS}	CS Setup Time	2.7V<=Vcc<=5.5V	50	-	-	ns
t_{DIS}	DI Setup Time	2.7V<=Vcc<=5.5V	100	-	-	ns
t_{CSH}	CS Hold Time	2.7V<=Vcc<=5.5V	0	-	-	ns
t_{DIH}	DI Hold Time	2.7V<=Vcc<=5.5V	100	-	-	ns

t_{PD1}	Output Delay to"1"	2.7V<=Vcc<=5.5V	-	-	250	ns
t_{PD0}	Output Delay to"0"	2.7V<=Vcc<=5.5V	-	-	250	ns
t_{SV}	CS to Status Valid	2.7V<=Vcc<=5.5V	-	-	250	ns
t_{DF}	CS to DO in High Impedance	2.7V<=Vcc<=5.5V	-	-	100	ns
t_{WP}	Write Cycle Time	4.5V<=Vcc<=5.5V	0.1	3	10	ms

* based on ATMEL 93C46 EEPROM data

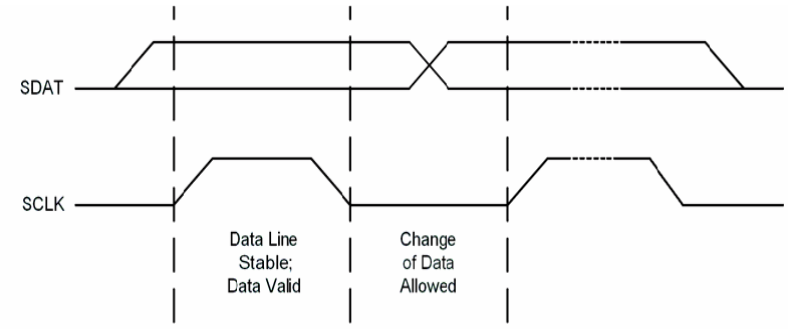
6.3 MCU Interface

On MCU serial interface, the CM119B functions as a slave device with bit rate up to 400Kbps (fast mode). MCU can read/write 3 bytes to the CM119B device with a 2-bit register address. Since host side and MCU can both access all of the internal registers, access contention should be avoided on application when both try to access the same register. The7-bit slave address of the CM119B is assigned as 7'b0111000.

When a one-byte data is written by MCU, the CM119B will transfer totally 4 bytes to the USB host via an additional interrupt pipe. The sequence of the upward HID report is given by: the button status first (address00); then register with address01; followed by register with address02; lastly, register with address03. The USB host will keep polling the upward HID report every 2mS. When there is any button pressed or released, or MCU data coming, the CM119B will transfer the 4 bytes of HID report to the USB host again.

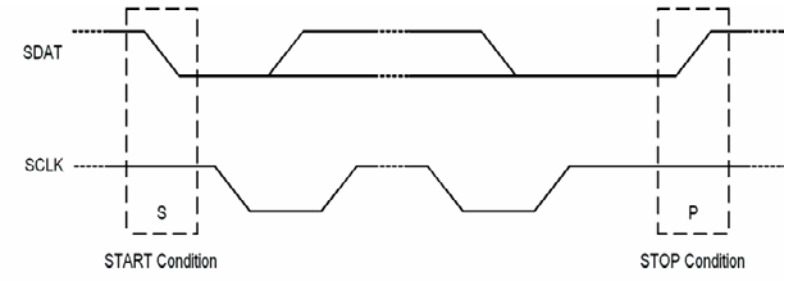
The CM119B can also transfer one byte MCU data from the USB host to its register. This is accomplished by a 'Set Output Report' HID class request via default control pipe. MCU can get this downward byte by interrupt or polling.

The CM119B has one input pin 'SCLK' where it gets serial clock from MCU, and one open-drain output pin 'SDAT' where it sends or receives serial signal to or from MCU. As shown below, 'SDAT' should best able when 'SCLK' is high, and can only have transition when 'SCLK' is low.



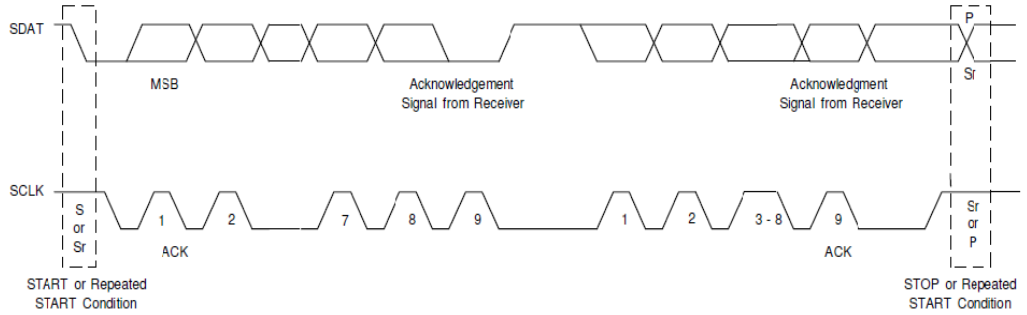
Bit Transfer on the MCU Interface

START and STOP conditions shown below are the exception. Every transaction begins from a START and ends with a STOP or another START (repeated START).

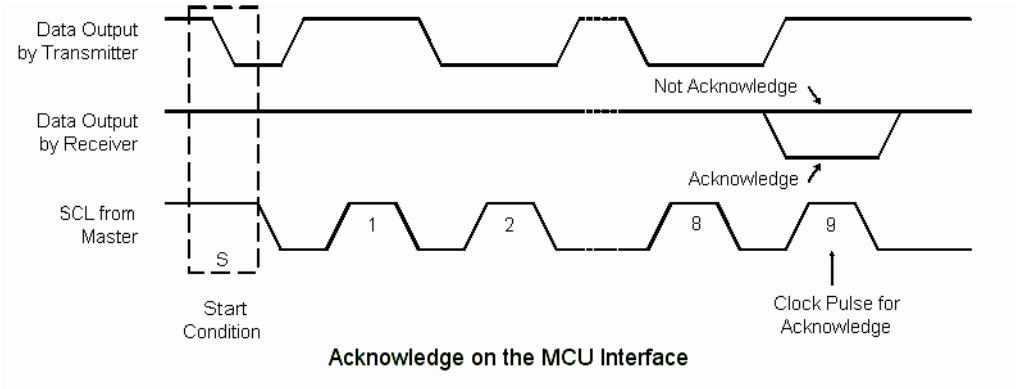


START and STOP Conditions

The figure below demonstrates a typical transaction. After every 8 bits sent by the transmitter, the receiver should send one bit low for positive acknowledgement or one bit high for negative acknowledgement. After the negative acknowledgement, a STOP or repeated START should follow. The next figure shows more detailed display about acknowledgement bit. Note that 'SCLK' is always driven by the master.

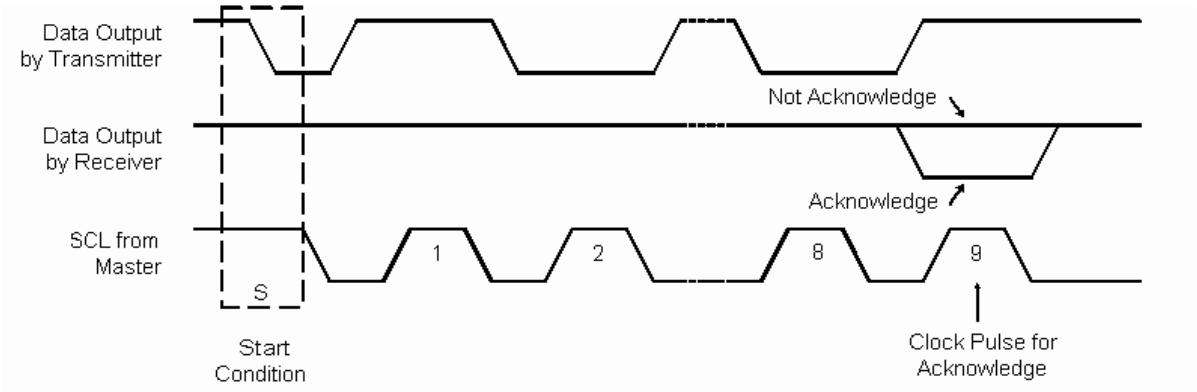


Data Transfer on the MCU Interface



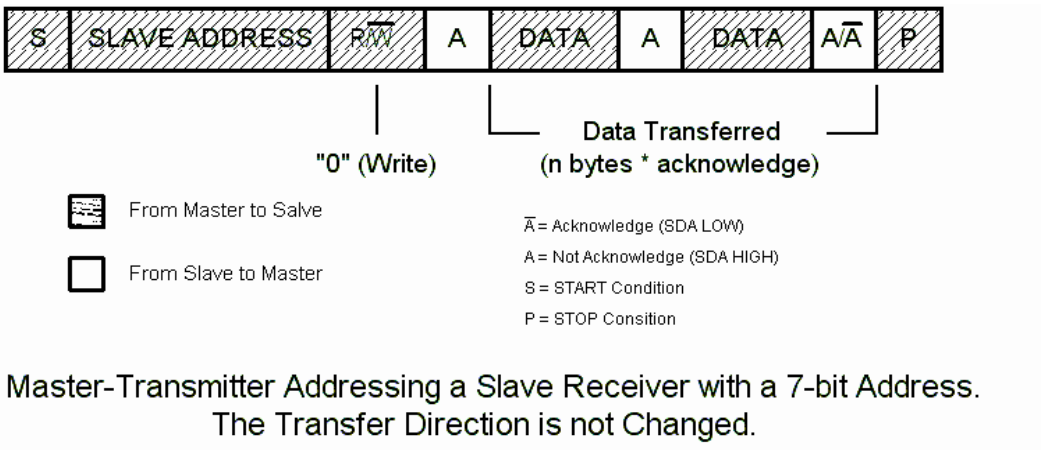
Acknowledge on the MCU Interface

The figure below shows a complete data transfer. After a START, MCU should send 7-bit slave address (7'b0111000) first and then the 8th bit denotes a read transfer when it's high; or a write transfer when it's low. The first acknowledgement is always from the CM119B.



Acknowledge on the MCU Interface

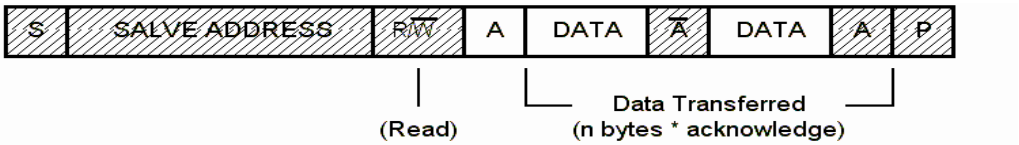
In the write transfer, MCU keeps acting as the master and the transfer direction is not changed. The following figure gives an example of one byte write transfer.



A Master-Transmitter Addressing a Slave Receiver with a 7-bit Address.
The Transfer Direction is not Changed.

The CM119B regards the first DATA byte as the register address. The second DATA byte is the content that MCU writes at the register address. If there is the third DATA byte, the CM119B will auto-increment this byte to the next register address.

The figure below shows an example of two bytes read transfer. Because the CM119B has auto-increment function, the second DATA byte will be the register data on the next address.



A Master reads a Salve immediately after the first Byte

Note: The USB host tries to get new HID data every 2mS. It's quite slow. If the continuous write transfers are too close in terms of time, the former transfer may have no effect.

The figure below shows typical transactions between MCU and the CM119B. After a START, MCU should send 7-bit slave address (0111000) first and then the 8th bit denotes a read transfer when it's high; or a write transfer when it's low.

MCU write:

S	0x70	0	0x00	0	Byte 0	0	Byte 1	0	Byte 2	0	Byte 3	0	P

MCU read:

S	0x70	0	0x04	0							
S	0x71	0	Byte 0	0	Byte 1	0	Byte 2	0	Byte 3	1	P

	From CM119A to MCU		From MCU to CM119A
S	START condition	P	STOP condition
0	Positive acknowledge	1	Negative acknowledge
Byte n	One byte data (address n)		

In a write transfer, MCU keeps acting as the transmitter. The CM119B regards the first DATA byte as the start register address (it's better to be 0x00). The next four DATA bytes are the contents that MCU writes to the register addresses. In a read transfer, two transactions are necessary. MCU resets start register address by the first transaction. Then MCU changes in order to be the receiver during the second transaction to get four bytes of data.

Note: Bits 0~3 of the first HID byte always reflect the button activity, so they cannot be written by MCU.

6.4 Jumper Pins and Mode Setting

Jumper pins can be used to set the configuration of CM119B. These jumper pin settings affect both USB descriptors and USB audio topology.

6.4.1 Mode Pin and MSEL Pin

If MODE pin is switched up (Speaker Mode), the playback only function is activated and there is no recording function declared to the host. At this setting, MSEL pin is ignored while only one input terminal, one output terminal and one feature unit is declared in the USB audio topology.

If MODE pin is switched down (Headset Mode), the full duplex playback and recording function is declared to the host. MSEL pin setting activates one mixer unit and one feature unit.

When MSEL = 1, Mixer is enable (AA-Path enable), but with default mute setting;

When MSEL = 0, Mixer is disable (AA-Path disable).

The above USB audio topology (7.1) is an example of headset mode with Mixer enabled.

6.4.2 Mode pin and PWRSEL pin

PWRSEL pin affects the power configuration of CM119B; together with MODE pin there are 4 combinations that are programmable.

Combinations		MODE	
		3.3V	GND
PWRSEL	3.3V	Speaker Mode: Playback Only (Self-Powered with 100mA)	Headset Mode: Playback + Recording (Bus Power with 100mA)
	GND	Speaker Mode: Playback Only (Bus Power with 500mA)	Headset Mode: Playback + Recording (Bus Power with 500mA)

6.5 HID Feature and Descriptor

The HID class consists primarily of devices that are used by humans to control the operation of computer systems. HID feature is provided by the CM119B, so user settings (volume up, volume down, and playback mute button pin) were all reported to the host to synchronize host side setting. In addition, all the CM119B internal registers can be accessed via HID function call.

USB protocols can configure devices at start up or when they are plugged in at run time. These devices are broken down into various device classes. Each device class defines the common behavior and protocols for devices that has similar functions. The HID (Human Interface Device) class is one of the device classes.

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6.5.1 HID Interface Descriptor

Offset	Field	Size	Value(Hex)	Description
0	bLength	1	09	Sizeofthisdescriptor:9byte
1	bDescriptorType	1	04	INTERFACE descriptor type
2	bInterfaceNumber	1	03	Number of interface: 3
3	bAlternateSetting	1	00	Alternate 0
4	bNumEndpoints	1	01	Number of endpoints used by this interface:1
5	bInterfaceClass	1	03	HID Interface Class
6	bInterfaceSubClass	1	00	No Subclass
7	bInterfaceProtocol	1	00	Must be set to 0
8	iInterface	1	00	Index of a string descriptor that characterizes this interface

6.5.2 HID Descriptor

Offset	Field	Size	Value(Hex)	Description
0	bLength	1	09	Total 9 bytes
1	bDescriptorType	1	21	HID descriptor type
2	bcdHID	2	0100	HID class version 1.00
4	bCountryCode	1	00	-
5	bNumDescriptors	1	01	-
6	bDescriptorType	1	22	Report descriptor
7	wDescriptorLength	2	003C	Numeric expression equal to the total size of the optional descriptor: 60 Bytes

6.5.3 Interrupt in Endpoint Descriptor

Offset	Field	Size	Value(Hex)	Description
0	bLength	1	07	Total 7 bytes
1	bDescriptorType	1	05	ENDPOINT descriptor type

2	bEndpointAddress	1	87	IN Endpoint Endpoint number=3
3	bmAttributes	1	03	Interrupt endpoint type
4	wMaxPacketSize	2	0004	Maximum packet size: 4 bytes
6	bInterval	1	2	2ms

6.6 Internal Registers

All internal registers of the CM119B can be accessed via generic HID functional calls without the need to develop kernel mode driver. Total of 4bytes of data can be read or write from HID. Input report is for read while output report is for write. Internal registers of the CM119B are used to control GPIO, S/PDIF output, EEPROM and MCU data access. Host side HID or external MCU can access the CM119B internal registers. With both sides accessed to the same set of registers, two-way communication can be achieved.

6.6.1 Access via HID Class Command

HID_IR0 to HID_IR3 are HID input reports and are used by host side receiving data to the CM119B. HID_OR0 to HID_OR3 are HID output report and are used by host side sending data to the CM119B

HID interrupt will occur when HID_IR0-3 are updated by button status MCU (and GPI in case HID_IR0[7:6]

==2'b00).

HID_IR0 (HID input report byte 0)
Offset:0x00

Bits	Read/Write	Description	Default
7-6	R	When HID_OR0[7]==1'b0: HID_IR0-3 are programmed by MCU (and GPI) 0:HID_IR1 is used as GPI 1:HID_IR0-3 are used as generic HID registers 2:Values written to HID_IR0-3 are also mapped to MCU_CTRL, EEPROM_DATA0-1, EEPROM_CTRL 3:Reserved	0x0
5-4	R	When HID_OR0[7]==1'b0: Generic registers programmed by MCU When HID_OR0[7]==1'b1: Mapped from MCU_CTRL[5:4]	0x0
3	R	0: No activity on Record-Mute button 1: Record-Mute button pressed then released	0x0
2	R	0:No activity on Playback-Mute button 1: Playback-Mute button pressed then released	0x0
1	R	0: Volume-down button released 1: Volume-down button pressed	0x0
0	R	0: Volume-up button released 1: Volume-up button pressed	0x0

HID_IR1 (HID input report byte 1)
Offset:0x01

Bits	Read/Write	Description	Default
7-0	R	When HID_OR0[7]==1'b0: GPI (when HID_IR0[7:6] == 2'b00); or Generic registers programmed by MCU (otherwise) When HID_OR0[7]==1'b1: Mapped from EEPROM_DATA0	0x00

HID_IR2 (HID input report byte2)
Offset:0x02

Bits	Read/Write	Description	Default
7-0	R	When HID_OR0[7]==1'b0: Generic registers programmed by MCU When HID_OR0[7]==1'b1: Mapped from EEPROM_DATA1	0x00

HID_IR3 (HID input report byte3)
Offset:0x03

Bits	Read/Write	Description	Default
7-0	R	When HID_OR0[7]==1'b0: Generic registers programmed by MCU When HID_OR0[7]==1'b1: Mapped from EEPROM_CTRL	0x00

HID_OR0 (HID output report byte 0)
Offset:0x04

Bits	Read/Write	Description	Default
7-6	R/W	0:HID_OR1-2 are used for GPO; HID_OR0, 3 are used for buzzer and SPDIF 1:HID_OR0-3 are used as generic HID registers 2:Values written to HID_OR0-3 are also mapped to MCU_CTRL, EEPROM_DATA0-1, EEPROM_CTRL(see Note) 3:Reserved	0x0
5	R/W	When HID_OR0[7]==1'b0: 0:Buzzeroff 1:Buzzeron When HID_OR0[7]==1'b1: Mapped to MCU_CTRL[5]	0x0
4	R/W	When HID_OR0[7]==1'b0: Valid bit in SPDIF frame When HID_OR0[7]==1'b1: Mapped to MCU_CTRL[4]	0x0
3-0	R/W	When HID_OR0[7]==1'b0: First nibble of SPDIF status channel When HID_OR0[7] == 1'b1: Reserved	0x0

Note: When EEPROM access is finished, HID interrupt will occur. USB host can get the result from interrupt pipe (endpoint3).

HID_OR1 (HID output report byte 1)
Offset:0x05

Bits	Read/Write	Description	Default
7-0	R/W	When HID_OR0[7:6] == 2'b00: 0:GPO drives L 1:GPO drives H When HID_OR0[7:6] == 2'b01: Generic HID registers When HID_OR0[7:6] == 2'b1x: Mapped to EEPROM DATA0	0x00

HID_OR2 (HID output report byte 2)
Offset:0x06

Bits	Read/Write	Description	Default
7-0	R/W	When HID_OR0[7:6] == 2'b00: 0:Set GPIO to input mode 1:Set GPIO to output mode When HID_OR0[7:6] == 2'b01: Generic HID registers When HID_OR0[7:6] == 2'b1x: Mapped to EEPROM_DATA1	0x00

HID_OR3(HID output report byte 3)
Offset:0x07

Bits	Read/Write	Description	Default
7-0	R/W	When HID_OR0[7]==1'b0: Category byte of SPDIF status channel When HID_OR0[7] == 1'b1: Mapped to EEPROM_CTRL	0x00

Note: HID_OR3 is used for SPDIF when SPDIF_CONFIG[5]==1'b0

6.6.2 Access via External Serial Interface by MCU

External MCU can write data to HID_IR0 to HID_IR3 and read data from HID_OR0 to HID_OR3. MINT will be active when HID_OR0-3 are updated by Set_Output_Report HID class command, and will be cleared after HID_OR0-3 are read by MCU.

HID_IR0(HID input report byte 0)
Offset:0x00

Bits	Read/Write	Description	Default
7-6	R/W	0:HID_IR0-3 are not used by MCU 1:HID_IR0-3 are used as generic HID registers 2:Values written to HID_IR0-3 are also mapped to MCU_CTRL, EEPROM_DATA0-1, EEPROM_CTRL(see Note) 3:Reserved	0x0
5	R/W	When HID_IR0[7] == 1'b0: 0:Buzzer off 1:Buzzer on When HID_IR0[7] == 1'b1: Mapped to MCU_CTRL[5]	0x0
4	R/W	When HID_IR0[7] == 1'b0: Generic HID register When HID_IR0[7] == 1'b1: Mapped to MCU_CTRL[4]	0x0

3	R	0: No activity on Record-Mute button 1: Record-Mute button pressed then released	0x0
2	R	0: No activity on Playback-Mute button 1: Playback-Mute button pressed then released	0x0
1	R	0: Volume-Down button released 1: Volume-Down button pressed	0x0
0	R	0: Volume-Up button released 1: Volume-Up button pressed	0x0

Note: When EEPROM access is finished, MINT will be active. MCU should read HID_OR0-3 to get the result and then MINT will be cleared.

HID_IR1 (HID input report byte1)
Offset:0x01

Bits	Read/Write	Description	Default
7-0	R/W	When HID_IR0[7] == 1'b0: Generic HID registers When HID_IR0[7] == 1'b1: Mapped to EEPROM_DATA0	0x00

HID_IR2 (HID input report byte2)
Offset:0x02

Bits	Read/Write	Description	Default
7-0	R/W	When HID_IR0[7] == 1'b0: Generic HID registers When HID_IR0[7] == 1'b1: Mapped to EEPROM_DATA1	0x00

HID_IR3(HID input report byte3)
Offset:0x03

Bits	Read/Write	Description	Default
7-0	R/W	When HID_IR0[7] == 1'b0: Generic HID registers When HID_IR0[7] == 1'b1: Mapped to EEPROM_CTRL	0x00

HID_OR0 (HID output report byte 0)
Offset:0x04

Bits	Read/Write	Description	Default
7-6	R	When HID_IR0[7] == 1'b0: HID_OR0-3 are programmed by USB host 0: HID_OR1-2 are used for GPO 1:HID_OR0-3 are used as generic HID registers 2:Values written to HID_OR0-3 are also mapped to MCU_CTRL, EEPROM_DATA0-1, EEPROM_CTRL 3:Reserved When HID_IR0[7] == 1'b1: Always 2'b11	0x0
5-4	R	When HID_IR0[7] == 1'b0: Generic registers programmed by USB host When HID_IR0[7] == 1'b1: Mapped from MCU_CTRL[5:4]	0x0

3-0	R	When HID_IR0[7] == 1'b0: Generic registers programmed by USB host When HID_IR0[7] == 1'b1: Always 4'h0	0x0

HID_OR1 (HID output report byte 1)
Offset:0x05

Bits	Read/Write	Description	Default
7-0	R	When HID_IR0[7] == 1'b0: Generic registers programmed by USB host When HID_IR0[7] == 1'b1: Mapped from EEPROM_DATA0	0x00

HID_OR2 (HID output report byte 2)
Offset:0x06

Bits	Read/Write	Description	Default
7-0	R	When HID_IR0[7] == 1'b0: Generic registers programmed by USB host When HID_IR0[7] == 1'b1: Mapped from EEPROM_DATA1	

HID_OR3 (HID output report byte 3)
Offset:0x07

Bits	Read/Write	Description	Default
7-0	R	When HID_IR0[7] == 1'b0: Generic registers programmed by USB host When HID_IR0[7] == 1'b1: Mapped from EEPROM_CTRL	0x00

6.6.3 Indirect Accessed Registers

MCU_CTRL (MCU control)
Offset:0x08

Bits	Read/Write	Description	Default
7-6	--	Reserved	0x0
5-4	R/W	0:MCLK operating at 1.5 MHz 1:MCLK operating at 3 MHz 2:MCLK operating at 6 MHz 3:Reserved	0x0
3-0	--	Reserved	0x0

EEPROM_DATA0 (Low byte of EEPROM data)
Offset: 0x09

Bits	Read/Write	Description	Default
7-0	R/W	Low byte of EEPROM data to be accessed	0x00

EEPROM_DATA1 (High byte of EEPROM data)
Offset:0x0a

Bits	Read/Write	Description	Default
7-0	R/W	High byte of EEPROM data to be accessed	0x00

EEPROM_CTRL (Serial EEPROM access control)
Offset:0x0b

Bits	Read/Write	Description	Default
7	R/W	When Register Read: 0:No EEPROM access pending 1:Last EEPROM access pending When Register Write: 0:No action 1:Start EEPROM access (will clear to 0 automatically)	0x0
6	R/W	0:Read EEPROM 1:Write EEPROM	0x0
5-0	R/W	Address of serial EEPROM	0x00

7 Electrical Characteristics

7.1 Absolute Maximum Rating

Symbol	Parameter	Value	Unit
Dvmin	Min Digital Supply Voltage	– 0.3	v
Dvmax	Max Digital Supply Voltage	+ 6	v
Avmin	Min Analog Supply Voltage	– 0.3	v
Avmax	Max Analog Supply Voltage	+ 6	v
Dvinout	Voltage on any Digital Input or Output Pin	–0.3 to +5.5	v
Avinout	Voltage on any Analog Input or Output Pin	–0.3 to +3.96	v
TBstgB	Storage Temperature Range	-40 to +125	P0PC
ESD (HBM)	ESD Human Body Mode	+-4000	v
ESD (MM)	ESD Machine Mode	+-200	v
Latch Up	JEDEC Standard No.78, Mar 1997	200	mA

7.2 Operation Conditions

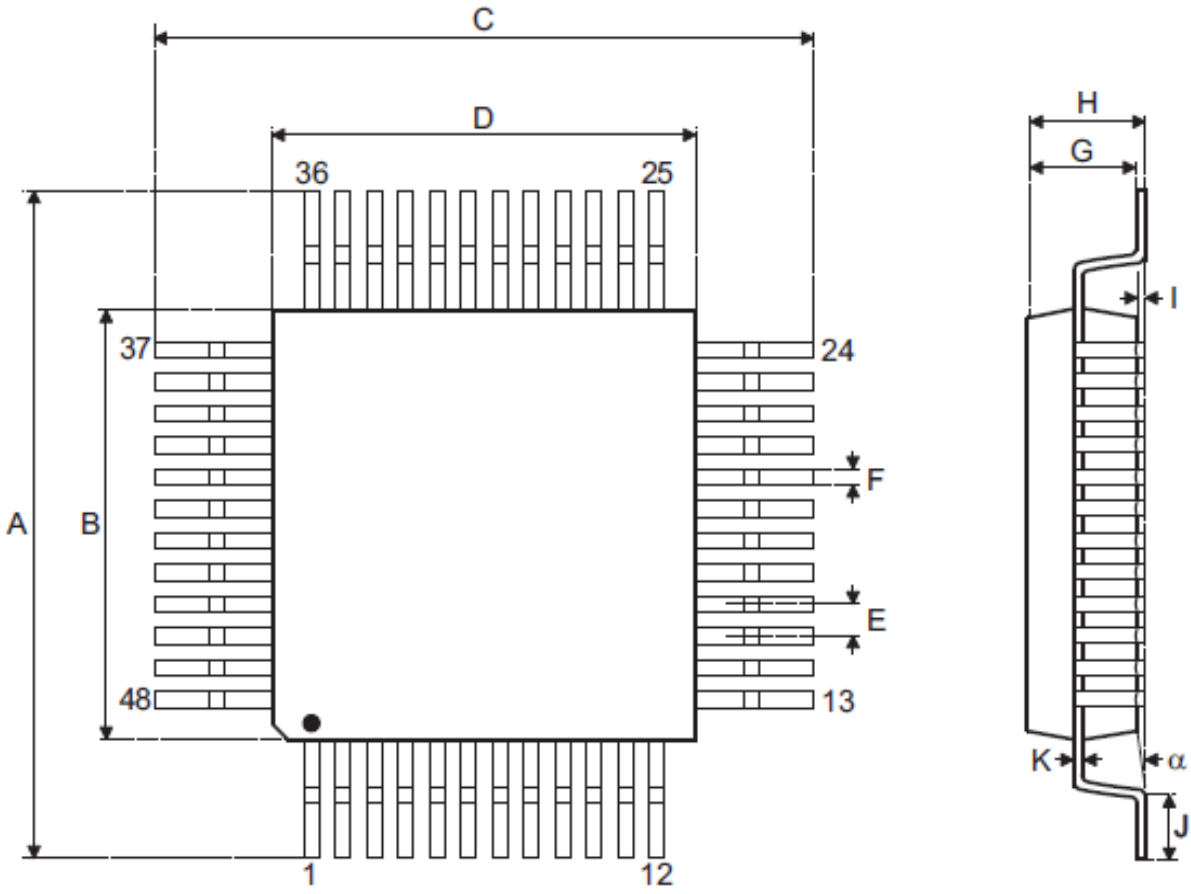
Operation conditions				
	Min	**Typ**	**Max**	**Unit**
Analog Supply Voltage	4.5	5.0	5.5	v
Digital Supply Voltage	4.5	5.0	5.5	v
Total Power Consumption	-	37.25	-	mA
Suspend Mode Power Consumption	-	1.58	-	mA
Operating ambient temperature	-15	-	70	PoPC

7.3 Electrical Parameters

	Min	**Typ**	**Max**	**Unit**
DAC (10K Ohm Loading)				
Resolution	-	16	-	bits
THD + N (-3dBr)@1KHz	-	-72	-	dB
SNR	-	93	-	dB
Silent SNR	-	98	-	dB
Dynamic range	-	92	-	dB
Frequency response 48KHz	20	-	20K	Hz
Frequency Response 44.1KHz	20	-	20K	Hz
Output Voltage (rms)*	-	0.995	-	Vrms
DAC (32 Ohm Loading)				
Resolution	-	16	-	bits
THD + N (-3dBr) @1KHz	-	-70	-	dB
SNR	-	93	-	dB
Silent SNR	-	98	-	dB
Dynamic range	-	92	-	dB
Frequency response 48KHz	20	-	20K	Hz
Frequency Response 44.1KHz	20	-	20K	Hz
Output Voltage (rms) *	-	0.442	-	Vrms
ADC				
Resolution	-	16	-	bits
THD + N (-3dBr) @1KHz	-	-84	-	dB
SNR	-	90	-	dB

Dynamic Range	-	88.5	-	dB
Frequency Response 48KHz	100	-	20K	Hz
Frequency Response 44.1KHz	100	-	20K	Hz
Input Range	0	-	2.88	Vpp
Amplification				
Volume Control Initial Value		-10		dB
Volume Control Level	-37	-	0	dB
Volume Control Step	-	38	-	steps
Microphone Input				
Boost Gain	-	12 / 22 (EEPROM)	-	dB
Gain Adjustment Initial Value		8		dB
Gain Adjustment Range	-12	-	23	dB
Gain Adjustment Steps	**-**	**36**	**-**	**steps**
Mixer Gain Initial Value		**-7**		dB
Mixer Gain Adjustment	**-23.0**	**-**	**8.0**	**dB**
Mixer Gain Adjustment Steps	**-**	**32**	**-**	**steps**

8 Package Dimensions



Symbol	Dimensions in mm		
	Minimum	Normal	Maximum
A	8.90	—	9.10
B	6.90	—	7.10
C	8.90	—	9.10
D	6.90	—	7.10
E	—	0.50	—
F	—	0.20	—
G	1.35	—	1.45
H	—	—	1.60
I	—	0.10	—
J	0.45	—	0.75
K	0.10	—	0.20
α	0°	—	7°

Reference

- Universal Serial Bus Specification, Version 2.0
- Universal Serial Bus Device Class Definitionfor Audio Devices, Version 1.0.
- Universal Serial Bus Device Class Definitionfor Human InterfaceDevices, Version 1.11

—End of Datasheet—

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