Data Sheet

BCM5340X

10GbE Embedded Switch

GENERAL DESCRIPTION

The Broadcom® BCM5340X System-on-a-Chip (SoC) switch family offers industry-leading integration and performance in a small footprint. The device offers up to 16 multilayer 10GbE ports in a 25 mm x 25 mm package. Offering the industry's highest level of integration, the BCM5340X family of switches has embedded SerDes supporting KX, KR, XAUI, RXAUI and SGMII modes. The BCM5340X is ideal for cost-sensitive edge connectivity applications, such as embedded designs for control plane applications or WebSmart and unmanaged switches for small and medium businesses (SMB).

The BCM5340X device family offers multiple I/O configurations and speeds (1G/2.5G/10G) that address key segments of edge connectivity.

With a 2 MB integrated packet buffer and the industry's lowest power consumption, the BCM5340X family of switches are designed to reduce overall system costs.

The optimized I/O map reduces system design effort and enables low-cost PCB design. The BCM5340X device family offers many advanced features such as IEEE 802.1Q VLAN, VLAN translation, enhanced Denial of Service (DoS) protection, IPv4 and IPv6 support, an advanced ContentAware™ engine, and IEEE 802.1p Quality of Service (QoS).

FEATURES

- Highly integrated 10 Gbps Ethernet switch SoC with integrated 1G/2.5G/5G/10G SerDes.
- Diverse selection of natively supported interfaces (KX, KR, XFI, XAUI, RXAUI, SGMII).
- Priority-based Flow Control (PFC).
- Timestamping support with IEEE 1588 1-step and 2-step transparent clock (TC) and Synchronized Ethernet (SyncE) as well as OAM (IEEE 802.1ag).
- Nonblocking architecture, line-rate for all packet sizes.
- Fully integrated packet buffer (2MB).
- Intelligent memory management unit (MMU) optimized for handling bursty data traffic.
- L2, IPv4/IPv6 L3 packet classification.
- Flexible Access Control List (ACL).
- IPv4 and IPv6 L3 routing support.
- Enhanced DoS attack statistics gathering.
- Energy Efficient Ethernet (EEE) support.
- Support for industrial temperatures.
- Low-power consumption.
- Integrated 500 MHz ARM R5 microcontroller.
- Flexible TCAM based single-stage ContentAware engine for ACL and QoS.
- Optimized for embedded control plane and WebSmart applications in SMB networks.
- Nonblocked, full wirespeed performance for 16x 10GbE systems.
- Enhanced buffer management for robust burst absorption.
- Low-power EEE support.
- Enterprise-class L2 scalability.
- Low-power 28 nm CMOS process.

5340X-DS112

Corporate Headquarters: San Jose, CA

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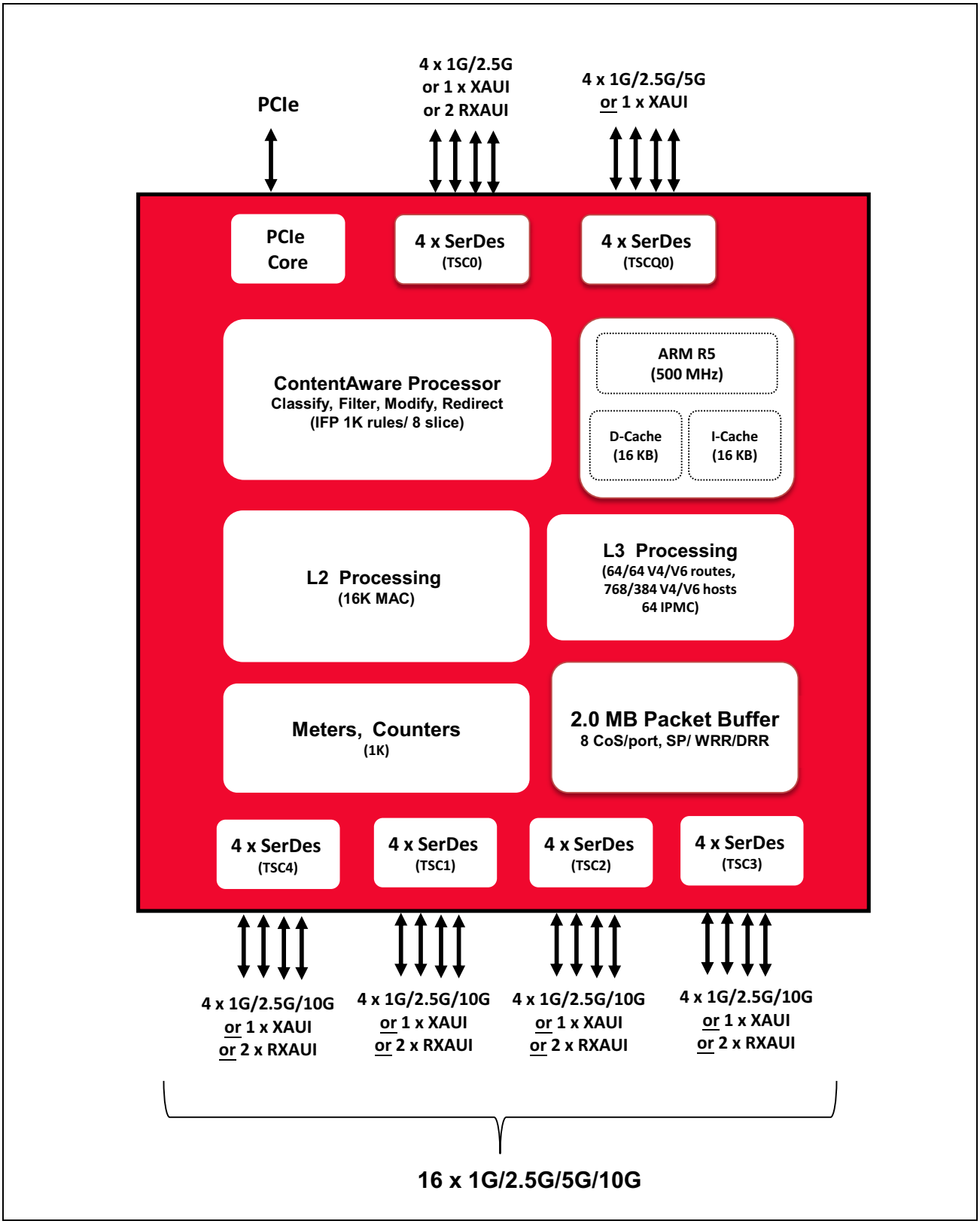
- Based on industry-leading and market-proven StrataConnect™ architecture.
- Single-chip switch SoC optimized for embedded control plane as well as WebSmart connectivity applications for SMB networks.
- Seamless connection to StrataXGS® fabric via HiGig2™ protocol.
- Enhanced memory technology delivers optimum usage of packet-buffer resources.
- Eight flexible Class of Service (CoS) queues per port assure the lowest latency to high-priority traffic.
- IPv6 support provides future-proofing.
- Leverages the Broadcom unified API for software reuse and quick time-to-market.
- Optimized ball pattern for low-cost PCB design and single-system clock source.

Figure 1: BCM5340X Functional Block Diagram



Revision History

Revision	Date	Change Description
5340X-DS112	01/05/18	**Updated:** • Table 6: “TSC Configurations,” on page 38 – Added HG[10] to 3.125G 1 port. – Corrected number of supported ports for 6.25G from 1 to 4. – Formatted notes for clarity. • Table 12: “Supply Voltage Range,” on page 63 by adding ESD specifications. • “Heat Sink Attachment” on page 101
5340X-DS111	03/13/17	**Updated:** • Jumbo frames from 9 KB to 9600B: – Table 6: “Switch Features,” on page 37 – Table 9: “System Interfaces,” on page 52
5340X-DS110-R	03/11/16	**Updated:** • Removed the data sheet qualifier “Advance” from the document type. • Table 7: “Switch Internal Memory Table,” on page 41 • Table 106: “Ordering Information,” on page 169 **Deleted:** • BroadSync Electrical Signals • BroadSync Interface Timing
5340X-DS109-R	12/03/15	**Updated:** • Table 1: “BCM5340X SoC Port Configurations,” on page 16 • Table 9: “Pin Description—Grouped by Function,” on page 41 • “Maximum Device Power” on page 61 • Table 22: “BSC Electrical Signals,” on page 65 • Table 28: “BSC Master/Slave Standard-Mode Timing,” on page 70 • Table 42: “XTALP/XTALN Input Requirements,” on page 86 • Table 43: “LC_PLL1_REFCLK Input Requirements,” on page 87 • Table 44: “TS_PLL_REFCLK Input Requirements,” on page 88 • Table 45: “BS[1:0]_PLL_REFCLK Input Requirements,” on page 89 • Table 56: “Serial Interface Transmit Characteristics,” on page 97
5340X-DS108-R	02/25/15	**Updated:** • Table 50: “XTALP/XTALN Input Requirements,” on page 123 • Table 70: “Ordering Information,” on page 141 **Added:** • “TS_PLL_REFCLK Clock Requirements” on page 125

Revision	*Date*	*Change Description*
5340X-DS107-R	11/25/14	**Updated:** • Table 1: “BCM5340X SoC Port Configurations,” on page 25 • Table 68: “QSPI BSPI Mode Master Interface Timing Specifications,” on page 145 **Added:** • Table 27: “BCM53406 Maximum Power (Tj = 110°C),” on page 115 • Table 28: “BCM53405 Maximum Power (Tj = 110°C),” on page 115 • Table 29: “BCM53402 Maximum Power (Tj = 110°C),” on page 116 • Table 66: “AC Specifications for the DDR3-1600 Interface,” on page 143
5340X-DS106-R	08/25/14	**Updated:** • Table 1: “BCM5340X SoC Port Configurations,” on page 25
5340X-DS105-R	06/02/14	**Updated:** • Figure 1: “BCM5340X Functional Block Diagram,” on page 4 • Table 1: “BCM5340X SoC Port Configurations,” on page 23 • Table 8: “System Interfaces,” on page 48 • Table 9: “TSC Configurations,” on page 51 • Table 16: “Pin Description—Grouped by Function,” on page 67 • Table 18: “Ball Out by Ball Number (Preliminary—Subject to Change),” on page 91 • Table 19: “Ball Out by Ball Name,” on page 96 • Table 67: “XTALP/XTALN Input Requirements,” on page 144 • Table 68: “LC_PLL1_REFCLK Input Requirements,” on page 145
5340X-DS104-R	01/24/14	**Added:** • Section 8: “AC Timing Characteristics,” on page 119 **Updated:** • Figure 1: “BCM5340X Functional Block Diagram,” on page 3
5340X-DS103-R	12/17/13	**Added:** • Section 7: “Electrical Characteristics,” on page 113 • Section 9: “Thermal Specifications,” on page 158 • Section 10: “Mechanical Information,” on page 160 **Updated:** • Figure 1: “BCM5340X Functional Block Diagram,” on page 3 • “TDM-based SerDes Controller” on page 49: Changed from Warpcore™ throughout • Table 16: “Pin Description—Grouped by Function,” on page 66: Renamed BSC signals and Warpcore/TSC signals and updated Ground signals. • Table 18: “Ball Out by Ball Number (Preliminary—Subject to Change),” on page 85 and Table 19: “Ball Out by Ball Name,” on page 94
5340X-DS102-R	11/14/13	**Added:** • Section 6: “Signal Description and Pin Lists,” on page 61 **Updated:** • Table 40: “Ordering Information,” on page 119: Corrected part numbers.

Revision	*Date*	*Change Description*
5340X-DS101-R	08/29/13	**Updated:** • Minor changes.
5340X-DS100-R	05/03/13	Initial release.

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About This Document

Purpose and Audience

This document describes the Broadcom® BCM5340X SoC. The Broadcom BCM5340X integrates an Ethernet switch controller with 24 multilayer GbE ports and up to four configurable XFI ports.

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

Acronyms and abbreviations in this document are also defined in Appendix A: “Acronyms and Abbreviations,” on page 105.

For a comprehensive list of acronyms and other terms used in Broadcom documents, go to: http://www.broadcom.com/press/glossary.php.

Document Conventions

The following conventions may be used in this document:

Convention	*Description*
Bold	User input and actions: for example, type **exit**, click **OK**, press **Alt+C**
`Monospace`	Code: `#include <iostream>` HTML: `<td rowspan = 3>` Command line commands and parameters: `wl [-l] <command>`
< >	Placeholders for *required* elements: enter your <username> or `wl <command>`
[ ]	Indicates *optional* command-line parameters: `wl [-l]` Indicates bit and byte ranges (inclusive): [0:3] or [7:0]

Technical Support

Broadcom provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates through its customer support portal (https://support.broadcom.com). For a CSP account, contact your Sales or Engineering support representative.

In addition, Broadcom provides other product support through its Downloads and Support site (http://www.broadcom.com/support/).

Section 1: Introduction

Overview

The Broadcom BCM5340X is an SoC for different embedded, backplane, or switching applications.

The BCM5340X SoC port configurations are shown in Table 1 on page 16.

Table 1: BCM5340X SoC Port Configurations

Device	*CPU*	*XAUI*	*10GbE*	*1G/2.5G*	*QSGMII*	*TSCQ0*	*TSC0*	*TSC1*	*TSC2*	*TSC3*	*TSC4*
BCM53405	R5	0	16	0	0	OFF	OFF	4 x 1G/2.5G/5G/10G or 1 x XAUI or 2 x RXAUI	4 x 1G/2.5G/5G/10G or 1 x XAUI or 2 x RXAUI	4 x 1G/2.5G/5G/10G or 1 x XAUI or 2 x RXAUI	4 x 1G/2.5G/5G/10G or 1 x XAUI or 2 x RXAUI
BCM53406	R5	0	12	12	0	4 x 1G/2.5G/5G or 1 x XAUI	4 x 1G/2.5G	4 x 1G/2.5G	4 x 1G/2.5G/5G/10G or 1 x XAUI or 2 x RXAUI	4 x 1G/2.5G/5G/10G or 1 x XAUI or 2 x RXAUI	4 x 1G/2.5G/5G/10G or 1 x XAUI or 2 x RXAUI
		4	8	0	0	1 x XAUI	1 x XAUI	1 x XAUI	1 x XAUI	4 x 1G/2.5G/5G/10G or 1 x XAUI or 2 x RXAUI	4 x 1G/2.5G/5G/10G or 1 x XAUI or 2 x RXAUI
		4	4	0	0	1 x XAUI	1 x XAUI	1 x XAUI	1 x XAUI	4 x 1G/2.5G/5G/10G	OFF
		0	15	9	0	4 x 1G	4 x 1G	1 x 1G + 3 x 1G/2.5G/10G	4 x 1G/2.5G/5G/10G or 1 x XAUI or 2x RXAUI	4 x 1G/2.5G/5G/10G or 1 x XAUI or 2 x RXAUI	4 x 1G/2.5G/5G/10G or 1 x XAUI or2 x RXAUI
BCM53402	R5	0	8	0	0	OFF	OFF	4 x 1G/2.5G/5G/10G or 1 x XAUI or 2 x RXAUI	4 x 1G/2.5G/5G/10G or 1 x XAUI or 2 x RXAUI	OFF	OFF

Ethernet Switch Controller

The BCM5340X is a highly integrated solution ideally suited for embedded switches as well as aggregation switches. The switch controller combines all the functions of a high-speed switch system, including packet buffer, SerDes, media access controllers, address management, and a nonblocking switch fabric. The BCM5340X device supports auto-DoS attack prevention and SNMP, IEEE 802.1x, Spanning Tree, and Rapid Spanning Tree protocols.

The BCM5340X:

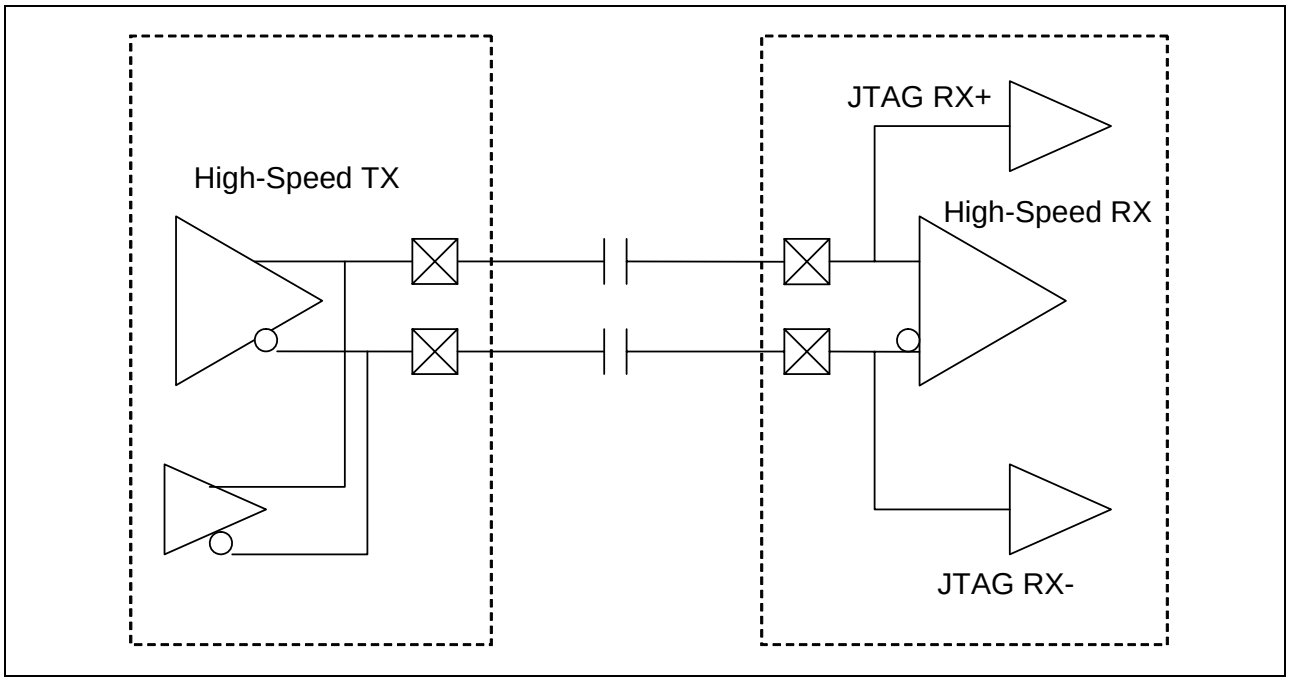
- Provides sixteen 10GbE ports with BCM53405 chip. The 10GbE port supports 1GbE/2.5GbE/10GbE speeds on an XFI interface.
- Provides twelve 1GbE/2.5GbE ports. The 1GbE/2.5GbE port supports SGMII, 1000BASE-X, 2500BASE-X or HiGig-Lite protocol.
- Provides twelve 10GbE ports plus twelve 1GbE/2.5GbE ports with a BCM53406 chip.
- Integrates 2 MB internal memory in the Common Buffer Pool (CBP) for packet buffering.
- Provides hardware support for IPv4 and IPv6 protocols.
- Supports a Broadcom Serial Control (BSC) controller for communicating with external devices such as parallel port devices.
- Supports a serial interface for the MII management (MDC/MDIO) of physical layer devices.
- Supports a PCIe interface for external CPU host communication.
- Contains the memory needed to host L2 and L3 switching tables.
- Supports VLAN double-tagging.
- Supports advanced QoS shaping for service provider networks.
- Integrates sophisticated metering, statistics, and traffic management features, optimizing the QoS for voice, video, and data convergence.
- Provides built-in security functions for highly secure enterprise networks like Random number generators and Public Key Accelerators.
- ContentAware processing (via the Filter Processor (FP) feature) enables unmatched flexibility and programmability. The ContentAware engine can be used for applications such as policy-based routing or Access Control List (ACL) operation.
- One MDIO interface

Section 2: Common Interfaces

JTAG and EJTAG

Traditional JTAG provides the capability to test for short and open conditions when the device is mounted in the PCB, based on a direct connection. Present technology, where most high-speed differential signals are required to be AC–coupled, can produce false results due to traditional DC tests for short and open. To provide a means of testing high-speed differential signals, the BCM5340X supports the latest JTAG specification IEEE Std.1149.6 (also known as AC-JTAG). To determine manufacturing faults on a high-speed differential line within a PCB, the device incorporates independent transceivers with low-load capacitance to avoid an adverse effect on the high-speed differential line (see Figure 2).

Figure 2: AC-JTAG Test Block



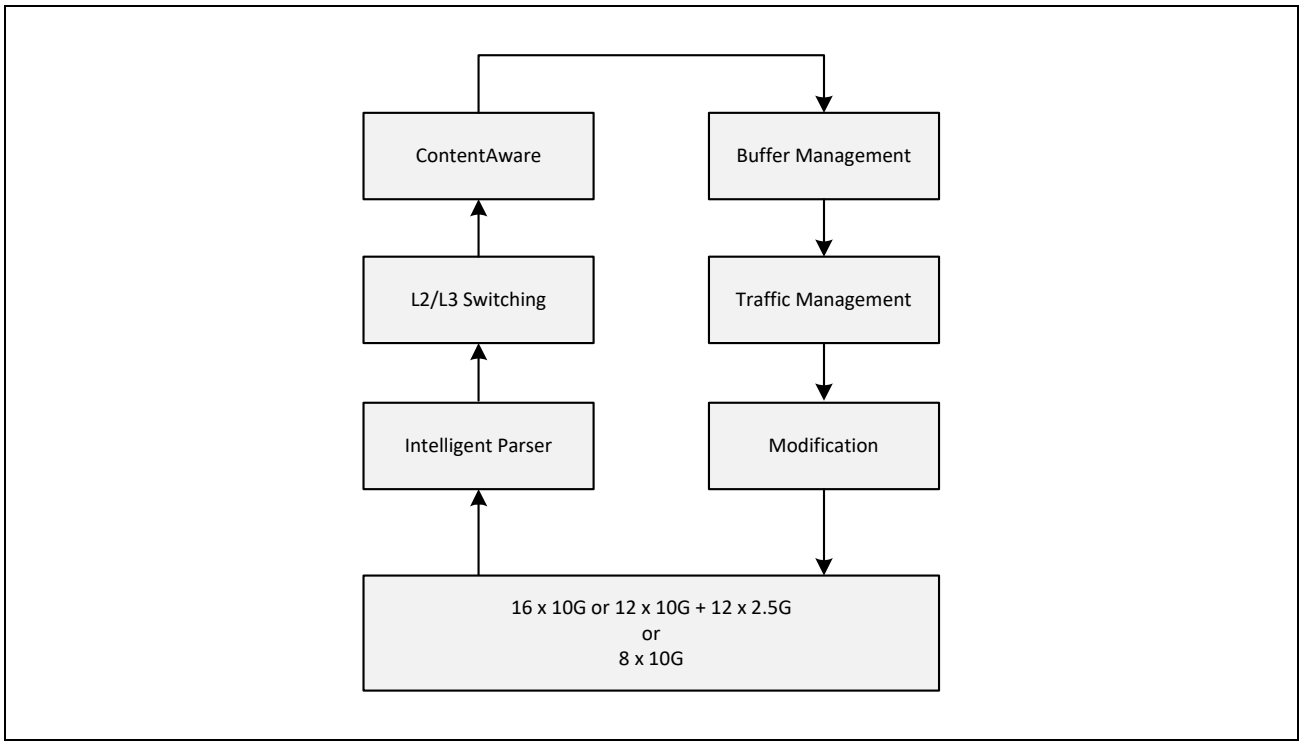
Section 3: Ethernet Switch Controller Features Description

Architecture

The integrated Ethernet Switch Controller has a modular, high-performance pipelined packet-switching (BroadScale®) architecture. This enables:

- Cost reduction
- Migration to different process technologies without architectural changes
- Flexible port configurations
- Scalable throughput
- Scalable custom features

Figure 3: Typical BCM5340X BroadScale Switching Architecture



Feature Overview

Some switch features and port counts may vary depending on the device ID (see “Overview” on page 15 for additional details).

Table 2: Switch Features

Feature	*Description*
Configuration	• Versatile port configurations. See Table 1 on page 16 for overall configuration. The Flexible TDM-based SerDes Controller (TSC) contains four SerDes lanes: – Supports 10GbE across a single lane: XFI/SFI/10GBASE-KR/-LR/-CR/-SR. – Supports 1000BASE-X/2500BASE-X across a single lane. – Supports 10GbE across four lane: XAUI. – Supports 10GbE across two lane: RXAUI. • Dynamic buffer management. • Supports: – Ethernet/IEEE 802.3 packet sizes (64 bytes to 1522 bytes). – Jumbo packets up to 9600B.
L2 Switching	• Supports: – Learning up to 16K MAC addresses depending on device. – Static entries. – MAC limiting per port/LAG/VLAN. • Line-rate switching for all packet sizes. • Shared and Independent VLAN learning. • VLAN flooding for broadcast and DLF packets. • Hardware-based address learning. • Support policy-based learning. • Hardware-and software-based aging. • Software insertion/deletion/lookups of the L2 table. • Same port bridging supported.
L2 Multicast	• Supports L2 multicast groups. • Line-rate switching for all packet sizes. • Three port filtering modes to control multicast packet behavior.

Table 2: Switch Features (Cont.)

Feature	*Description*
VLAN	• Supports 4K VLANs and assign VLAN for untagged and priority tagged packet on: – MAC-based VLANs. – Protocol-based VLANs. – IP-subnet based VLANs. – IEEE 802.1p. – IEEE 802.1Q. • Independent and Shared VLAN Learning (IVL and SVL). • Ingress filtering for IEEE 802.1Q VLAN security. • VLAN-based packet filtering. • VLAN translation on ingress and egress.
Double VLAN Tagging	• Support for IEEE 802.1ad provider bridging: – Unqualified learning/forwarding. – Ability to add, remove, and translate (replace) both service-provider VLAN tag and customer VLAN tag. – Support for four programmable outer TPIDs with nonoverlapping VLANs. • Support for double tagging requirements of Broadband Forum TR-101. – Packet forwarding is supported based on: • S-VLAN bridging (L2 switch based on MAC_DA and S-VID). • S-VLAN cross-connect: Destination port is based on S-VID only. • Double VLAN cross-connect: Destination port is based on (S-VID, C-VID) combination. – Supports for 2K shared {S-VID, C-VID}.
Source Port Filtering	• Egress port block masks. • Trunk group blocking masks.
Storm Control	• Four meters for packet-based or byte-based rate control with the below packet types: – Unknown unicast (DLF) packet rate control. – Broadcast packet rate control. – Known L2MC packets rate control. – Unknown L2MC packets rate control. – Known IPMC packets rate control. – Unknown IPMC packets rate control. – Enable individual threshold per port.
Spanning Tree	• Supports: – IEEE 802.1D spanning tree protocol (single spanning tree per port). – IEEE 802.1s for multiple spanning trees. – IEEE 802.1w rapid spanning tree protocol—delete and/or replace per port, per VLAN, or per port per VLAN. • Spanning tree protocol packets detected and sent to the CPU.

Table 2: Switch Features (Cont.)

Feature	*Description*
IEEE 802.3ad Link Aggregation	• 128 trunk groups supported with up to eight members per group. • No adjacency limitation. • Traffic load distribution for L2 switched and L3 routed packets. • Trunk port selection based on hash on source/destination MAC, VLAN, EtherType, source/destination IP address, TCP/UDP ports. • Trunk port selection for DLF, broadcast, and multicast packets.
Mirroring	• Ingress/egress mirroring support. • Mirror-to-port receives unmodified packet for ingress mirroring. • Mirror-to-port receives modified packet for egress mirroring. • Mirroring across stacked modules. • Remote Switched Port Analyzer (RSPAN) mirroring, VLAN mirroring, flow mirroring. • Encapsulated Remote Switched Port Analyzer (ERSPAN) mirroring. • Mirror-to-port can be a link aggregation group.
DSCP	• Per port DSCP remarking. • DSCP remarking based on a FP filter match. • DSCP to IEEE 802.1p mapping. • Remap incoming DSCP to new outgoing DSCP.
L3 Routing (IPv4, IPv6)	• 768 (IPv4) or 384 (IPv6)hosts line-rate routing for all packet sizes and conditions. • Supports: – Directly-attached hosts in the L3 table. – Longest prefix match (LPM) based routing. • Software based aging support. • Up to 64 LPM entries (IPv4) or 64 LPM entries (IPv6).
IP Multicast	• Line-rate operation for all packet sizes and conditions. • Simultaneous L2 bridging and L3 routing. • Flexible multicast packet replication support for up to 4K VLANs. • Optional source port and VLAN checks. • Dual lookup: {S, G, V} and {*, G, V}. • PIM-SM, PIM-DM, PIM-SSM, and DVMRP on a per VLAN basis. • Reverse path forwarding checks. • Ability to fall back to L2 multicast lookup on IPMC miss. • Port Filter Mode (PFM) per VLAN for L2 multicast, IPv4 multicast, and IPv6 multicast packets. • Control trapping of unknown IPMC packets to CPU on a per VLAN per IP-type basis. • IP multicast address consistency check with destination MAC address.

Table 2: Switch Features (Cont.)

Feature	*Description*
ContentAware—Ingress Filter Processing	• Up to 1K FP rules with eight slices allowing eight parallel lookup and match. • Layer 2–7 packet classification. • Intelligent Protocol Aware processor with backward compatible byte-based classification option. • Parses up to 128 bytes per packet. • Multiple look-ups per packet. • Supports: – Multiple matches and actions per packet. – ACL-based policing. – Ingress/egress port based filtering. – MAC destination address remarking. – Class-based marking for SLAs. – Traffic class definition based on the filter. – Classification of different packet formats (IPv6, IPv4, double tagged, HTLS, IEEE 802.1Q, Ether II, IEEE 802.3). • Hierarchical min/max programmable meters allows policing of flows. • Metering granularity from 8 Kbps to 1 Gbps. • Dual leaky bucket meters support two rate three-color marking. • srTCM, trTCM, and modified trTCM (RFC2697, RFC2698, RFC4115). • Metering support on ingress ports and CPU queues. • Jumbo packet metering. • TCP/UDP port number range checking. • IPv6 filtering (128 bits). • Filtering IP packets with options.
QoS Features	• Eight CoS queues per port. • Enhanced eight CoS queues for CPU. • Three drop precedence colors. • Per port, per CoS drop profiles. • Minimum/maximum bandwidth guarantee (shaping) per CoS, per port. • Traffic shaping available on CPU queues: bandwidth based and packet-per-second based. • Programmable priority to CoS queue mapping. • Provides two levels of drop precedence per queue. • Explicit congestion notification support. • Strict Priority (SP), Weighted Round Robin (WRR), and Deficit Round Robin (DRR) mechanism for shaped queue selection. • Programmable bucket size of egress port shaping and COS shaping. • Support for ingress port rate based policing and pause flow control. • Mapping of incoming priority, CFI to outgoing priority and drop precedence. • Supports IEEE 802.1bb Priority Flow Control (PFC). PFC PAUSE quanta may exceed the final IEEE 802.1Qbb specification.

Table 2: Switch Features (Cont.)

Feature	*Description*
Port Security	• Supports IEEE 802.1x. • Blocking of egress ports on per ingress port or LAG basis (source port filtering). • Blocking of egress ports on per MAC address basis. • Blocking of egress ports for broadcast, unknown unicast, and multicast packets.
Denial of Service (DoS) Attack Prevention/Protocol Checkers	• Built-in illegal address check (IPv4, IPv6). • Denial of Service detection/prevention. • Land packets (SIP = DIP). • NullScan (TCP sequence number = 0, control bits = 0). • Ping flood (flood of IPMC packets). • SYN/SYN-ACK flooding. • SYN with sPort < 1024. • Smurf attack. • Individual control over handling of DOS packet.
CPU Protocol Packet Processing	• Ability to individually control CPU protocol packet handling, including BPDU, Address Resolution Protocol (ARP), Internet Group Management Protocol (IGMP), Multicast Listener Discovery (MLD), and DHCP. • Individual control of trapping protocol packets and setting internal priority. • Extensive control of handling of IGMP and MLD packet types.
Stacking Links	• Supports L2/L3 across stacked modules. • L2MC. • VLAN membership supported across stacked modules. • Seamless CoS support. • Mirroring and remote mirroring support. • Supports up to 64 stacked modules. • IPMC. • Trunking of stacking ports. • ContentAware processing on stacking port.
Management Information Base	• sFLOW support, RFC 3176. • RMON statistics group, IETF RFC 2819. • SNMP interface group, IETF RFC 1213, 2836. • Ethernet-like MIB, IETF RFC 1643. • Ethernet MIB, IEEE 802.3u. • Bridge MIB, IETF RFC 1493.
Ethernet OAM	• Supports IEEE 802.1ag connectivity fault management solution, including hardware CCM transmission, CCM fault monitoring, and loopback reply. • ITU Y.1731 on-demand/proactive loss measurement and one-way delay measurement.
Energy Efficient Ethernet (EEE)	• System power saving by informing external PHY into Low Power Idle (LPI) state. • Only MAC layer of EEE requirements are implemented on 1G/10G ports.

Table 2: Switch Features (Cont.)

Feature	Description
Network TimeSync	• Supports IEEE 802.1AS and IEEE 1588 network time distribution. • Supports layer 1 clock recovery.

Memory

The BCM5340X device integrates all table memory necessary to support its functions. Table 3 indicates the major internal table memory allocations and their functions for switching, routing, and classification.

Table 3: Switch Internal Memory Table

Table Name	Size	Function
Port Table	One entry per each GbE, XFI and CPU port	Per port configuration settings and attributes, that is, L2 learning, port discards, VLAN handling, priority assignment.
IP Subnet-Based VLAN Table	256 Subnet	Assigns VLAN based on source IP subnet for untagged and priority tagged packets.
MAC-Based VLAN Table	1K MAC addresses	Assigns VLAN based on source MAC address for untagged and priority tagged packets. This table is shared with the VLAN Translation table.
IPV4-MAC Binding and ARP Spoofing Table	1K table for ingress[a]	Checks the IPV4-MAC binding of IP packets as well as ARP/RARP request/reply messages for sender IPV4-sender MAC address binding.
VLAN Translation Table	1K table for ingress 1K table for egress	Translates VLAN between customer VLAN and service provider VLAN for provider bridging. This table is shared with MAC-based VLAN table.
Protocol-Based VLAN Table	16 per port	Assigns VLAN based on packet protocol for untagged and priority tagged packets.
VLAN Table	4K VLANs	Indicates port membership and spanning tree group for each VLAN.
DSCP Table	1920 entries	Remaps ingress and egress DSCP to new DSCP and priority.
Spanning Tree Group Table	128 groups	Indicates spanning tree state for each port for each spanning tree group.
MAC Address Table	16K MAC addresses	Contains learned and programmed MAC addresses: indicates destination port and additional properties of each MAC address, i.e., source/destination discard, priority, blocking, mirroring.
Reserved MAC Address Table	128 entries	Contains reserved MAC addresses, programmed by software for special handling, i.e., copy to CPU, drop, flood, for control packets, BPDUs. Reserved MAC Address table can also be used as an overflow for MAC address table. The only difference between these two tables is that the Reserved MAC table is managed by software.
MAC Block Table	32 groups	Allows for selective blocking and flooding to egress ports based on source MAC address groups.

Table 3: Switch Internal Memory Table (Cont.)

Table Name	Size	Function
Layer 2 Multicast Table	512 groups	Indicates port membership for Layer 2 multicast groups.
Link Aggregation Group Table	128 groups	Indicates port membership of link aggregation groups and hash selection criteria.
Layer 3 Host Route Table	768 IPv4 hosts 384 IPv6 hosts	Contains host IPv4 and IPv6 addresses for Layer 3 host routing, used as ARP cache.
Layer 3 LPM Route Table	64 IPv4 routes 64 IPv6 routes	Contains IPv4 and IPv6 subnets for longest prefix match routing, including ECMP/WCMP routing.
Layer 3 IP Multicast Table	64 groups	Indicates port membership for Layer 3 IP multicast (S,G) or (*,G) lookups, and controls replication of IPMC packets on egress ports with multiple VLANs.
Ingress ContentAware Processor Table	1K rules, 8 parallel lookups	Rules for L2–L7 packet classification on ingress, ACLs, metering, and statistics.

a. Shared with ingress VLAN translation table.

Table 4: OAM Table

Table Name	Size	Function
LMEP	512	For generating hardware CCM packets.
LMEP DA	512	For generating hardware CCM packets.
L3 Entry IPV4 Unicast	512	MP Group Lookup Table shared with IPV4 Unicast Route Entry Table.
MA Index	512	Provide session id for each MEP and the opcode profile pointer.
MAID Reduction	512	Compare the reduced MAID from the packet to the configured value in the table.
MA State	512	Track the state of the local MEP for CCM packets.
RMEP	2K	Track the state of the remote MEP for CCM packets.
OAM Opcode Control Profile	16	For action control defined for processing each opcode.
OAM LM Counter	4K	Counters for OAM loss measurement.

Address Management

The BCM5340X switch contains all of the tables required to manage station MAC addresses on the device. The address table (also referred to as the L2 table) has space for 16,384 entries. New entries in the table are automatically learned when packets are received on the ports. These entries can also be updated or created by the CPU. Learning is based on the source MAC address and VLAN ID. Entries that are not used for an extended period of time are automatically aged out. The device can be configured to age static entries as well.

For any valid incoming packet, the source MAC address along with the VLAN ID (either from the packet or from VLAN tables inside the device) is used to search the tables. On a successful match of (S-MAC, VLAN-ID) the device performs station move checks. If the incoming port does not match a port in the MAC table, the entry is relearned with the new incoming port value.

The destination MAC address, along with the VLAN ID, is used as a search key for the packet's output port. If a match is found, then the packet is switched out on that port. If a match is not found, then a Destination Lookup Failure (DLF) occurs, and the packet is switched out on all ports that are members of the VLAN.

Class of Service

The IEEE 802.1D specification defines eight levels of priority 0–7, with priority 7 being the highest priority. This information is carried in the 3-bit priority field of the VLAN tag header. This service applies to all network ports.

The BCM5340X switch supports up to eight CoS queues per egress port. For tagged packets, the incoming packet priority can be mapped to one of the eight CoS queues, based on the priority field in the tag header or from the result of filtering mechanisms. For untagged packets, the CoS priority is derived either from a programmable field within the VLAN address tables or from the result of filtering mechanisms. After the packets are mapped into a CoS queue, they are forwarded or conditioned using either Strict Priority (SP), Deficit Round Robin (DRR), or Weighted Round Robin (WRR) schedulers.

Strict Priority-Based Scheduling

In SP policy, any packet residing in the higher priority queues is transmitted first. Only when these queues are empty, will packets in lower priority queues be transmitted. The disadvantage of this scheme is potential starvation of packets in lower-priority queues.

Weighted Round Robin Scheduling

In the WRR scheme, each queue is assigned a weight. The number of packets sent from each priority queue depends on the weight. Because the unit of the weight is one packet, the weight can be anywhere from 64 bytes to 1522 bytes, or 9600B (when supporting jumbo frames).

> ***Example:*** If there are four CoS queues of A, B, C, and D and the respective weights are 4, 3, 2, and 1, and if the packets are present in all the queues, the packets are sent in the sequence of A1, B1, C1, D1; A2, B2, C2; A3, B3; A4, accordingly.

Deficit Round Robin Scheduling

The Deficit Round Robin (DRR) scheme provides relative bandwidth sharing across all active COS queues. The DRR weights are relative to each other. If minimum bandwidth is configured in this mode, then it is served first. Any excess bandwidth is then shared according to the DRR weights.

Backpressure Handling

The BCM5340X switch supports mechanisms to handle backpressure, allowing for flexible flow control on packet transactions. The limit at which backpressure is detected is based on the amount of memory utilized by the packets on an input port. A backpressure message (XOFF) is sent when the lower of the two conditions (cell count limit or packet count limit) is reached. When the corresponding count goes below the high threshold and reaches the low threshold, an XON message is sent. This limit flow control is applied to the:

- IEEE 802.3x flow control. If the port is configured in full-duplex mode, IEEE 802.3x flow control is used and the MAC control PAUSE frame is sent to inhibit traffic on that port for a specified period of time.
- Enable jamming signal. If the port is configured in half-duplex mode and enabled to send a jamming signal, the jamming signal is asserted.

For ports that continue to receive packets, even after applying the above-noted flow control, the packets are discarded. Similarly, when the packets are switched out and the memory utilization falls below the limit, incoming packets are handled again. For full-duplex ports, another PAUSE frame is sent, with the time period set to 0, upon which the remote port can transmit again. For half-duplex ports, if the jamming signal was asserted, it will now be deasserted.

Per Port Packet Rate (Storm) Control

The BCM5340X provides a per port packet or byte rate control mechanism to prevent the packets from flooding into other parts of the network. These programmable threshold limits apply to all ports. Several types of packets can be monitored:

- DLF/Unknown unicast packets
- Broadcast packets
- Unknown L2 Multicast packets
- Known L2 Multicast packets
- Unknown IPMC Multicast packets
- Known IPMC Multicast packets

The packet types are flexibly mapped to four leaky bucket mechanisms, and packets are discarded if the respective bucket becomes out of profile.

Mirroring

Mirroring is a useful feature for monitoring the traffic coming in or going out on a particular port. A port can be ingress-mirrored or egress-mirrored. The mirrored-to port can be programmed as a sniffer port to monitor all traffic on the mirrored ports. When a port is ingress-mirrored, any packet received on that port is sent to a mirrored–to port, and any packet transmitted from the egress-mirrored port is also sent to the mirrored-to port.

The BCM5340X supports the following packet mirroring functions:

- Mirror frames destined for an egress-specific port (egress mirroring)
- Egress mirroring of packets sent by the CPU
- Mirror frames coming from ingress-specified port (ingress mirroring)
- Mirror frames coming from a specific ingress port sent to a specific egress port
- Mirror frames that match a certain rule in the filtering processor
- Mirror frames destined to a specific MAC address

The BCM5340X supports mirror across stack.

Spanning Tree Support

The BCM5340X provides a number of features for compliance with the IEEE 802.1D and IEEE 802.1S spanning tree support specifications, as well as some optimizations for IEEE 802.1W rapid spanning tree support:

- The state bits in the spanning tree group are configured by the CPU to indicate a specific spanning tree state, and the necessary action is taken on the incoming packet. The spanning tree states supported are: disable, blocking, listening, learning, and forwarding.
- Entries marked as static in the MAC table are not aged out.
- The MAC table entry allows for detecting a hit on an address entry. If there is no hit on an entry for the spanning tree age limit duration, the address entry is deleted.
- All nonreserved addresses are self–learned.
- Reserved addresses from 0x0180c2000000 to 0x0180c2000010 and from 0x0180c2000020 to 0x0180c200002F are detectable, and these packets are forwarded to the CPU.
- Supports multiple 256 spanning trees (IEEE 802.1s). Each VLAN can be associated with one spanning tree group, which allows spanning tree-per-VLAN operation.
- Support for IEEE 802.1W Rapid Spanning Tree Protocol, with the ability to delete MAC table entries or replace the associated port information based on search criteria such as port and VLAN.

IEEE 802.1D Support

The BCM5340X supports the IEEE 802.1D specification for traffic class expediting and dynamic multicast filtering support. On a per VLAN basis, the following bridge-filtering and port-filtering modes are supported:

Port Filtering Mode A

Forwards all addresses. In this mode, forwarding operates as bridge filtering mode 1. The port bitmap from the VLAN tables is used to determine the destination ports.

Port Filtering Mode B

Forwards all unregistered addresses. In this mode, if the group MAC address registration entries exist in the multicast table, frames destined for the corresponding group MAC addresses are forwarded only on ports identified in the member port set, which is identified by the port bitmap. If the group MAC address does not exist in the multicast table, then Mode A filtering mechanism is used.

Port Filtering Mode C

Filters all unregistered addresses. In this mode, frames destined for group MAC addresses are forwarded only if such forwarding is explicitly permitted by a group address entry in the multicast table. In other words, if the group MAC address exists in the multicast table, then the packets are forwarded using the port bitmap from that entry. Otherwise, the packets are dropped.

IEEE 802.1Q Support

The BCM5340X supports the IEEE 802.1Q specification for virtual bridged local area networks by providing the following features:

- For untagged (frame without a VLAN header) or priority tagged (frame with a tag header of VLAN ID = 0) frames, the ability to assign a VLAN based on the Source MAC Address, Source IP Address, or on a protocol. If a match is not found via these tables, then a default VLAN ID can be assigned per ingress port.
- Identification of the GVRP address 0x01-80-C2-00-00-21 and forwarding these frames to the CPU.

Link Aggregation

Link aggregation or trunking is a mechanism which bundles together up to eight ports to form a port bundle or a trunk. The port bundle is like one logical link and is useful when high bandwidth and/or redundancy between switches are required. The features include:

- Trunk ports in a bundle are always configured for full duplex.
- Trunking of network ports provides aggregate throughput up to a maximum of eight front-panel ports per trunk group.

- Provides incremental bandwidth dependent upon requirements.
- Provides link redundancy. In case of trunk port failure, the trunk group is modified and the port that failed is removed from the group.
- Provides load distribution on the trunk ports.

The BCM5340X supports 128 trunk groups, and each trunk group can have up to eight trunk ports. The trunk links are selected using a hashing function based on a combination of: MAC DA, MAC SA, VLAN, EtherType, IP DA, and IP SA. The BCM5340X supports link aggregation, with no adjacency limitation, within the same switch module and across stack.

Note: The Uplink ports may be included as trunk link members.

Double-Tagging

The BCM5340X provides full support for double tagging as specified in the emerging IEEE standard, including the following features:

- The Service Provider VLAN ID (SPVID) can be inserted based on ingress port or ingress port and customer VLAN.
- The Protocol field on the SPVID is fully programmable.
- The priority bits in the SPVID can be programmed by the provider or from the customer VLAN tag in the packet.
- The ability to distinguish customer control packets (such as spanning tree BPDUs). They may be discarded or processed locally depending on configuration.

Forwarding Control Block Mask

On certain ports in the switch, DLF unicast and multicast packets should be prevented from being forwarded. However, broadcast packets should always be forwarded to all ports.

To implement this feature:

1. Three separate registers, UNKNOWN_UCAST_BLOCK_MASK, UNKNOWN_MCAST_BLOCK_MASK, and BCAST_BLOCK_MASK are bitmasks for unknown unicast, unknown multicast, and unknown broadcast packets.
   a. The bits not set in these bitmasks define a set of egress ports to which unknown unicast, multicast, and broadcast frames should be forwarded.
   b. To block broadcast packets to a specific port, the appropriate bit is set in the BCAST_BLOCK_MASK.
   c. To forward broadcast packets to all ports of the VLAN, set all the bits in BCAST_BLOCK_MASK to 0.
2. Ingress logic will pick up the port bitmap from the VLAN tables, using the VLAN ID assigned to the packet, for unknown unicast, unknown multicast, and broadcast packets.
   a. For unknown unicast packets, the port bitmap is ANDed with the UNKNOWN_UCAST_BLOCK_MASK bitmask.

b. For unknown multicast packets, the port bitmap is ANDed with the UNKNOWN_MCAST_BLOCK_MASK bitmask.
c. For broadcast packets, the port bitmap is ANDed with the BCAST_BLOCK_MASK bitmask.

ContentAware Processing

ContentAware processing is described in the following sections.

Ingress Filter Processor

The Ingress Filter Processor (IFP) is for packets ingressing on the GbE and 10GbE ports. Ingress lookups occur on L2 and L3 pre-routed packets. The IFP is the most flexible and powerful of the three ContentAware Filter Processors. Filtering can be done by parsing the first 128 bytes of the packet using either predefined protocol fields such as VLAN, L2, and L3 addresses or using User Defined fields. Assigning a new priority, route, drop, or redirecting the packet are some of the actions that can be performed.

Ethernet Operation, Administration and Maintenance

The BCM5340X supports the Ethernet Operation, Administration, and Maintenance (OAM) management capabilities within the Ethernet layer. The OAM support is divided into the following two areas:

- Link-Level OAM, IEEE 802.3ah, Clause 57
  - Link Monitoring: A mechanism to detect failed or degraded link status as well as the ability to poll any part of a peer's Management Information Base (MIB).
  - Fault Signaling: A mechanism to advertise detected path failures to peers.
  - Remote Loopback: A mechanism to support data link layer frame loopback for fault localization purposes.
- Service-Level OAM, IEEE 802.1ag and ITU Y.1731
  - Path discovery: A mechanism to determine the path taken by a destination MAC address, MIP by MIP, from one MEP to another MEP across an MA. Path discovery is performed with LinkTrace Messages (LTM) and LinkTrace Replies (LTR).
  - Fault Detection: A mechanism to detect connectivity failures as well as unintended connectivity between services. Fault detection is performed with Continuity Check Messages (CCM).
  - Fault Verification: A mechanism to diagnose and isolate faults within an MA. Fault verification and isolation are performed with LoopBack Messages (LBM) and LoopBack Replies (LBR).
  - Fault Notification: A mechanism utilized by a MEP to notify peer MEPs and MIPs of a CFM failure. Fault notification is performed with standard CFM messages.
  - Delay Measurement: A mechanism for measuring network delay and jitter characteristics to guarantee SLA.
  - Loss Measurement: A mechanism for measuring network loss characteristic to guarantee SLA.

Network Management Support

The BCM5340X provides a set of counters to support the following Management Information Base (MIB) specifications:

- RMON statistics group (IETF RFC 2819)
- SNMP interface group (IETF RFC 1213 and 2863)
- Ethernet-like MIB (IETF RFC 1643)
- Ethernet MIB (IEEE 802.3u)
- Bridge MIB (IETF RFC 1493)

CPU/Management Interface

In low-cost Layer 2 switching systems, the BSC interface can be used for the setup, configuration, maintenance, and management of the BCM5340X-based switch system. In high-end systems, with CPUs running the sophisticated routing protocol stacks required to support multilayer switching functions, the PCIe Interface is necessary to fulfill the bandwidth and performance demands of real-time packet switching. It is also used to move data to and from the CPU or a PCIe uplink.

External CPU with PCIe Bus

The BCM5340X device has PCIe Interface that is conformed to the PCIe Version 2.0 specifications. The BCM5340X supports single lane of PCIe. No external glue logic is required to support this interface. The protocols and electrical requirements of the PCIe specifications are strictly implemented.

Energy Efficient Ethernet

The BCM5340X device supports Energy Efficient Ethernet (EEE) to reduce power consumption by enabling the external PHYs to enter a Low Power Idle (LPI) state, during extended idle periods that may exist between packets. The power savings aspects of EEE are largely implemented in the PHYs, however, the PHYs are reliant upon the MACs to inform them of when to enter and leave the LPI state. The MACs make these determinations by examining the state of the transmit queues associated with each MAC. The EEE signaling between a MAC and its PHY is conveyed by the SGMII signals between them. The EEE feature is only supported on 1GbE ports, not supported on uplink/stacking ports.

When the transmit MAC asserts its LPI signal to the PHY, the PHY transmits a sleep symbols on the wire for a short period. This informs the link partner's receive PHY that it is entering the LPI state. After the sleep symbols have been transmitted, a quiet period is entered where there is no signaling. At the beginning of the first quiet period, the receive PHY indicates to its MAC that it has entered the LPI mode. The transmit PHY interrupts the quiet period periodically to send refresh symbols that are used to keep PLLs, filters, and other functions in sync, so that the LPI state can be exited quickly. When the transmit MAC deasserts, the PHY wakes up and transmits wake symbols for a short period to the link partner's PHY, informing it that it is time to wake up. The time between the transmit MAC deasserting and its resumption of packet transmission may be adjusted upward from the minimum PHY wake up time to allow for other system components to wake up and be ready for packet reception. Therefore, an idle period may precede the appearance of the first packet after a LPI sequence.

In general, EEE operates in an asymmetric mode. Meaning, the transmit direction and receive direction may enter and exit the LPI state independently. For 1000BASE-T, however, symmetric operation is required in order to truly benefit from EEE. In symmetric mode, both the transmit and receive paths must be indicating with sleep symbols before either side will enter the quiet state. Therefore, the transmit half of a PHY will send sleep signals until either sleep symbols are received from the link partner or the PHY has been commanded to exit the LPI state by the MAC.

Section 4: Ethernet Switch Controller System Interfaces

Overview

The BCM5340X includes the following physical layer interfaces:

- MIIM (IEEE 802.3u): Communication with physical layer devices.
- JTAG: For IEEE Std. 1149.6 boundary scan.
- BSC: For low-speed configuration (as a slave) and low-speed communications (as a CPU-controlled master/slave).
- LED: For system LED support.
- XFI: Allows connection to external 10G PHY or other XFI port through backplane for 10GbE support.
- SFI: Allows connection to SFP+ connector for 10GbE support.
- XAUI: Allows connection to external 10G PHY or other XAUI port for 10GbE support.

Table 5: System Interfaces

Interface	*Description*
10GbE port	• Up to sixteen 10G ports – Integrated SerDes, IEEE 802.3ae-compliant XAUI/XFI/SFI interface – Support for HiGig+™/HiGig2 header formats – For different part numbers, ports are individually set for either one XAUI, two RXAUI, four XFI/SFI, four 1G/2.5G, or 2 x HiGig-Duo™[13] . • Support for jumbo frames up to 9600B
GbE port	• Full-duplex mode of operation, compliant to IEEE 802.3 • Support for 10/100/1000 Mbps using auto-negotiation • Support for jumbo frames up to 9600B
PCIe	• Supports single lane (x1) at 2.5G or 5G • PCIe v2.0-compliant • Supports root complex and end point mode.
QSPI	• Supports Quad-SPI Flash controller.
UART	• Supports two UART • One dedicate full-set UART • One simple UART

Table 5: System Interfaces (Cont.)

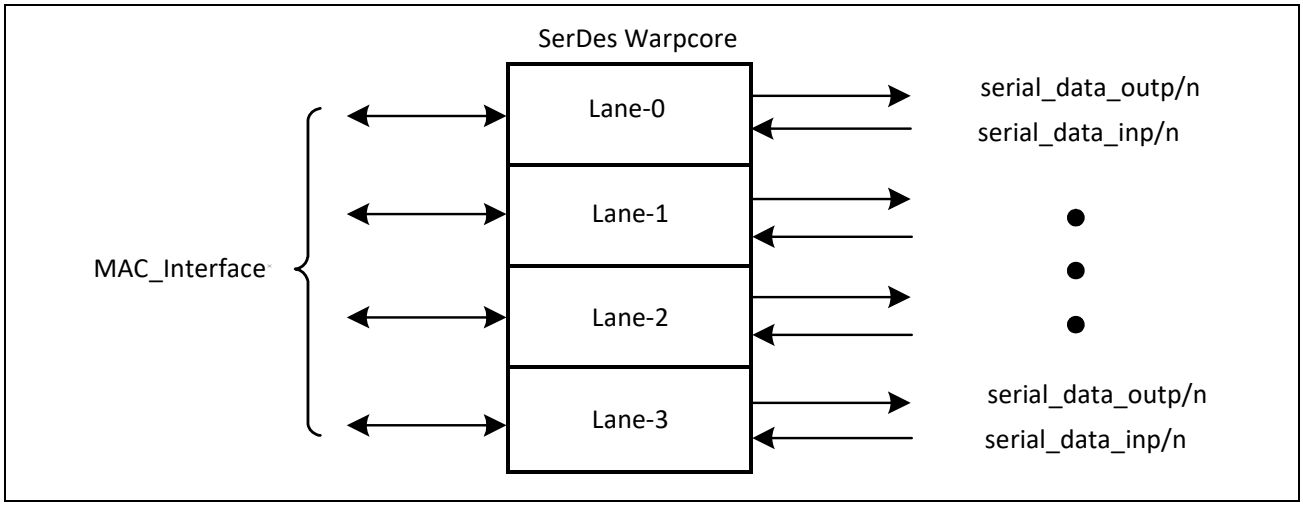
Interface	*Description*
Serial LED	• Control of up to 255 system LEDs at a 30 Hz refresh rate • Simple microcontroller with instructions optimized for LED control • Low-cost two-wire interface to system LEDs • 256 bytes of program RAM • 256 bytes of data RAM • Direct access to per port speed, duplex state, flow control state, link state, transmit and receive activity, and collision activity.
MIIM (MDC/MDIO)	• IEEE 802.3u-compliant MIIM interface for communication with external PHY devices • 2.5 MHz operation • IEEE 802.3 Clause 22-compliant • IEEE 802.3 Clause 45-compliant
BSC	• BSC-compliant interface–The Broadcom serial control (BSC) bus is Philips I^2C-compatible. • Supports slave mode, allowing an external microcontroller to configure the BCM5340X device • CPU-controlled master mode to communicate with other BSC devices
Synchronous Ethernet	• Output of a primary and secondary recovered line clock • Input recovered clock from an external device such as the EPON/GPON MAC or GbE PHY.
JTAG	• JTAG-compliant interface used to support boundary scan operations • 20 MHz operation

TDM-based SerDes Controller

The TDM-based SerDes Controller (TSC) is the versatile physical layer interface for the BCM5340X. The device serial interface supports the following features:

- Quad SerDes block supporting four serial links.
- Support for line rates of 1.25 Gbps, 3.125 Gbps, 5.0 Gbps, 6.25 Gbps, 6.5625 Gbps, and 10.3125 Gbps per serial link.
- 5-tap DFE with adaptive control and VGA with AGC.
- Programmable RX equalizer with 0–8 dB boost, approximately 0.5 dB/step.
- Transmitter with 32-level post-cursor and 16 level precursor preemphasis. Figure 4 shows a conceptual block diagram.

Figure 4: Conceptual Block Diagram



BCM5340X device family incorporates a macro called TDM SerDes controller. This macro allows the device to support low latency throughput and oversubscription capability. The TSC macro consists of the digital control logic and a Warpcore analog block. Throughout the document, TSC and Warpcore may be used interchangeably. A Warpcore is used at the physical interface, whereas a TSC is used at the application level.

HiGig+ and HiGig2 are supported across 1, 2, or 4 single lanes. In 1-lane mode, it supports HG[10] and HG[11] or HG-Lite over 1G/2.5G. In 2-lane mode, it supports HGD[13]. In 4-lane mode, it support HG[10].

Note: When using HiGig™ or HiGig2 in the four–lane mode, the minimum IPG can be as low as 8 bytes.

Table 6 shows the TSC configurations.

Table 6: TSC Configurations

Lane Speed (Gbaud)	*Number of Ports Supported*	*Encoding*	*Protocol: Interface*	*Ethernet Traffic (HiGig+)*	*Ethernet Traffic (HiGig2)*
1.25G	4	8b/10b	1GbE: 1000BASE-X, SGMII	N/A	N/A
3.125G	4	8b/10b	2.5GbE: 2500BASE-X	N/A	N/A
	1	8b/10b	10GbE: CX4, KR4, XAUI, HG[10]	N/A	N/A
5.16125G	4	64b/66b	5GbE: 5000BASE-X	N/A	N/A
6.5625G	2	64b/66b	HGD[13]: 2 x SerDes	12.73G	12.15G
10.3125G	4	64b/66b	10GbE: XFI, KR, SFI	10G	9.5454G
	4	64b/66b	HG[10]: 1 x SerDes	10G	9.5454G
10.9375G	4	64b/66b	HG[11]: 1 x SerDes	10.6G	10.12G
5G	4	8b/10b	QSGMII: 4 x SGMII	N/A	N/A

- TSC can support any combination of Ethernet or HiGig/HiGig2 ports running at Ethernet rate. HG[10] with HiGig2 will result in lower than 10Gbps performance because the packet length is increased by 4 bytes.
- This table defines the capabilities of the TSC. However, the specific configuration(s) which are enabled are defined inTable 1 on page 16.One or more lanes of TSC form a port as indicated in the table above. A port can be statically configured to be either Ethernet or HiGig, but cannot support both formats simultaneously.
- A TSC can support any combination of Ethernet or HiGig/HiGig2 ports running at Ethernet rate.
- Any combination of Ethernet 1G and 10G ports can co-exist in the same TSC. Also, any combination of 1G and 2.5G TSC can co-exist in the same TSC.
- A HG[10] port can be statically configured to support Broadcom's HiGig+ or HiGig2 format. A HG[10] port with HiGig2 will result in lower than 10Gbps performance because the packet length is increased by 4 bytes.
- A HG[10] port can co-exist with other Ethernet or HG[10] ports in the same TSC. For example, if one lane of a TSC is statically configured to be HG[10], the other lanes can support any combination of HG[10], 1G, or 10G Ethernet.
- A HG[11] port cannot co-exist with any other type of port in the same TSC. For example, if a TSC lane is configured to be a HG[11] port, each of the other TSC lanes can only support HG[11].

HIGIG+/HIGIG2 Interface

The HiGig+/HiGig2 interface complies with the standard XAUI interface for 10GbE, but a proprietary Broadcom HiGig+/HiGig2 module header is added to each packet for interchip communication.

The HiGig+/HiGig2 protocol allows for many features across the stack link, including:

- VLAN transparency
- Port and traffic mirroring
- Trunking
- Trunk failover
- Daisy chaining of BCM5340X1 devices for multistage fabrics

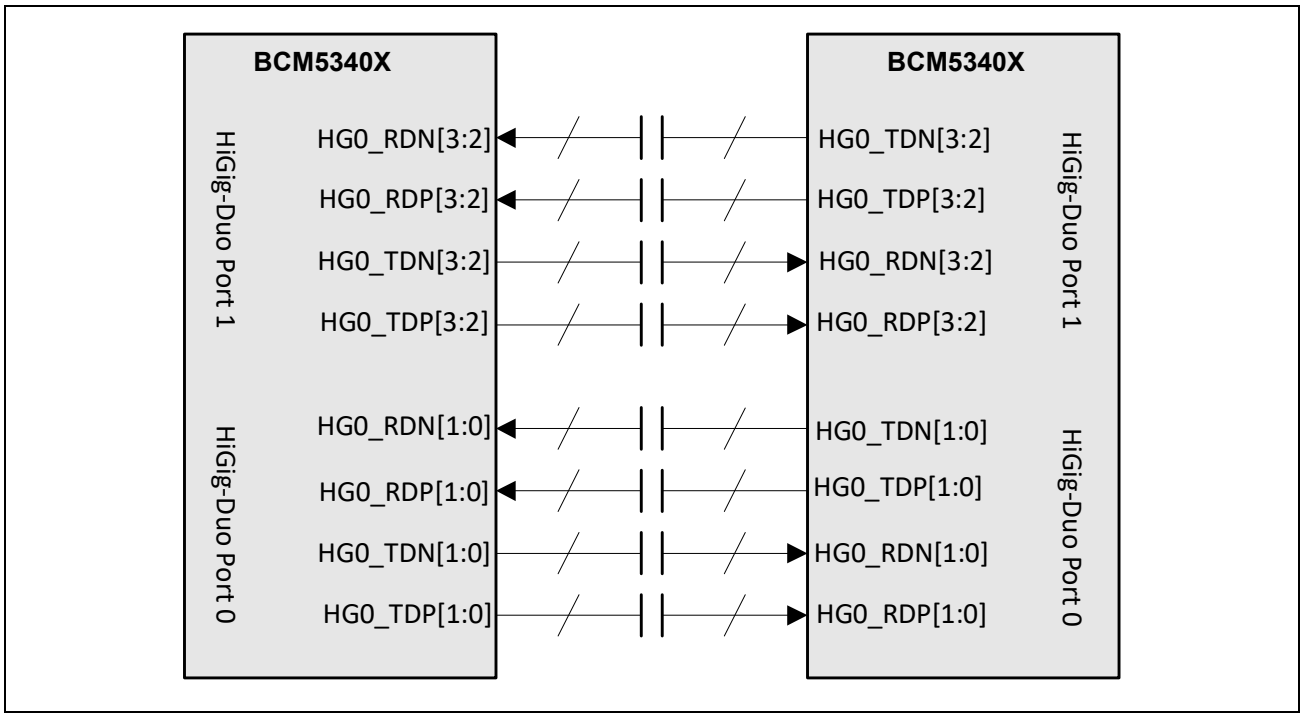
HiGig-Duo[13] Interface

The HiGig-Duo[13] mode can be configured by software. The HiGig-Duo interface uses two separate differential lanes to transmit and receive data. The receive clock is recovered from the data stream. Each lane or channel is programmed to operate at 12.73 Gbps data rate (Table 7 on page 39). These interfaces are used for connecting multiple BCM5340X devices. The connection of the HiGig-Duo[13] ports is shown in Figure 5 on page 39.

Table 7: Data Rates of HiGig-Duo Ports

Port Configuration	*SerDes Frequency*	*Port Baud Rate*	*Port Data Rate*
HiGig-Duo[13]	6.5625G	13.125G	12.73G

Figure 5: 2 x HiGig-Duo Interface Connection



1G/2.5G Interface

1G/2.5G ports use a single lane to transmit and receive data. When set to 1GbE speed, the port supports SGMII (10/100/1000M) or 1000BASE-X (fiber) mode. When set to 2.5 or 5GbE speed, the port can support 2.5 or 5GbE or overclocked-Ethernet mode.

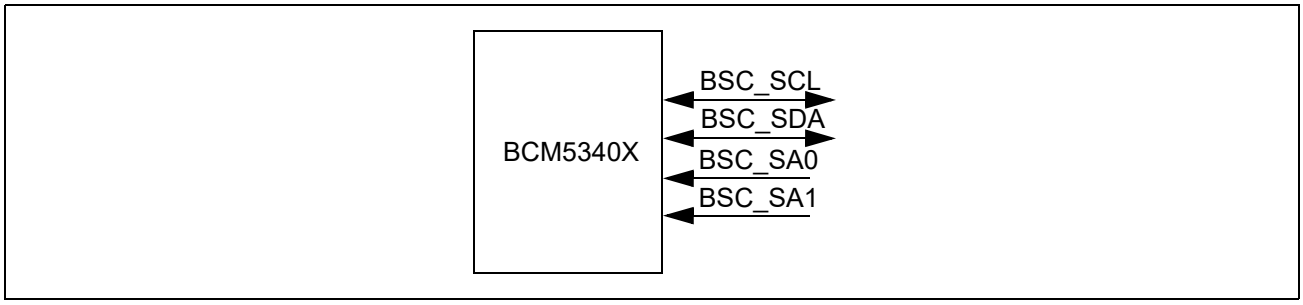
MII Management

The CPU Management Interface Controller (CMIC) supports an IEEE 802.3u standard MII Management (MIIM) interface. This is a two-wire serial bus controlled by the CMIC. It allows register access to all system PHYs. PHY data can be read/written–to using this interface. The two signals for MIIM are MDC (clock) and MDIO (bidirectional data). The CPU programs the PHY registers using this interface. After the initialization sequence, the CPU could read the link up/down register bit to detect any link changes. Alternatively, the CPU can enable the MIIM_AUTO_LINK_SCAN_EN bit. In this mode, CMIC will scans the PHYs and detect link status for each port. The link status register is updated at the end of each scan. If a link status change is detected, CMIC sends a notification to the CPU.

Broadcom Serial Interface (BSC)

The BCM5340X switch provides two BSC interfaces to communicate with other devices that support a similar interface. The signals supported are shown in Figure 6.

Figure 6: BSC Interface



The BSC1 interface can be configured to operate in either master or slave mode. The IP_BSC0 interface can only support master mode. The supported BSC data protocol format is big endian, which is consistent with the BSC protocol supported by other vendors.

Upon reset, the BCM5340X switch enters the default slave mode. In this mode, an external BSC master device can communicate with the BCM5340X switch and initialize the device using the BSC_SDA and BSC_SCL lines. The external master can write the 16-bit address of the register to be accessed, followed by the 32-bit data to be written. When all 32 bits (4 bytes) of data are provided, a write to the internal register is performed.

Note: There is no mechanism to support any interrupt structure or bus mastering in the BSC slave-only mode.

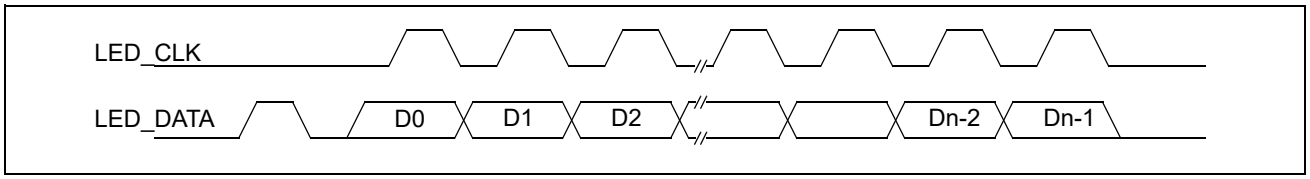
A default BSC slave address of 0b1000100 is used for the slave-only mode. Additionally, the BSC_SA0 and BSC_SA1 inputs can be strapped high or low, to change the default slave address, giving a range of 0b1000100 to 0b1000111. Both 7-bit and 10-bit addressing schemes are supported.

Optionally, CPU-controlled master/slave mode is supported. This mode is disabled by default and is useful to connect other BSC devices, such as a time-of-day chip, temperature sensors, parallel ports, and so forth, to the BCM5340X switch. In master mode, read and write BSC operations are initiated under program control of the host CPU. A block of registers accessible by the CPU controls this function.

LED Interfaces

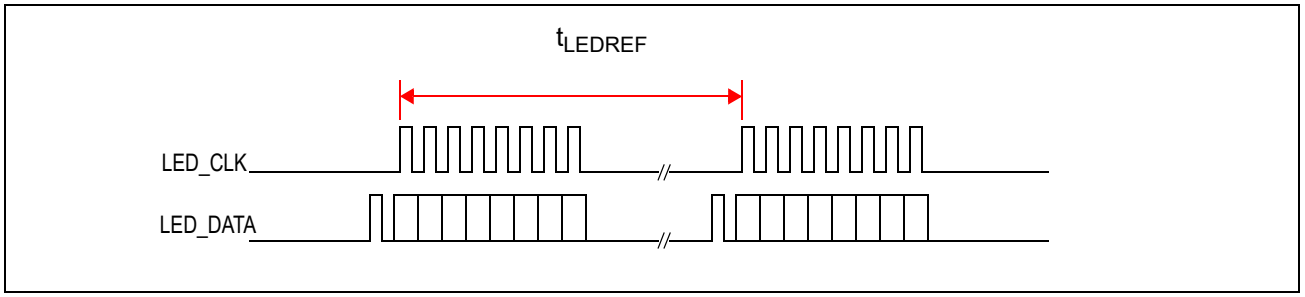
A two-wire (clock and data) LED interface is provided to control system LEDs. Both LED_CLK and LED_DATA are outputs. When active, LED_CLK is a 5 MHz clock. Both signals are held low during periods of inactivity. A single LED refresh cycle consists of clocking out a programmable number of LED_DATA bits. The LED_DATA signal is pulsed high at the start of each LED refresh cycle (see Figure 7). The LED refresh cycle is repeated every 30 ms to refresh the LEDs. Alternatively, the LED interfaces can be controlled by software on an embedded ARM R5 overriding the LED hardware refresh cycles. The ARM software can read device registers (e. g., MIB counters) and update the LEDs at any rate.

Figure 7: Single LED Refresh Cycle



The LED refresh cycle is repeated periodically (every 30 ms) to refresh the LEDs (see Figure 8).

Figure 8: LED Refresh Cycle



Section 5: Signal Description and Pin Lists

This section describes the device hardware signals. Table 8 lists conventions that are used, followed by signal name description tables.

Table 8: Signal I/O Descriptions

I/O	*Descriptions*
B	Bidirectional signal
B_{OD}	Open-drain bidirectional signal
B_{PD}	Bidirectional signal with internal pull-down
B_{PU}	Bidirectional signal with internal pull-up
GND	Ground plane
I	Input signal
I_{PD}	Input with internal pull-down
I_{PU}	Input with internal pull-up
NC	No connect
O	Output signal
O_{OD}	Open-drain output
P	Power plane
REF	Reference voltage input
TST	Test pin

Table 9: Pin Description—Grouped by Function

Signal Name	*I/O*	*Rate*	*Type*	*Description*
Chip Misc Signals				
SYS_RST_L	I_{PU}	–	CMOS, 3.3V	Chip system reset (active low).
POR_OUT_L	O	–	CMOS, 3.3V	Power-On-Reset Output (active low)
RESCAL_REXT	I	–	CMOS, 3.3V	External Resistor. Connect to 4.53 kΩ 1% resistor to RESCAL_AVSS.
IP_BOOT_DEV[2:0]	I_{PD}	–	CMOS, 3.3V	Select the device that is used to boot the system IP_BOOT_DEV[2:0]: • 3'b000 = SPI flash on IP_QSPI interface. • others = reserved. ***Note:*** For external CPU support, use the default setting.
IP_QSPI_4BYTE_ADDR	I_{PD}	–	CMOS, 3.3V	Select the address mode of QSPI flash. • 1'b0 = 3 byte address mode. • 1'b1 = 4 byte address mode.

Table 9: Pin Description—Grouped by Function (Cont.)

Signal Name	I/O	Rate	Type	Description
IP_PCIE_RC_MODE	I_{PD}	–	CMOS, 3.3V	Configures the PCI Express interface(s) to operate as a Root Complex or End Point: • 1'b0 = The PCI Express interface is operating as an End Point. • 1'b1 = The PCI Express interface is operating as a Root Complex.
OSC_XTAL_SEL	I_{PD}	–	CMOS, 3.3V	Select External Oscillator or Crystal for system clock source. • 1'b0 = Use External Crystal • 1'b1 = Use External Oscillator
LC_PLL1_REFCLK_SEL	I_{PD}	–	CMOS, 3.3V	Select clock source for LC_PLL1_REFCLK: • 1'b0 = Use external 156.25 MHz differential clock source. • 1'b1 = Use internal clock source. Shared with L1_RCVRD_CLK_BKUP_VALID.
XG_MIIM0_VOLT_SEL	I_{PD}	–	CMOS, 3.3V	Select voltage level of power source XG_MIIM0_VDDO for XG_MIIM0 interface. • 1'b0 = Select 1.2V. • 1'b1 = Select 2.5V/3.3V.
AVS0	O	–	CMOS, 3.3V	Adjustable Voltage Scale indicator to decide voltage for VDDC, TSC[4:0]_VDD, and TSCQ0_VDD. • High = AVS capable chip for 0.9V VDDC. • Low = Non-AVS capable chip for 1.0V VDDC.
TSCQ0_PWR_OFF	I_{PD}	–	CMOS, 3.3V	Indicate TSCQ0 is power off 0: Power On 1: Power Off
TSC4_PWR_OFF	I_{PD}	–	CMOS, 3.3V	Indicate TSC4 is power off 0: Power On 1: Power Off
TSC3_PWR_OFF	I_{PD}	–	CMOS, 3.3V	Indicate TSC3 is power off 0: Power On 1: Power Off
TSC2_PWR_OFF	I_{PD}	–	CMOS, 3.3V	Indicate TSC2 is power off 0: Power On 1: Power Off
TSC1_PWR_OFF	I_{PD}	–	CMOS, 3.3V	Indicate TSC1 is power off 0: Power On 1: Power Off

Table 9: Pin Description—Grouped by Function (Cont.)

Signal Name	I/O	Rate	Type	Description
TSC0_PWR_OFF	I_{PD}	–	CMOS, 3.3V	Indicate TSC0 is power off 0: Power On 1: Power Off Shared with XG_MDC0 pin ***Note:*** Must be pulled up to the same power rail as XG_MIIM0_VDDO when set to 1.
XTAL_FREQ_SEL	I_{PD}	–	CMOS, 3.3V	Crystal clock frequency Selection 1: 50 MHz 0: 25 MHz
IP_PCIE_REFCLK_SEL	I_{PD}	–	CMOS, 3.3V	Configures the device to use an internally generated clock for the PCI Express reference clock, or an external clock provided on the PCIE_REFCLKP/N inputs: • 1'b0 = Reference clock is provided by an internally generated clock. (default) • 1'b1 = Reference clock is provided by an external clock source connected to the PCIE_REFCLKP/N inputs.
IP_PCIE_FORCE_GEN1	I_{PD}	–	CMOS, 3.3V	Force PCIe GEN 1 Compliant: • 1'b0: GEN 2 mode (Default). • 1'b1: Force GEN 1 compliant.
Quad Serial Peripheral Interface (QSPI) Interface				
IP_QSPI_CS_L	O	–	CMOS, 3.3V	iProc QSPI slave select (active low).
IP_QSPI_SCK	O	15.625 MHz/ 25 MHz/ 32.5 MHz/ 50 MHz/ 62.5 MHz	CMOS, 3.3V	iProc QSPI clock.
IP_QSPI_MISO	B_{PD}	15.625 MHz/ 25 MHz/ 32.5 MHz/ 50 MHz/ 62.5 MHz	CMOS, 3.3V	iProc QSPI master in slave out.
IP_QSPI_MOSI	B	15.625 MHz/ 25 MHz/ 32.5 MHz/ 50 MHz/ 62.5 MHz	CMOS, 3.3V	iProc QSPI master out slave in.
IP_QSPI_HOLD_L	B	–	CMOS, 3.3V	iProc QSPI HOLD signal (active low).
IP_QSPI_WP_L	B	–	CMOS, 3.3V	iProc QSPI write protect (active low).
PCIe Interface				
PCIE_RDP PCIE_RDN	I	2.5/5.0 Gbps	CML, 1.0V	PCI Express receive serial data. 2.5 Gbps/ 5.0 Gbps differential interface.
PCIE_TDP PCIE_TDN	O	2.5/5.0 Gbps	CML, 1.0V	PCI Express transmit serial data. 2.5 Gbps/ 5.0 Gbps differential interface.

Table 9: Pin Description—Grouped by Function (Cont.)

Signal Name	I/O	Rate	Type	Description
PCIE_REFCLKP PCIE_REFCLKN	I	100 MHz	HCSL, 1.0V	PCI Express Internal PLL differential reference clock. Inputs require external AC-coupling capacitors and an optional 100Ω differential termination on the board, depending on the amplitude of the incident clock voltage. The PCIe reference clock also requires series termination resistors to dampen the edge rate of the clock driver by creating a voltage divider.
PCIE_INTR_L	B_{PU}	–	CMOS, 3.3V	PCI Express Interrupt (active low).
PCIE_PERST_L	B_{PU}	–	CMOS, 3.3V	PCI Express fundamental reset signal (active low).
PCIE_WAKE_L	B_{OD}	–	CMOS, 3.3V	PCI Express wake signal (active low). External 4.7kΩ pull-up resistor to 3.3V is needed.
Broadcom Serial Controller (BSC) Interface				
IP_BSC0_SCL	B_{OD}	100 kHz/ 400 kHz	CMOS, 3.3V	iProc BSC interface clock (100 kHz/ 400 kHz). This signal requires an external pull-up resistor to 3.3V, even if the interface is unused.
IP_BSC0_SDA	B_{OD}	100 kHz/ 400 kHz	CMOS, 3.3V	iProc BSC interface data. This signal requires an external pull-up resistor to 3.3V, even if the interface is unused.
UART Interface				
IP_UART0_TX	O	384 kHz	CMOS, 3.3V	iProc UART port 0 Serial Data Transmit. This pin should be made accessible for iProc processor debugging.
IP_UART0_RX	I	384 kHz	CMOS, 3.3V	iProc UART port 0 Serial Data Receive. This pin should be made accessible for iProc processor debugging.
IP_UART0_CTS_L	I	–	CMOS, 3.3V	iProc UART port 0 Clear to Send status input (active low). When low indicates that the MODEM or data set is ready to exchange data. This pin should be made accessible for iProc processor debugging.
IP_UART0_RTS_L	O	–	CMOS, 3.3V	iProc UART port 0 Request to Send status output (active low). This pin should be made accessible for iProc processor debugging.
IP_UART0_DTR_L	O	–	CMOS, 3.3V	iProc UART port 0 Data Terminal Ready output (active low). This pin should be made accessible for iProc processor debugging.
IP_UART0_DCD_L	I	–	CMOS, 3.3V	iProc UART port 0 Data Carrier Detect input (active low). This pin should be made accessible for iProc processor debugging.
IP_UART0_DSR_L	I	–	CMOS, 3.3V	iProc UART port 0 Data Set Ready input (active low). This pin should be made accessible for iProc processor debugging.

Table 9: Pin Description—Grouped by Function (Cont.)

Signal Name	I/O	Rate	Type	Description
IP_UART0_RI_L	I	–	CMOS, 3.3V	iProc UART port 0 Ring Indicator input (active low). This pin should be made accessible for iProc processor debugging.
General Purpose I/O				
IP_GPIO[3:0]	B_{PU}	–	CMOS, 3.3V	iProc General Purpose Input/Outputs.
TSC Technology Quad SerDes Interface				
TSC[4:0]_TD[3:0]P	O	1.25 Gbps – 10.9375 Gbps	CML, 1.0V	TSC technology transmit serial data: positive leg of the differential pair.
TSC[4:0]_TD[3:0]N	O	1.25 Gbps – 10.9375 Gbps	CML, 1.0V	TSC technology transmit serial data: negative leg of the differential pair.
TSC[4:0]_RD[3:0]P	I	1.25 Gbps – 10.9375 Gbps	CML, 1.0V	TSC technology receive serial data: positive leg of the differential pair.
TSC[4:0]_RD[3:0]N	I	1.25 Gbps – 10.9375 Gbps	CML, 1.0V	TSC technology receive serial data: positive leg of the differential pair.
TSCQ0_TD[3:0]P	O	1.25 Gbps – 10.9375 Gbps	CML, 1.0V	TSC technology transmit serial data: positive leg of the differential pair.
TSCQ0_TD[3:0]N	O	1.25 Gbps – 10.9375 Gbps	CML, 1.0V	TSC technology transmit serial data: negative leg of the differential pair.
TSCQ0_RD[3:0]P	I	1.25 Gbps – 10.9375 Gbps	CML, 1.0V	TSC technology receive serial data: positive leg of the differential pair.
TSCQ0_RD[3:0]N	I	1.25 Gbps – 10.9375 Gbps	CML, 1.0V	TSC technology receive serial data: positive leg of the differential pair.
MII Management Interface (MIIM)				
XG_MDC0	B_{PD}	12.5 MHz	1.2V/2.5V/ 3.3V	Serial management clock Clause 22/Clause 45, used to communicate to external 1GbE/ 10GbE PHY device under software control. XG_MIIM0 interface voltage set by XG_MIIM0_VOLT_SEL.
XG_MDIO0	B_{PU}	12.5 MHz	1.2V/2.5V/ 3.3V	Serial management data Clause 22/Clause 45, used to communicate to external 1GbE/ 10GbE PHY device under software control. XG_MIIM0 interface voltage set by XG_MIIM0_VOLT_SEL. External pull-up resistor recommended.
System Reference Clocks				
XTALP XTALN	I	25 MHz/50 MHz	CML, 1.0V	25 MHz/50 MHz Chip clock source, either differential clock source or single-end clock source, depends on the OSC_XTAL_SEL strap pin. It requires external 100Ω termination when differential clock source is used.

Table 9: Pin Description—Grouped by Function (Cont.)

Signal Name	I/O	Rate	Type	Description
LC_PLL1_REFCLKP LC_PLL1_REFCLKN	I	156.25 MHz	CML, 1.0V	Differential 156.25 MHz reference clock for Warpcore Technology SerDes interface. Inputs require external AC-coupling capacitors but have internal DC biasing, and therefore do not require external biasing resistors. Inputs have internal 100Ω termination. This clock can be terminated according to HDG if function is unused.
BS[1:0]_PLL_REFCLKP BS[1:0]_PLL_REFCLKN	I	25 MHz/ 50 MHz	CML, 1.0V	Differential CML input reference clock for the BroadSync (BS) PLLs. Required for driving the BroadSync interface. Inputs require external AC-coupling capacitors, but have internal DC biasing, and therefore, do not require external biasing resistors. Inputs have internal 100Ω termination. This clock can be terminated according to HDG if function is unused.
TS_PLL_REFCLKP TS_PLL_REFCLKN	I	50 MHz	CML, 1.0V	Differential CML reference clock for the Time Sync (TS) PLL. Used for driving the time stamping functions such as 1588. Inputs require external AC-coupling capacitors and external biasing resistors. This clock can be terminated according to HDG if function is unused.
Broadcom Serial Controller (BSC) Interface				
BSC1_SCL	B_{OD}	100 kHz/ 400 kHz	CMOS, 3.3V	BSC interface clock (100 kHz/400 kHz). This signal requires an external pull-up resistor to 3.3V, even if the interface is unused.
BSC1_SDA	B_{OD}	100 kHz/ 400 kHz	CMOS, 3.3V	BSC interface data. This signal requires an external pull-up resistor to 3.3V, even if the interface is unused.
BSC1_SA[1:0]	I_{PD}	–	CMOS, 3.3V	BSC interface address. Configures lower two address bits when operating in BSC slave mode.
Serial Port Interface (SPI)				
SPI_MISO	B	–	CMOS, 3.3V	Master Input data, Slave Output data.
SPI_MOSI	B_{PD}	–	CMOS, 3.3V	Master Output data, Slave Input data.
SPI_SS_L	B_{PU}	–	CMOS, 3.3V	Slave Select (active low).
SPI_SCK	B_{PU}	–	CMOS, 3.3V	Serial Clock. Speed of SPI varies for application.
Time Synchronous Ethernet Interface				
L1_RCVRD_CLK	O	156.25 MHz/ 44.643 MHz/ 28.409 MHz/ 73.661 MHz/ 46.875 MHz	CMOS, 3.3V	Primary recovered clock. Recovered clock is not supported for 10M and 100M speeds. This clock is sent out to support L1 synchronization.

Table 9: Pin Description—Grouped by Function (Cont.)

Signal Name	I/O	Rate	Type	Description
L1_RCVRD_CLK_VALID	O	–	CMOS, 3.3V	Indicates the primary recovered clock is valid Link status needed for the recovered clock. When this signal is set to 1, L1_RCVRD_CLK is generated based on the recovered clock. This pin can be configured to output the inverse of L1_RCVRD_CLK signal.
L1_RCVRD_CLK_BKUP	O	156.25 MHz/ 44.643 MHz/ 28.409 MHz/ 73.661 MHz/ 46.875 MHz	CMOS, 3.3V	Secondary recovered clock. Recovered clock is not supported for 10M and 100M speeds. This clock is sent out to support L1 synchronization.
L1_RCVRD_CLK_ BKUP_VALID	O	–	CMOS, 3.3V	Indicates the secondary recovered clock is valid Link status needed for the recovered clock. When this signal is set to 1, L1_RCVRD_CLK_BKUP is generated based on the recovered clock. This pin can be configured to output the inverse of L1_RCVRD_CLK signal.
EXT_RCVRD_CLK0	I_{PD}	–	CMOS, 3.3V	External Recovered Clock Source 0.
EXT_RCVRD_CLK0_VLD	I_{PD}	–	CMOS, 3.3V	Indicates the external recovered clock 0 is valid.
EXT_RCVRD_CLK1	I_{PD}	–	CMOS, 3.3V	External Recovered Clock Source 1.
EXT_RCVRD_CLK1_VLD	I_{PD}	–	CMOS, 3.3V	Indicates the external recovered clock 1 is valid.
TS_GPIO[1:0]	B_{PU}	–	CMOS, 3.3V	Synchronous signals for additional timestamping capability. These signals can be configured through the CMIC register as an output or an input.
JTAG Interface				
JTCE0 JTCE1	I_{PD}	–	CMOS, 3.3V	JTAG test enable. [JTCE1, JTCE0]. • 2'b00 = Normal Mode. • 2'b01 = ARM Debug Mode. • 2'b10 = reserved. • 2'b11 = JTAG Mode. Must be pulled low during normal switch operation.
JTCK	I_{PD}	12.5 MHz	CMOS, 3.3V	JTAG test clock.
JTDO	O	12.5 MHz	CMOS, 3.3V, 8 mA	JTAG test data output.
JTDI	I_{PU}	12.5 MHz	CMOS, 3.3V	JTAG test data input.
JTMS	I_{PU}	12.5 MHz	CMOS, 3.3V	JTAG mode select.
JTRST	I_{PU}	12.5 MHz	CMOS, 3.3V	JTAG reset. Must be pulled low during normal switch operation.
Serial LED Interface				

Table 9: Pin Description—Grouped by Function (Cont.)

Signal Name	I/O	Rate	Type	Description
LED_CLK	O	5 MHz	CMOS, 3.3V	LED Clock outputs from the integrated LED processors. It is used to latch in the LED_DATA.
LED_DATA	O	5 MHz	CMOS, 3.3V	LED Data outputs from the integrated LED processors. It is used to display port status.
SerDes Loss of Signals				
LOS[5:0]	I_{PD}	–	CMOS, 3.3V	Loss of signal inputs.
Power				
VDDC	I	P	1.0V	1.0V digital core power. Could be 0.9V or 1V decided by AVS0 pin.
VDDO1P8	I	P	1.8V	1.8V digital I/O power.
VDDO3P3	I	P	3.3V	3.3V digital I/O power.
XG_MIIM0_VDDO	I	P	1.2V/2.5V/ 3.3V	Digital power for XG_MIIM0 interface. This power must connect to: • 1.2V when XG_MIIM0_VOLT_SEL pin set to 0. • 2.5V/3.3V, when XG_MIIM0_VOLT_SEL pin set to 1.
XG_MIIM0_VDDP	I	P	1.2V/1.8V	Digital power for XG_MII0 interface. This power must be connect to: • 1.2V when XG_MIIM0_VDDO is 1.2V. • 1.8V when XG_MIIM0_VDDO is 2.5V/ 3.3V.
TSC[4:0]_VDD	I	P	1.0V	1.0V digital power for TSC[4:0] core. Could be 0.9V or 1.0V decided by AVS0 pin.
TSC[4:0]_PVDD	I	P	1.0V	1.0V analog power for TSC[4:0] PLL.
TSC[4:0]_TVDD	I	P	1.0V	1.0V analog power for TSC[4:0] transmit.
TSC[4:0]_RVDD	I	P	1.0V	1.0V analog power for TSC[4:0] receive.
TSCQ0_VDD	I	P	1.0V	1.0V digital power for TSC Q0 core. Could be 0.9V or 1.0V decided by AVS0 pin.
TSCQ0_PVDD	I	P	1.0V	1.0V analog power for TSC Q0 PLL.
TSCQ0_TVDD	I	P	1.0V	1.0V analog power for TSC Q0 transmit.
TSCQ0_RVDD	I	P	1.0V	1.0V analog power for TSC Q0 receive.
PCIE_PVDD1P0	I	P	1.0V	1.0V analog power for PCI Express PLL.
PCIE_TVDD1P0	I	P	1.0V	1.0V analog power for PCI Express transmit.
PCIE_RVDD1P0	I	P	1.0V	1.0V analog power for PCI Express receive.
LC_PLL0_AVDD1P8	I	P	1.8V	1.8V analog power for LC_PLL0.
LC_PLL1_AVDD1P8	I	P	1.8V	1.8V analog power for LC_PLL1.
XG_PLL2_AVDD1P8	I	P	1.8V	1.8V analog power for XG_PLL2.
BS[1:0]_PLL_AVDD1P8	I	P	1.8V	1.8V analog power for BS[1:0]_PLL.
TS_PLL_AVDD1P8	I	P	1.8V	1.8V analog power for TS_PLL.
XTAL_AVDD1P8	I	P	1.8V	1.8V analog power for crystal PLL.

Table 9: Pin Description—Grouped by Function (Cont.)

Signal Name	I/O	Rate	Type	Description
CORE_PLL_VDD1P8	I	P	1.8V	1.8V analog power for core PLL.
GEN_PLL_VDD1P8	I	P	1.8V	1.8V analog power for general PLL.
AVDD1P8	I	P	1.8V	1.8V analog power.
IHOST_PLL_AVDD1P8	I	P	1.8V	1.8V analog power for CPU PLL.
VDD1P8	I	P	1.8V	1.8V power for OTP.
Ground				
DVSS	I	P	GND	Digital ground.
DVSS_1K	I	P	GND	Digital ground. Need connect to a 1 kΩ resistor to ground on each pin. One resistor per pin.
TSC_AVSS	I	P	GND	Analog ground.
PCIE_AVSS	I	P	GND	Analog ground.
LC_PLL1_AVSS	I	P	GND	Analog ground.
IHOST_PLL_AVSS	I	P	GND	Analog ground.
XG_PLL2_AVSS	I	P	GND	Analog ground.
PLL1_AVSS	I	P	GND	Analog ground.
PLL2_AVSS	I	P	GND	Analog ground.
XTAL_AVSS	I	P	GND	Analog ground.
CORE_PLL_AVSS	I	P	GND	Analog ground.
AVSS	I	P	GND	Analog ground.
RESCAL_AVSS	I	P	GND	Analog ground.
Test Signals				
XG_MIIM1_VOLT_SEL	I_{PD}	–	CMOS, 3.3V	Internal use only. Must pull-up to 3.3V through 4.7K ohm resistor.
XG_MIIM2_VOLT_SEL	I_{PD}	–	CMOS, 3.3V	Internal use only. Must pull-up to 3.3V through 4.7K ohm resistor.
DNC	–	–	–	Do Not Connect. For factory use only.
CORE_PLL_REFCLKP CORE_PLL_REFCLKN	I	–	CML, 1.0V	Core PLL reference clock. For factory use only.
GEN_PLL_REFCLKP GEN_PLL_REFCLKN	I	–	CML, 1.0V	General PLL reference clock. For factory use only.
LC_PLL0_REFCLKP LC_PLL0_REFCLKN	I	50 MHz	CML, 1.0V	Internal test only. Differential 25 MHz reference clock. Inputs require external AC-coupling capacitors but have internal DC biasing, and therefore do not require external biasing resistors. Inputs have internal 100Ω termination.
VDD_SENSE	I	–	CMOS, 3.3V	Factory use only.
VSS_SENSE	I	–	CMOS, 3.3V	Factory use only.

Table 9: Pin Description—Grouped by Function (Cont.)

Signal Name	I/O	Rate	Type	Description
XG_PLL2_REFCLKP XG_PLL2_REFCLKN	I	50 MHz	CML, 1.0V	Internal test only. Differential 25 MHz reference clock. Inputs require external AC-coupling capacitors but have internal DC biasing, and therefore do not require external biasing resistors. Inputs have internal 100Ω termination.

Note: When one I/O pin is connected to a pull-up resistor to 3.3V, it must be connected to the same 3.3V power rail of VDDO3V3.

Table 10: Ball Out by Ball Number

Ball	Ball Name
A1	DEPOP
A2	IP_GPIO0
A3	IP_GPIO2
A4	LOS0
A5	DEPOP
A6	TS_GPIO0
A7	JTDO
A8	DEPOP
A9	JTCK
A10	POR_OUT_L
A11	DEPOP
A12	PCIE_INTR_L
A13	PCIE_PERST_L
A14	PCIE_AVSS
A15	PCIE_AVSS
A16	PCIE_RDP
A17	PCIE_AVSS
A18	PCIE_TDP
A19	PCIE_AVSS
A20	DVSS
A21	DVSS
A22	DVSS
A23	IP_QSPI_CS_L
A24	IP_QSPI_SCK
A25	IP_QSPI_MISO
A26	IP_UART0_RX
A27	IP_UART0_RTS_L
A28	IP_UART0_DTR_L
A29	IP_UART0_RI_L
A30	DEPOP
B1	IP_GPIO1
B2	IP_GPIO3
B3	LOS1
B4	LOS2
B5	LOS3
B6	TS_GPIO1
B7	JTCE1
B8	JTMS
B9	JTDI
B10	SYS_RST_L
B11	XG_MIIM0_VOLT_SEL
B12	IP_PCIE_RC_MODE
B13	PCIE_PME_WAKE_L
B14	PCIE_AVSS
B15	PCIE_RVDD1P0
B16	PCIE_RDN
B17	PCIE_TVDD1P0
B18	PCIE_TDN
B19	PCIE_AVSS
B20	DVSS
B21	DVSS
B22	DVSS
B23	IP_QSPI_HOLD_L
B24	IP_QSPI_WP_L
B25	IP_QSPI_MOSI
B26	IP_UART0_TX
B27	IP_UART0_CTS_L
B28	IP_UART0_DCD_L
B29	IP_UART0_DSR_L
B30	DVSS
C1	EXT_PHY_RCVRD_CLK0_VALID
C2	EXT_PHY_RCVRD_CLK1_VALID
C3	DVSS
C4	LOS4
C5	LOS5
C6	DNC
C7	JTCE0
C8	JTRST_L
C9	AVS0
C10	OSC_XTAL_SEL
C11	IP_BOOT_DEV0
C12	IP_BOOT_DEV1
C13	IP_QSPI_4BYTE_ADDR
C14	PCIE_AVSS
C15	PCIE_AVSS
C16	PCIE_RVDD1P0
C17	PCIE_AVSS
C18	PCIE_TVDD1P0
C19	PCIE_AVSS
C20	XG_PLL2_REFCLKN
C21	XG_PLL2_REFCLKP
C22	XG_PLL2_AVSS
C23	DVSS
C24	DVSS
C25	DVSS
C26	DVSS
C27	DVSS
C28	DVSS
C29	SPI_SCK
C30	SPI_SS_L
D1	EXT_PHY_RCVRD_CLK0
D2	EXT_PHY_RCVRD_CLK1
D3	VDDO3P3
D4	DNC
D5	DVSS
D6	VDDO3P3
D7	DNC
D8	DVSS
D9	VDDO3P3
D10	DNC
D11	IP_BOOT_DEV2
D12	VDDO3P3
D13	XG_MIIM1_VOLT_SEL
D14	DVSS
D15	PCIE_AVSS
D16	DNC
D17	PCIE_PVDD1P0
D18	PCIE_REFCLKP
D19	PCIE_AVSS
D20	XG_PLL2_AVSS
D21	XG_PLL2_AVDD1P8
D22	DNC
D23	DVSS
D24	DVSS
D25	DVSS
D26	DVSS
D27	VDDO3P3
D28	DVSS
D29	SPI_MISO
D30	SPI_MOSI
E1	L1_RCVRD_CLK_VALID
E2	L1_RCVRD_CLK_BKUP_VALID
E3	DVSS
E4	DNC
E5	DNC
E6	DNC
E7	DNC
E8	DNC
E9	DNC
E10	DNC
E11	DVSS
E12	DNC
E13	XG_MIIM2_VOLT_SEL
E14	DVSS
E15	PCIE_AVSS
E16	DNC
E17	PCIE_PVDD1P0
E18	PCIE_REFCLKN
E19	PCIE_AVSS
E20	DNC
E21	DNC
E22	DNC
E23	DVSS
E24	VDDO1P8
E25	DVSS
E26	VDDO3P3
E27	DVSS
E28	DVSS
E29	IP_BSC0_SDA
E30	IP_BSC0_SCL
F1	L1_RCVRD_CLK
F2	L1_RCVRD_CLK_BKUP
F3	DNC
F4	DNC
F5	TSC2_PWR_OFF
F6	DNC
F7	VDDO1P8
F8	DVSS
F9	VDDO1P8
F10	DVSS
F11	VDDO1P8
F12	DNC
F13	DNC
F14	DNC
F15	PCIE_AVSS
F16	PCIE_AVSS
F17	PCIE_AVSS
F18	PCIE_AVSS
F19	PCIE_AVSS
F20	XG_PLL2_AVSS
F21	XG_PLL2_AVSS
F22	DVSS
F23	VDDO1P8
F24	DVSS
F25	DVSS
F26	DVSS

Ball	Ball Name
F27	VDDO3P3
F28	DVSS
F29	BSC1_SDA
F30	BSC1_SCL
G1	XG_MDC0
G2	XG_MDIO0
G3	DVSS
G4	XG_MIIM0_VDDO
G5	XG_MIIM0_VDDP
G6	TSC1_PWR_OFF
G7	DNC
G8	VDD1P8
G9	DVSS
G10	DVSS
G11	DVSS
G12	DNC
G13	DNC
G14	DVSS
G15	DVSS
G16	PCIE_AVSS
G17	PCIE_AVSS
G18	PCIE_AVSS
G19	DVSS
G20	DVSS
G21	DVSS
G22	DVSS
G23	DVSS
G24	VDD1P8
G25	DVSS
G26	VDDO3P3
G27	DVSS
G28	DVSS
G29	BSC1_SA1
G30	BSC1_SA0
H1	XTAL_AVSS
H2	XTAL_AVSS
H3	XTAL_AVSS
H4	XTAL_AVSS
H5	LC_PLL0_REFCLKN
H6	LC_PLL0_REFCLKP
H7	DNC
H8	PLL2_AVSS
H9	DNC
H10	DNC
H11	DNC
H12	PLL2_AVSS
H13	BS1_PLL_AVDD1P8
H14	PLL2_AVSS
H15	DNC
H16	DVSS_1K
H17	DVSS_1K
H18	DVSS
H19	DVSS
H20	DVSS
H21	DVSS
H22	DVSS
H23	VDDO1P8
H24	DVSS
H25	DVSS
H26	DVSS
H27	DVSS
H28	DVSS
H29	LED_DATA
H30	LED_CLK
J1	XTALP
J2	XTALN
J3	XTAL_AVDD1P8
J4	DNC
J5	PLL2_AVSS
J6	LC_PLL0_AVDD1P8
J7	DNC
J8	PLL2_AVSS
J9	BS0_PLL_AVDD1P8
J10	DNC
J11	PLL2_AVSS
J12	BS1_PLL_REFCLKN
J13	BS1_PLL_REFCLKP
J14	PLL2_AVSS
J15	DNC
J16	DVSS_1K
J17	DVSS_1K
J18	DVSS
J19	IHOST_PLL_AVSS
J20	IHOST_PLL_AVDD1P8
J21	DVSS
J22	DVSS
J23	DVSS
J24	DVSS
J25	DVSS
J26	DNC
J27	DNC
J28	DVSS
J29	DVSS
J30	DVSS
K1	XTAL_AVSS
K2	XTAL_AVSS
K3	DNC
K4	XTAL_AVSS
K5	DNC
K6	DNC
K7	PLL2_AVSS
K8	BS0_PLL_REFCLKN
K9	BS0_PLL_REFCLKP
K10	DEPOP
K11	DEPOP
K12	DEPOP
K13	DEPOP
K14	DEPOP
K15	DEPOP
K16	DEPOP
K17	DEPOP
K18	DEPOP
K19	DEPOP
K20	DEPOP
K21	DEPOP
K22	DNC
K23	DVSS
K24	DNC
K25	DNC
K26	PLL1_AVSS
K27	TS_PLL_AVDD1P8
K28	DVSS
K29	DNC
K30	DNC
L1	TSC_AVSS
L2	TSC_AVSS
L3	TSC_AVSS
L4	TSC_AVSS
L5	TSC_AVSS
L6	TSC_AVSS
L7	TSC_AVSS
L8	TSC_AVSS
L9	PLL2_AVSS
L10	DEPOP
L11	VDDC
L12	VDDC
L13	DVSS
L14	DVSS
L15	VDDC
L16	VDDC
L17	DVSS
L18	DVSS
L19	VDDC
L20	VDDC
L21	DEPOP
L22	DNC
L23	PLL1_AVSS
L24	GEN_PLL_VDD1P8
L25	PLL1_AVSS
L26	TS_PLL_REFCLKN
L27	TS_PLL_REFCLKP
L28	DVSS
L29	DNC
L30	TSC3_PWR_OFF
M1	TSCQ0_TD0P
M2	TSCQ0_TD0N
M3	TSC_AVSS
M4	TSCQ0_RD0P
M5	TSCQ0_RD0N
M6	TSC_AVSS
M7	TSCQ0_TVDD1P0
M8	TSC_AVSS
M9	TSC_AVSS
M10	DEPOP
M11	VDDC
M12	VDDC
M13	DVSS
M14	DVSS
M15	VDDC
M16	VDDC
M17	DVSS
M18	DVSS
M19	VDDC
M20	VDDC
M21	DEPOP
M22	AVDD1P8
M23	DVSS
M24	GEN_PLL_REFCLKN
M25	GEN_PLL_REFCLKP
M26	DVSS
M27	PLL1_AVSS
M28	DVSS
M29	IP_PCIE_REFCLK_SEL
M30	IP_PCIE_FORCE_GEN1

Ball	Ball Name
N1	TSC_AVSS
N2	TSC_AVSS
N3	TSC_AVSS
N4	TSC_AVSS
N5	TSC_AVSS
N6	TSCQ0_TVDD1P0
N7	TSCQ0_TVDD1P0
N8	DNC
N9	TSC_AVSS
N10	DEPOP
N11	DVSS
N12	DVSS
N13	VDDC
N14	VDDC
N15	DVSS
N16	DVSS
N17	VDDC
N18	VDDC
N19	DVSS
N20	DVSS
N21	DEPOP
N22	AVSS
N23	TSC_AVSS
N24	TSC_AVSS
N25	TSC_AVSS
N26	TSC_AVSS
N27	TSC_AVSS
N28	XTAL_FREQ_SEL
N29	TSC4_PWR_OFF
N30	TSCQ0_PWR_OFF
P1	TSCQ0_TD1P
P2	TSCQ0_TD1N
P3	TSC_AVSS
P4	TSCQ0_RD1P
P5	TSCQ0_RD1N
P6	TSC_AVSS
P7	TSCQ0_TVDD1P0
P8	DNC
P9	TSC_AVSS
P10	DEPOP
P11	DVSS
P12	DVSS
P13	VDDC
P14	VDDC
P15	DVSS
P16	DVSS
P17	VDDC
P18	VDDC
P19	DVSS
P20	DVSS
P21	DEPOP
P22	TSC_AVSS
P23	TSC_AVSS
P24	TSC_AVSS
P25	TSC_AVSS
P26	TSC_AVSS
P27	TSC_AVSS
P28	TSC_AVSS
P29	TSC_AVSS
P30	TSC_AVSS
R1	TSC_AVSS
R2	TSC_AVSS
R3	TSC_AVSS
R4	TSC_AVSS
R5	TSC_AVSS
R6	TSCQ0_RVDD1P0
R7	TSC_AVSS
R8	TSCQ0_PVDD1P0
R9	TSC_AVSS
R10	DEPOP
R11	VDDC
R12	VDDC
R13	VDD_SENSE
R14	VSS_SENSE
R15	VDDC
R16	VDDC
R17	DVSS
R18	DVSS
R19	VDDC
R20	VDDC
R21	DEPOP
R22	TSC_AVSS
R23	TSC_AVSS
R24	TSC_AVSS
R25	TSC_AVSS
R26	TSC4_RD3P
R27	TSC4_RD3N
R28	TSC_AVSS
R29	TSC4_TD3P
R30	TSC4_TD3N
T1	TSCQ0_TD2P
T2	TSCQ0_TD2N
T3	TSC_AVSS
T4	TSCQ0_RD2P
T5	TSCQ0_RD2N
T6	TSCQ0_RVDD1P0
T7	TSCQ0_RVDD1P0
T8	DNC
T9	TSC_AVSS
T10	DEPOP
T11	DVSS
T12	TSCQ0_VDD
T13	DVSS
T14	DNC
T15	DNC
T16	CORE_PLL_REFCLKN
T17	CORE_PLL_REFCLKP
T18	DVSS
T19	VDDC
T20	VDDC
T21	DEPOP
T22	TSC_AVSS
T23	DNC
T24	TSC_AVSS
T25	TSC4_RVDD1P0
T26	TSC_AVSS
T27	TSC_AVSS
T28	TSC_AVSS
T29	TSC_AVSS
T30	TSC_AVSS
U1	TSC_AVSS
U2	TSC_AVSS
U3	TSC_AVSS
U4	TSC_AVSS
U5	TSC_AVSS
U6	TSCQ0_RVDD1P0
U7	TSC_AVSS
U8	DNC
U9	TSC_AVSS
U10	DEPOP
U11	TSCQ0_VDD
U12	TSCQ0_VDD
U13	DVSS
U14	VDDC
U15	CORE_PLL_VDD1P8
U16	CORE_PLL_AVSS
U17	VDDC
U18	VDDC
U19	DVSS
U20	DVSS
U21	DEPOP
U22	TSC_AVSS
U23	DNC
U24	TSC4_RVDD1P0
U25	TSC4_RVDD1P0
U26	TSC4_RD2P
U27	TSC4_RD2N
U28	TSC_AVSS
U29	TSC4_TD2P
U30	TSC4_TD2N
V1	TSCQ0_TD3P
V2	TSCQ0_TD3N
V3	TSC_AVSS
V4	TSCQ0_RD3P
V5	TSCQ0_RD3N
V6	TSC_AVSS
V7	TSC_AVSS
V8	TSC_AVSS
V9	LC_PLL1_AVSS
V10	DEPOP
V11	TSCQ0_VDD
V12	DVSS
V13	VDDC
V14	DVSS
V15	RESCAL_AVSS
V16	RESCAL_REXT
V17	DVSS
V18	DVSS
V19	DVSS
V20	TSC4_VDD
V21	DEPOP
V22	TSC_AVSS
V23	TSC4_PVDD1P0
V24	TSC_AVSS
V25	TSC4_RVDD1P0
V26	TSC_AVSS
V27	TSC_AVSS
V28	TSC_AVSS
V29	TSC_AVSS
V30	TSC_AVSS
W1	TSC_AVSS
W2	TSC_AVSS
W3	TSC_AVSS
W4	TSC_AVSS
W5	TSC_AVSS
W6	TSC_AVSS

Ball	Ball Name
W7	LC_PLL1_AVSS
W8	DNC
W9	DNC
W10	DEPOP
W11	DVSS
W12	TSC0_VDD
W13	DVSS
W14	TSC1_VDD
W15	DVSS
W16	TSC2_VDD
W17	DVSS
W18	TSC3_VDD
W19	DVSS
W20	TSC4_VDD
W21	DEPOP
W22	TSC_AVSS
W23	DNC
W24	TSC4_TVDD1P0
W25	TSC_AVSS
W26	TSC4_RD1P
W27	TSC4_RD1N
W28	TSC_AVSS
W29	TSC4_TD1P
W30	TSC4_TD1N
Y1	DNC
Y2	DNC
Y3	TSC0_PVDD1P0
Y4	TSC_AVSS
Y5	TSC_AVSS
Y6	TSC_AVSS
Y7	LC_PLL1_REFCLKN
Y8	LC_PLL1_AVDD1P8
Y9	DNC
Y10	DEPOP
Y11	DVSS
Y12	TSC0_VDD
Y13	DVSS
Y14	TSC1_VDD
Y15	DVSS
Y16	TSC2_VDD
Y17	DVSS
Y18	TSC3_VDD
Y19	DVSS
Y20	TSC4_VDD
Y21	DEPOP
Y22	TSC_AVSS
Y23	DNC

Ball	Ball Name
Y24	TSC4_TVDD1P0
Y25	TSC4_TVDD1P0
Y26	TSC_AVSS
Y27	TSC_AVSS
Y28	TSC_AVSS
Y29	TSC_AVSS
Y30	TSC_AVSS
AA1	TSC0_TVDD1P0
AA2	TSC0_TVDD1P0
AA3	TSC_AVSS
AA4	DNC
AA5	DNC
AA6	TSC_AVSS
AA7	LC_PLL1_REFCLKP
AA8	LC_PLL1_AVSS
AA9	DNC
AA10	DEPOP
AA11	DEPOP
AA12	DEPOP
AA13	DEPOP
AA14	DEPOP
AA15	DEPOP
AA16	DEPOP
AA17	DEPOP
AA18	DEPOP
AA19	DEPOP
AA20	DEPOP
AA21	DEPOP
AA22	TSC_AVSS
AA23	TSC_AVSS
AA24	TSC4_TVDD1P0
AA25	TSC_AVSS
AA26	TSC4_RD0P
AA27	TSC4_RD0N
AA28	TSC_AVSS
AA29	TSC4_TD0P
AA30	TSC4_TD0N
AB1	TSC0_TVDD1P0
AB2	TSC0_TVDD1P0
AB3	TSC_AVSS
AB4	TSC0_RVDD1P0
AB5	TSC0_RVDD1P0
AB6	TSC_AVSS
AB7	TSC_AVSS
AB8	TSC_AVSS
AB9	TSC_AVSS
AB10	TSC_AVSS

Ball	Ball Name
AB11	TSC_AVSS
AB12	TSC_AVSS
AB13	TSC_AVSS
AB14	TSC_AVSS
AB15	TSC_AVSS
AB16	TSC_AVSS
AB17	TSC_AVSS
AB18	TSC_AVSS
AB19	TSC_AVSS
AB20	TSC_AVSS
AB21	TSC_AVSS
AB22	TSC_AVSS
AB23	TSC_AVSS
AB24	TSC_AVSS
AB25	TSC_AVSS
AB26	TSC_AVSS
AB27	TSC_AVSS
AB28	TSC_AVSS
AB29	TSC_AVSS
AB30	TSC_AVSS
AC1	TSC0_TD0N
AC2	TSC0_TD0P
AC3	TSC_AVSS
AC4	TSC0_RVDD1P0
AC5	TSC0_RVDD1P0
AC6	TSC_AVSS
AC7	TSC_AVSS
AC8	DNC
AC9	DNC
AC10	TSC1_PVDD1P0
AC11	DNC
AC12	DNC
AC13	TSC_AVSS
AC14	TSC_AVSS
AC15	TSC_AVSS
AC16	DNC
AC17	DNC
AC18	TSC2_PVDD1P0
AC19	DNC
AC20	DNC
AC21	TSC_AVSS
AC22	TSC_AVSS
AC23	TSC_AVSS
AC24	DNC
AC25	DNC
AC26	TSC3_PVDD1P0
AC27	DNC

Ball	Ball Name
AC28	DNC
AC29	TSC_AVSS
AC30	TSC_AVSS
AD1	TSC_AVSS
AD2	TSC_AVSS
AD3	TSC_AVSS
AD4	TSC0_RD0P
AD5	TSC0_RD0N
AD6	TSC_AVSS
AD7	TSC1_TVDD1P0
AD8	TSC1_TVDD1P0
AD9	TSC1_TVDD1P0
AD10	TSC_AVSS
AD11	TSC1_RVDD1P0
AD12	TSC_AVSS
AD13	TSC_AVSS
AD14	TSC_AVSS
AD15	TSC2_TVDD1P0
AD16	TSC2_TVDD1P0
AD17	TSC2_TVDD1P0
AD18	TSC_AVSS
AD19	TSC2_RVDD1P0
AD20	TSC_AVSS
AD21	TSC_AVSS
AD22	TSC_AVSS
AD23	TSC3_TVDD1P0
AD24	TSC3_TVDD1P0
AD25	TSC3_TVDD1P0
AD26	TSC_AVSS
AD27	TSC3_RVDD1P0
AD28	TSC_AVSS
AD29	TSC_AVSS
AD30	TSC_AVSS
AE1	TSC0_TD1N
AE2	TSC0_TD1P
AE3	TSC_AVSS
AE4	TSC_AVSS
AE5	TSC_AVSS
AE6	TSC_AVSS
AE7	TSC_AVSS
AE8	TSC1_TVDD1P0
AE9	TSC_AVSS
AE10	TSC1_RVDD1P0
AE11	TSC1_RVDD1P0
AE12	TSC1_RVDD1P0
AE13	TSC_AVSS
AE14	TSC_AVSS

Ball	Ball Name
AE15	TSC_AVSS
AE16	TSC2_TVDD1P0
AE17	TSC_AVSS
AE18	TSC2_RVDD1P0
AE19	TSC2_RVDD1P0
AE20	TSC2_RVDD1P0
AE21	TSC_AVSS
AE22	TSC_AVSS
AE23	TSC_AVSS
AE24	TSC3_TVDD1P0
AE25	TSC_AVSS
AE26	TSC3_RVDD1P0
AE27	TSC3_RVDD1P0
AE28	TSC3_RVDD1P0
AE29	TSC_AVSS
AE30	TSC_AVSS
AF1	TSC_AVSS
AF2	TSC_AVSS
AF3	TSC_AVSS
AF4	TSC0_RD1P
AF5	TSC0_RD1N
AF6	TSC_AVSS
AF7	TSC1_RD0N
AF8	TSC_AVSS
AF9	TSC1_RD1N
AF10	TSC_AVSS
AF11	TSC1_RD2N
AF12	TSC_AVSS
AF13	TSC1_RD3N
AF14	TSC_AVSS
AF15	TSC2_RD0N
AF16	TSC_AVSS
AF17	TSC2_RD1N
AF18	TSC_AVSS
AF19	TSC2_RD2N
AF20	TSC_AVSS
AF21	TSC2_RD3N
AF22	TSC_AVSS
AF23	TSC3_RD0N
AF24	TSC_AVSS
AF25	TSC3_RD1N
AF26	TSC_AVSS
AF27	TSC3_RD2N
AF28	TSC_AVSS
AF29	TSC3_RD3N
AF30	TSC_AVSS
AG1	TSC0_TD2N
AG2	TSC0_TD2P
AG3	TSC_AVSS
AG4	TSC_AVSS
AG5	TSC_AVSS
AG6	TSC_AVSS
AG7	TSC1_RD0P
AG8	TSC_AVSS
AG9	TSC1_RD1P
AG10	TSC_AVSS
AG11	TSC1_RD2P
AG12	TSC_AVSS
AG13	TSC1_RD3P
AG14	TSC_AVSS
AG15	TSC2_RD0P
AG16	TSC_AVSS
AG17	TSC2_RD1P
AG18	TSC_AVSS
AG19	TSC2_RD2P
AG20	TSC_AVSS
AG21	TSC2_RD3P
AG22	TSC_AVSS
AG23	TSC3_RD0P
AG24	TSC_AVSS
AG25	TSC3_RD1P
AG26	TSC_AVSS
AG27	TSC3_RD2P
AG28	TSC_AVSS
AG29	TSC3_RD3P
AG30	TSC_AVSS
AH1	TSC_AVSS
AH2	TSC_AVSS
AH3	TSC_AVSS
AH4	TSC0_RD2P
AH5	TSC0_RD2N
AH6	TSC_AVSS
AH7	TSC_AVSS
AH8	TSC_AVSS
AH9	TSC_AVSS
AH10	TSC_AVSS
AH11	TSC_AVSS
AH12	TSC_AVSS
AH13	TSC_AVSS
AH14	TSC_AVSS
AH15	TSC_AVSS
AH16	TSC_AVSS
AH17	TSC_AVSS
AH18	TSC_AVSS
AH19	TSC_AVSS
AH20	TSC_AVSS
AH21	TSC_AVSS
AH22	TSC_AVSS
AH23	TSC_AVSS
AH24	TSC_AVSS
AH25	TSC_AVSS
AH26	TSC_AVSS
AH27	TSC_AVSS
AH28	TSC_AVSS
AH29	TSC_AVSS
AH30	TSC_AVSS
AJ1	TSC0_TD3N
AJ2	TSC0_TD3P
AJ3	TSC_AVSS
AJ4	TSC_AVSS
AJ5	TSC_AVSS
AJ6	TSC_AVSS
AJ7	TSC1_TD0P
AJ8	TSC_AVSS
AJ9	TSC1_TD1P
AJ10	TSC_AVSS
AJ11	TSC1_TD2P
AJ12	TSC_AVSS
AJ13	TSC1_TD3P
AJ14	TSC_AVSS
AJ15	TSC2_TD0P
AJ16	TSC_AVSS
AJ17	TSC2_TD1P
AJ18	TSC_AVSS
AJ19	TSC2_TD2P
AJ20	TSC_AVSS
AJ21	TSC2_TD3P
AJ22	TSC_AVSS
AJ23	TSC3_TD0P
AJ24	TSC_AVSS
AJ25	TSC3_TD1P
AJ26	TSC_AVSS
AJ27	TSC3_TD2P
AJ28	TSC_AVSS
AJ29	TSC3_TD3P
AJ30	TSC_AVSS
AK1	DEPOP
AK2	TSC_AVSS
AK3	TSC_AVSS
AK4	TSC0_RD3P
AK5	TSC0_RD3N
AK6	TSC_AVSS
AK7	TSC1_TD0N
AK8	TSC_AVSS
AK9	TSC1_TD1N
AK10	TSC_AVSS
AK11	TSC1_TD2N
AK12	TSC_AVSS
AK13	TSC1_TD3N
AK14	TSC_AVSS
AK15	TSC2_TD0N
AK16	TSC_AVSS
AK17	TSC2_TD1N
AK18	TSC_AVSS
AK19	TSC2_TD2N
AK20	TSC_AVSS
AK21	TSC2_TD3N
AK22	TSC_AVSS
AK23	TSC3_TD0N
AK24	TSC_AVSS
AK25	TSC3_TD1N
AK26	TSC_AVSS
AK27	TSC3_TD2N
AK28	TSC_AVSS
AK29	TSC3_TD3N
AK30	DEPOP

Note: DEPPOP means there is no ball on the package.

Table 11: Ball Out by Ball Name

Ball Name	Ball
AVDD1P8	M22
AVS0	C9
AVSS	N22
BS0_PLL_AVDD1P8	J9
BS0_PLL_REFCLKN	K8
BS0_PLL_REFCLKP	K9
BS1_PLL_AVDD1P8	H13
BS1_PLL_REFCLKN	J12
BS1_PLL_REFCLKP	J13
BSC1_SA0	G30
BSC1_SA1	G29
BSC1_SCL	F30
BSC1_SDA	F29
CORE_PLL_AVSS	U16
CORE_PLL_REFCLKN	T16
CORE_PLL_REFCLKP	T17
CORE_PLL_VDD1P8	U15
DEPOP	A1
DEPOP	A5
DEPOP	A8
DEPOP	A11
DEPOP	A30
DEPOP	K10
DEPOP	K11
DEPOP	K12
DEPOP	K13
DEPOP	K14
DEPOP	K15
DEPOP	K16
DEPOP	K17
DEPOP	K18
DEPOP	K19
DEPOP	K20
DEPOP	K21
DEPOP	L10
DEPOP	L21
DEPOP	M10
DEPOP	M21
DEPOP	N10
DEPOP	N21
DEPOP	P10
DEPOP	P21
DEPOP	R10
DEPOP	R21
DEPOP	T10
DEPOP	T21
DEPOP	U10
DEPOP	U21
DEPOP	V10
DEPOP	V21
DEPOP	W10
DEPOP	W21
DEPOP	Y10
DEPOP	Y21
DEPOP	AA10
DEPOP	AA11
DEPOP	AA12
DEPOP	AA13
DEPOP	AA14
DEPOP	AA15
DEPOP	AA16
DEPOP	AA17
DEPOP	AA18
DEPOP	AA19
DEPOP	AA20
DEPOP	AA21
DEPOP	AK1
DEPOP	AK30

Note: DEPOP means there is no ball on the package.

Ball Name	Ball
DNC	C6
DNC	D4
DNC	D7
DNC	D10
DNC	D16
DNC	D22
DNC	E4
DNC	E5
DNC	E6
DNC	E7
DNC	E8
DNC	E9
DNC	E10
DNC	E12
DNC	E16
DNC	E20
DNC	E21
DNC	E22
DNC	F3
DNC	F4
DNC	F6
DNC	F12
DNC	F13
DNC	F14
DNC	G7
DNC	G12
DNC	G13
DNC	H7
DNC	H9
DNC	H10
DNC	H11
DNC	H15
DNC	J4
DNC	J7
DNC	J10
DNC	J15
DNC	J26
DNC	J27
DNC	K3
DNC	K5
DNC	K6
DNC	K22
DNC	K24
DNC	K25
DNC	K29
DNC	K30
DNC	L22
DNC	L29
DNC	N8
DNC	P8
DNC	T8
DNC	T14
DNC	T15
DNC	T23
DNC	U8
DNC	U23
DNC	W8
DNC	W9
DNC	W23
DNC	Y1
DNC	Y2
DNC	Y9
DNC	Y23
DNC	AA4
DNC	AA5
DNC	AA9
DNC	AC8
DNC	AC9
DNC	AC11
DNC	AC12
DNC	AC16
DNC	AC17
DNC	AC19
DNC	AC20
DNC	AC24
DNC	AC25
DNC	AC27
DNC	AC28
DVSS	A20
DVSS	A21
DVSS	A22
DVSS	B20
DVSS	B21
DVSS	B22
DVSS	B30
DVSS	C3
DVSS	C23
DVSS	C24
DVSS	C25
DVSS	C26
DVSS	C27
DVSS	C28
DVSS	D5
DVSS	D8
DVSS	D14
DVSS	D23
DVSS	D24
DVSS	D25
DVSS	D26
DVSS	D28
DVSS	E3
DVSS	E11
DVSS	E14
DVSS	E23
DVSS	E25
DVSS	E27
DVSS	E28
DVSS	F8
DVSS	F10
DVSS	F22
DVSS	F24

Ball Name	Ball
DVSS	F25
DVSS	F26
DVSS	F28
DVSS	G3
DVSS	G9
DVSS	G10
DVSS	G11
DVSS	G14
DVSS	G15
DVSS	G19
DVSS	G20
DVSS	G21
DVSS	G22
DVSS	G23
DVSS	G25
DVSS	G27
DVSS	G28
DVSS	H18
DVSS	H19
DVSS	H20
DVSS	H21
DVSS	H22
DVSS	H24
DVSS	H25
DVSS	H26
DVSS	H27
DVSS	H28
DVSS	J18
DVSS	J21
DVSS	J22
DVSS	J23
DVSS	J24
DVSS	J25
DVSS	J28
DVSS	J29
DVSS	J30
DVSS	K23
DVSS	K28
DVSS	L13
DVSS	L14
DVSS	L17
DVSS	L18
DVSS	L28
DVSS	M13
DVSS	M14
DVSS	M17
DVSS	M18

Ball Name	Ball
DVSS	M23
DVSS	M26
DVSS	M28
DVSS	N11
DVSS	N12
DVSS	N15
DVSS	N16
DVSS	N19
DVSS	N20
DVSS	P11
DVSS	P12
DVSS	P15
DVSS	P16
DVSS	P19
DVSS	P20
DVSS	R17
DVSS	R18
DVSS	T11
DVSS	T13
DVSS	T18
DVSS	U13
DVSS	U19
DVSS	U20
DVSS	V12
DVSS	V14
DVSS	V17
DVSS	V18
DVSS	V19
DVSS	W11
DVSS	W13
DVSS	W15
DVSS	W17
DVSS	W19
DVSS	Y11
DVSS	Y13
DVSS	Y15
DVSS	Y17
DVSS	Y19
DVSS_1K	H16
DVSS_1K	H17
DVSS_1K	J16
DVSS_1K	J17
EXT_PHY_RCVRD_CLK0	D1
EXT_PHY_RCVRD_CLK0_VALID	C1
EXT_PHY_RCVRD_CLK1	D2

Ball Name	Ball
EXT_PHY_RCVRD_CLK1_VALID	C2
GEN_PLL_REFCLKN	M24
GEN_PLL_REFCLKP	M25
GEN_PLL_VDD1P8	L24
IHOST_PLL_AVDD1P8	J20
IHOST_PLL_AVSS	J19
IP_BOOT_DEV0	C11
IP_BOOT_DEV1	C12
IP_BOOT_DEV2	D11
IP_BSC0_SCL	E30
IP_BSC0_SDA	E29
IP_GPIO0	A2
IP_GPIO1	B1
IP_GPIO2	A3
IP_GPIO3	B2
IP_PCIE_FORCE_GEN1	M30
IP_PCIE_RC_MODE	B12
IP_PCIE_REFCLK_SEL	M29
IP_QSPI_4BYTE_ADDR	C13
IP_QSPI_CS_L	A23
IP_QSPI_HOLD_L	B23
IP_QSPI_MISO	A25
IP_QSPI_MOSI	B25
IP_QSPI_SCK	A24
IP_QSPI_WP_L	B24
IP_UART0_CTS_L	B27
IP_UART0_DCD_L	B28
IP_UART0_DSR_L	B29
IP_UART0_DTR_L	A28
IP_UART0_RI_L	A29
IP_UART0_RTS_L	A27
IP_UART0_RX	A26
IP_UART0_TX	B26
JTCE0	C7
JTCE1	B7
JTCK	A9
JTDI	B9
JTDO	A7
JTMS	B8
JTRST_L	C8
L1_RCVRD_CLK	F1
L1_RCVRD_CLK_BKUP	F2

Ball Name	Ball
L1_RCVRD_CLK_VALID	E1
L1_RCVRD_CLK_BKUP_VALID	E2
LC_PLL0_AVDD1P8	J6
LC_PLL0_REFCLKN	H5
LC_PLL0_REFCLKP	H6
LC_PLL1_AVSS	V9
LC_PLL1_AVSS	W7
LC_PLL1_AVSS	AA8
LC_PLL1_AVDD1P8	Y8
LC_PLL1_REFCLKN	Y7
LC_PLL1_REFCLKP	AA7
LED_CLK	H30
LED_DATA	H29
LOS0	A4
LOS1	B3
LOS2	B4
LOS3	B5
LOS4	C4
LOS5	C5
OSC_XTAL_SEL	C10
PCIE_AVSS	A14
PCIE_AVSS	A15
PCIE_AVSS	A17
PCIE_AVSS	A19
PCIE_AVSS	B14
PCIE_AVSS	B19
PCIE_AVSS	C14
PCIE_AVSS	C15
PCIE_AVSS	C17
PCIE_AVSS	C19
PCIE_AVSS	D15
PCIE_AVSS	D19
PCIE_AVSS	E15
PCIE_AVSS	E19
PCIE_AVSS	F15
PCIE_AVSS	F16
PCIE_AVSS	F17
PCIE_AVSS	F18
PCIE_AVSS	F19
PCIE_AVSS	G16
PCIE_AVSS	G17
PCIE_AVSS	G18
PCIE_INTR_L	A12
PCIE_PERST_L	A13
PCIE_PME_WAKE_L	B13
PCIE_PVDD1P0	D17

Ball Name	Ball
PCIE_PVDD1P0	E17
PCIE_RDN	B16
PCIE_RDP	A16
PCIE_REFCLKN	E18
PCIE_REFCLKP	D18
PCIE_RVDD1P0	B15
PCIE_RVDD1P0	C16
PCIE_TDN	B18
PCIE_TDP	A18
PCIE_TVDD1P0	B17
PCIE_TVDD1P0	C18
PLL1_AVSS	K26
PLL1_AVSS	L23
PLL1_AVSS	L25
PLL1_AVSS	M27
PLL2_AVSS	H8
PLL2_AVSS	H12
PLL2_AVSS	H14
PLL2_AVSS	J5
PLL2_AVSS	J8
PLL2_AVSS	J11
PLL2_AVSS	J14
PLL2_AVSS	K7
PLL2_AVSS	L9
POR_OUT_L	A10
RESCAL_AVSS	V15
RESCAL_REXT	V16
SPI_MISO	D29
SPI_MOSI	D30
SPI_SCK	C29
SPI_SS_L	C30
SYS_RST_L	B10
TSC0_PVDD1P0	Y3
TSC0_RD0N	AD5
TSC0_RD0P	AD4
TSC0_RD1N	AF5
TSC0_RD1P	AF4
TSC0_RD2N	AH5
TSC0_RD2P	AH4
TSC0_RD3N	AK5
TSC0_RD3P	AK4
TSC0_RVDD1P0	AB4
TSC0_RVDD1P0	AB5
TSC0_RVDD1P0	AC4
TSC0_RVDD1P0	AC5
TSC0_TD0N	AC1
TSC0_TD0P	AC2

Ball Name	Ball
TSC0_TD1N	AE1
TSC0_TD1P	AE2
TSC0_TD2N	AG1
TSC0_TD2P	AG2
TSC0_TD3N	AJ1
TSC0_TD3P	AJ2
TSC0_TVDD1P0	AA1
TSC0_TVDD1P0	AA2
TSC0_TVDD1P0	AB1
TSC0_TVDD1P0	AB2
TSC0_VDD	W12
TSC0_VDD	Y12
TSC1_PVDD1P0	AC10
TSC1_PWR_OFF	G6
TSC1_RD0N	AF7
TSC1_RD0P	AG7
TSC1_RD1N	AF9
TSC1_RD1P	AG9
TSC1_RD2N	AF11
TSC1_RD2P	AG11
TSC1_RD3N	AF13
TSC1_RD3P	AG13
TSC1_RVDD1P0	AD11
TSC1_RVDD1P0	AE10
TSC1_RVDD1P0	AE11
TSC1_RVDD1P0	AE12
TSC1_TD0N	AK7
TSC1_TD0P	AJ7
TSC1_TD1N	AK9
TSC1_TD1P	AJ9
TSC1_TD2N	AK11
TSC1_TD2P	AJ11
TSC1_TD3N	AK13
TSC1_TD3P	AJ13
TSC1_TVDD1P0	AD7
TSC1_TVDD1P0	AD8
TSC1_TVDD1P0	AD9
TSC1_TVDD1P0	AE8
TSC1_VDD	W14
TSC1_VDD	Y14
TSC2_PVDD1P0	AC18
TSC2_PWR_OFF	F5
TSC2_RD0N	AF15
TSC2_RD0P	AG15
TSC2_RD1N	AF17
TSC2_RD1P	AG17
TSC2_RD2N	AF19

Ball Name	Ball
TSC2_RD2P	AG19
TSC2_RD3N	AF21
TSC2_RD3P	AG21
TSC2_RVDD1P0	AD19
TSC2_RVDD1P0	AE18
TSC2_RVDD1P0	AE19
TSC2_RVDD1P0	AE20
TSC2_TD0N	AK15
TSC2_TD0P	AJ15
TSC2_TD1N	AK17
TSC2_TD1P	AJ17
TSC2_TD2N	AK19
TSC2_TD2P	AJ19
TSC2_TD3N	AK21
TSC2_TD3P	AJ21
TSC2_TVDD1P0	AD15
TSC2_TVDD1P0	AD16
TSC2_TVDD1P0	AD17
TSC2_TVDD1P0	AE16
TSC2_VDD	W16
TSC2_VDD	Y16
TSC3_PVDD1P0	AC26
TSC3_PWR_OFF	L30
TSC3_RD0N	AF23
TSC3_RD0P	AG23
TSC3_RD1N	AF25
TSC3_RD1P	AG25
TSC3_RD2N	AF27
TSC3_RD2P	AG27
TSC3_RD3N	AF29
TSC3_RD3P	AG29
TSC3_RVDD1P0	AD27
TSC3_RVDD1P0	AE26
TSC3_RVDD1P0	AE27
TSC3_RVDD1P0	AE28
TSC3_TD0N	AK23
TSC3_TD0P	AJ23
TSC3_TD1N	AK25
TSC3_TD1P	AJ25
TSC3_TD2N	AK27
TSC3_TD2P	AJ27
TSC3_TD3N	AK29
TSC3_TD3P	AJ29
TSC3_TVDD1P0	AD23
TSC3_TVDD1P0	AD24
TSC3_TVDD1P0	AD25
TSC3_TVDD1P0	AE24

Ball Name	Ball
TSC3_VDD	W18
TSC3_VDD	Y18
TSC4_PVDD1P0	V23
TSC4_PWR_OFF	N29
TSC4_RD0N	AA27
TSC4_RD0P	AA26
TSC4_RD1N	W27
TSC4_RD1P	W26
TSC4_RD2N	U27
TSC4_RD2P	U26
TSC4_RD3N	R27
TSC4_RD3P	R26
TSC4_RVDD1P0	T25
TSC4_RVDD1P0	U24
TSC4_RVDD1P0	U25
TSC4_RVDD1P0	V25
TSC4_TD0N	AA30
TSC4_TD0P	AA29
TSC4_TD1N	W30
TSC4_TD1P	W29
TSC4_TD2N	U30
TSC4_TD2P	U29
TSC4_TD3N	R30
TSC4_TD3P	R29
TSC4_TVDD1P0	W24
TSC4_TVDD1P0	Y24
TSC4_TVDD1P0	Y25
TSC4_TVDD1P0	AA24
TSC4_VDD	V20
TSC4_VDD	W20
TSC4_VDD	Y20
TSCQ0_PVDD1P0	R8
TSCQ0_PWR_OFF	N30
TSCQ0_RD0N	M5
TSCQ0_RD0P	M4
TSCQ0_RD1N	P5
TSCQ0_RD1P	P4
TSCQ0_RD2N	T5
TSCQ0_RD2P	T4
TSCQ0_RD3N	V5
TSCQ0_RD3P	V4
TSCQ0_RVDD1P0	R6
TSCQ0_RVDD1P0	T6
TSCQ0_RVDD1P0	T7
TSCQ0_RVDD1P0	U6
TSCQ0_TD0N	M2
TSCQ0_TD0P	M1

Ball Name	Ball
TSCQ0_TD1N	P2
TSCQ0_TD1P	P1
TSCQ0_TD2N	T2
TSCQ0_TD2P	T1
TSCQ0_TD3N	V2
TSCQ0_TD3P	V1
TSCQ0_TVDD1P0	M7
TSCQ0_TVDD1P0	N6
TSCQ0_TVDD1P0	N7
TSCQ0_TVDD1P0	P7
TSCQ0_VDD	T12
TSCQ0_VDD	U11
TSCQ0_VDD	U12
TSCQ0_VDD	V11
TSC_AVSS	L1
TSC_AVSS	L2
TSC_AVSS	L3
TSC_AVSS	L4
TSC_AVSS	L5
TSC_AVSS	L6
TSC_AVSS	L7
TSC_AVSS	L8
TSC_AVSS	M3
TSC_AVSS	M6
TSC_AVSS	M8
TSC_AVSS	M9
TSC_AVSS	N1
TSC_AVSS	N2
TSC_AVSS	N3
TSC_AVSS	N4
TSC_AVSS	N5
TSC_AVSS	N9
TSC_AVSS	N23
TSC_AVSS	N24
TSC_AVSS	N25
TSC_AVSS	N26
TSC_AVSS	N27
TSC_AVSS	P3
TSC_AVSS	P6
TSC_AVSS	P9
TSC_AVSS	P22
TSC_AVSS	P23
TSC_AVSS	P24
TSC_AVSS	P25
TSC_AVSS	P26
TSC_AVSS	P27
TSC_AVSS	P28
TSC_AVSS	P29
TSC_AVSS	P30
TSC_AVSS	R1
TSC_AVSS	R2
TSC_AVSS	R3
TSC_AVSS	R4
TSC_AVSS	R5
TSC_AVSS	R7
TSC_AVSS	R9
TSC_AVSS	R22
TSC_AVSS	R23
TSC_AVSS	R24
TSC_AVSS	R25
TSC_AVSS	R28
TSC_AVSS	T3
TSC_AVSS	T9
TSC_AVSS	T22
TSC_AVSS	T24
TSC_AVSS	T26
TSC_AVSS	T27
TSC_AVSS	T28
TSC_AVSS	T29
TSC_AVSS	T30
TSC_AVSS	U1
TSC_AVSS	U2
TSC_AVSS	U3
TSC_AVSS	U4
TSC_AVSS	U5
TSC_AVSS	U7
TSC_AVSS	U9
TSC_AVSS	U22
TSC_AVSS	U28
TSC_AVSS	V3
TSC_AVSS	V6
TSC_AVSS	V7
TSC_AVSS	V8
TSC_AVSS	V22
TSC_AVSS	V24
TSC_AVSS	V26
TSC_AVSS	V27
TSC_AVSS	V28
TSC_AVSS	V29
TSC_AVSS	V30
TSC_AVSS	W1
TSC_AVSS	W2
TSC_AVSS	W3
TSC_AVSS	W4
TSC_AVSS	W5
TSC_AVSS	W6
TSC_AVSS	W22
TSC_AVSS	W25
TSC_AVSS	W28
TSC_AVSS	Y4
TSC_AVSS	Y5
TSC_AVSS	Y6
TSC_AVSS	Y22
TSC_AVSS	Y26
TSC_AVSS	Y27
TSC_AVSS	Y28
TSC_AVSS	Y29
TSC_AVSS	Y30
TSC_AVSS	AA3
TSC_AVSS	AA6
TSC_AVSS	AA22
TSC_AVSS	AA23
TSC_AVSS	AA25
TSC_AVSS	AA28
TSC_AVSS	AB3
TSC_AVSS	AB6
TSC_AVSS	AB7
TSC_AVSS	AB8
TSC_AVSS	AB9
TSC_AVSS	AB10
TSC_AVSS	AB11
TSC_AVSS	AB12
TSC_AVSS	AB13
TSC_AVSS	AB14
TSC_AVSS	AB15
TSC_AVSS	AB16
TSC_AVSS	AB17
TSC_AVSS	AB18
TSC_AVSS	AB19
TSC_AVSS	AB20
TSC_AVSS	AB21
TSC_AVSS	AB22
TSC_AVSS	AB23
TSC_AVSS	AB24
TSC_AVSS	AB25
TSC_AVSS	AB26
TSC_AVSS	AB27
TSC_AVSS	AB28
TSC_AVSS	AB29
TSC_AVSS	AB30
TSC_AVSS	AC3
TSC_AVSS	AC6
TSC_AVSS	AC7
TSC_AVSS	AC13
TSC_AVSS	AC14
TSC_AVSS	AC15
TSC_AVSS	AC21
TSC_AVSS	AC22
TSC_AVSS	AC23
TSC_AVSS	AC29
TSC_AVSS	AC30
TSC_AVSS	AD1
TSC_AVSS	AD2
TSC_AVSS	AD3
TSC_AVSS	AD6
TSC_AVSS	AD10
TSC_AVSS	AD12
TSC_AVSS	AD13
TSC_AVSS	AD14
TSC_AVSS	AD18
TSC_AVSS	AD20
TSC_AVSS	AD21
TSC_AVSS	AD22
TSC_AVSS	AD26
TSC_AVSS	AD28
TSC_AVSS	AD29
TSC_AVSS	AD30
TSC_AVSS	AE3
TSC_AVSS	AE4
TSC_AVSS	AE5
TSC_AVSS	AE6
TSC_AVSS	AE7
TSC_AVSS	AE9
TSC_AVSS	AE13
TSC_AVSS	AE14
TSC_AVSS	AE15
TSC_AVSS	AE17
TSC_AVSS	AE21
TSC_AVSS	AE22
TSC_AVSS	AE23
TSC_AVSS	AE25
TSC_AVSS	AE29
TSC_AVSS	AE30
TSC_AVSS	AF1
TSC_AVSS	AF2
TSC_AVSS	AF3
TSC_AVSS	AF6
TSC_AVSS	AF8

Ball Name	Ball
TSC_AVSS	AF10
TSC_AVSS	AF12
TSC_AVSS	AF14
TSC_AVSS	AF16
TSC_AVSS	AF18
TSC_AVSS	AF20
TSC_AVSS	AF22
TSC_AVSS	AF24
TSC_AVSS	AF26
TSC_AVSS	AF28
TSC_AVSS	AF30
TSC_AVSS	AG3
TSC_AVSS	AG4
TSC_AVSS	AG5
TSC_AVSS	AG6
TSC_AVSS	AG8
TSC_AVSS	AG10
TSC_AVSS	AG12
TSC_AVSS	AG14
TSC_AVSS	AG16
TSC_AVSS	AG18
TSC_AVSS	AG20
TSC_AVSS	AG22
TSC_AVSS	AG24
TSC_AVSS	AG26
TSC_AVSS	AG28
TSC_AVSS	AG30
TSC_AVSS	AH1
TSC_AVSS	AH2
TSC_AVSS	AH3
TSC_AVSS	AH6
TSC_AVSS	AH7
TSC_AVSS	AH8
TSC_AVSS	AH9
TSC_AVSS	AH10
TSC_AVSS	AH11
TSC_AVSS	AH12
TSC_AVSS	AH13
TSC_AVSS	AH14
TSC_AVSS	AH15
TSC_AVSS	AH16
TSC_AVSS	AH17
TSC_AVSS	AH18
TSC_AVSS	AH19
TSC_AVSS	AH20
TSC_AVSS	AH21
TSC_AVSS	AH22

Ball Name	Ball
TSC_AVSS	AH23
TSC_AVSS	AH24
TSC_AVSS	AH25
TSC_AVSS	AH26
TSC_AVSS	AH27
TSC_AVSS	AH28
TSC_AVSS	AH29
TSC_AVSS	AH30
TSC_AVSS	AJ3
TSC_AVSS	AJ4
TSC_AVSS	AJ5
TSC_AVSS	AJ6
TSC_AVSS	AJ8
TSC_AVSS	AJ10
TSC_AVSS	AJ12
TSC_AVSS	AJ14
TSC_AVSS	AJ16
TSC_AVSS	AJ18
TSC_AVSS	AJ20
TSC_AVSS	AJ22
TSC_AVSS	AJ24
TSC_AVSS	AJ26
TSC_AVSS	AJ28
TSC_AVSS	AJ30
TSC_AVSS	AK2
TSC_AVSS	AK3
TSC_AVSS	AK6
TSC_AVSS	AK8
TSC_AVSS	AK10
TSC_AVSS	AK12
TSC_AVSS	AK14
TSC_AVSS	AK16
TSC_AVSS	AK18
TSC_AVSS	AK20
TSC_AVSS	AK22
TSC_AVSS	AK24
TSC_AVSS	AK26
TSC_AVSS	AK28
TS_GPIO0	A6
TS_GPIO1	B6
TS_PLL_AVDD1P8	K27
TS_PLL_REFCLKN	L26
TS_PLL_REFCLKP	L27
VDD1P8	G8
VDD1P8	G24
VDDC	L11
VDDC	L12

Ball Name	Ball
VDDC	L15
VDDC	L16
VDDC	L19
VDDC	L20
VDDC	M11
VDDC	M12
VDDC	M15
VDDC	M16
VDDC	M19
VDDC	M20
VDDC	N13
VDDC	N14
VDDC	N17
VDDC	N18
VDDC	P13
VDDC	P14
VDDC	P17
VDDC	P18
VDDC	R11
VDDC	R12
VDDC	R15
VDDC	R16
VDDC	R19
VDDC	R20
VDDC	T19
VDDC	T20
VDDC	U14
VDDC	U17
VDDC	U18
VDDC	V13
VDDO1P8	E24
VDDO1P8	F7
VDDO1P8	F9
VDDO1P8	F11
VDDO1P8	F23
VDDO1P8	H23
VDDO3P3	D3
VDDO3P3	D6
VDDO3P3	D9
VDDO3P3	D12
VDDO3P3	D27
VDDO3P3	E26
VDDO3P3	F27
VDDO3P3	G26
VDD_SENSE	R13
VSS_SENSE	R14
XG_MDC0	G1

Ball Name	Ball
XG_MDIO0	G2
XG_MIIM0_VDDO	G4
XG_MIIM0_VDDP	G5
XG_MIIM0_VOLT_SEL	B11
XG_MIIM1_VOLT_SEL	D13
XG_MIIM2_VOLT_SEL	E13
XG_PLL2_AVSS	C22
XG_PLL2_AVSS	D20
XG_PLL2_AVSS	F20
XG_PLL2_AVSS	F21
XG_PLL2_AVDD1P8	D21
XG_PLL2_REFCLKN	C20
XG_PLL2_REFCLKP	C21
XTALN	J2
XTALP	J1
XTAL_AVDD1P8	J3
XTAL_AVSS	H1
XTAL_AVSS	H2
XTAL_AVSS	H3
XTAL_AVSS	H4
XTAL_AVSS	K1
XTAL_AVSS	K2
XTAL_AVSS	K4
XTAL_FREQ_SEL	N28

Section 6: Electrical Characteristics

Operating Conditions

Table 12 shows the recommended operating conditions.

Table 12: Supply Voltage Range

Parameters	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
0.9V +-3%, AVS core voltage	VDDC, TSCx_VDD	0.873	0.9	0.927	V
1.0V +-3%, non-AVS core voltage	VDDC, TSCx_VDD	0.97	1.0	1.03	V
1.0V +-3%, analog voltage	–	0.97	1.0	1.03	V
1.5V +-3%, DDR voltage	–	1.455	1.5	1.545	V
1.8V +-3%, analog voltage	–	1.746	1.8	1.854	V
3.3V +-3%, I/O voltage	–	3.201	3.3	3.399	V
Storage temperature	–	-40	–	125	°C
Ambient temperature	T_a	0	–	70	°C
Junction temperature	T_j	–	–	110	°C
Electrostatic Discharge (ESD) (non-SerDes pins)	V_{ESD}	–	–	–	–
• Human Body Model (HBM) per EIA/JS-001-2012		–	–	±1000	V
• Charge Device Model (CDM) per EIA/JESD22-C101E		–	–	±200	V
ESD (GbE Ports, iProc PCIe, TSC4Q, and TSC SerDes pins)	V_{ESD}	–	–	–	–
• Human Body Model per EIA/JS-001-2012		–	–	±1000	V
• Charge Device Model per EIA/JESD22-C101E		–	–	±200	V
Note: 3% tolerance includes 1% power DC accuracy and 2% AC ripple.					

Maximum Device Power

Table 13 and Table 14 show the maximum power for the BCM53406. Table 15 and Table 16 show the maximum power for the BCM53405. Table 17 and Table 18 show the maximum power for the BCM53402.

Table 13: BCM53406 non-AVS Maximum Power (Tj = 110°C)

Voltage (V)	*Power Rails*	*Current (A)*	*Power (W)*
1.0V + 1%	VDDC, TSCx_VDDC	8.015	8.095
1.0V + 1%	Other 1.0V	2.565	2.591

Table 13: BCM53406 non-AVS Maximum Power (Tj = 110°C)

Voltage (V)	Power Rails	Current (A)	Power (W)
1.5V + 1%	DDR_VDDO	–	–
1.8V + 1%	–	0.142	0.259
3.3V + 1%	–	0.014	0.047
Total			10.992

Table 14: BCM53406 AVS Maximum Power (Tj = 110°C)

Voltage (V)	Power Rails	Current (A)	Power (W)
0.9V + 1%	VDDC, TSCx_VDDC	6.899	6.271
1.0V + 1%	–	2.448	2.472
1.5V + 1%	DDR_VDDO	–	–
1.8V + 1%	–	0.134	0.243
3.3V + 1%	–	0.014	0.047
Total			9.033

Table 15: BCM53405 non-AVS Maximum Power (Tj = 110°C)

Voltage (V)	Power Rails	Current (A)	Power (W)
1.0V + 1%	VDDC, TSCx_VDDC	7.463	7.538
1.0V + 1%	Other 1.0V	1.819	1.837
1.5V + 1%	DDR_VDDO	–	–
1.8V + 1%	–	0.142	0.259
3.3V + 1%	–	0.014	0.047
Total			9.681

Table 16: BCM53405 AVS Maximum Power (Tj = 110°C)

Voltage (V)	Power Rails	Current (A)	Power (W)
0.9V + 1%	VDDC, TSCx_VDDC	6.557	5.961
1.0V + 1%	–	1.737	1.754
1.5V + 1%	DDR_VDDO	–	–
1.8V + 1%	–	0.134	0.243
3.3V + 1%	–	0.014	0.047
Total			8.005

Table 17: BCM53402 non-AVS Maximum Power (Tj = 110°C)

Voltage (V)	Power Rails	Current (A)	Power (W)
1.0V + 1%	VDDC, TSCx_VDDC	5.130	5.181

Table 17: BCM53402 non-AVS Maximum Power (Tj = 110°C)

Voltage (V)	Power Rails	Current (A)	Power (W)
1.0V + 1%	Other 1.0V	0.866	0.875
1.5V + 1%	DDR_VDDO	–	–
1.8V + 1%	–	0.145	0.263
3.3V + 1%	–	0.015	0.049
Total			6.368

Table 18: BCM53402 AVS Maximum Power (Tj = 110°C)

Voltage (V)	Power Rails	Current (A)	Power (W)
0.9V + 1%	VDDC, TSCx_VDDC	4.433	4.029
1.0V + 1%	–	0.841	0.849
1.5V + 1%	DDR_VDDO	–	–
1.8V + 1%	–	0.138	0.250
3.3V + 1%	–	0.014	0.047
Total			5.176

MIIM Electrical Signals

Table 19 shows the MIIM electrical signals.

Table 19: MIIM Electrical Signals

Parameters	Symbol	Min.	Typ.	Max.	Units
Input voltage (Clause 45, when MDIO_VDDO = 1.2V)	VIN	0	–	1.32	V
Input low voltage (Clause 45, when MDIO_VDDO = 1.2V)	VIL	–	–	0.3 × MDIO_VDDO	V
Input high voltage (Clause 45, when MDIO_VDDO = 1.2V)	VIH	0.7 × MDIO_VDDO	–	–	V
Output low voltage (Clause 45, when MDIO_VDDO = 1.2V)	VOL	–	–	0.2	V
Output high voltage (Clause 45, when MDIO_VDDO = 1.2V)	VOH	MDIO_VDDO– 0.2	–	–	V
Input voltage (Clause 22, when MDIO_VDDO = 2.5V)	VIN	0	–	2.75	V
Input low voltage (Clause 22, when MDIO_VDDO = 2.5V)	VIL	–	–	0.7	V
Input high voltage (Clause 22, when MDIO_VDDO = 2.5V)	VIH	1.7	–	–	V
Output low voltage (Clause 22, when MDIO_VDDO = 2.5V)	VOL	–	–	0.4	V
Output high voltage (Clause 22, when MDIO_VDDO = 2.5V)	VOH	MDIO_VDDO– 0.4	–	–	V
Input voltage (Clause 22, when MDIO_VDDO = 3.3V)	VIN	0	–	3.63	V

Table 19: MIIM Electrical Signals (Cont.)

Parameters	Symbol	Min.	Typ.	Max.	Units
Input low voltage (Clause 22, when MDIO_VDDO = 3.3V)	VIL	–	–	0.8	V
Input high voltage (Clause 22, when MDIO_VDDO = 3.3V)	VIH	2	–	–	V
Output low voltage (Clause 22, when MDIO_VDDO = 3.3V)	VOL	–	–	0.4	V
Output high voltage (Clause 22, when MDIO_VDDO = 3.3V)	VOH	MDIO_VDDO–0.4	–	–	V

JTAG Electrical Signals

Table 20 shows the JTAG electrical signals.

Table 20: JTAG Electrical Signals

Parameters	Symbol	Min.	Typ.	Max.	Units
Input voltage	VIN	0	–	3.63	V
Input voltage low	VIL	–	–	0.8	V
Input voltage high	VIH	2	–	–	V
Output voltage low	VOL	–	–	0.4	V
Output voltage high	VOH	VDDO33–0.4	–	–	V

AC-JTAG

The serial interface AC-JTAG characteristics are shown in Table 21.

Table 21: Serial Interface AC-JTAG Characteristics

Parameter	Symbol	Description	Min.	Typ.	Max.	Units
Fault resistance detect	R_{sc}	Short Circuit	0	–	5	Ω
	R_{oc}	Open Circuit	20	–	–	kΩ
Transmit voltage levels	V_{TX}	Differential p-p	0.34	0.44	0.55	V
Transmit data rate	–	EXTEST_TRAIN	1	–	TBD	Mbps
Output resistance	R_{DRV}	DP or DM to VDD	–	50	–	Ω
Transmit supply current	I_{DD}	Operating mode	–	12	–	mA
Receiver input capacitance	C_{IN}	DP or DM to GND	–	0.4	–	pF
Common-mode voltage	V_{CM}	–	–	–	V_{DD}–0.2	V
Comparator hysteresis	V_{HYS}	Peak-to-peak	0	75	90	mV
Receive data rate	–	EXTEST_TRAIN	1	–	TBD	Mbps
Receive supply current	I_{DD}	Operating mode	–	500	–	µA

Table 22 and Table 23 on page 67 show the AC-JTAG settings and the corresponding typical voltages.

Table 22: AC-JTAG Transmit Settings

Transmit AC-JTAG Configuration Driver Bias Current	*Transmit Amplitude (Vppd)*
1111	0.45
1110	0.47
1101	0.48
1100	0.50
1011	0.52
1010	0.53
1001	0.54
1000	0.55
0111	0.34
0110	0.35
0101	0.36
0100	0.38
0011	0.40
0010	0.41
0001	0.43
0000	0.44

Table 23: AC-JTAG Receive Configuration

Receive AC-JTAG Configuration	*RX Hysteresis (mVppd)*
111	65
110	58
101	35
100	20
011	0
010	90
001	80
000	75

LED Electrical Signals

Table 24 shows the LED electrical signals.

Table 24: LED Electrical Signals

Parameters	Symbol	Min.	Typ.	Max.	Units
Output voltage low	VOL	–	–	0.4	V
Output voltage high	VOH	VDDO33–0.4	–	–	V

BSC Electrical Signals

Table 25 shows the BSC electrical signals.

Table 25: BSC Electrical Signals

Parameters	Symbol	Min.	Typ.	Max.	Units
Input voltage low	VIL	–	–	0.8	V
Input voltage high	VIH	2	–	–	V
Output voltage low	VOL	–	–	0.4	V
Output voltage high	VOH	VDDO33–0.4	–	–	V

TSC Electrical Signals

Table 26 shows the 1 Gbps/2.5 Gbps/10 Gbps electrical signals.

Table 26: Electrical Signals

Parameters	Symbol	Min.	Typ.	Max.	Units
Differential input voltage	VIN	85	–	1600	mVppd
Differential input impedance	VRIN	80	100	120	Ω
Differential output voltage	VOD	700	1000	1100	mVppd
Differential output impedance	VROUT	–	100	–	Ω

Table 27: 10Gbps SerDes Specifications

Mode	Spec	Functionality
SerDes Interface		
XFI	XFP MSA	Interchip connection
KR	IEEE 802.3AP	10G backplane
Switch Port Interface		

Table 27: 10Gbps SerDes Specifications

Mode	*Spec*	*Functionality*
XAUI 3.125 Gbaud (8B10B)	IEEE 802.3 CL 47	10G (four lanes)

PCIe Electrical Signals

Table 28 shows the parameters for PCIe electrical signals.

Table 28: PCIe Electrical Signals

Parameters	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
Differential input voltage	VIN	120	–	1000	mVppd
Differential input impedance	VRIN	80	100	120	Ω
Differential output voltage	VOD	800	–	1200	mVppd
Differential output impedance	VROUT	80	100	120	Ω

Power Sequencing

As is common in multiple-supply devices, the power supply pins may sink or source large amounts of current when a given supply is powered up while another is powered down. This may also be the case when supplies are partially powered at intermediate voltage levels (such as when the 3.3V supply has ramped to 2.0V while the 1.0V supply is at 0.5V). This current is due to ESD diode paths and other supply-related current paths in the device.

In some cases, the power-up current may be on the order of several amps. This current will not damage the device, but it may affect the power supply or other related components. Supplies that are not fully powered may be pulled up (a voltage potential observed on the pins) during this time. In addition, the high start-up current may cause damage to other board components (that is, the external transistor on a switching regulator if it is unable to support the current load).

Broadcom recommends that all power supplies ramp up from 0V to their full voltages within 5 ms (t2 and t3 in Figure 9). In addition, they must sequence from the I/O power (3.3V/2.5V/1.8V/1.2V) to the core power (1.0V). See Figure 9. The power up delay between I/O power and core power should be less than 5 ms (t1 in Figure 9). Besides, the core power should be OFF until the I/O power reaches at least 0.8V. The switching regulator must be selected in such a way that it can process the high current during power-up, or that it can limit the supply current while still ramping the supplies.

I/O states are not guaranteed when the I/O supplies are ramped before the CORE supply. Ramping in this order causes no known problems, but can result in bus contention and elevated current. This can be minimized by ramping the supplies simultaneously or rapidly or both.

There is no specific power-off sequence. Either turning off I/O power or core power first is okay. The only requirement for power-off timing is the delay time between I/O power and core power. The delay time should be less than 5 ms.

Figure 9: Power and Reset Sequence

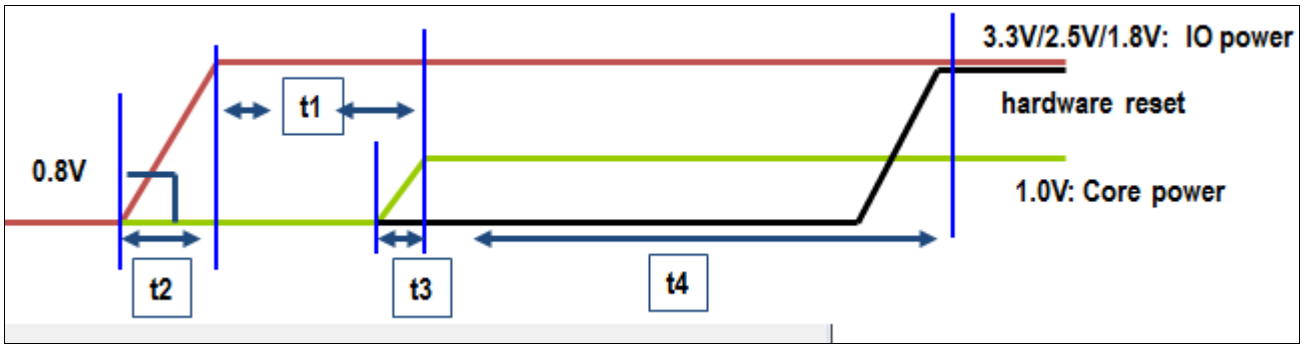


Table 29: Power Sequence Timing

Parameter	*Min.*	*Max.*	*Units*
t1	–	5.0	ms
t2 for 3.3V	0.66	5.0	ms
t2 for 2.5V	0.50	5.0	ms
t2 for 1.8V	0.36	5.0	ms
t3	0.05	5.0	ms
t4	100.0	–	ms

Section 7: AC Timing Characteristics

AC Characteristics

AC Timing for Reset

The SYS_RST_L signal is synchronized internal to the IC and, as such, asynchronous assertion and deassertion are acceptable.

BSC AC Characteristics

The BSC interface can be operated in two modes:

- Slave mode
- CPU-controlled master/slave mode

The external master drives BSC_SDA during a write operation and samples BSC_SDA during a read operation.

Figure 10: BSC Timing Diagram

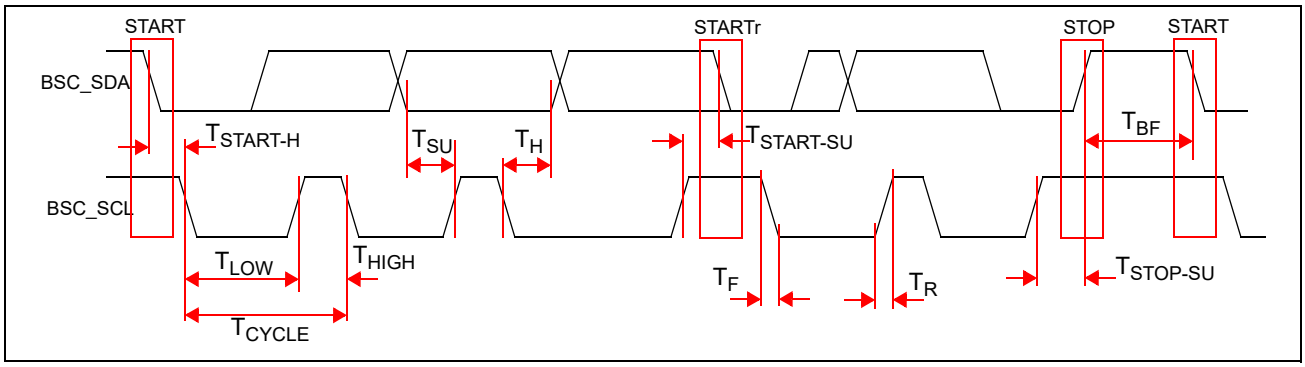


Table 30: BSC Master/Slave Fast-Mode Timing

Parameter	Symbol	Min.	Typ.	Max.	Units
BSC_SCL Cycle Time	T_{CYCLE}	2.5	–	–	µs
BSC_SCL Low Time	T_{LOW}	1.3	–	–	µs
BSC_SCL High Time	T_{HIGH}	0.6	–	–	µs
Data Hold Time	T_{H}	0	–	–	µs
Data Setup Time	T_{SU}	100	–	–	ns
Rise Time, Clock and Data (See Note)	T_{R}	–	–	300	ns
Fall Time, Clock and Data (GBD)	T_{F}	–	–	300	ns
Hold Time, START or repeated START	$T_{START–H}$	0.6	–	–	µs
Setup Time, repeated START	$T_{START–SU}$	0.6	–	–	µs
Setup Time, STOP	$T_{STOP–SU}$	0.6	–	–	µs
Bus Free Time (Between STOP and START)	T_{BF}	1.3	–	–	µs

Table 31: BSC Master/Slave Standard-Mode Timing

Parameter	Symbol	Min.	Typ.	Max.	Units
BSC_SCL Cycle Time	T_{CYCLE}	10	–	–	µs
BSC_SCL Low Time	T_{LOW}	4.7	–	–	µs
BSC_SCL High Time	T_{HIGH}	4	–	–	µs
Data Hold Time	T_{H}	0	–	–	µs
Data Setup Time	T_{SU}	250	–	–	ns
Rise Time, Clock and Data (See Note)	T_{R}	–	–	1000	ns
Fall Time, Clock and Data (GBD)	T_{F}	–	–	300	ns
Hold Time, START or repeated START	$T_{START–H}$	4	–	–	µs
Setup Time, repeated START	$T_{START–SU}$	4.7	–	–	µs
Setup Time, STOP	$T_{STOP–SU}$	4	–	–	µs
Bus Free Time (Between STOP and START)	T_{BF}	4.7	–	–	µs

Note: BSC_SCL and BSC_SDA are open-drain outputs. The rise time is dependent on the strength of the external pull-up resistor, which should be chosen to meet the rise time requirement.

The BCM5340X device drives the BSC_SCL clock, with a programmable speed of 100 kHz or 400 kHz based on the mode bit called MODE_400. The BCM5340X drives BSC_SDA during a write operation and samples BSC_SDA during a read operation.

SPI AC Characteristics

The SPI interface can be operated in two modes:

- Master mode
- Slave mode

Figure 11: SPI Interface Master Mode Timing Diagram

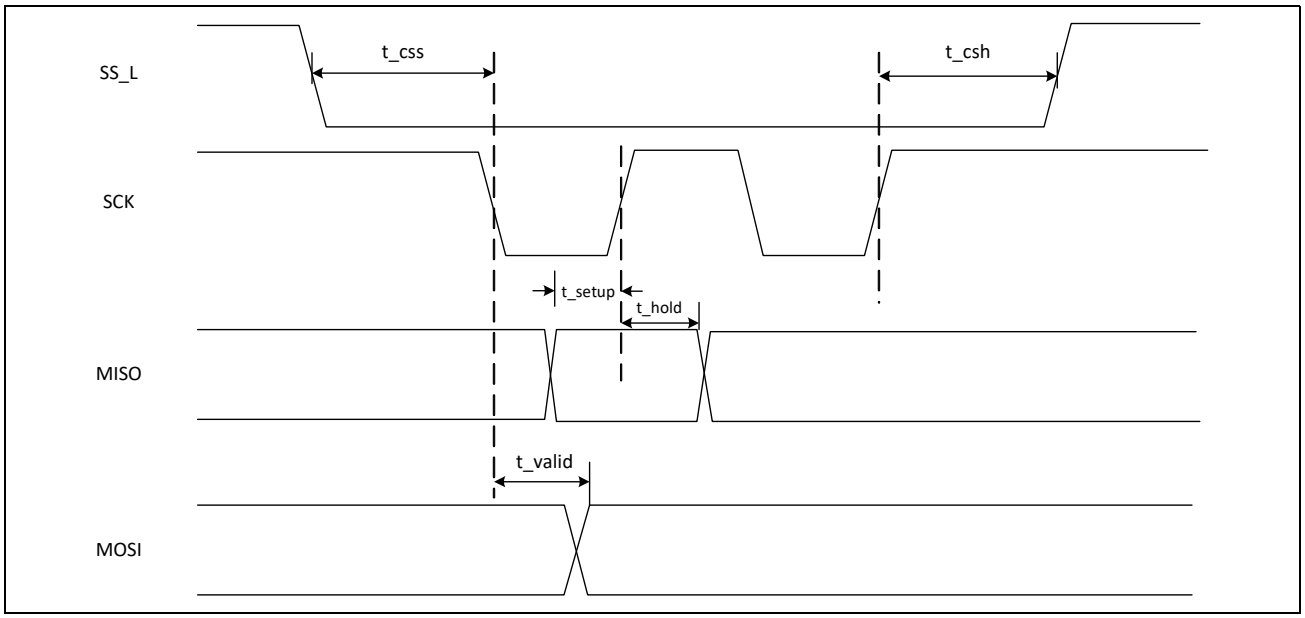


Table 32: SPI Master Mode Timing

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
SCK Cycle Time	T_{CYCLE}	64	–	–	ns
SS_L Output Setup Time	t_css	–	$T_{CYCLE}/2$	–	ns
SS_L Output Hold Time	t_csh	20	–	–	ns
MOSI Valid Time	t_valid	–	–	20	ns
MISO Setup Time	t_setup	12	–	–	ns
MISO Hold Time	t_hold	12	–	–	ns

Figure 12: SPI Interface Slave Mode Timing Diagram

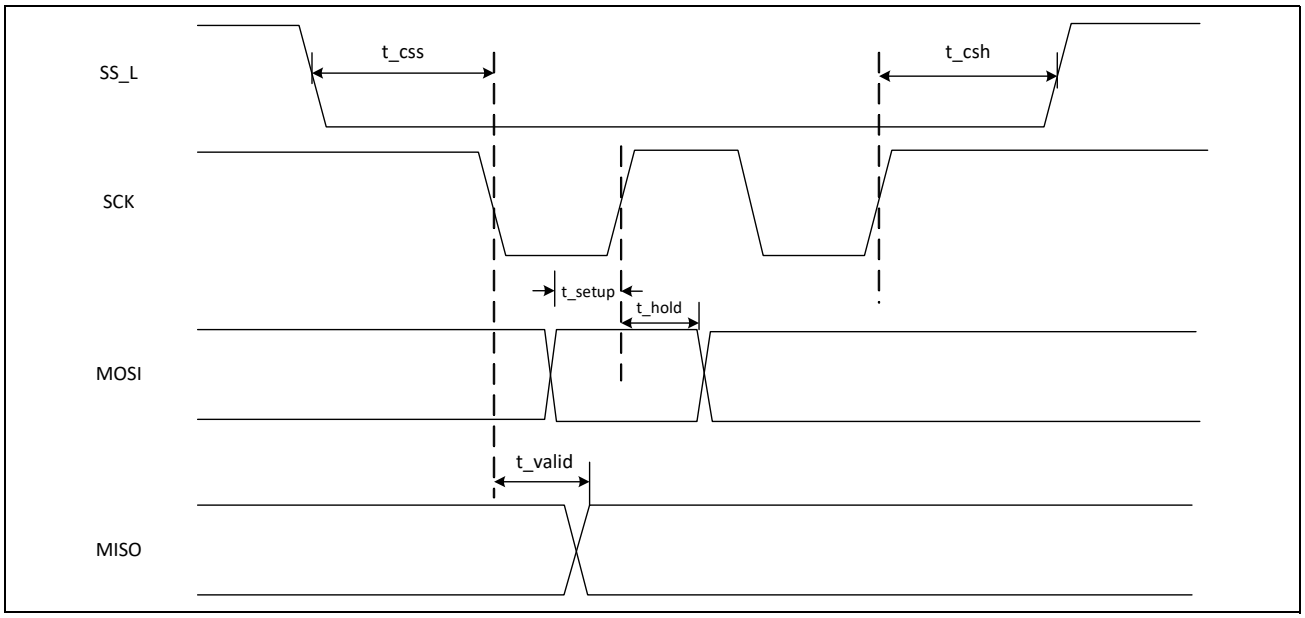


Table 33: SPI Slave Fast Mode Timing

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
SCK Cycle Time	T_{CYCLE}	32	–	–	ns
SS_L Setup Time	t_css	7	–	–	ns
SS_L Hold Time	t_csh	0.5	–	–	ns
MOSI Setup Time	t_setup	7	–	–	ns
MOSI Hold Time	t_hold	0.5	–	–	ns
MISO Valid Time	t_valid	–	–	9	ns

MDIO AC Characteristics

Figure 13: MIIM Interface Timing Diagram

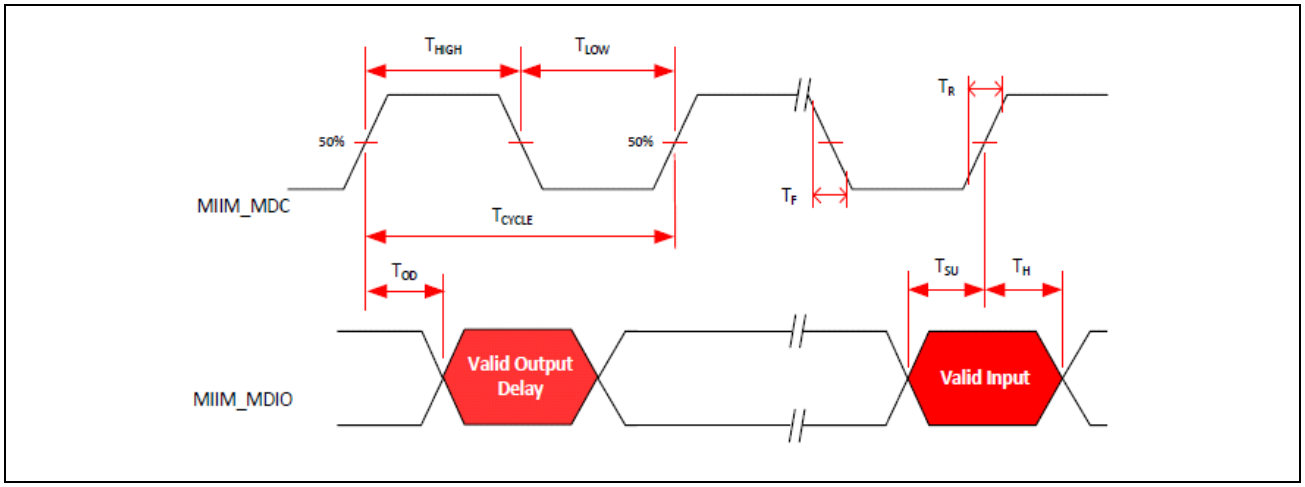


Table 34: MDC/MDIO Timing

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
MDC Cycle Time	T_{CYCLE}	80	400	–	ns
MDC Duty Cycle	–	40	–	60	%
MDC Rise/Fall Time (Requirement 20%–80%)	T_R, T_F	–	–	10	ns
MDIO Setup Time	T_S	20	–	–	ns
MDIO Hold Time	T_H	0	–	–	ns
MDIO Output Delay	T_{OD}	10	–	30	ns

JTAG AC Specifications

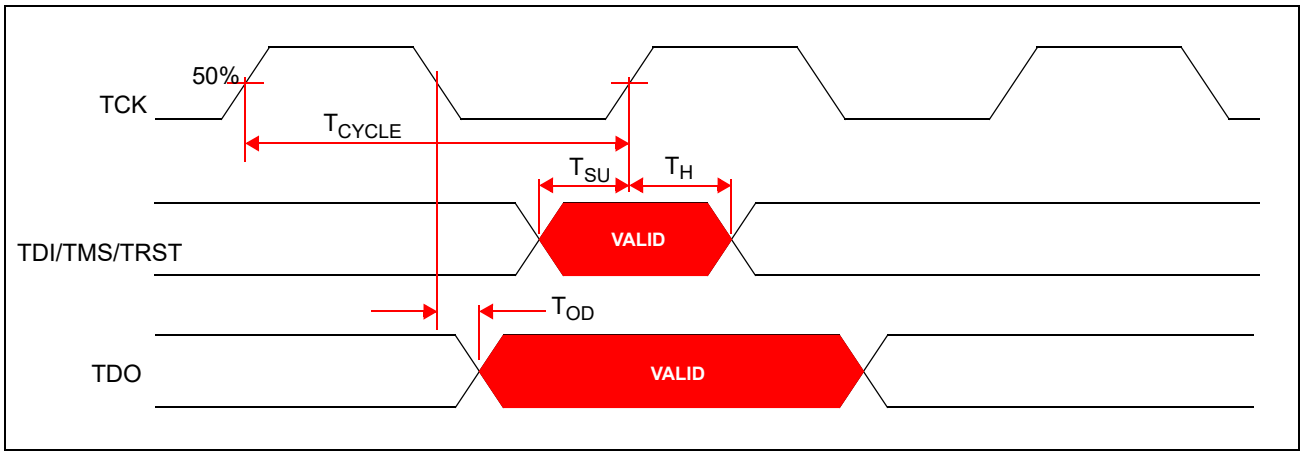
Table 35: AC Characteristics for JTAG

Parameter	Symbol	Min.	Typ.	Max.	Unit
j_tck cycle time	t_{CYCLE}	80.0	–	–	ns
j_tck falling edge to output valid. Applicable to j_tdo.	t_{OD}	0	–	25	ns
Data input setup time before j_tck. Applicable to j_tdi and j_tms.	t_{SU_JT}	15	–	–	ns
Data hold time after j_tck rise Applicable to j_tdi and j_tms.	t_{H_JT}	5	–	–	ns

Note: Unless otherwise noted, the specifications are valid across the following operating conditions:

- The threshold value is at 50% of the applicable I/O rail voltage.
- The default loading on an output is 5 pF.

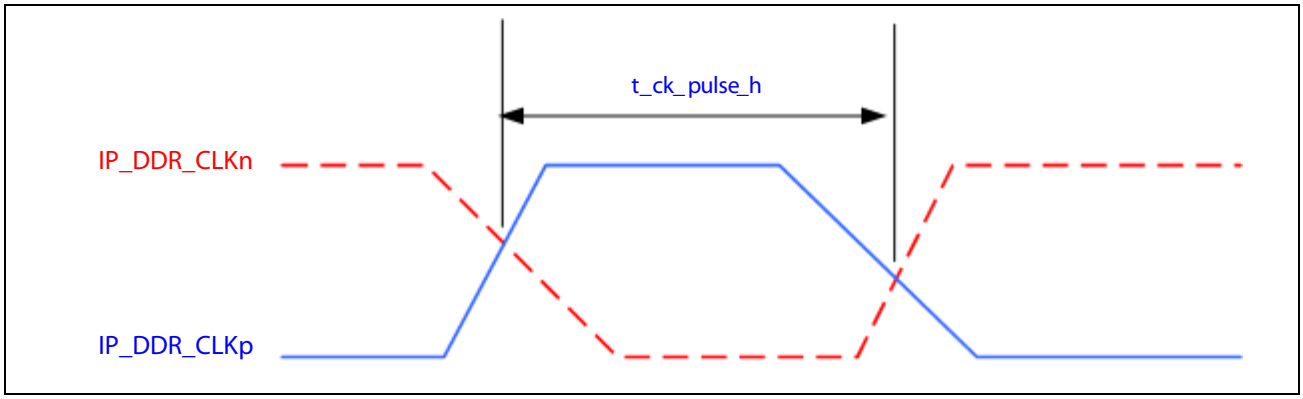
Figure 14: JTAG Timing



DDR3 Interface AC Specifications

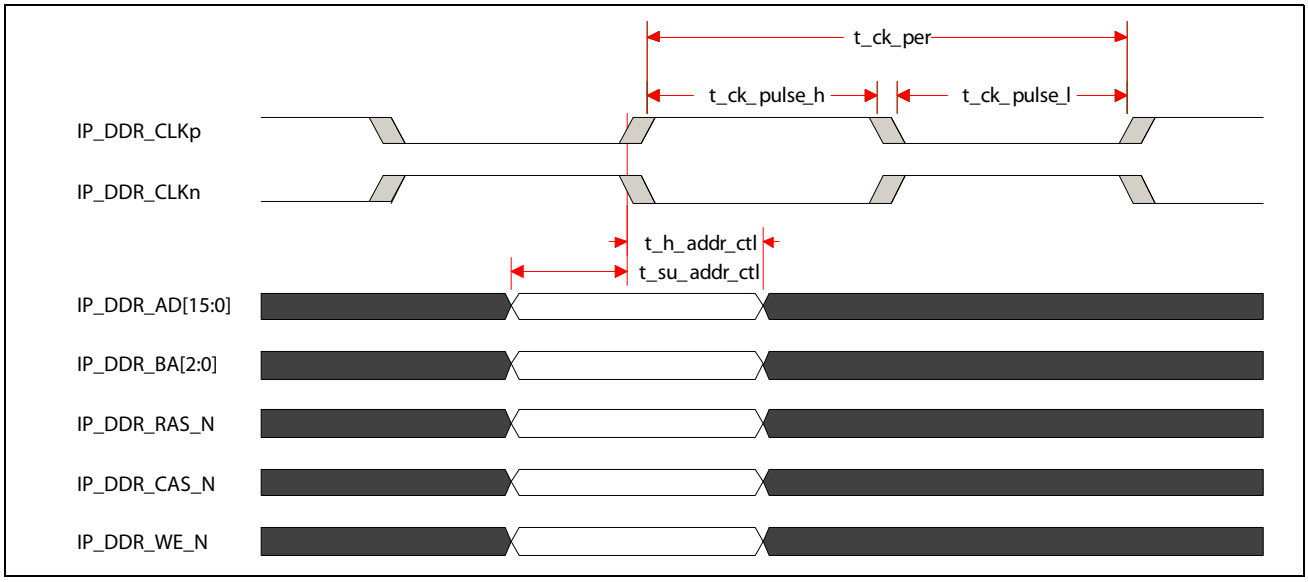
All parameters with respect to IP_DDR_CLK_P rising (IP_DDR_CLK_N falling) are specified relative to the common voltage crossing of the differential pair, as illustrated in Figure 15.

Figure 15: DDR3 CLK Differential Crossing Timing Example



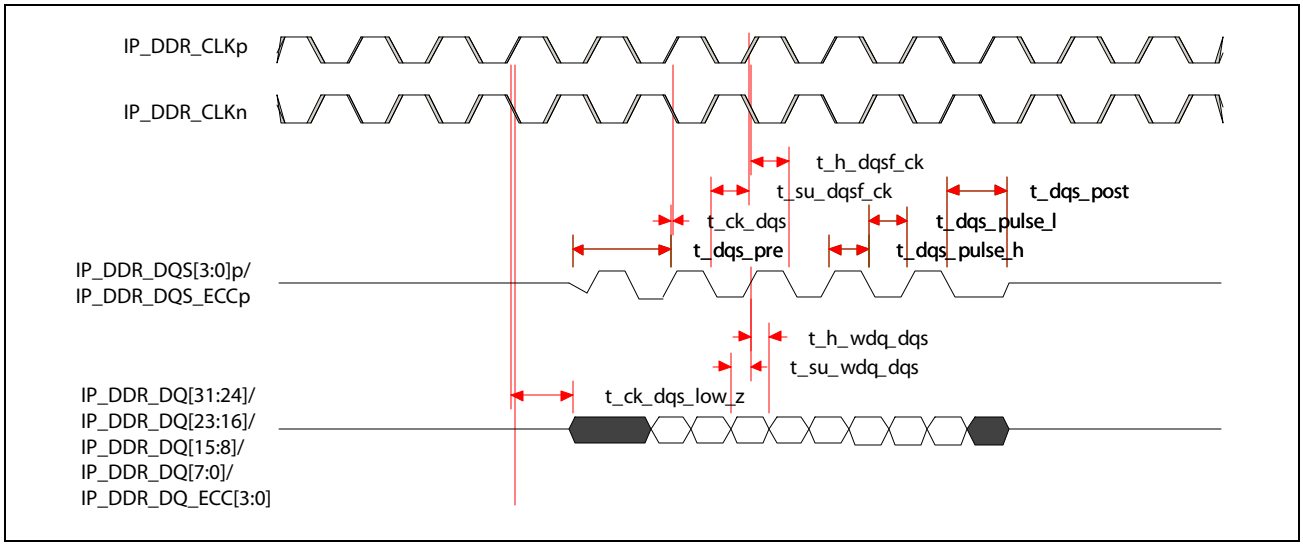
DDR3 Address and Control Timing

Figure 16: DDR3 Address and Control Timing



DDR3 Write Timing

Figure 17: DDR3 Write Timing



DDR3 Read Timing

Figure 18: DDR3 Read Timing

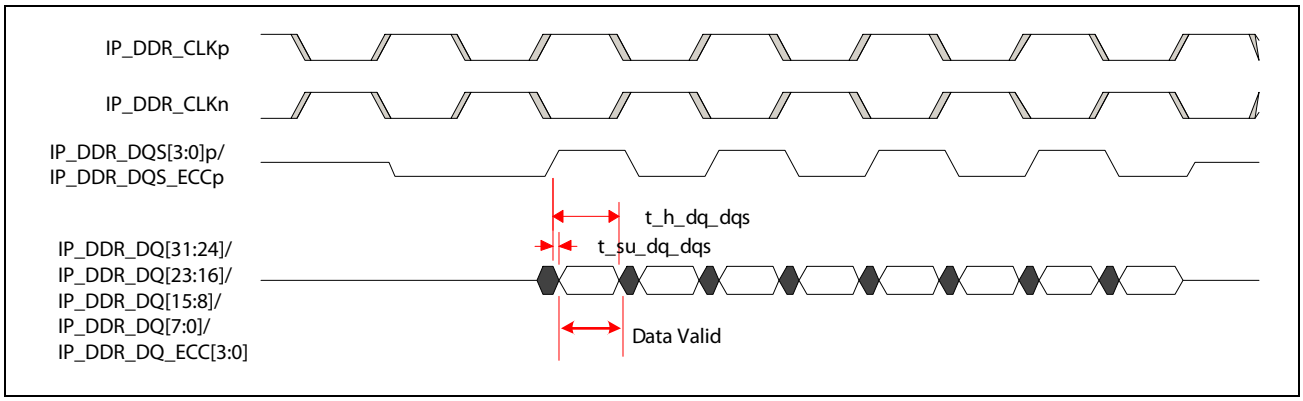


Table 36: AC Specifications for the DDR3-1333 Interface [ab]

Symbol	Parameter [c]	Min[d].	Max.	Units
Address and Control Timing				
t_ck_jitter	CLK Jitter: IP_DDR_CLK_P rising (IP_DDR_CLK_N falling) cycle-to-cycle jitter	–	±0.080	ns
t_ck_per	CLK Period	1.5	–	ns
t_ck_pulse_h	IP_DDR_CLK_P high (IP_DDR_CLK_N low) minimum pulse width	0.47	0.53	t_ck_per
t_ck_pulse_l	IP_DDR_CLK_P low (IP_DDR_CLK_N high) minimum pulse width	0.47	0.53	t_ck_per
t_su_addr_ctl	Address and Control Setup: time that outputs are valid before IP_DDR_CLK_P rising (IP_DDR_CLK_N falling)	190	–	ps
t_h_addr_ctl	Address and Control Hold: time that outputs remain valid after IP_DDR_CLK_P rising (IP_DDR_CLK_N falling)	140	–	ps
Write Timing				
t_ck_dqs	CLK to DQS delay from IP_DDR_CLK_P rising (IP_DDR_CLK_N falling) to IP_DDR_DQS[1:0]_P rising	–0.25	+0.25	t_ck_per
t_su_dqsf_ck	DQS Fall to CLK Rise Setup: delay from IP_DDR_DQS[1:0]_P falling to IP_DDR_CLK_P rising (IP_DDR_CLK_N falling)	0.2	–	t_ck_per
t_h_dqsf_ck	DQS Fall to CLK Rise Hold: delay from IP_DDR_CLK_P rising (IP_DDR_CLK_N falling) to IP_DDR_DQS[1:0]_P falling	0.2	–	t_ck_per
t_dqs_pulse_h	IP_DDR_DQS[1:0]_P high minimum pulse width	0.45	0.55	t_ck_per
t_dqs_pulse_l	IP_DDR_DQS[1:0]_P low minimum pulse width	0.45	0.55	t_ck_per
t_dqs_pre	DQS Preamble: time from tristate-to-low to first rising edge of IP_DDR_DQS[1:0]_P	0.9	–	t_ck_per
t_dqs_post	DQS Postamble: time from last falling edge of IP_DDR_DQS[1:0]_P to tristate	0.3	–	t_ck_per
t_dq_pulse	IP_DDR_DQ[15:0] minimum data valid width	400	–	ps
t_su_wdq_dqs	DQ to DQS Write Setup: time from IP_DDR_DQ[15:8]/IP_DDR_DQ[7:0] output valid to rising or falling edge of IP_DDR_DQS[1:0]_P	30	–	ps
t_h_wdq_dqs	DQ to DQS Write Hold: time IP_DDR_DQ[15:8]/ IP_DDR_DQ[7:0] remains valid after rising or falling edge of IP_DDR_DQS[1:0]_P	65	–	ps
t_ck_dqs_low_z	CLK to DQS LowZ: time from IP_DDR_CLK_P rising (IP_DDR_CLK_N falling) to IP_DDR_DQS[1:0]_P tristate-to-low-z	–500	250	ps

Table 36: AC Specifications for the DDR3-1333 Interface (Cont.)[ab]

Symbol	Parameter [c]	Min[d].	Max.	Units
Read Timing				
t_su_dq_dqs	DQ to DQS Read Setup[e]: time that IP_DDR_DQ[15:8]/IP_DDR_DQ[7:0] must be valid before the rising or falling edge of IP_DDR_DQS[1:0]_P	NA	–	ps
t_h_dq_dqs	DQ to DQS Read Hold: time that IP_DDR_DQ[15:8]/ IP_DDR_DQ[7:0] must remain valid after the rising or falling edge of IP_DDR_DQS[1:0]_P	0.3	–	t_ck_per

a. All values in the table reflect 50% voltage level timing. Timing shown with 1/4 cycle vdl settings at 667 MHz.
b. All the input signals must meet electrical specifications i.e VIH/VIL & SR specifications.
c. All values in the table reflect Static Timing Analysis (STA) constraints.
d. All STA outputs were timed into a 5 pF standard load.
e. DQ and DQS are nominally aligned. The DQS signal is internally delayed to sample relevant DQ data at the middle of the valid DQ window.

Table 37: AC Specifications for the DDR3-1600 Interface

Symbol	Parameter	Min.	Max.	Units
Address and Control Timing				
t_ck_jitter	CLK Jitter: IP_DDR_CLK_P rising (IP_DDR_CLK_N falling) cycle-to-cycle jitter	–70	70	ns
t_ck_per	CLK Period	1.25	–	ns
t_ck_pulse_h	IP_DDR_CLK_P high (IP_DDR_CLK_N low) minimum pulse width	0.47	0.53	t_ck_per
t_ck_pulse_l	IP_DDR_CLK_P low (IP_DDR_CLK_N high) minimum pulse width	0.47	0.53	t_ck_per
t_su_addr_ctl	Address and Control Setup: time that outputs are valid before IP_DDR_CLK_P rising (IP_DDR_CLK_N falling)	170	–	ps
t_h_addr_ctl	Address and Control Hold: time that outputs remain valid after IP_DDR_CLK_P rising (IP_DDR_CLK_N falling)	120	–	ps
Write Timing				
t_ck_dqs	CLK to DQS delay from IP_DDR_CLK_P rising (IP_DDR_CLK_N falling) to IP_DDR_DQS[3:0]P rising	–0.27	0.27	t_ck_per
t_su_dqsf_ck	DQS Fall to CLK Rise Setup: delay from IP_DDR_DQS[3:0]P falling to IP_DDR_CLK_P rising (IP_DDR_CLK_N falling)	0.18	–	t_ck_per
t_h_dqsf_ck	DQS Fall to CLK Rise Hold: delay from IP_DDR_CLK_P rising (IP_DDR_CLK_N falling) to IP_DDR_DQS[3:0]P falling	0.18	–	t_ck_per
t_dqs_pulse_h	IP_DDR_DQS[3:0]P high minimum pulse width	0.45	0.55	t_ck_per
t_dqs_pulse_l	IP_DDR_DQS[3:0]P low minimum pulse width	0.45	0.55	t_ck_per
t_dqs_pre	DQS Preamble: time from tristate-to-low to first rising edge of IP_DDR_DQS[3:0]P	0.9	–	t_ck_per
t_dqs_post	DQS Postamble: time from last falling edge of IP_DDR_DQS[3:0]P to tristate	0.3	–	t_ck_per
t_dq_pulse	IP_DDR_DQ[31:0] minimum data valid width	360	–	ps
t_su_wdq_dqs	DQ to DQS Write Setup: time from IP_DDR_DQ[31:24]/ IP_DDR_DQ[23:16]/IP_DDR_DQ[15:8]/IP_DDR_DQ[7:0] output valid to rising or falling edge of IP_DDR_DQS[3:0]P	10	–	ps
t_h_wdq_dqs	DQ to DQS Write Hold: time IP_DDR_DQ[31:24]/ IP_DDR_DQ[23:16]/IP_DDR_DQ[15:8]/IP_DDR_DQ[7:0] remains valid after rising or falling edge of IP_DDR_DQS[3:0]P	45	–	ps
t_ck_dqs_low_z	CLK to DQS Low Z: time from IP_DDR_CLK_P rising (IP_DDR_CLK_N falling) to IP_DDR_DQS[3:0]P tristate-to-low-Z	–450	225	ps
Read Timing				
t_su_dq_dqs	DQ to DQS Read Setup: time that IP_DDR_DQ[31:24]/ IP_DDR_DQ[23:16] /IP_DDR_DQ[15:8]/IP_DDR_DQ[7:0] must be valid before the rising or falling edge of IP_DDR_DQS[3:0]P	NA	–	ps
t_h_dq_dqs	DQ to DQS Read Hold: time that IP_DDR_DQ[31:24]/ IP_DDR_DQ[23:16]/IP_DDR_DQ[15:8]/IP_DDR_DQ[7:0] must remain valid after the rising or falling edge of IP_DDR_DQS[3:0]P	0.38	–	t_ck_per
Data Valid	Read data valid window for all DQ clocked by internal 90-degree shifted DQS signal	–	–	ps

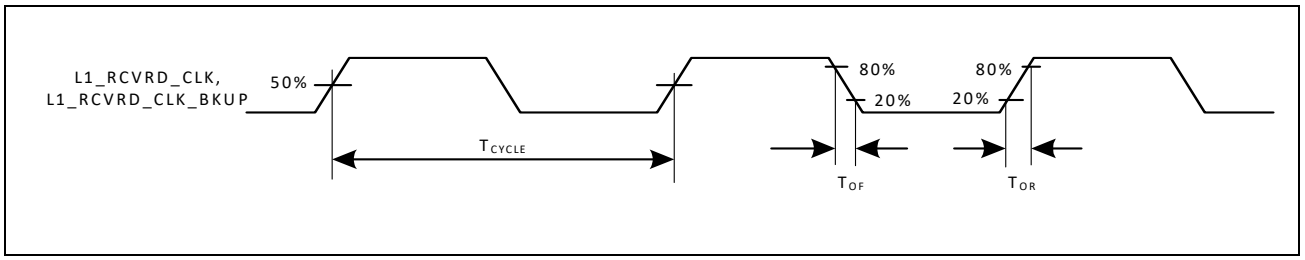
Synchronous Ethernet Interface Timing

L1_RCVRD_CLK and L1_RCVRD_CLK_BKUP Output Timing

Table 38: L1_RCVRD_CLK and L1_RCVRD_CLK_BKUP Output Timing

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
L1_RCVRD_CLK, L1_RCVRD_CLK_BKUP Cycle Time	T_{CYCLE}	6.4	–	40	ns
L1_RCVRD_CLK, L1_RCVRD_CLK_BKUP Duty Cycle	T_{HIGH}	45	–	55	%
L1_RCVRD_CLK, L1_RCVRD_CLK_BKUP Rise Time from 20% to 80%	T_{OR}	–	–	–	ns
L1_RCVRD_CLK, L1_RCVRD_CLK_BKUP Fall Time from 20% to 80%	T_{OF}	–	–	–	ns

Figure 19: Synchronous Ethernet Output Timing Diagram



QSPI Flash Interface Timing

QSPI BSPI Mode

The QSPI interface operates as a Master, allowing access to an external SPI Flash or EEPROM from which the microcontroller boot code can be loaded.

Figure 20: QSPI BSPI Mode Master Interface Timing

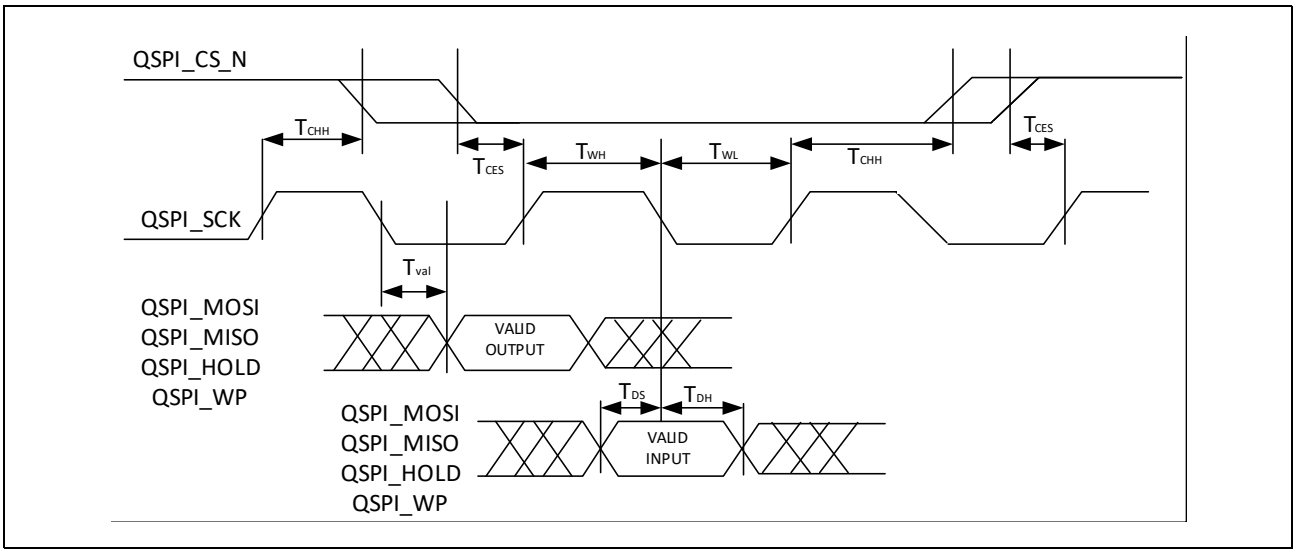


Table 39: QSPI BSPI Mode Master Interface Timing Specifications

Parameters	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
QSPI Clock Frequency[a]	F_{CLK}	–	62.5	62.5	MHz
QSPI Clock Cycle Time	T_{CK}	–	$1/F_{CLK}$	–	ns
QSPI Clock High Time	T_{WH}	$0.4T_{CK}$	–	$0.6T_{CK}$	ns
QSPI Clock Low Time	T_{WL}	$0.4T_{CK}$	–	$0.6T_{CK}$	ns
Chip Select (QSPI _CS_N) Output Setup Time	T_{CES}	5	–	–	ns
Chip Select (QSPI_CS_N) Output Hold Time	T_{CHH}	5	–	–	ns
Data Out (QSPI_MOSI) Valid Time	T_{Val}	–3	–	4	ns
Data In (QSPI_MISO) Setup Time	T_{DS}	4	–	–	ns
Data In (QSPI_MISO) Hold Time	T_{DH}	1	–	–	ns
Rise Time[b]	T_R	–	–	1.5	ns
Fall Time[b]	T_F	–	–	1.5	ns

a. QSPI BSPI mode is used for initial code download when IP_BOOT_DEV = 3'b000 and read operations during runtime. The frequency is set to a reset default value of 25 MHz through CRU_CONTROL_QSPI_CLK_SEL. When register access is established, the same register can be written to change the QSPI interface frequency to a value of 25 MHz, 31.25 MHz, 50 MHz, or 62.5 MHz.

b. This parameter only applies to the output signals.

QSPI MSPI Mode

The QSPI interface can run in MSPI mode, which is working as an SPI master mode.

Figure 21: QSPI MSPI Mode Master Interface Timing

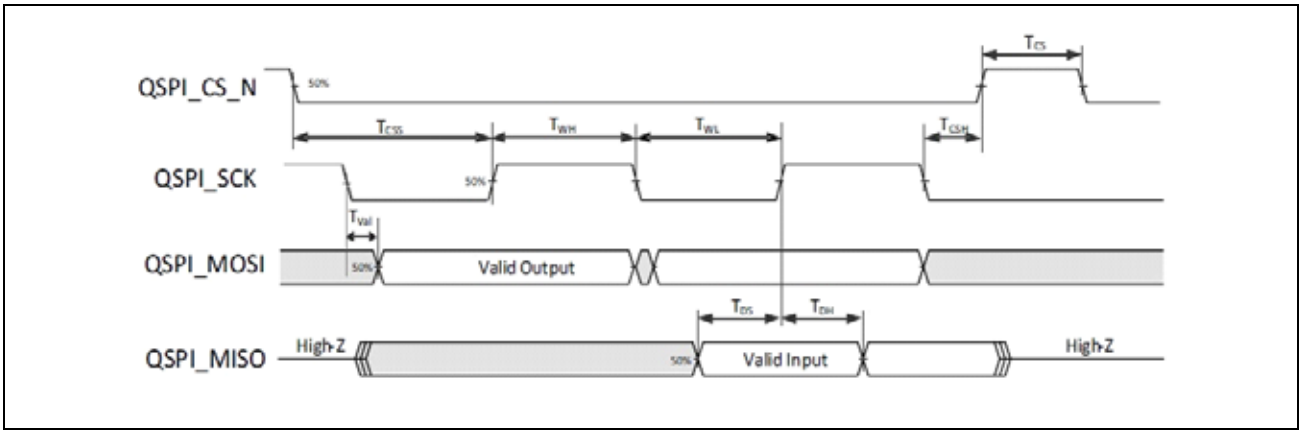


Table 40: QSPI MSPI Mode Master Interface Timing

Parameter	Symbol	Min.	Typ.	Max.	Units
QSPI Clock Frequency[a]	F_{CLK}	–	–	12.5	MHz
QSPI Clock Cycle Time	T_{CK}	–	$1/F_{CLK}$	–	ns
QSPI Clock High time	T_{WH}	$0.4T_{CK}$	–	$0.6T_{CK}$	ns
QSPI Clock Low time	T_{WL}	$0.4T_{CK}$	–	$0.6T_{CK}$	ns
Chip Select (QSPI_CS_N) Output Setup time	T_{CSS}	–	$T_{CK}/2$	–	ns
Chip Select (QSPI_CS_N) Output HOLD time	T_{CSH}	25	–	–	ns
Data Out (QSPI_MOSI) Valid time	T_{Val}	0	–	$0.225T_{CK}$	ns
Data In (QSPI_MISO) Setup time	T_{DS}	12	–	–	ns
Data In (QSPI_MISO) Hold time	T_{DH}	12	–	–	ns
Rise Time[b] (20% to 80%)	T_R	–	–	1.5	ns
Fall Time[b] (20% to 80%)	T_F	–	–	1.5	ns

a. QSPI MSPI mode is typically used during runtime whenever write or erase operation are required.
b. This parameter applies to the output signals only.

PCIe Interface Timing

PCIE_REFCLK Timing

Figure 22: PCIE_REFCLK Timing

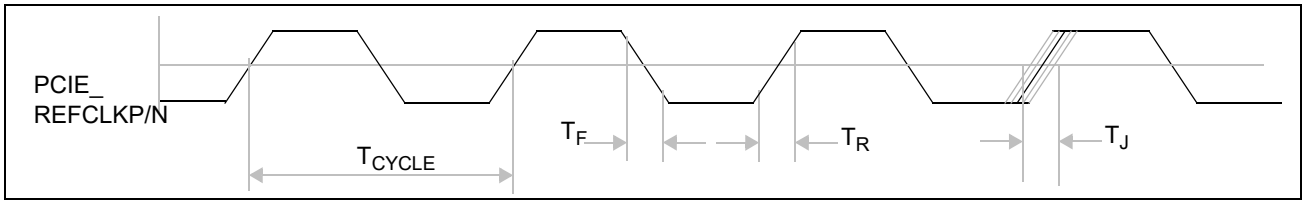


Table 41: PCIE_REFCLK (HCSL)

Parameters	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
Frequency ($1/T_{CYCLE}$)	FREQ	–	100	–	MHz
Tolerance	TOL	–50	–	+50	ppm
Amplitude (Differential pk-pk)	VID	0.30	–	1.6	Vp-p
Duty Cycle	T_h/T_l	40	50	60	%
Rise/Fall Time	T_R/T_F	0.6	–	4.0	ns
Jitter RMS Max (10 kHz–1.5 MHz) for Gen2 5.0 Gbps Operation	T_J	–	–	3.0	ps
Cycle-to-Cycle Jitter for Gen1 2.5 Gbps Operation	–	–	–	150	ps

Note:

- AC-coupled externally.
- Internal termination.
- Series and pull-down termination externally.
- VIH HCSL 660 min 850 max mV (Single ended)
- VIL HCSL -150 min 0 max mV (Single ended)

PCIe_RX Timing

Figure 23: PCIe_RX Timing

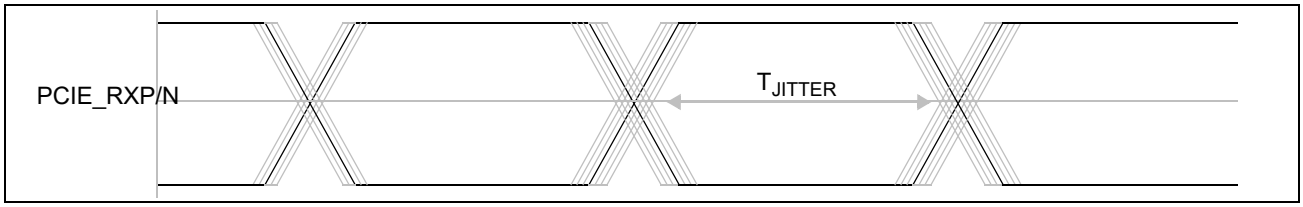


Table 42: PCIe_RX

Parameters	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
Baud Rate	FREQ	–	2.5 or 5.0	–	Gbaud
Input Impedance (Differential)	RIN	80	100	120	Ω
Input Voltage (Differential pk-pk)	VID	120	–	1000	mVp-p
Jitter Tolerance (Min Rx EYE width)	T_J	0.4	–	–	UI

PCIe_TX Timing

Figure 24: PCIe_TX Timing

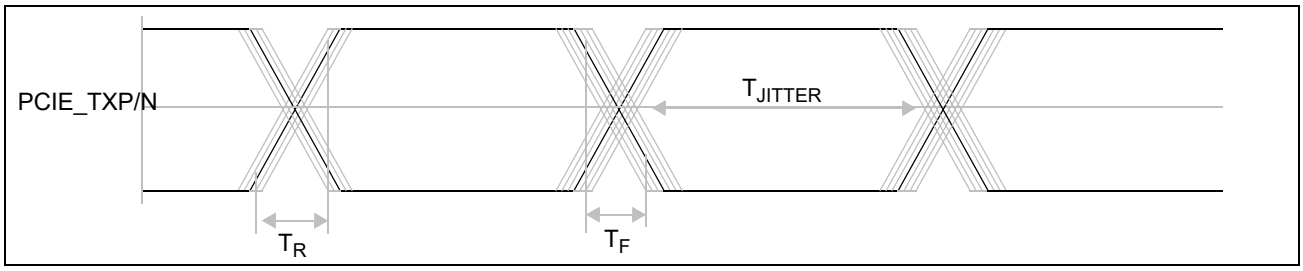


Table 43: PCIe_TX

Parameters	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Units*
Baud Rate	FREQ	–	–	2.5 or 5.0	–	Gbaud
Output Impedance (Differential)	R_{OUT}	–	80	100	120	Ω
Output Voltage (Differential pk-pk)	V_{OD}	–	800	1000	1200	mVp-p
Output Rise/Fall Time (20%–80%)	T_R/T_F	–	0.125	–	–	UI
Output De-Emphasis[a]	V_{OEQ}	Gen1 2.5 Gbps	–3.0	–3.5	–4.0	dB
		Gen1 5.0 Gbps	–5.5	–6.0	–6.5	
Rise/Fall Time (20%–80%)	T_R/T_F	Gen1 2.5 Gbps	0.125	–	–	ns
		Gen1 5.0 Gbps	0.150	–	–	
Jitter (min Tx EYE width)	T_J	–	0.75	–	–	UI

a. Output Deemphasis figures listed in this table are the default settings. TX Deemphasis can be software configured in the range of 0–8 dB, overriding the defaults.

LED Controller Interface

LED_CLK and LED_DATA are outputs. LED_CLK output clock period is 200 ns (5.0 MHz).

Figure 25: LED Timing Diagram

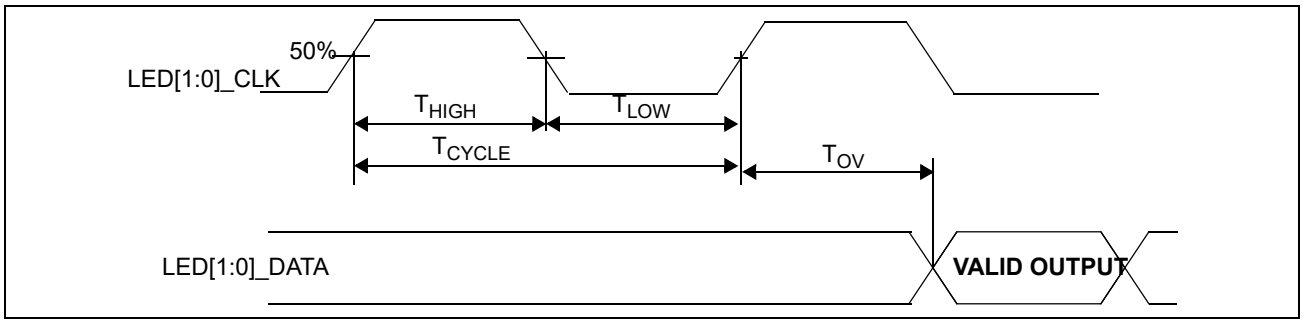


Table 44: LED Timing[a]

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
LED_CLK Cycle Time	T_{CYCLE}	–	200	–	ns
LED_CLK High Time	T_{HIGH}	70	100	130	ns
LED_CLK Low Time	T_{LOW}	70	100	130	ns
LED_DATA Output Valid Time	T_{OV}	0	–	20	ns

a. Timing figures are specified at the 50% crossing thresholds.

XTAL Clock Requirements

The Master clock (XTALP/XTALN) when driven by external oscillator requires a 25 or 50 MHz differential source with characteristics shown in Figure 26 and meets requirements outlined in Table 45.

Figure 26: XTALP/XTALN Input Timing Diagram

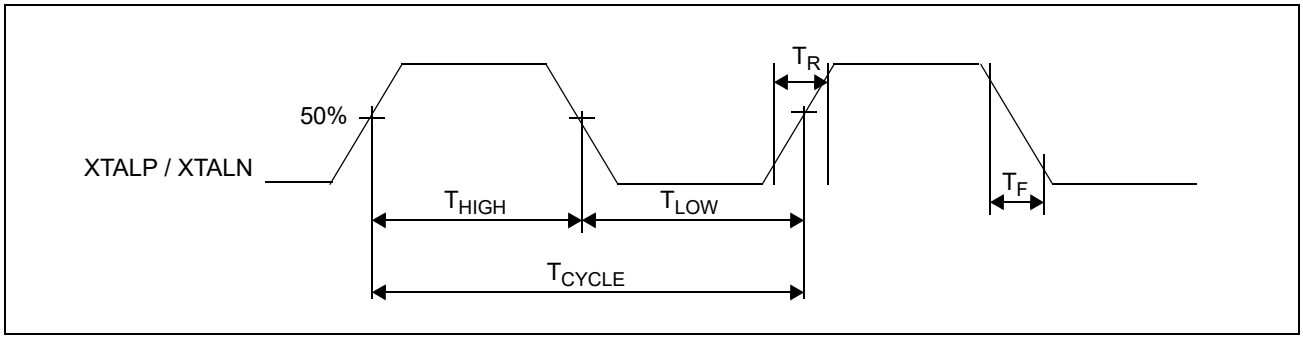


Table 45: XTALP/XTALN Input Requirements

Requirement	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
XTALP/XTALN Frequency	–	–	25 or 50	–	MHz
XTALP/XTALN Accuracy	–	–50	–	+50	ppm
XTALP/XTALN Duty Cycle	–	45	–	55	%
Input Voltage Range (differential clock)	VIN	800	–	1800	mVpp diff
Input Voltage (single-ended)	V_{IH}	1.4	–	1.89	V
Single-end clock Rise/Fall Time (20% to 80%)	$T_{R,}$ T_F	–	–	0.5	ns
XTALP/XTALN Jitter RMS Max (10 kHz to 5 MHz)	–	–	–	0.5	ps

Note:

- AC-coupled externally.
- Need external 100Ω termination when differential clock source is used.

LC_PLL1_REFCLK Clock Requirements

The Warpcore Technology clocks (LC_PLL1_REFCLKP/N) each require 156.25 MHz differential source with characteristics shown in Figure 27.

Figure 27: LC_PLL1_REFCLKP/N Input Timing Diagram

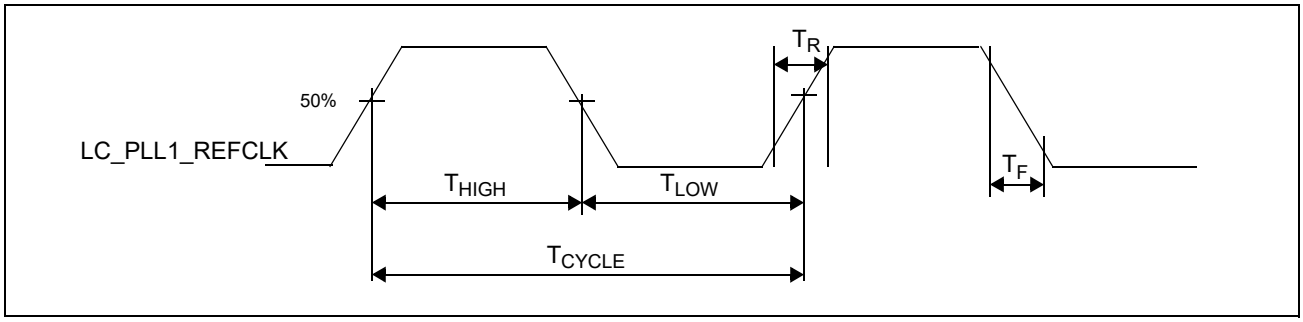


Table 46: LC_PLL1_REFCLK Input Requirements

Requirement	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
LC_PLL1_REFCLK Frequency	–	–	156.25	–	MHz
LC_PLL1_REFCLK Accuracy	–	–50	–	+50	ppm
LC_PLL1_REFCLK Duty Cycle	–	45	–	55	%
Input Voltage Range	VIN	500	–	2000	mVpp diff
LC_PLL1_REFCLK Rise/Fall Time (20% to 80%)	T_R, T_F	–	–	0.5	ns
LC_PLL1_REFCLK (156.25 MHz) Jitter RMS Max (12 kHz to 12.5 MHz)	–	–	–	0.5	ps

Note:

- Sample part Valpey Fisher VF900892-156.25 or Raltron Electronics CS9-TSH-156.250 LVPECL Crystal Oscillator or Vectron VCC6-1286-156M250, or MtronPTI M2013S232 (156.25 MHz).
- AC-coupled externally.
- Internal 100Ω termination.

TS_PLL_REFCLK Clock Requirements

The TS clock (TS_PLL_REFCLKP/N) requires either a 12.8 MHz, 20 MHz, 25 MHz, or 32 MHz differential source with characteristics shown in Figure 28.

Figure 28: TS_PLL_REFCLKP/N Input Timing Diagram

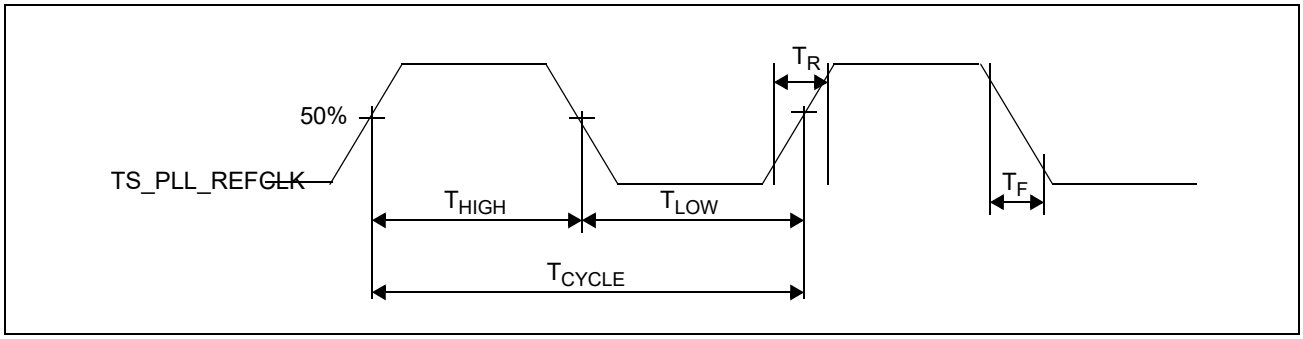


Table 47: TS_PLL_REFCLK Input Requirements

Requirement	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
TS_PLL_REFCLK Frequency	–	–	50	–	MHz
TS_PLL_REFCLK Accuracy	–	–50	–	+50	ppm
TS_PLL_REFCLK Duty Cycle	–	40	–	60	%
Input Voltage Range	VIN	500	–	2000	mVpp diff
TS_PLL_REFCLK Rise/Fall Time (20% to 80%)	$T_{R,}$ T_F	–	–	2.0	ns
TS_PLL_REFCLK Jitter RMS Max (12 kHz to 12.5 MHz)	–	–	–	2.0	ps

Note:

- Sample part Rakon Limited P5473LF (OCXO) crystal oscillator.
- AC-coupled externally.

BS[1:0]_PLL_REFCLK Input Requirements

Figure 29: BS[1:0]_PLL_REFCLK Input Diagram

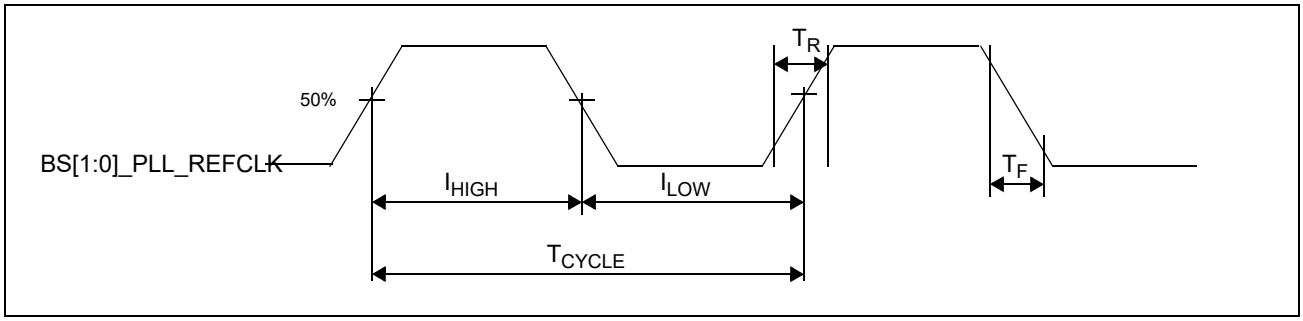


Table 48: BS[1:0]_PLL_REFCLK Input Requirements

Requirement	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
BS[1:0]_PLL_REFCLK Frequency	–	–	25 or 50	–	MHz
BS[1:0]_PLL_REFCLK Accuracy	–	–50	–	50	ppm
BS[1:0]_PLL_REFCLK Duty Cycle	–	40	–	60	%
Input Voltage Range	VIN	500	–	2000	mVpp diff
BS[1:0]_PLL_REFCLK Rise/Fall Time (20% to 80%)	$T_{R,}$ T_F	–	–	0.5	ns

Note:

- Sample part Vectron VCC6-QAB-25M00 LVPECL Crystal Oscillator.
- AC-coupled externally.
- Internal 100Ω termination.

AC Specifications

Transmitter

Figure 30: Transmit Eye Mask

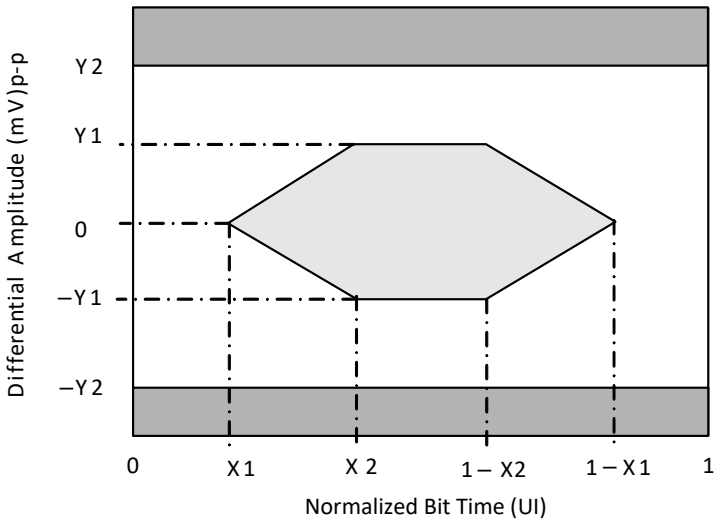


Table 49: TX

Parameters	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
Output Speed per lane	–	–100 ppm	+5.0	+100 ppm	Gbaud
Differential Resistance	Rin	80	100	120	Ω
Differential Output Voltage (pk-pk)	VOD	400	–	900	mVp-p
Transmit Eye Mask (Figure 30)	X1	–	–	0.15	UI
Transmit Eye Mask (Figure 30)	X2	–	–	0.40	UI
Transmit Eye Mask (Figure 30)	Y1	200	–	–	mV
Transmit Eye Mask (Figure 30)	Y2	–	–	450	mV
Common Mode Voltage	VCM	550	–	1060	mV
Differential Output Return Loss (min)	Equation[a]	–	–	–8	dB
Common-mode Output Return Loss (min)	Equation[b]	–	–	–6	dB
Output Rise Time (20%–80%)	Tr	30	–	–	pS
Output Fall Time (20%–80%)	Tf	30	–	–	pS
Output Jitter @ $1e^{-12}$ BER					
Uncorrelated	sut	–	–	0.15	UIpp
Total	st	–	–	0.30	UIpp

a. Return Loss (f) –8 dB for 100 MHz ≤ f< 2.5 GHz
Return Loss (f) ≤ [–8+ 16.6log(f/2.5)]dB for 2.5 GHz ≤ f ≤ 5 GHz, where f is in Gigahertz.
b. Return Loss (f) ≤ –6 dB for 100 MHz ≤ f < 2.5 GHz

Receiver

Figure 31: Receive Eye Mask

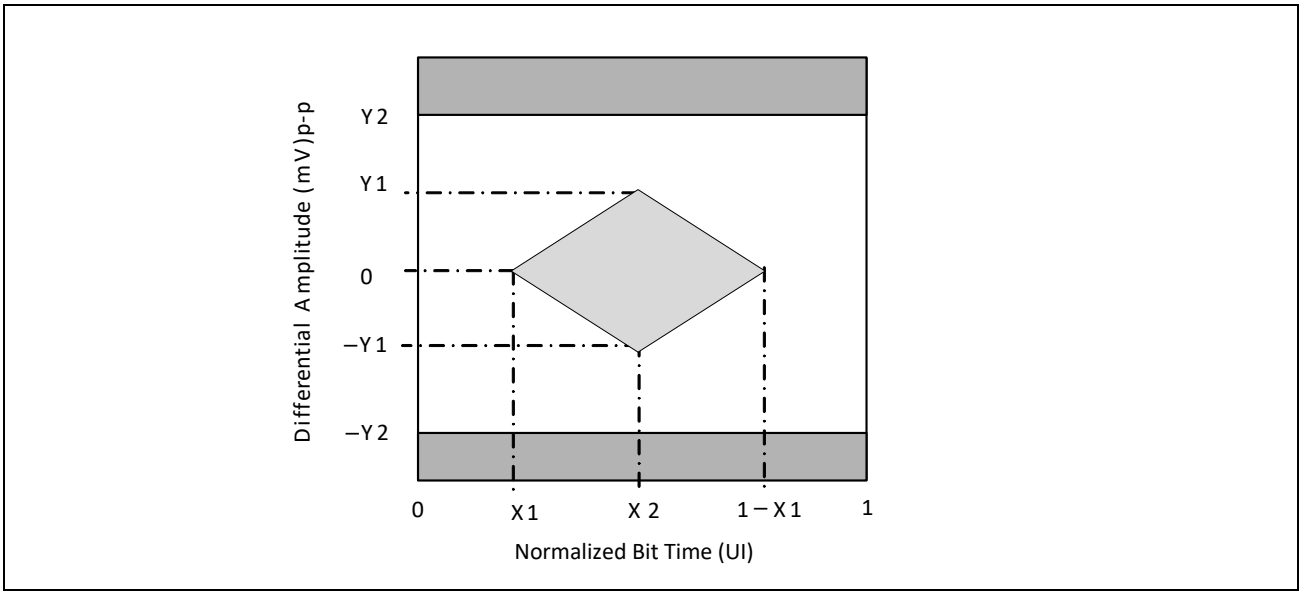
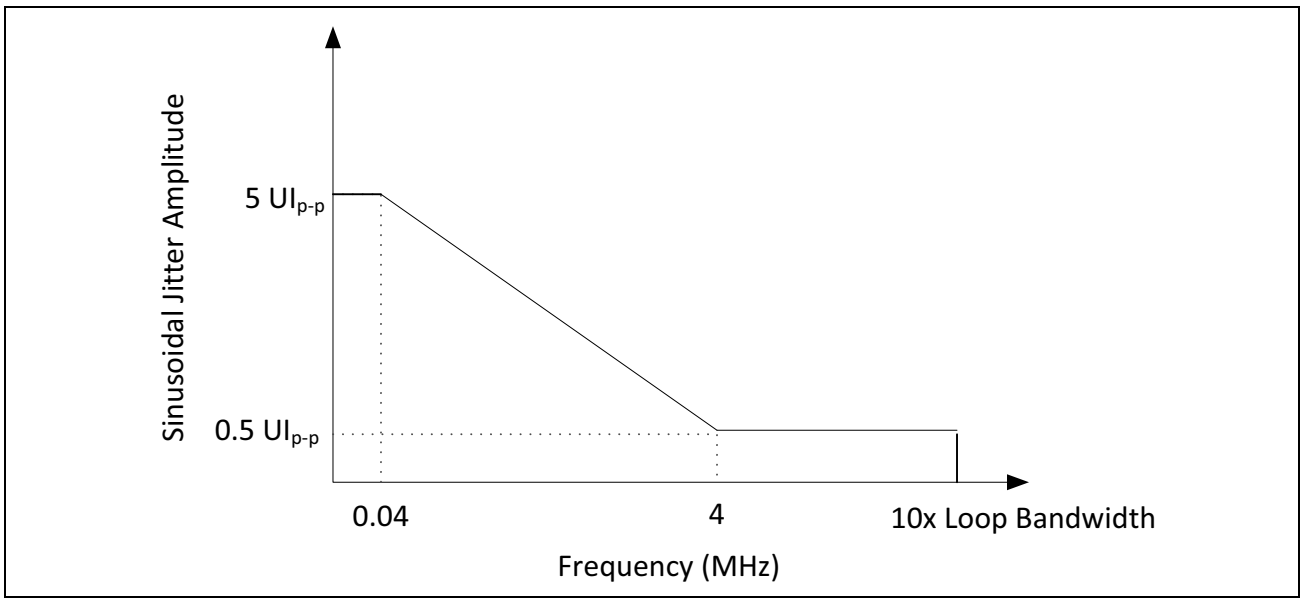


Table 50: RX

Parameters	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
Receiver coupling	AC	–	0.1	–	µF
Differential Resistance	Rin	80	100	120	Ω
Receive eye mask (Figure 31 on page 94)	X1	–	–	0.30	UI
Receive eye mask (Figure 31 on page 94)	X2	–	–	0.5	UI
Receive eye mask (Figure 31 on page 94)	Y1	50	–	–	mV
Receive eye mask (Figure 31 on page 94)	Y2	–	–	450	mV
Differential input return loss	Equation[a]	–	–	–8	dB
Common mode input return loss	Equation[b]	–	–	–6	dB
Receiving speed per lane	–	–100 ppm	+5.0	+100 ppm	Gbaud
Sinusoidal jitter tolerance	Figure 32 on page 95	–	–	0.05	UIpp
Bit error rate based channel characteristics per Clause 83A in IEEE802.3ba.	–	–	–	1e-12	bps

a. Return loss (f) ≤ –8 dB for 100 MHz ≤ f < 2.5 GHz.
Return loss ≤ [–8 + 16.6log(f/2.5)]dB for 2.5 GHz ≤ f ≤ 5 GHz, where f is in Gigahertz.
b. Return loss (f) ≤ –6 dB for 100 MHz ≤ f < 2.5 GHz, where f is in Gigahertz.

Figure 32: Single-Tone Sinusoidal Jitter Mask



SGMII AC Specifications

This subsection specifies timing information for the Serial Interface.

SGMII/SerDes Interface Output Timing

Figure 33: SGMII Serial Interface Output Timing

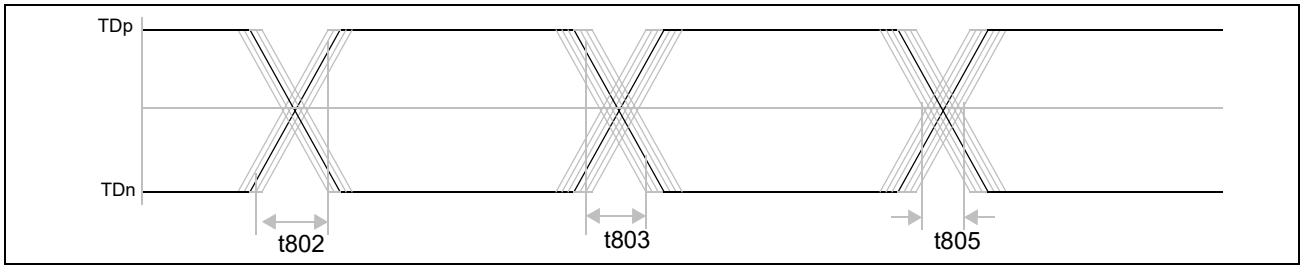


Table 51: SGMII Serial Interface Output Timings

Description	*Parameter*	*Min.*	*Typ.*	*Max.*	*Units*
Transmit Data Signaling Speed	t801	–	1.25	–	Gbaud
Transmit Data Rise Time (20%–80%)	t802	100	–	200	ps
Transmit Data Fall Time (20%–80%)	t803	100	–	200	ps
Transmit Data Total Jitter	t805	–	–	0.24	UI

SGMII/SerDes Interface Input Timing

Figure 34: Serial Interface Input Timing

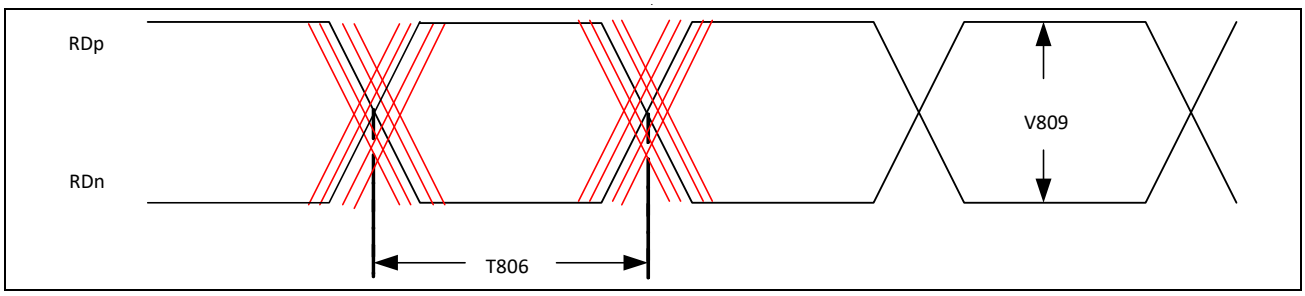


Table 52: SGMII Serial Interface Input Timings

Description	*Parameter*	*Min.*	*Typ.*	*Max.*	*Units*
Receive Data Signaling Speed	t806	–	1.25	–	Gbaud
Receive Data Differential Input (pk-pk)	V809	0.1	–	–	V

2.5GbE SerDes AC Specifications

This subsection specifies timing information for the SerDes Interface running at this rate.

2.5GbE/SerDes Interface Output Timing

Figure 35: 2.5GbE/SerDes Interface Output Timing

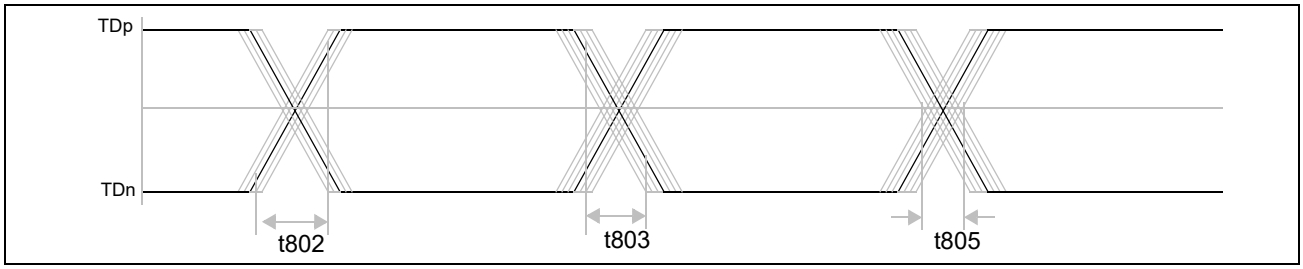


Table 53: 2.5GbE/SerDes Interface Output Timings

Description	*Parameter*	*Min.*	*Typ.*	*Max.*	*Units*
Transmit Data Signaling Speed	t801	–	3.125	–	Gbaud
Transmit Data Rise Time (20%–80%)	t802	60	100	130	ps
Transmit Data Fall Time (20%–80%)	t803	60	–	130	ps
Transmit Data Total Jitter	t805	–	–	0.65	ps
Transmit P to N Differential Skew	T_{SKEW}	–	–	15	ps

2.5GbE/SerDes Interface Input Timing

Figure 36: 2.5GbE/SerDes Interface Input Timing

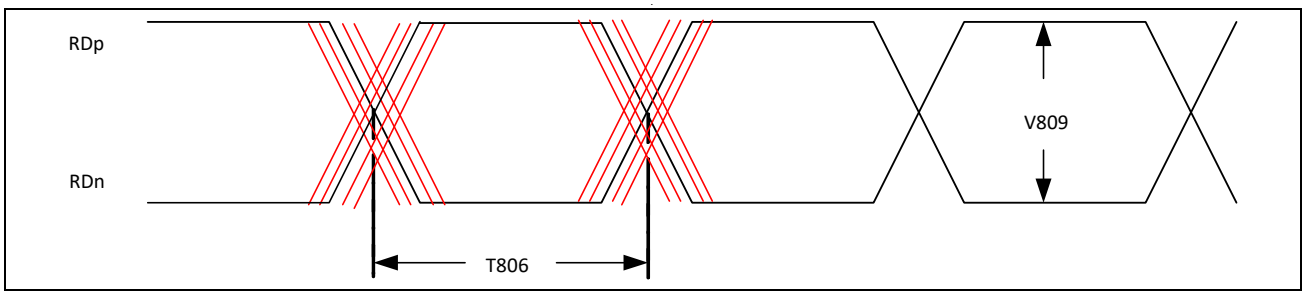


Table 54: 2.5GbE/SerDes Interface Input Timings

Description	*Parameter*	*Min.*	*Typ.*	*Max.*	*Units*
Receive Data Signaling Speed	t806	–	3.125	–	Gbaud
Receive Data Differential Input (pk-pk)	V809	0.1	–	1.6	V

Warpcore Technology Serial Interface AC Specification

The device serial interface supports the following features:

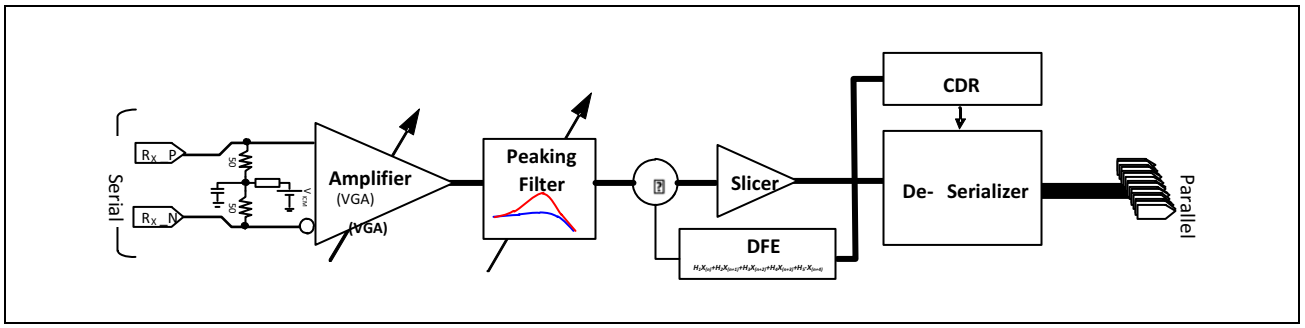
- Quad SerDes block supporting four serial links.
- Support for line rates of 1.25 Gbps, 3.125 Gbps, 5.1625 Gbps, 6.5625 Gbps, and 10.3125 Gbps per serial link.
- Includes a 5-tap DFE with adaptive control and VGA with AGC.
- Programmable RX equalizer with 0 dB–8 dB boost, approximately 0.5 dB/step.
- Transmitter with 32-level post-cursor and 16-level precursor preemphasis.
- CML driver with 2 × 50Ω internal termination.
- Controlled peak-to-peak amplitude.
- 4-Tap FIR with configurable weights:
  - 1-Tap of Precurser emphasis (16 steps)
  - 1-Tap of Post-curser emphasis (32 steps)
  - Additional second Post-curser emphasis (8 steps)

The serial interface operating conditions are shown in Table 55.

Table 55: Warpcore Technology Serial Interface Operating Conditions

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
Baud, symbol rate	B_{PS}	1.25	–	10.9375	Gbaud
Unit Interval	UI	91.4	–	800	ps

Figure 37: Conceptual Diagram of the SerDes Receiver



The Serial Interface receive characteristics are shown in Table 56.

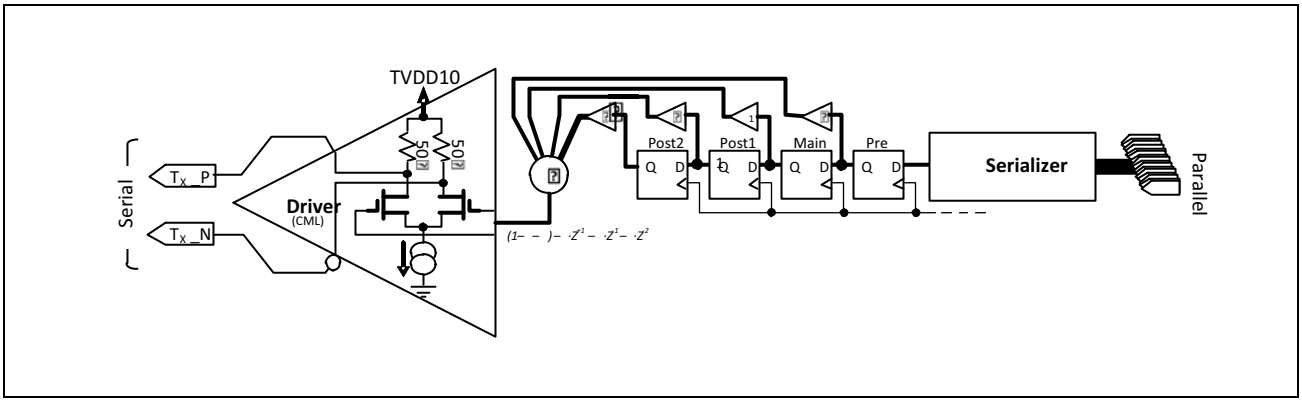
Table 56: Serial Interface Receive Characteristics

Parameter	*Symbol*	*Description*	*Min.*	*Typ.*	*Max.*	*Units*
Input Voltage	V_{ID}	AC coupled, differential p-p	85	–	1600	mVppd
Input Impedance	R_{in}	Differential, integrated on-chip	80	100	120	Ω

Table 56: Serial Interface Receive Characteristics (Cont.)

Parameter	Symbol	Description	Min.	Typ.	Max.	Units
Jitter Tolerance	delta-t_{RXtot}	Total, peak-peak	–	–	0.65	UI
	delta-t_{RXdet}	Deterministic, peak-peak	–	–	0.37	UI

Figure 38: Conceptual Diagram of the SerDes Transmitter



The serial interface transmit characteristics are shown in Table 57.

Table 57: Serial Interface Transmit Characteristics

Parameter	Symbol	Description	Min.	Typ.	Max.	Units
Output Voltage	V_{OD}	Differential peak-peak Programmable in 16 steps	0.7	1.0	1.1	Vptpd
Preemphasis	alpha	FIR tap coefficient in 32 steps. alpha ~= 0.0125i, where i = 0 ~ 31	0	–	0.3875	–
	beta	FIR tap coefficient in 16 steps. beta ~= 0.0125i, where i = 0 ~ 15	0	–	0.1875	–
	beta	FIR tap coefficient in 8 steps. beta ~= 0.00625i, where i = 0 ~ 7	0	–	0.0375	–
Output Impedance	R_{out}	Differential, integrated on-chip	–	100	–	Ω
Output voltage fall-time	t_{fall}	80% to 20% (based on 10GBASE-KR waveform, 8–1s, 8–0s)	24	–	47	ps
Output voltage rise-time	t_{rise}	20% to 80%	24	–	47	ps
Output Differential Skew	t_{skewo}	50% rising/falling versus 50% falling/rising edge	–	–	5	ps
Transmit Output Jitter	delta-t_{TXWDM}	Total, peak-peak WDM	–	–	0.17	UI
	delta-t_{TXtot}	Total, peak-peak	–	–	0.28	UI
	delta-t_{TXdet}	Deterministic, peak-peak	–	–	0.17	UI

10GBASE-KR Electrical Characteristics

Transmitter

Table 58: 10GBASE-KR TX

Parameters	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
Output Speed	–	–100 ppm	+10.3125	+100 ppm	Gbaud
Differential Impedance	R_{in}	80	100	120	Ω
Differential Output Voltage (pk-pk) based on 101010.. pattern	VOD	–	–	1200	mVp-p
Output Voltage (pk-pk) when TX is disabled	VOD	–	–	30	mVp-p
Common Mode Voltage	VCM	TBD	0.55	TBD	V
Differential Output Return Loss (min)	Equation[a]	–	–	–	dB
Common-mode Output Return Loss (min)	Equation[b]	–	–	–	dB
Output Rise Time (20%–80%)	Tr	24	–	47	pS
Output Fall Time (20%–80%)	Tf	24	–	47	pS
Output Jitter @ 1e-12 BER					
Random	sr	–	–	0.15	UI
Deterministic	sdt	–	–	0.15	UI
Duty Cycle Distortion	sdc	–	–	0.035	UI
Total	st	–	–	0.28	UI

a. Return Loss (f) ≥ 9 dB for 50 MHz ≤ f < 2500 MHz
Return Loss (f) ≥ [9−12log(f/2500 MHz)] dB for 2500 MHz ≤ f ≤ 7500 MHz, where f is in Megahertz.

b. Return Loss (f) ≥ 6 dB for 50 MHz ≤ f < 2500 MHz
Return Loss (f) ≥ [6−12log(f/2500 MHz)] dB for 2500 MHz ≤ f ≤ 7500 MHz, where f is in Megahertz.

Receiver

Table 59: 10GBASE-KR RX

Parameters	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
Differential Input Voltage (pk-pk)	VID	–	–	1200	mVp-p
Differential Input Return Loss (min)	Equation 1	–	–	–	dB
Receiving Speed	–	–100 ppm	+10.3125	+100 ppm	Gbaud
Differential Impedance	R_{in}	80	100	120	Ω

Section 8: Thermal Specifications

Package Thermal Specifications

Table 60 shows the preliminary package thermal specifications, with a heat sink for various airflow levels. To maintain a junction temperature below the maximum specified junction temperature, the Theta-JA must be smaller than the maximum calculated Theta-JA for the device. A heat sink and airflow are required, see “Heat Sink” on page 101.

Table 60: Estimated Package Thermal Specifications with 40 mm x 40 mm x 25 mm Heat Sink

Parameters	*Symbol*	*Value*	*Units*
Theta-JB (junction-to-board)	θ_{JB}	1.47	°C/W
Theta-JC (junction-to-case)	θ_{JC}	1.03	°C/W
Theta-JA (junction-to-ambient), 0 LFM	θ_{JA}	6.00	°C/W
Theta-JA (junction-to-ambient), 100 LFM	θ_{JA}	3.83	°C/W
Theta-JA (junction-to-ambient), 200 LFM	θ_{JA}	3.04	°C/W
Theta-JA (junction-to-ambient), 400 LFM	θ_{JA}	2.55	°C/W
Theta-JA (junction-to-ambient), 600 LFM	θ_{JA}	2.33	°C/W

Heat Sink

Heat Sink Selection

The device is required to be used with a heat sink. The end-use thermal environment, combined with the operating mode of the device, dictates the required thermal characteristics (size, thermal resistance, and so forth) of the heat sink.

Heat Sink Attachment

It is required that the heat sink used with the BCM5340X device package be mechanically mounted to the device. An adhesive-based or taped-based attachment scheme is not recommended. In a mechanically mounted configuration, contact between the heat sink and the package is maintained using an externally applied mechanical force. It is recommended that the heat sink be held in place by clamp or fixture to the printed circuit board. The heat sink should not be clamped to the package (the package/heat sink combination should not be free-standing).

A nonadhesive thermal interface material (such as phase change film or thermal grease) should be used between the heat sink and the package top to maintain a low thermal resistance path between the package and the heat sink. The applied operating force between the heat sink and the package should be sufficient to meet the thermal interface material manufacturer's recommendations, but should not exceed 40 lbs total force on the package. The exact configuration of the mounting scheme and clamping mechanism is at the user's discretion.

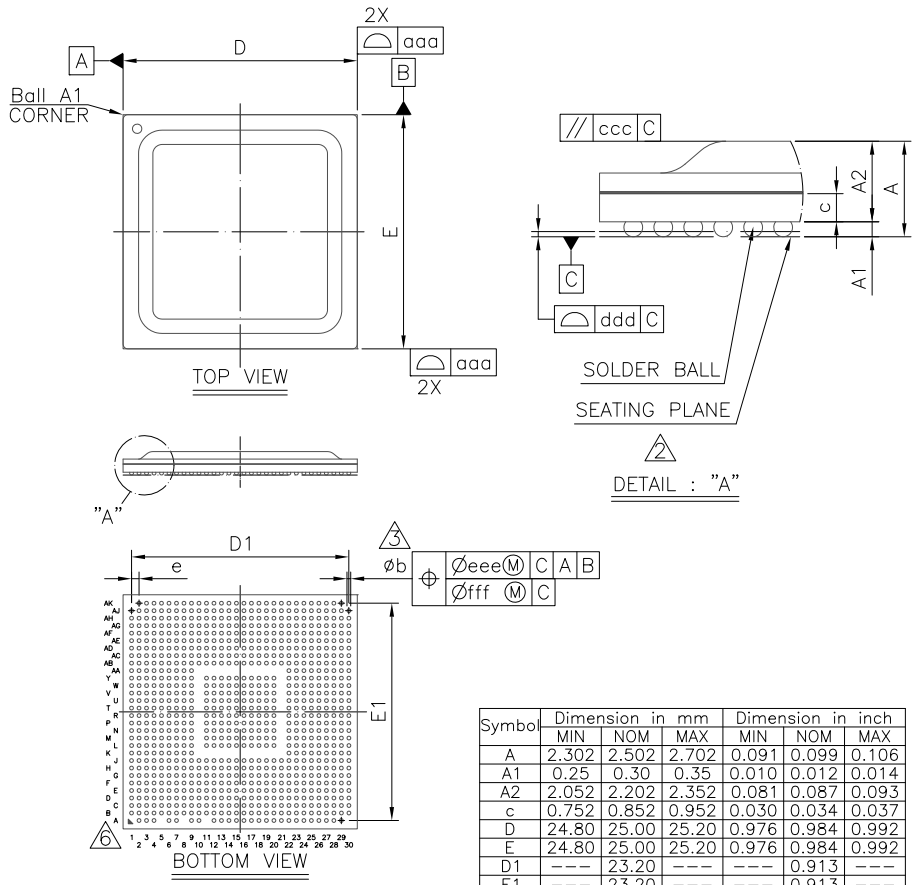
- For 25 mm × 25 mm package:
  - The maximum allowed force during heat sink attachment at room temperature is 35 lb/15.9 kgf for a maximum of 30 seconds.
  - The maximum allowed sustained force during device lifespan is 10.6 lb/4.8 kgf
- The applied operating force should be evenly distributed across the package top.
- Tooling holes and/or clamp locations should be selected to minimize PCB warpage.
- The clamping mechanism should not clamp to package underside.
- The clamping structure should withstand the user's mechanical testing requirements (such as shock and vibration).

Note: Heat sink attachment area is 19 mm × 19 mm.

Section 9: Mechanical Information

849-Pin FCBGA

Figure 39: 849-Pin FCBGA (25 mm x 25 mm)



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.302	2.502	2.702	0.091	0.099	0.106
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	2.052	2.202	2.352	0.081	0.087	0.093
c	0.752	0.852	0.952	0.030	0.034	0.037
D	24.80	25.00	25.20	0.976	0.984	0.992
E	24.80	25.00	25.20	0.976	0.984	0.992
D1	---	23.20	---	---	0.913	---
E1	---	23.20	---	---	0.913	---
e	---	0.80	---	---	0.031	---
b	0.35	0.40	0.45	0.014	0.016	0.018
aaa	0.20			0.008		
ccc	0.25			0.010		
ddd	0.15			0.006		
eee	0.20			0.008		
fff	0.08			0.003		
MD/ME	30 / 30			30 / 30		

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: A , ddd
5. THE TILT OF HEAT SINK SHOULD BE WITHIN 10MIL(0.254 MM) (VERTICAL POSITION)
6. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.

Section 10: Ordering Information

Table 61: Ordering Information

Part Number	*Description*	*Package*	*Ambient Temperature*
BCM53402A0KFSBG	8*10G	25 mm x 25 mm	0°C~70°C
BCM53402A0IFSBG	8*10G	25 mm x 25 mm	–40°C~85°C
BCM53405A0KFSBG	16*10G	25 mm x 25 mm	0°C~70°C
BCM53405A0IFSBG	16*10G	25 mm x 25 mm	–40°C~85°C
BCM53406A0KFSBG	12*10G + 12*1G/2.5G	25 mm x 25 mm	0°C~70°C
BCM53406A0IFSBG	12*10G + 12*1G/2.5G	25 mm x 25 mm	–40°C~85°C

Appendix A: Acronyms and Abbreviations

For a more complete list of acronyms and other terms used in Broadcom documents, go to: http://www.broadcom.com/press/glossary.php.

Term	*Description/Usage*
ACA	Accessory Charger Adapter
ACI	Adjacent Channel Interference
ACL	Access Control Logic
ACP	Accelerator Coherency Port
AH	Authentication
AHB	Advanced High Performance Bus
ALU	Arithmetic and Logic Unit 1. The unit of a computing system that contains the circuits that perform arithmetic operations. 2. A functional component of a computer system that performs arithmetic operations. See *vector unit* and *scalar unit*.
AOPC	Always-On Power Controller
APB	Advanced Peripheral Bus
AS	1. Autonomous System (ATM) 2. Access stratum (3GPP)
ATB	Advanced Trace Bus
AUTN	Authentication token (3GPP)
AXI	Advanced eXtensible Interface
BB	Baseband. (*Bluetooth*)
BBC	Backup battery charger
BCCH	Broadcast Control Channel
BER	Bit Error Rate
BIF	Battery Interface (MIPI Alliance)
BMC	Best Master Clock
BPS	Bits-Per-Second
BSC	Broadcom Serial Control: A proprietary Broadcom bus or interface that is compatible with the Philips® I^2C bus or interface.
CC	1. Call Control. (*Bluetooth*) 2. Constant Current
CCBS	Completion of Calls to Busy Subscribers or Call Completion on Busy Subscriber
CCI	Camera Control Interface
CCP	Compact Camera Port
CCP2	Compact Camera Port 2
CCU	Clock Control Unit
CDP	1. Compact display port 2. Charging Downstream Port

Term	*Description/Usage*
CFP	Compact Field Processor
CM	1. Configuration management: The detailed recording and updating of information that describes an enterprise's computer systems and networks, including all hardware and software components. 2. Congestion management. 3. Connection Manager or Connection Management.
CML	Common Mode Logic
CMSP	Content Management Service Provider
CoS	Class-of-Service
CPE	Customer Premise Equipment
CSI	Camera Serial Interface
CSI2	Camera Serial Interface 2 - 02/18/10
CSR	1. Control and Status Register 2. Core switching regulator
CTI	Cross trigger interface
CTM	Cross Trigger Matrix
CV	1. Credential Vault 2. Constant Voltage
DA	Destination Address
DAP	Debug Access Port
DBI	Display Bus Interface
DCP	Dedicated Charging Port
DCXO	Digitally Compensated Crystal Oscillator
DF	Do not Fragment
DigRF	Baseband/RF Digital interface specification
DLL	Data Link Layer
DLLP	Data Link Layer Packet
DMU	Device Management Unit
DoS	Denial of Service
DPI	Display Pixel Interface
DRM	1. Digital Rights Management 2. Digital Restrictions Management
DSI	1. Display Stream Interface: A high-speed serial interface for LCD modules. 2. Display Serial Interface
DT	Double Tag
DTE	Digital Timing Engine
DVFS	Dynamic Voltage and Frequency Scaling
DVS	Dynamic Voltage Scaling
EAPOL	Extensible Authentication Protocol over LAN
ECC	Error-Correction Code
ECRC	End-to-end CRC
ENS	Enhanced Network Selection (GPS)

Term	*Description/Usage*
ESP	Encapsulating Security Payload
ETB	Embedded Trace Buffer
ETM	Embedded Trace Macrocell (ARM Microprocessors)
EVM	Error Vector Magnitude
FG	Fuel gauge
GIC	General Interrupt Controller
GMM	GPRS Mobility Management
GPRS	General Packet Radio Service: A standard for wireless communications that run at speeds of up to 171 Kbps, compared with GSM systems, which run at 9.6 Kbps. GPRS, which supports a wide range of bandwidths, is an efficient use of limited bandwidth particularly suited for sending and receiving small bursts of data, such as for e-mail and Web browsing, as well as large volumes of data.
GSM	Global System for Mobile Communications: A second generation digital cellular technology developed by European countries in the 1980s to facilitate pan-European roaming. GSM uses time division multiple access technology and operates at both cellular and PCS frequencies (900 MHz, 1800 MHz, 1900 MHz). Other technologies used are CDMA, PDC & TDMA. In 1999, 66% of the world's cell phones were GSM (source: EMC World Cellular Database).
HOSTON	PMU state is on
HPLMN	Home Public Land Mobile Network
HSDPA	High-Speed Downlink Packet Access
HSUPA	High-Speed Upload Packet Access
HVS	Hardware Video Scaler
I^2S	1. Inter-IC Sound 2. Integrated Interchip Sound 3. Internet Information Server (*Microsoft*) Electrical serial bus interface standard for connecting digital audio devices. Up to 16 audio channels at up to 192 kHz.
IDT	Intelligent Double Tag
IF	1. Interface 2. Intermediate Frequency: A frequency below Radio Frequency (RF). In a GPS receiver, the RF chip converts the analog RF signal to IF and then converts it to a digital signal that is processed by the baseband device.
IHL	Internet Header Length
IMSI	International Mobile Subscriber Identity
IOSR	Input/Output Service Request
ISI	Intersymbol Interference
ITM	Instruction Trace Module
ITU	International Telecommunications Union
LA	Location Area
LAI	Location Area Identification
LDO	1. Low-Dropout 2. Low dropout regulator
Li-ion	Lithium ion battery

Term	*Description/Usage*
LNA	low noise amplifier: Analog radio amplifier, used as the first stage in a GPS front-end. The GL-LN22 RF chip contains an integrated LNA on-chip.
LPM	1. Longest Prefix Match: IP packet forwarding mechanism. 2. Longest Prefix Match: An algorithm used by routers in Internet Protocol (IP) networking to select an entry from a routing table. 3. Low power mode
MBC	main battery charger
MBRDY	PMU state is off, but it is ready to turn on
MBWV	Main Battery Working Voltage
MEMC	memory controller
MF	More Fragments
MIDI	Musical Instrument Digital Interface
MIPI	Mobile Industry Processor Interface
MLC	Multi-Level Cell
MM	1. Multimedia 2. Mixed Mode 3. ESD Machine Model
MMA	Mobility Management Adaptation
MME	Mobility Management Entity
MMR	Mobility Management Router
MS	1. Mobile station: Refers to the handset or mobile wireless device in a C-plane architecture. 2. Mobile subscriber
MSTP	Multiple Spanning Tree Protocol
MTT	Mobile Trace Terminal
NCO	Numerically Controlled Oscillator
NM	Normal mode
NNI	Service-Provider Network Interface
NTC	Negative Temperature Coefficient
OAM	Operations, Administration, and Maintenance
OCP	Open Core Protocol
ONFI	Open NAND Flash Interface
OTG	On-the-Go
P-TMSI	Packet Temporary Mobile Subscriber Identity (GSM 03.60 version 7.4.1)
PA	Power amplifier
PCGUI	Phone Control Graphical User Interface
PCIe	PCI Express
PCP	Priority Code Point
PD	1. Protocol Discriminator (GPRS LLC-layer address field format) 2. Phase Detector
PDM	Pulse density modulation
PDP	Packet Data Protocol

Term	*Description/Usage*
PDU	protocol data unit 1. OSI term for packet. 2. Information that is delivered as a unit between peer entities of a LAN or a MAN and contains control information, address information, and may contain user data. 3. A block of data that is exchanged between two devices using a protocol.
PHY	Physical Layer
PIM	1. Protocol-Independent Multicast: Multicast routing architecture that allows the addition of IP multicast routing protocols. Packets are forwarded on all outgoing interfaces until pruning and truncation occur. In dense mode, receivers are densely populated, and it is assumed that the downstream networks want to receive and will use the datagrams that are forwarded to them. The cost of using dense mode is its default flooding behavior. Sometimes referred to as Dense Mode PIM or PIM DM. Contrast with PIM Sparse Mode. 2. Personal information manager 3. Personal information management
PLMN	Public Land Mobile Network
PMM	1. Packet Mobility Management (in GPRS) 2. Performance Measurement Matrix 3. Pressurized Multipurpose Module
PMU	Power Management Unit
PPS	Packet-Per-Second
PSMS	Power System Monitoring and Simulation
PSRR	Power Supply Rejection Ratio
PTI	Parallel Trace-Data Interface
PTM	Program Trace Macrocell
PWM	Pulse-Width Modulator
PWRUP	PMU state is off and it is not ready to turn on
QoS	Quality of Service
RAI	Routing Area Identification
RNTI	Radio Network Temporary Identifier (3GPP)
RPLMN	Registered Public Land Mobile Network
RR	Radio Resource
RTOS	Real-time Operating Systems
RV	Rate Violation
S/PDIF	Sony/Philips Digital Interconnect Format
SAIC	Single Antenna Interference Cancellation
SCU	Snoop Control Unit
SDIO	Secure Digital Input/Output
SDP	1. Service Discovery Protocol 2. Session Description Protocol 3. Sockets Direct Protocol 4. Standard Downstream Port
SDSR	SD switching regulator
SLC	Single-Level Cell

Term	*Description/Usage*
SP	Strict Priority
SS	Supplementary Services
STM	System Trace Module
STP	System Trace Protocol
SWD	Serial Wire Debug
TBF	Temporary Block Flow
TC	Traffic Class
TL	Transaction Layer
TLB	Translation Lookaside Buffer
TLLI	Temporary Logical Link Identity (GPRS protocols, LLC layer)
TLP	Transaction Layer Packet
TOS	Type Of Service
TPID	Tag Protocol ID
TPIU	Trace Port Interface Unit
TTL	Time To Live
UDFs	User-Defined Fields
UMI	Unified Memory Interface
UMTS	Universal Mobile Telecommunications System: The third generation mobile standards that will build on the success of GSM/GPRS and on the GSM operators' existing investment in infrastructure. Data rates offered will be up to 2 million bits per second.
UNI	User Network Interface
USBC	USB charger
USIM	1. User Services Identity Module (UMTS) 2. Universal Mobile Telecommunications System 3. UMTS subscriber identity mode
USIMAP	USIM application process
UTRAN	UMTS Terrestrial Radio Access Network: A conceptual term identifying that part of the network which consists of Radio Network Controllers and Node Base stations.
VID	VLAN ID
VLAN	Virtual LAN
VMBAT	Main Battery Voltage
WAC	Wall adapter charger
WDT	Watchdog timer
WRR	Weighted-Round-Robin
XIP	Execute in Place

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