



Dual N-Channel MOSFET, 20V, 6A/5.2A

General Description

The VAD8205O utilizes the advanced Trench technology and low resistance package to achieve extremely low on-resistance device which makes the system design an efficient and reliable solution for use in a wide variety of applications.

Features

- 20V, 6A, $R_{DS(on)}=27\text{m}\Omega$ @ $V_{GS}=4.5\text{V}$
- 20V, 5.2A, $R_{DS(on)}=38\text{m}\Omega$ @ $V_{GS}=2.5\text{V}$
- High Efficiency
- Improved dv/dt, di/dt capability
- 100% EAS Guaranteed
- Green Device

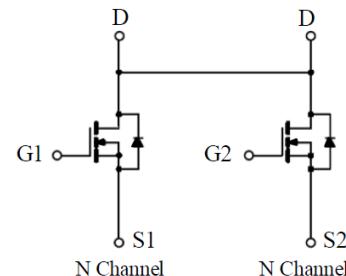
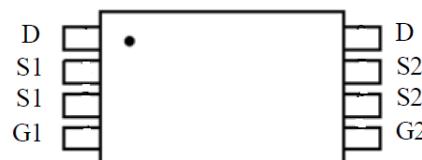
Application

Lithium-ion Battery Pack Applications

Product Summary

$V_{(BR)DSS}$	$R_{(DS)on}$	I_d
20V	4.5V@ 27 m Ω	6.0A
20V	2.5V@ 38 m Ω	5.2A

TSSOP-8



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Condition
Drain-Source Voltage	V_{DS}	20	V	
Continuous drain current ⁽¹⁾	I_D	6	A	$T_C=25\text{ }^\circ\text{C}$
Gate-Source Voltage	V_{GS}	± 12	V	Static
Pulsed drain current ⁽²⁾	I_{DM}	24	A	$T_C=25\text{ }^\circ\text{C}$
Power dissipation @ $T_C=25\text{ }^\circ\text{C}$	P_{diss}	1.5 0.96	W	$T_A=25\text{ }^\circ\text{C}$ $T_A=75\text{ }^\circ\text{C}$
Continuous diode forward current	I_S	1.7	A	$T_C=25\text{ }^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55 to 150	°C	
Operation Junction Temperature Range	T_J	-55 to 150	°C	

(1) Limited by $T_{j,\max}$.

(2) Pulse width T_p limited by $T_{j,\max}$



Thermal characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R_{thJA}	Thermal resistance, junction-ambient, max	---	---	83	°C/W
T_{sold}	Soldering temperature, max	---	---	260	°C

Package and Ordering Information

Device	Package	Marking	Packing
VAD8205O	TSSOP-8	8205A	5,000 / Reel



Electrical Characteristics ($T_j=25^\circ\text{C}$, unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Static Characteristic						
Drain-Source breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	20	---	---	V	$V_{GS}=0\text{V}, I_D=0.25\text{mA}$
Gate Threshold Voltage	$V_{(\text{GS})\text{th}}$	0.5	0.9	1.5	V	$V_{DS}=V_{GS}, I_D=0.25\text{mA}$
Drain-Source on resistance	$R_{(\text{DS})\text{on}}$	---	23	27	$\text{m}\Omega$	$V_{GS}=4.5\text{V}, I_D=6\text{A}, T_j=25^\circ\text{C}$
		---	30	38	$\text{m}\Omega$	$V_{GS}=2.5\text{V}, I_D=5.2\text{A}, T_j=25^\circ\text{C}$
Zero gate voltage drain current	I_{DSS}	---	---	1	μA	$V_{DS}=20\text{V}, V_{GS}=0\text{V}, T_j=25^\circ\text{C}$
Gate-Source leakage current	I_{GSS}	---	---	± 100	nA	$V_{GS}=\pm 12\text{V}, V_{DS}=0\text{V}$
Dynamic Characteristic						
Input Capacitance	C_{iss}	---	522	---	pF	$V_{GS}=0\text{V}, V_{DS}=8\text{V}, f=1\text{MHz}$
Output Capacitance	C_{oss}	---	124	---	pF	$V_{GS}=0\text{V}, V_{DS}=8\text{V}, f=1\text{MHz}$
Reverse Transfer Capacitance	C_{rss}	---	148	---	pF	$V_{GS}=0\text{V}, V_{DS}=8\text{V}, f=1\text{MHz}$
Turn-on delay time	$T_{d(\text{on})}$	---	10	---	nS	$V_{DD}=10\text{V}, V_{GS}=4.5\text{V}, I_D=1\text{A}, R_G=6\Omega;$ See Figure 9
Rise time	T_r	---	8.2	---	nS	
Turn-off delay time	$T_{d(\text{off})}$	---	2.5	---	nS	
Fall time	T_f	---	6	---	nS	
Gate Charge Characteristic						
Gate to source charge	Q_{gs}	---	1.7	---	nC	$V_{DD}=10\text{V}, I_D=3\text{A}, V_{GS}=4.5\text{V}$
Gate to drain charge	Q_{gd}	---	1.4	---	nC	
Gate charge total	Q_g	---	6.1	---	nC	
Reverse diode characteristic						
Diode forward voltage	V_{FD}	---	0.78	1.2	V	$V_{GS}=0\text{V}, I_F=1\text{A}, T_j=25^\circ\text{C}$
Continuous Source Current	I_{csc}	---	---	1.7	A	$V_G=V_D=0\text{V}$, Force current

Electrical Characteristic Diagrams

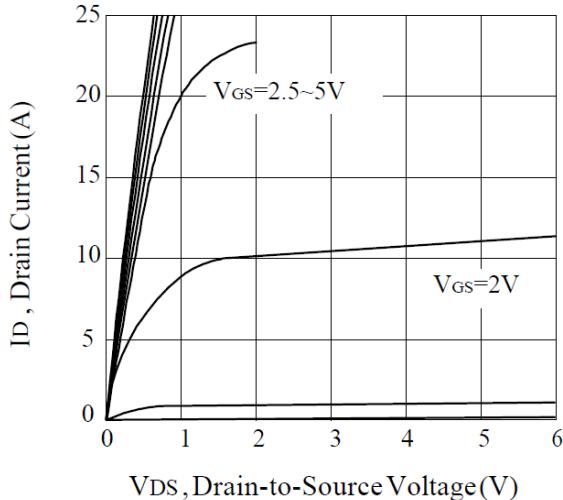


Figure 1 Output Characteristics

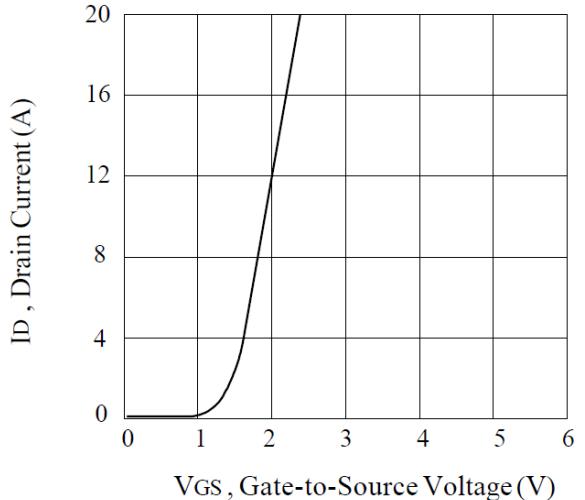


Figure 2 Transfer Characteristics

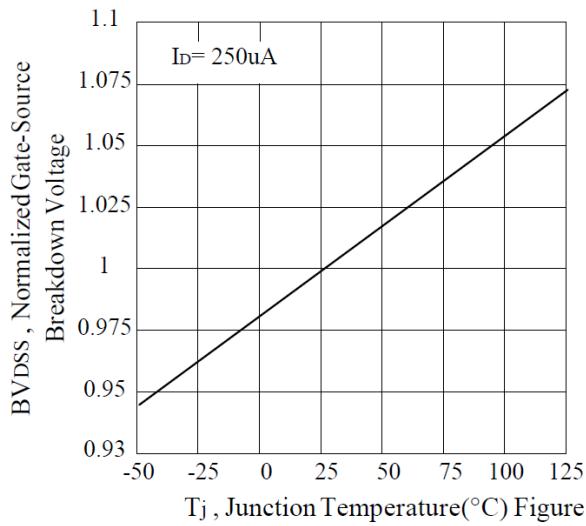


Figure 3 Breakdown Voltage vs. Junction Temperature

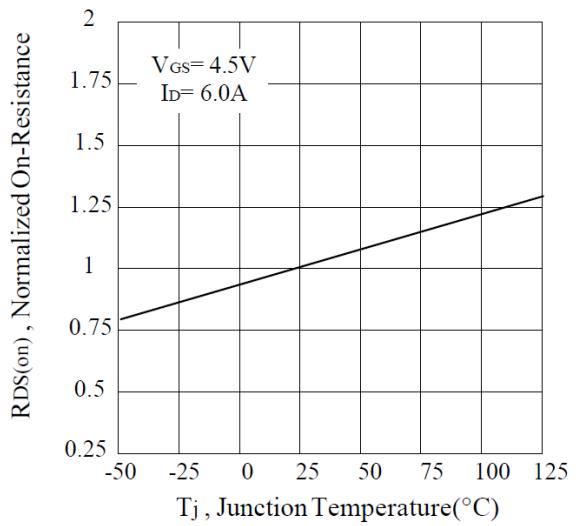


Figure 4 On Resistance vs. Junction Temperature

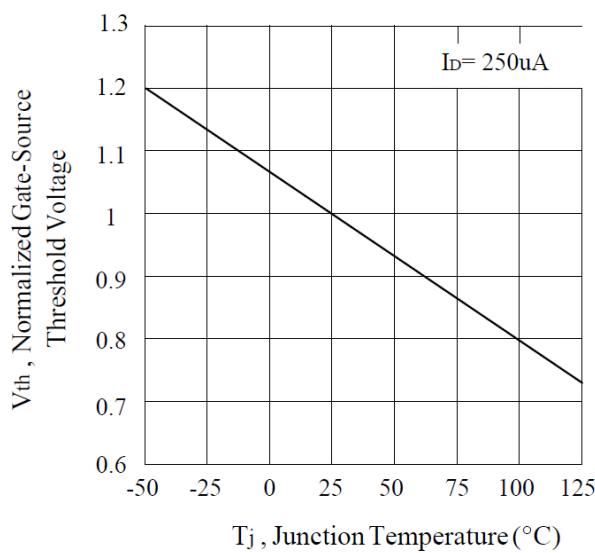


Figure 5 Gate Threshold vs. Junction Temperature

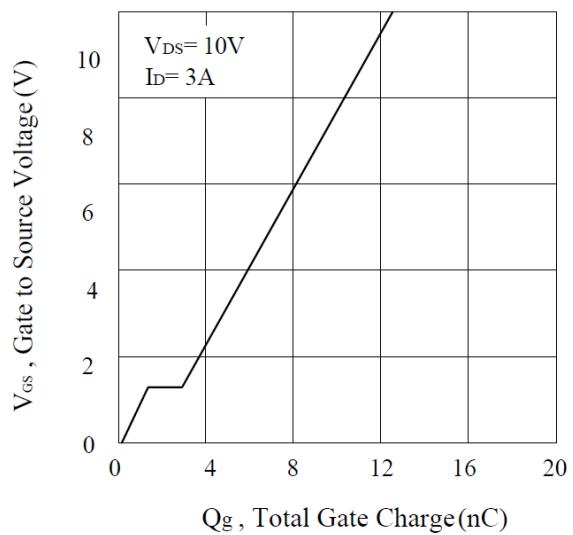


Figure 6 Gate Charge

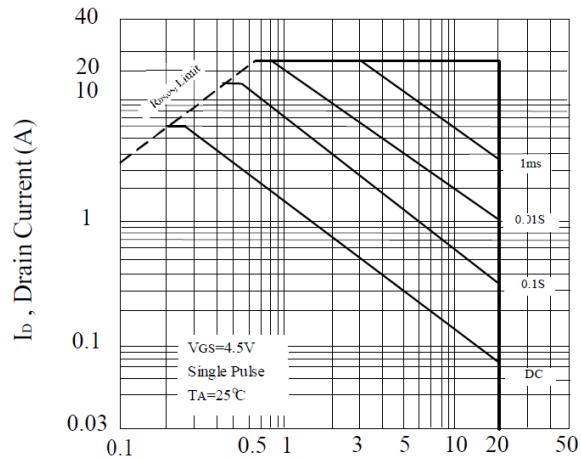


Figure 7 Maximum Safe Operating Area

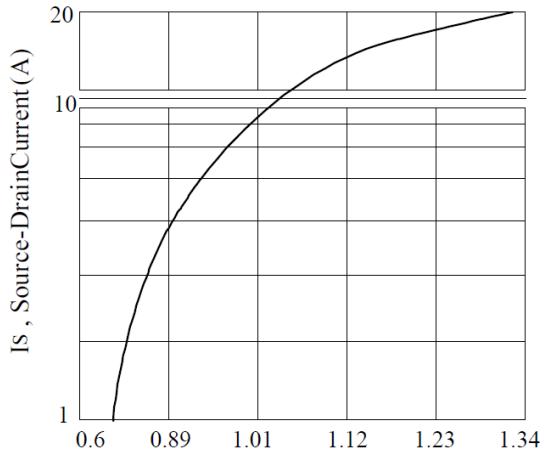


Figure 8 Is vs. Body diode Forward Voltage

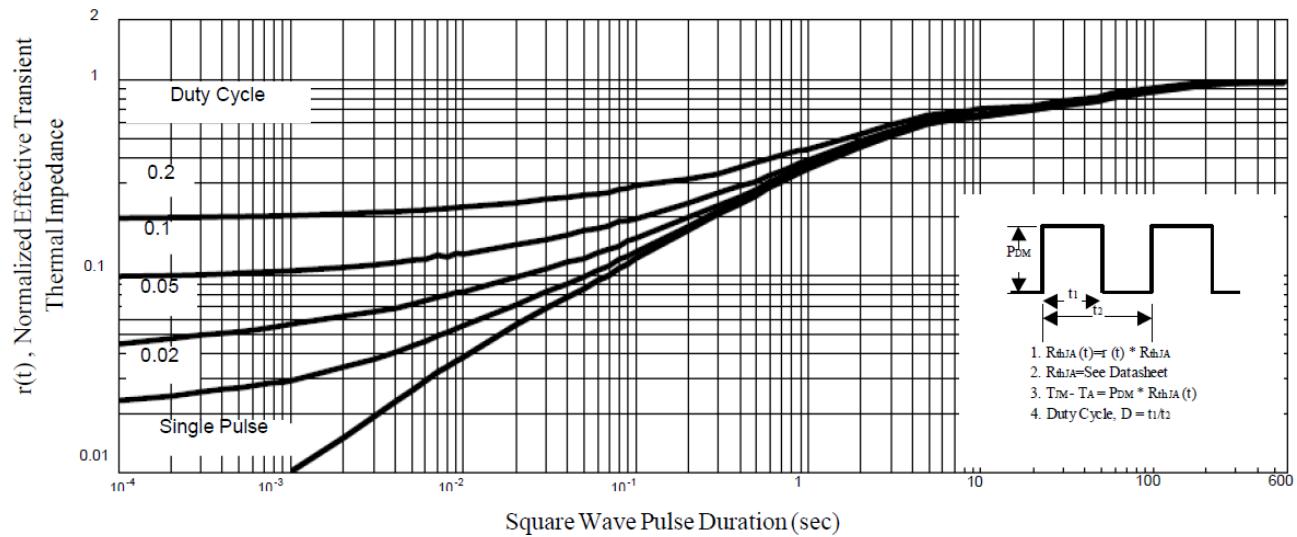


Figure 9 Normalized Thermal Transient Impedance Curve

Parameter Test Circuits

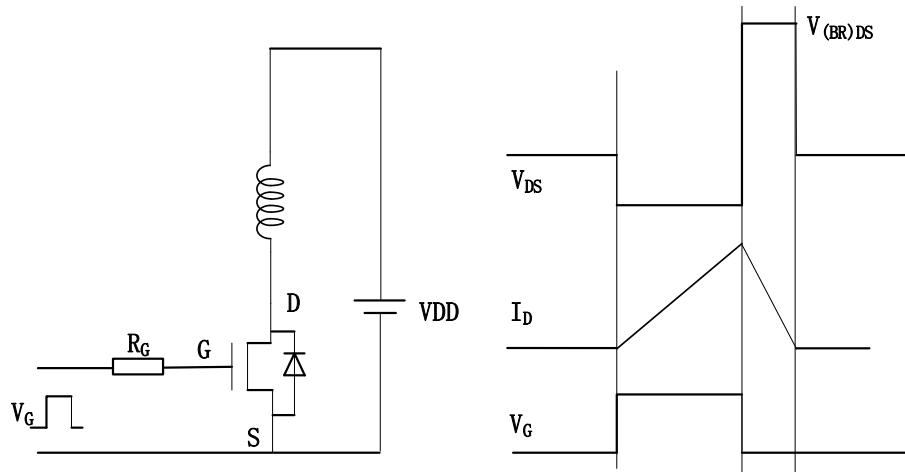


Figure 10 Unclamped Inductive Switching (UIS) Test circuit and waveforms

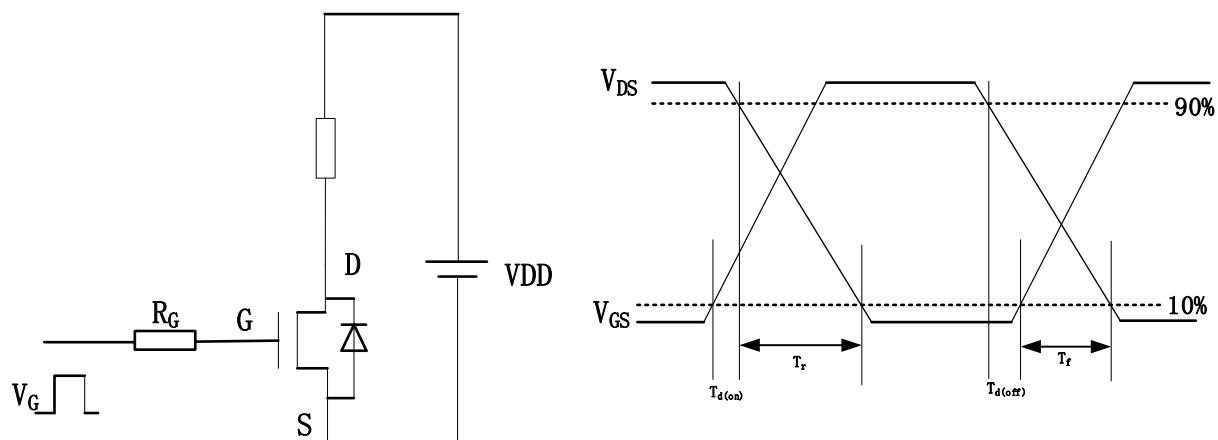


Figure 11 Resistive Switching time Test circuit and waveforms

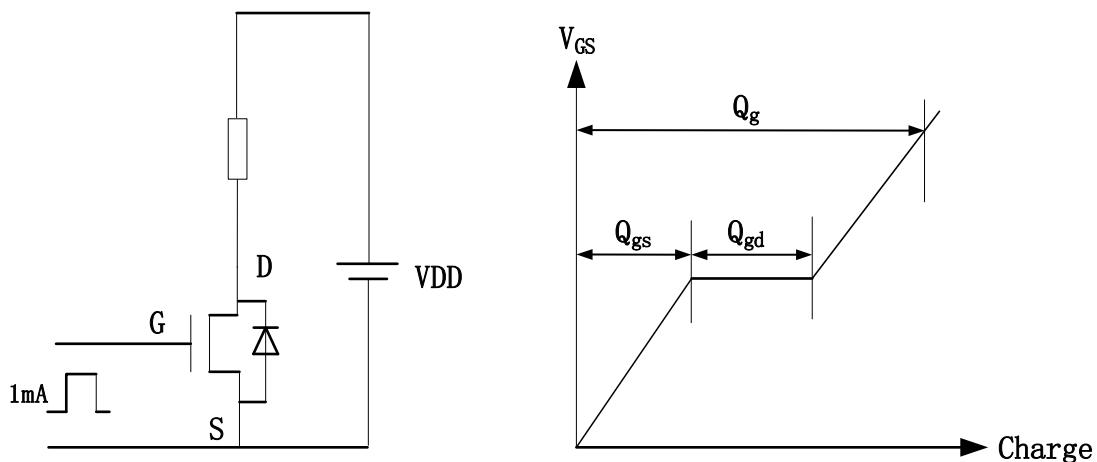


Figure 12 Gate charge Test circuit and waveforms



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