LC1813 Datasheet

Version 1.0.4

LC4.603.034UM

2013-04

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Revision History

Revision Number	Date	Description
v1.0.0	Jan 2013	Initial version
v1.0.1	Jan 2013	Modify *Table 3-2* COM_RAM size: to 4KB Modify *Table 3-4* SHRAM0/1 Corresponding External Space: to 0x8103_3FFF Remove the GSMIF0module in *Figure 1-1*, and modify the Digram
v1.0.2	Jan 2013	Remove NC pad in *Table 2-1* Add chapter *GPIO List* Modify *Figure 5-28* “rx” to “tx”
v1.0.3	Feb 2013	Modify *Figure 2-1,* adjust the ball number of DQ00-DQ31 Modify *Table 2-3*, adjust the ball number of DQ00-DQ31
v1.0.4	Feb 2013	1. Mdify A5 to A5_0, DTC3 to DTC3_0, and GSMIF to GSMIF0 2. Add DDR3 to MEMCTL module 3. Midfy the module sequence in Table 3-2, and add the SNOW3G module

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About the Book

The datasheet gives the main description of LC1813 features, system structure and detailed technical information of each module.

Applicable Object

LC1813 Chip datasheet provides engineers using the chip to design systems with necessary data and related guidelines. To use this manual to design system, users have to master the basic knowledge on communication and software programming and have some experience on using the working principle of ARM and DSP and the corresponding development tools.

Text Structure

The datasheet is separated into six chapters according to different functions and usages, main contents are summarized as follows:

- Chapter1 Overview: provides an introduction about LC1813 chip, including chip functional structure, memory, pin control, chip operation mode and modules overview.
- Chapter2 Pin Assignment and Signal Description: provides descriptions of pin allocation and package, including power/ground, analog signals and digital signals.
- Chapter3 Address Mapping: illustrates the Address Mapping relationship between internal registers and external memories.
- Chapter4 Interrupt System: lists all the interrupt sources and interrupt distribution of LC1813 chip.
- Chapter5 Electrical Characteristics: includes the electrical characteristics and recommended operation conditions of LC1813.
- Chapter6 Mechanical Characteristics: includes package information and package views.

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Definition of Terminologies

The following are abbreviations, full names in English explanation of the relevant terms used in the datasheet.

AC or ac	Alternating Current
AP	Application Processor
AHB	Advanced High-Performance Bus
ALU	Arithmetic and Logic Unit
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
ARM	Advanced RISC Machine
CMOS	Complementary Metal Oxide Silicon
CSI	Camera Serial Interface
CP	Communication Processor
DC or dc	Direct Current
DDR	Double Data Rate
DMA	Direct Memory Access
DSI	Display Serial Interface
DSP	Digital Signal Processor
DSDT	Dual SIM Dual Talk
EFUSE or eFuse	Electrical Fuse
EMU	Emulation
FIR	Fast Infrared
GPIO	General-Purpose Input Output
HS	High Speed
I2C	Inter-Integrated Circuit
I2S	Inter IC Sound
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
IO	Input Output

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IP	Intellectual Property
IR	Infrared
ISP	Image Signal Process
JEDEC	Joint Electron Device Engineering Council
JPEG	Joint Photographic Experts Group(Image format)
JTAG	Joint Test Action Group
LCD	Liquid-Crystal Display
LCDC	Liquid-Crystal Display Controller
LP	Low Power
MAC	Multiplier and Accumulator
MCU	Main Control Unit
MIPI	Mobile Industry Processor Interface (MIPI® is a registered trademark of Mobile Industry Processor (MIPI) Alliance.)
NA	Not Applicable
NAND	Not AND(Boolean Logic)
NOR	Not OR(Boolean Logic)
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PHY	Physical Layer
PLL	Phase-Locked Loop
POP	Package On Package
PWM	Pulse Width Modulation
RAW	Raw(Image format)
RGB	Red Green Blue(Image format)
RX	Receiver / Receive
SCL	Serial Clock: programmable serial clock used in the I2C interface (can be called also SCLK).
SDA	Serial Data: serial data bus in the I2C interface
SDIO	Secure Digital Input Output
SDMMC	Secure Digital MultiMedia Card

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SDRAM	Synchronous Dynamic Random Access Memory
SIM	Subscriber Identity Module
SIR	Slow Infrared
SoC	System on Chip
SRAM	Synchronous Random Access Memory
SSI	Synchronous Serial Interface
SYNC	Synchronous
SYS	System
TD-SCDMA	TD-Synchronized Code Division Multiple Access
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module
UTMI	USB2.0 Transceiver Macrocell Interface
YUV	Luminance + 2 Chrominance Difference Signals(PAL Y, Cr, Cb) Color Encoding

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Features

- **Low-power CMOS technology**
  - 40 nm LP(Low-Power) technology
  - 1.1V core voltage
  - IO Interface voltage:
    - 1.8V/1.2V
    - 1.8V/3V
    - 1.1V
    - 2.5V
    - 3.3V
    - 2.5V/1.1V
- **CPU**
  - Cortex-A7
    - Quad-core processor
    - L1 Cache(32KB ICache, 32KB DCache)
    - L2 Cache 512KB
  - ARM926(ARM926EJ-S)
    - Up to 468MHz
    - Cache(32KB ICache, 32KB DCache)
    - ITCM(8KB)
  - ZSP540
    - Up to 156MHz
    - Cache(32KB ICache, 16KB DCache)
    - On-chip Memory(128KB IMEM, 128KB DMEM)
- **Internal memories**
  - CP-side internal SHRAM
    - CP_SHRAM0 192KB
    - CP_SHRAM1 16KB
    - CP_SHRAM0 can be accessed by processor: ZSP540
    - CP_SHRAM1 can be accessed by processor: ARM926, ZSP540
  - SEC_RAM
    - 128KB
- **Multi-Media**
  - GPU(Graphics Processing Unit)
    - Mali400 Multi-Processor
    - Two Pixel Processors
    - A Geometry Processor
    - A 64KB Level 2 Cache
    - OpenGL ES 1.1/2.0 and OpenVG 1.1
    - Up to 312MHz
  - Video Decoder
    - MPEG-1/MPEG2 1080P@30fps
    - MPEG4 ASP Level 5 1080P@30fps
    - H.263 profile 0 level 70 D1(720×576)@30fps
    - H.264 HP level 4.1 1080P@30fps
    - VC-1 ASP level 3 1080P@30fps
    - DivX 1080P@30fps
    - AVS 1080P@30fps
    - VP6/VP7/VP8 1080P@30fps
    - Spark 1080P@30fps
    - RV 1080P@30fps
  - Video Encoder
    - MPEG-4 MP Level 4 720P@30fps
    - H.263 profile 0 Level 70 720P@30fps
    - H.264 HP level 5.1 1080P@30fps
    - VP8 1080P@30fps
  - ISP(Image Signal Processor)
    - System level
      - One MIPI 4-lane input interface
      - Serial SCCB interface
      - Parallel 10-bit DVP input interface
      - 12-bit RGB bayer input interface
    - Size and speed
      - Still capture mode
      - 5168x3876@30fps or @15fps 3D
      - Video mode
      - 2560x1600@30fps
      - 1080P@60fps or @30fps 3D
      - 720P@120fps or @60fps 3D
    - Basic ISP features

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- Auto exposure and gain control
- Auto white balancing
- Auto focus control
- Defect pixel correction
- Lens shading correction
- Color correction matrix
- 50/60Hz flicker cancellation
- Enhanced color interpolation
- Gamma correction
- Noise reduction
- Sharpness enhancement
- Brightness, saturation, hue and contrast control
- Digital zoom
- Auto dynamic range control
- Flash light control
- Mechanical shutter control

▪ Enhanced ISP features
- HDR/EDR video and still capture
- Video mode auto-focus
- Video anti-shaking
- ROI support
- Support RAW data capture
- EDR support
- HDR support
- Special effects support

– Display
▪ Supports MIPI interface
▪ MIPI DSI interface：
- Compliant with MIPI Alliance Specification for Display Serial Interface (DSI), Version 1.01.00 – 21 February 2008
- Supports up to 4 D-PHY Data Lanes

- **Communication**
– TH core
▪ Supports HSDPA/HSUPA
– A5_0/GEA/SNOW3G
▪ A5_0: A5_01/2/3 and KASUMI encryption
▪ GEA: GEA1/2/3, F8 and KASUMI encryption
▪ SNOW3G: UIA1/UIA2 and UEA1/UEA2
– Interfaces
▪ TD-IF: Supports single channel for receiving and transmitting
▪ GSM-IF: 1 interfaces, can be accessed by ZSP540
▪ SPI: 1 interfaces, for TDIF and GSMIF0
▪ SIM: 2 interfaces

- **Memory Interfaces**
– NAND FLASH
▪ 16/8-bit NAND FLASH
▪ 2 chip selects
▪ 1/4/8-bit ECC
– LPDDR2
▪ 2 chip selects
▪ 32-bit LPDDR2
▪ Up to 400MHz
▪ Up to 2GB address space

- **Security**
– Supports AES, SHA-1, SHA256 algorithms
– Supports Trust Zone

- **User Interfaces**
– Keyboard
▪ Supports 8 function keys
▪ Supports 2 Knob Encoders
– UART: UART0, UART1, UART2, UART3, COM_UART
– USB Interface
▪ 1 USB 2.0 High Speed OTG controller
– I2C: I2C0, I2C1, I2C2, I2C3, COM_I2C
– I2S: I2S0, I2S1
– SSI: SSI0, SSI1, SSI2, SSI3
– 2 PWM
– SDMMC: SDMMC0, SDMMC1, SDMMC2
– 2 JTAG

- **Interrupt Communication**
– CP_MAILBOX: Communication module of CP

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    - Interrupt communication for all CPUs in CP
    - Each interrupt source with 2-bit can be masked independently
    - Interrupt Communication between AP and CP
  - CTL: Communication module of AP
    - Interrupt communication between Cortex-A7
    - Interrupt Communication between CP and AP

- **DMA**
  - CP_DMAC
    - Common data exchange among CP_SHRAM0, CP_SHRAM1, ZSP540_RAM, and LPDDR2 in CP side
    - Supports memory to memory DMA transfers
    - Supports 3 channels
  - CP_DMAD
    - Fix every channel to specific module, and complete data exchange from module to memory, memory to module or memory to memory in CP side
    - Supports 17 channels
  - CP_DMAS
    - Complete data exchange between slow peripheral and memory in CP side
    - Supports peripheral to memory and memory to peripheral DMA transfers
    - Supports 4 channels
  - AP_DMAC
    - Common data exchange among, ISP ROM and LPDDR2 in AP side
    - Supports memory to memory DMA transfers
    - Supports 2 channels
  - AP_DMAG
    - complete data exchange between A9 Cache and LPDDR2 in AP side
    - Supports memory to memory DMA transfers
    - Supports 4 channels
    - Supports two-dimensional transmission
  - AUDIO_DMAS
    - Complete data exchange between audio peripheral and memory in AP side
    - Supports peripheral to memory and memory to peripheral DMA transfers
    - Supports 4 channels
  - AP_DMAS
    - Complete data exchange between slow peripheral and memory in AP side
    - Supports peripheral to memory and memory to peripheral DMA transfers
    - Supports 16 channels
- **Other Modules**
  - MUX_PIN: control of multiplexing function, pull-up and pull-down.
  - GPIO
    - Each GPIO can be independently configured to be input or output
    - Each GPIO can trigger interrupt

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Contents

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1 Chapter1 Overview

LC1813 is specially designed for mainstream multimedia TD-SCDMA Smartphone market. With CP and AP integrated in its SOC structure, LC1813 is based on Quad-Cortex-A7 processor, and 40nm LP CMOS technology, which leads to high performance, low power consumption. It supports 1080P HD video, 2D/3D hardware graphics unit and fast website exploring, imaging, games and other popular handset applications.

Figure 1-1 details the block diagram of LC1813.

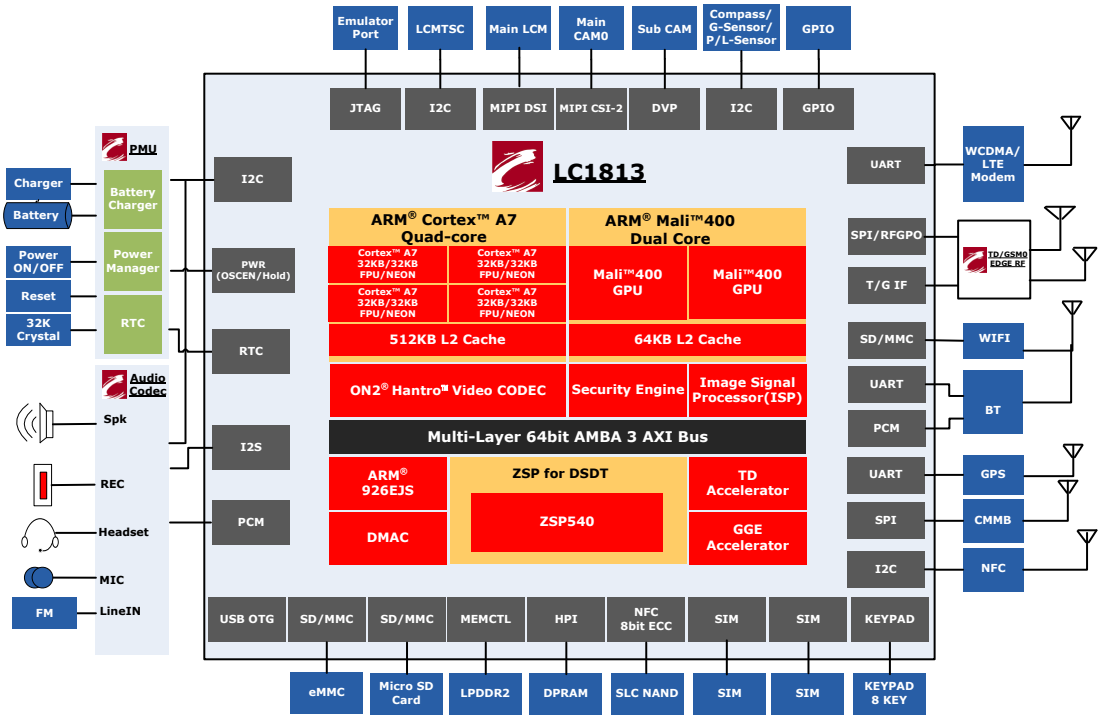

Figure 1-1 LC1813 BLOCK DIAGRAM

1.1 Functional Structure

The LC1813 is designed as a single chip solution that integrates the application processor (AP) and communication processor (CP). CP and AP functions are relatively separated, exchanging information via interrupts; both of them share one external memory controller to access external memory devices. COM_APB can be accessed by AP and CP.

LC1813's overall structure is as shown in *Figure 1-2*.

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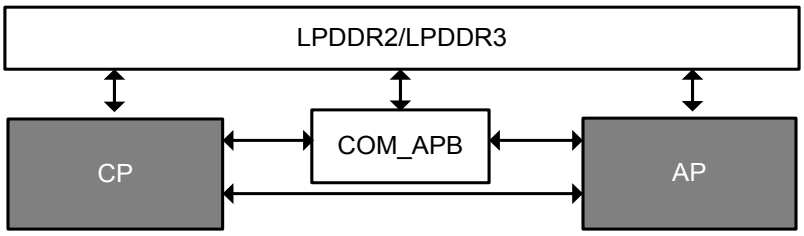

Figure 1-2 LC1813 Chip Overall Diagram

The main controllers of AP side is Cortex-A7 Quad-core processor, containing L2 Cache with 512KB. In addition, AP contains GPU, VEDIO_ACC, ISP and various peripheral controllers, etc. AP function structure is as shown in *Figure 1-3.*

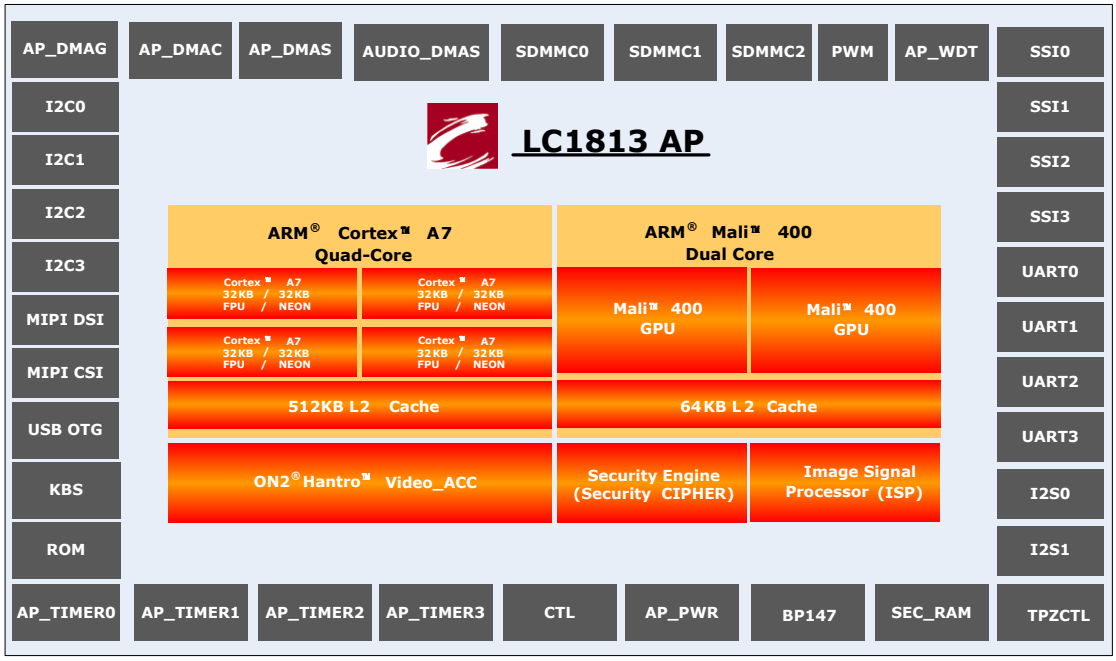

Figure 1-3 AP Function Diagram

CP is used to accomplish communication process function, which includes one ARM926 and one DSP processor (ZSP540), and associated with acceleration processors of TD-SCDMA/GSM. CP function structure is as shown in *Figure 1-4.*

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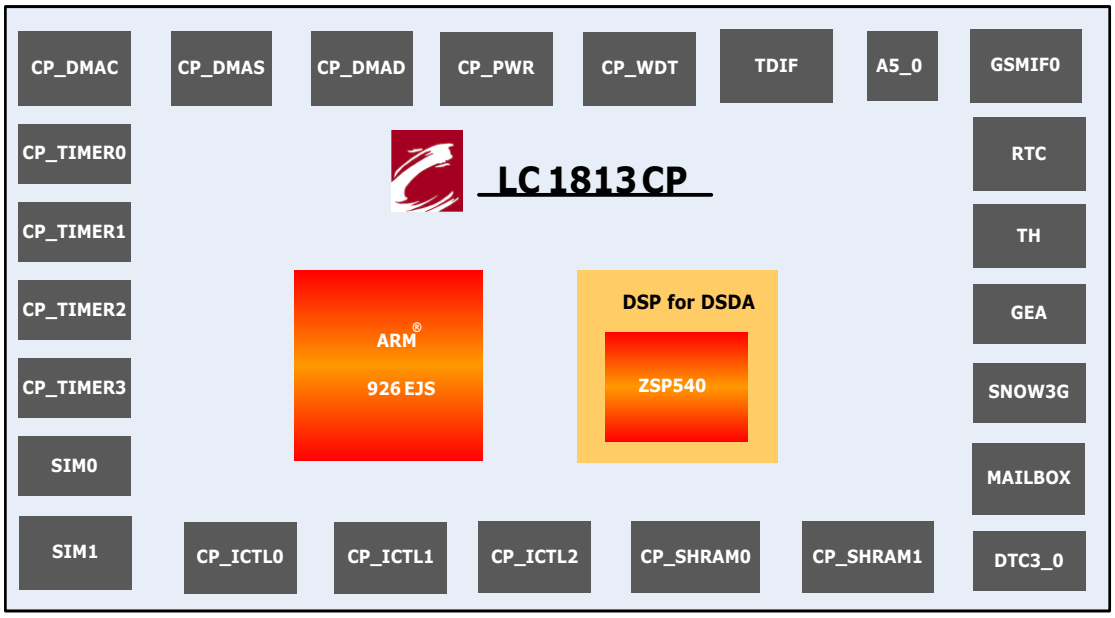

Figure 1-4 CP Function Diagram

COM_APB includes modules need to be accessed by AP and CP, the function structure is as shown in *Figure 1-5*.

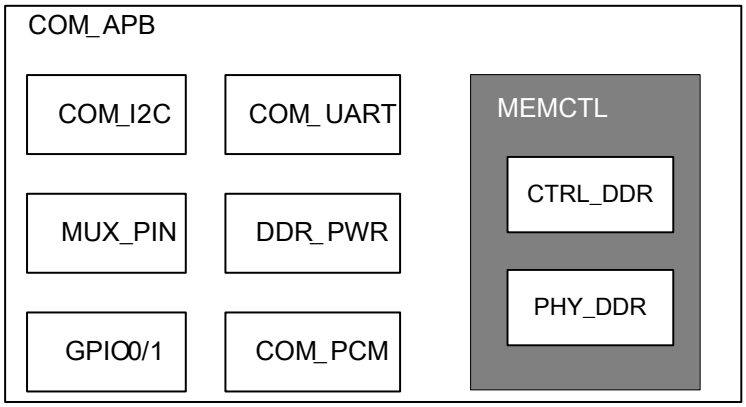

Figure 1-5 COM_APB Function Diagram

1.2 Memories

- Boot ROM: 64KB ROM
- Cortex-A7 internal RAM
  - 32KB ICache, 32KB DCache
  - 512KB L2 Cache
- ARM926 internal RAM
  - 32KB ICache, 32KB DCache
  - 8KB ITCM

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- ZSP540 internal RAM
  - 128KB IMEM, 128KB DMEM
  - 32KB ICache, 16KB DCache
- CP shared internal memory
  - 192KB CP_SHRAM0, 16KB CP_SHRAM1
- LPDDR2//LPDDR3
  - 32-bit data width
  - 2 chip selections
  - Up to 2GB address space

1.3 Pin Control

The pins of LC1813 chip includes anolog signals, power and ground signals, and digital signals. Most of the digtal signal pins are multiplex, namely, there are 2-4 digtal signals corresponding to a digtal signal pin. Additionally some pins have the pull-up or pull-down control. Please refer to the MUX_PIN module for all the detail descriptions about pin control.

1.4 Chip Operation Mode

- Power-on
  - When the chip is powered-on, AP_PWR starts to work at first, guiding AP to boot.
  - By default, CP is in sleep state when the chip is powered-on.
- Boot
  - AP boot: after powered-on, AP starts to boot up. Cortex-A7 enters working state.
  - CP boot: After receiving the interrupt from AP, CP starts to boot up. ARM926 first enters working state, while the processor ZSP540 is in reset state.
- Work
  - AP work: All CPU and modules on AP enter work mode
  - CP work: All CPU and modules on CP enter work mode
- power-off
  - Performed by AP

LC1813 Operation Status is as shown in *Figure 1-6*.

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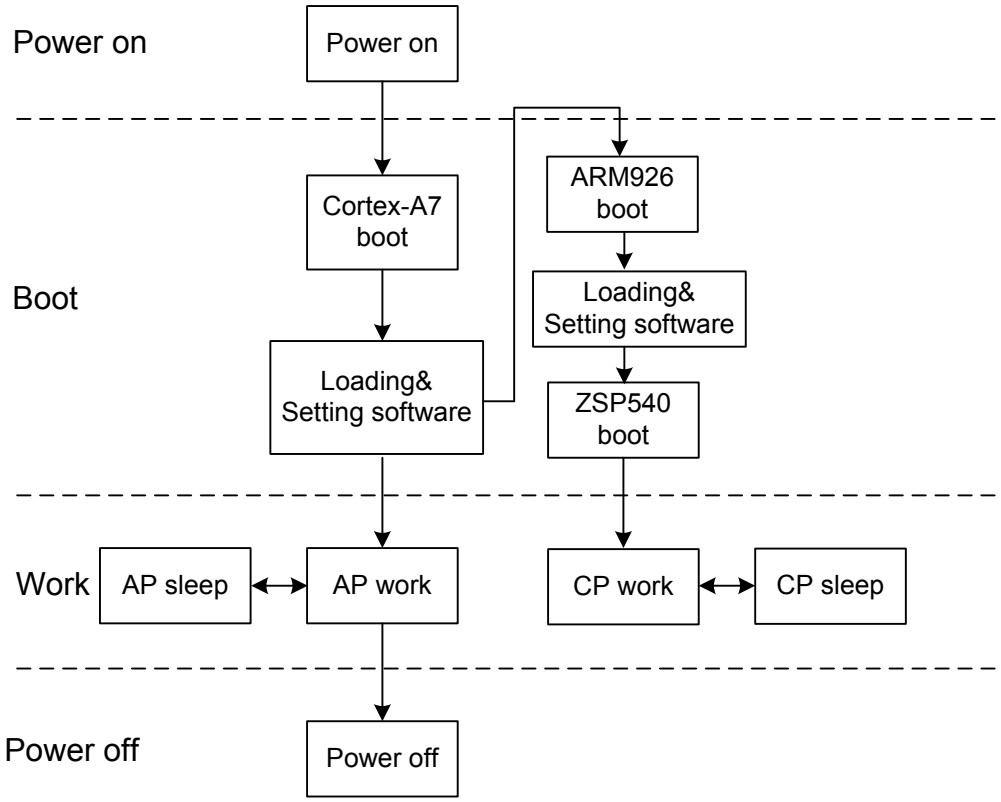

Figure 1-6 LC1813 Operation Status Diagram

1.4.1 Power-on Stage

The chip accomplishes the power-on operation as follows: start-up of external 32K clock (clk32k), start-up of external 26M clock (OSC26M0) and stabilization of PLL on AP. Then each clock of AP and COM_APB gets stable, and AP enters the boot stage while CP is in sleep state.

- During clk32k initialization, power-on reset signal (prst_n) remains LOW, when the clk32k is stabilized; prst_n goes to HIGH, which makes chip exit the global reset state. After about three clk32k cycles with prst_n remaining high, the signal osc_en0 goes to HIGH. The chip enters stage of OSC26M0 initialization.
- Osc_en0 enables OSC26M0 to start-up 26M clock, OSC26M0 stabilizing duration is fixed to 5ms in the power-on stage, so the user must ensure that OSC26M0 gets stable in 5ms.
- After OSC26M0 stable, internal PLL of AP starts up, and the stabilizing duration is 1.125ms.

The whole time of power-on stage is that the time of prst_n being low after power-on + 3* 32k cycle + 6.125ms.

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1.4.2 Boot Stage

After the chip is powered-on, Cortex-A7 enters working state.

1.4.2.1 AP boot

Initialization of AP is completed in the boot stage.

After the chip is powered-on, Cortex-A7 enters booting state: After AP_PWR accomplishing the reset of Cortex-A7 and suppling clock to Cortex-A7, Cortex-A7 enters working state and runs programs.

The booting manner of Cortex-A7 is decided according to the state of boot_ctl[0] (pin name is BOOTCTL0), boot_ctl[1] (pin name is BOOTCTL1), and boot_ctl[2] (pin name is BOOTCTL2) signals.

1.4.2.2 CP boot

After received interrupt from AP (for details please refer to the part of CTL module in manual), CP initialization is completed by the control of CP_PWR. Boot stage of CP includes three steps: ARM926 boot, Program loading and configuration, and ZSP540 boot.

- ARM926 boot

Receiving the interrupt from AP, ARM926 starts to work from address 0x0. ZSP540 is in reset state.

- Program loading and configuration

Program loading and configuration means some specific operations for the booting of ZSP540, such as moving its program to specified address, etc.

- ZSP540 boot

ZSP540 is in reset mode after power on and enters work mode once released by ARM926.

1.4.3 Work Stage

1.4.3.1 AP work stage

In the work stage, AP is in either running or sleep state. When AP is in the running state, If AP_PWR supervises the work state of Cortex-A7 and each DMA (AP_DMAG, AP_DMAS, AP_DAMC and AUDIO_DMAS), and if Cortex-A7 and each DMA are in idle state, then AP_PWR will make AP enter sleep state.

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In the sleep state, most modules' clocks in AP are disabled, and the modules which have independent power supplies can power off, so that AP enters into low power consumption state.

AP_PWR enters the wake-up process if interrupt is asserted, and control AP to running state from sleep state.

1.4.3.2 CP work stage

In the work stage, CP is in either running or sleep state. When CP is in the running state, CP_PWR supervises the wirk state of ARM926, ZSP540 and each DMA (CP_DMAC, CP_DMAD and CP_DMAS). If ARM926, ZSP540 and each DMA are in idle state, then CP_PWR will make CP enter sleep state.

In the sleep state, most modules' clocks in CP are disabled. The parts of 32KHz clock field in CP_PWR, RFIF, and RTC modules is active, and the power supply of COM_ACC and ARM926 can powered off.

CP_PWR enters the wake-up process if interrupt is asserted, and control CP to running state from sleep state.

1.4.4 Power-off Stage

When chip is in running state, the processor will control the chip to enter the power-off stage after receiving the appropriate triggers (such as press the Power-off key). In the Power-off stage, the application program performs relative operations, and notifies PMU to power off by de-asserting "PWEN".

1.5 Chip Module Overview

1.5.1 AP Functional Module

1.5.1.1 Cortex-A7

The subsystem of Cortex-A7 includes:

1. Cortex-A7 MPCore
2. The Cortex-A7 MPCore consists of 4 Cortex-A7 cores in a cluster and a Snoop Control Unit (SCU) that can be used to ensure coherency within the cluster.
3. Coresight components

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Standard Coresight Components integrated internally, and it is used for invasive debugging and noninvasive debugging of Cortex-A7, including four ETMs, four CTIs, a ROM table, a CTM, etc.

4. MBIST controllers of Cortex-A7

Built-in MBIST controllers are used for memory testing of Cortex-A7.

1.5.1.2 Shared RAM of AP (AP_SEC_RAM)

AP_SEC_RAM is a memory module with size of 128KB, supporting 8bits (Byte), 16bits (Halfword), 32bits (Word) and 64bits (Dword) reading-writing operations.

AP_SEC_RAM consists of RAM with redundancy check. Cooperating with EFUSE, and AP_SEC_RAM can remap certain damaged bit line to redundant bit line to perform self-reparing.

AP_SEC_RAM can be used for exchanging data between several masters as a shared memory. AP_SEC_RAM can be accessed by Cortex-A7 and AP_DMAG.

The secure region of AP_SEC_RAM can be configured by setting register BP147_SR_SIZE of BP147 module; and the secure region of AP_SEC_RAM can be accessed only if master issues secure access.

1.5.1.3 ROM

ROM is used to store booting program with size of 64KB.It can be accessed by Cortex-A7 only.

1.5.1.4 AP System Controller (CTL)

CTL is used for interrupt communications among multiple CPUs, and also for configuration of some modules which includes ICM priority control of AP.

CTL can be accessed by Cortex-A7.

Features:

- interrupt communications among CPUs
  - the interruption from ARM926 to AP(32 sources. Interrupt enable register, interrupt status register, interrupt raw status register are in CTL module; and interrupt generate register is in CP MAILBOX module) is sent to Cortex-A7.

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- the interruption from AP to ARM926(32 sources. Interrupt generate register, interrupt generate signal register are in CTL module; interrupt enable register, interrupt status register,and interrupt raw status register are in CP MAILBOX module).

Each interrupt source is maskable. The interrupt is asserted by sender but de-asserted by receiver. The control signal is returned by ARM926 of CP side to clear interrupt from AP to ARM926.

- ICM priority control
  - Controls system ICM to arbitrate the priority levels of masters
- Low power control function
  - Includes low power control of AP_DMAC module, CTL module and MH2X channel
- 32k debounce functional control register
- Arbitration function
- Registers associated with USB0
- Registers associated with Cortex-A7 booting address
- Configurable registers associated with ISP PHY
- Registers associated with SSI protocol
- Responding time control of RAM

1.5.1.5 General Direct Memory Access Controller (AP_DMAG)

AP_DMAG supplies DMA function, and is used for data transfer with up to four channels. Each channel has a set of corresponding registers.

AP_DMAG can be accessed by Cortex-A7.

Features:

- Up to four channels, with programmable channel priority.
  - FIFO per channel, with the width of 64 bits and the depth of 16
  - Source and destination address of each channel can point to both AP address space and LPDDR2/LPDDR3 address space
  - Source reading of channel0, destination writing of channel1, and channel2 will first access Cortex-A7 via ACP port. Please refer to CTL module chapter for the operation
- Supports two-dimensional transmission
- Programmable source and destination address

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- The unit of channel data transfer is Byte, supporting unaligned transfer
- Programmable X-direction Size with a range of 1 Byte - 65535 Bytes
- Programmable Y-direction Size with a range of 1 Byte - 65535 Bytes
- Supports transfers using linked lists, with a embedded 4Kb RAM for storing linked list items
- Supports of switching off the channel forcedly
- Supports low power mode

1.5.1.6 AP Direct Memory Access Controller (AP_DMAC)

An AP_DMAC is integrated in LC1813 as the flow controller for massive data transfers, and can be used as master device or slave device. As a slave device, AP_DMAC can be accessed by Cortex-A7. While as a master device, it can access ISP ROM, and DDR2, and perform data transfers among them.

There are two channels of AP_DMAC with related registers per channel.

Features:

- Up to two channels, with programmable channel priority, and unidirectional data transfers. FIFO per channel, with the same depth of 64
- Master device interface
- Address generation
  - Supports the programmable source address and destination address
  - Supports three modes of address change
  - Supports three modes of multi-block transfers
  - multi-block transfer source address and destination address are independently controlled
  - Source gather/destination scatter(GATHER/SCATTER)
- Access control
  - Programmable channel transfer type
  - Programmable enable and disable of DMA channel
  - Supports the suspending of AP_DMAC operation
  - Programmable size of Block
  - Programmable transfer width

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- Interrupt
  - Supports 3 interrupt types
  - Supports Interrupt Enable

1.5.1.7 Reduced Direct Memory Access Controller (AUDIO_DMAS)

AUDIO_DMAS comes with DMA function, enabling to automatically migrate data from peripheral to memory and vice versa under CPU control.

It can be accessed by Cortex-A7

Features:

- Transfer channel is divided into DMA receiving channel and DMA transmitting channel of peripheral.
- Contains 3 peripheral receiving channels and 3 transmitting channels, with channel priority configurable

DMA Receiving Channel of Peripheral:

- Source addresses remain unchanged, and width of FIFO addresses corresponding to peripherals can be set as Byte, Halfword and Word
- Destination addresses change continuously by adding 1.
- Transfer is divided into block transfer and variable-length transfer.
- Block transfer works in this way:
  - With block transfer enabled, DMA transfers data automatically, and receives set length of block data before returning and issuing interrupt
  - Length of block, which is measured in byte, can be set
  - Starting address of destination buffer is aligned with 4 Bytes, and size of buffer is integral multiple of 4 Bytes
  - Current destination buffer address indicates data address written to current destination buffer.
- Variable-length transfer works in this way:
  - After being started, DMA automatically detects and receives data from relevant peripherals. The internal cache is enough for a 32Byte to be written in designation buffer after Burst.
  - Destination buffer supports circular buffer address mode;

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- Current destination buffer address indicates data address written to current destination buffer
- CPU writable register will write residual data of internal buffer in DMA channel to destination buffer
- Enable hardware to detect activity status of peripheral. If no data arrive within a given time interval (it can be set by the software), write residual data in internal buffer to destination buffer, and generate Flush interrupt;

DMA Transmitting Channel of Peripheral:

- Destination addresses remain unchanged, and width of corresponding FIFO addresses can be set as Byte, Halfword and Word.
- Source addresses change continuously by adding 1.
- Supports single block transfer and continuous transfer.
- Length of block, which is measured in byte, can be set.
- Source addresses change continuously by adding, while destination addresses remain unchanged.
- The starting address of source buffer can be arbitrary.

1.5.1.8 Simplified Dedicated Memory Access Controller (AP_DMAS)

AP_DMAS provides DMA function, which can automatically move the data from peripheral to Memory and from Memory to peripheral under the control of CPU.

It can be accessed by Cortex-A7.

Features:

- Up to 8 receiving channels and 8 transmitting channels, with configurable channel priority.

DMA receiving channel:

- Fixed source address pointing to peripheral FIFO with width value set of Byte, Halfword and Word
- Successive destination address increment of 1
- Block transfer mode and variable-length transfer mode
- block transfer mode

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- Transfers data automatically once started, returns to idle state and asserts interrupt if blocks of programmed Block Length are received.
- Programmable Block Length in byes
- The start address of target buffer is aligned to 4 bytes boundaries, and the buffer size is multiples of 4-byte
- Current target buffer address indicates the address of last entered data

- Variable-length transfer mode
  - When it is started, DMA will automatically detect and receive related peripheral data. When internal buffer reaches 32Bytes, it will be written into target buffer.
  - Target buffer supports cyclic addressing mode
  - Current target buffer address indicates the address of last entered data
  - Specific register is configured by CPU to write data left in internal buffer into target buffer
  - Supports hardware detection of peripheral activity state to perform transfers of data left in internal buffer to target buffer if no data entering in some duration(software programmable), and assert interrupt

DMA transmitting channel:

- Fixed target address pointing to peripheral FIFO with width value set of Byte, Halfword and Word
- Successive destination address increment of 1
- Supports single Block transfer and continuous Block transfer
- Programmable Block Length in byes
- Starting address of target buffer is arbitrary

1.5.1.9 Display Subsystem (DISPLAY)

Display subsystem accomplishes to output video frames or image frame of on-chip or off-chip memory to peripheral display devices. It contains one LCDC controller and one MIPI interface controller, EDPI connects MIPI interface with LCDC interface. DISPLAY module can be interfaced display devices with MIPI.

DISPLAY module can be accessed by Cortex-A7.

The features will be listed on the basis of MIPI interface.

Display System:

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- Supports MIPI interface
- Supports resolution up to 1920x1080@60Hz
- Supports security property, software can configure each layer's security property of LCDC controller via BP147 module

LCDC Controller:

- Supports input image formats of ARGB8888, ABGR8888, RGB1555, RGB888(unpacked), RGB666(unpacked), RGB565 and YUV422(packed)
- Independent pixel data FIFO: layer0 FIFO with 64-bit width and 384 depth; the other two layers with 64-bit width and 256 depth
- Each layer supports input data bytes swapping. When a layer's bytes swapping is enabled, high/ low 16bits data of each 32bits word will be swapped firstly, and then the data will be written into FIFO
- Supports overlapping output of three layers at most; supports two modes: the same alpha coefficient for overlapping entire layer, and different alpha coefficient for overlapping each pixel(input pixel must be in ARGB, ABGR or RGB1555 format)
- The screen's background color is fixed as black
- Each layer's window can be enabled and disabled independently
- The display order of 3 layers is fixed as layer0 at top layer and layer2 at bottom layer
- Each layer window can be configured by following coefficients: window size(the width in pixels), the display starting position of window in background screen(the starting position of X direction in pixels), key color(each layer's window can be enabled independently), 8-bit transparency(can be enabled per layer independently)
- Layer1 and layer2 support video YCrCb4: 2: 2 format data input, and support transition from YCrCb4: 2: 2 to RGB format
- Support auto-refresh regularly, the cycle of auto-refresh is configurable
- Each layer has two source addresses, and supports dual-frame operation, each layer's source address can be selected
- MIPI video interface, the interface between LCDC controller and IP of MIPI DSI controller. It supports DPI-2 standard
- Supports hardware cursor
  - 2bits per pixel mode, up to 64 pixels x64 lines
  - 1bit per pixel mode, up to 128 pixels x64 lines
  - Cursor overlapping supports four modes
    - Transparent

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  - Invert
  - Color1
  - Color2

- LCDC can issue security or insecurity layer accessing, and each layer has a LOCK controlling signal from BP147. The layer's address and size's parameter are locked and can't be configured once the signal gets HIGH.

MIPI:

- APB BUS interface
- Supports MIPI DSI interface protocol
- Supports RGB565, RGB666(packed or unpacked), RGB888(packed or unpacked) format
- Supports MIPI PPI D-PHY
- Supports command mode and video mode
- Supports the maximum of 4 D-PHY data lanes, and Lane0 supports intercommunication and Escape mode.
- Display resolution is configurable
- Supports virtual channel
- Supports low power mode
- Supplies error detection and resuming function
- Supports EoTp(End of Transmission Packet)
- Supports ECC and checksum

1.5.1.10 Image Signal Processor (ISP)

LC1813 contains an image signal processor. Cooperating with interfaced image sensor, it can accomplish the function of sampling and processing of image signals. Image signal processor is called ISP for short.

ISP supports most CMOS image sensors, and has parallel and serial interfaces. Serial interface adopts high-speed CSI-2 MIPI.ISP also supports some simple CMOS image sensors without image preprocessing. Internal interfaces of ISP are 32-bit AHB and 64-bit AXI, and ISP can process internal image data through these interfaces.

ISP supports the image resolutions from QCIF to 13MP and functions of sophisticated defected pixel cancellation and image noise reduction, so high quality image can be guaranteed when common CMOS image sensors with low cost and high resolution are used

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for mobile devices.

ISP module can be accessed by Cortex-A7.

Features:

- Interface type:
  - Camera interface with 12bit RGB bayer input
  - One 4-MIPI input interfaces(only static image is supported)
  - One SCCB interface
  - Parallel 10-bit DVP input interface
  - Maximum image pixeles 1300w(4224x3168)
  - Maximum system clock no slower than 132M
  - 32-bit AHB slave interface
  - 64-bit AXI master interface
- Basic characteristics
  - AECAGC, automatic exposure and gain control
  - AWB, automatic white balance
  - AFC, autofocus
  - 50/60Hz flashing light elimination
  - Flashlight control
  - mechanical shutter control
  - LENC, lens shadow correction
  - DPC, dead point detection
  - Filter of sharping and reducing-noise
  - Enhence color
  - CCM, Color Correction Matrix(RGB bayer eliminating mosaic)
  - γCorrection
  - Digital zoom lens and continuous size adjustment
  - YcbCr 422/420 process
  - Special effects support

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1.5.1.11 Video Codec Unit(VIDEO_ACC)

VIDEO_ACC accomplishes hardware acceleration of video encoder and decoder; supports protocols such as MPEG4, H.263, H.264, RV9, AVS, JPEG, etc. This module can implement hardware acceleration of frame-level video decoding operations to accomplish video image codec. VIDEO_ACC module contains one decoder and two encoders. The encoder's work clock frequency is up to 208MHz, and the decoder's is up to 312MHz.VIDEO_ACC module supports independent power-off.

Features:

- Video Decoder
  - Supports H.264 decoding with image maximum resolution of 1080P
  - Supports SVC decoding
  - Supports MPEG-4 decoding
  - Supports H.263 decoding with image maximum resolution of 720x576
  - Supports Sorenson Spark decoding
  - Supports MPEG-2 decoding
  - Supports MPEG-1 decoding
  - Supports VC1 decoding
  - Supports JPEG decoding
  - Supports RV decoding
  - Supports VP6/7/8 decoding
  - Supports AVS decoding
  - Supports DivX decoding
  - Supports Post-Processor, including Alpha Blending, Deinterlacing, Dithering, Scaling, Rotation and RGB Conversion
  - Supports OpenMAX IL v1.1.2 base profile
- Video Encoder
  - Supports MPEG-4 encoding with image maximum resolution of 1280x1024
  - Supports H.263 encoding with image maximum resolution of 720x576
  - Supports image preprocessing, including RGB to YUV420 format conversion, YUV422 format to YUV420 format, angle switching and image cutting
  - Video Stabilization

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- Supports H.264 encoding
- Supports VP8 encoding
- Supports JPEG encoding
- Supports image preprocessing
- Video Stabilization
- Supports OpenMAX v1.1.2 base profile

1.5.1.12 Graphics Processing Unit (GPU)

Mali-400 MP GPU, which is a hardware accelerator and is broadly used in 2D/3D system, is integrated to perform graphic process in LC1813.

GPU contains several parts as following:

- Two pixel processors
- A Geometry Processor
- A L2 CACHE controller
- Three memory management units
- A power management unit

GPU supports following features:

- Supports OpenGL ES 2.0
- Supports OpenGL ES 1.1
- Supports OpenVG 1.1
- Frequency of up to 312MHz
- Pixel processor features:
  - Each pixel processor used processes a different tile, enabling a faster turnaround
  - Programmable fragment shader
  - Alpha blending
  - supports Complete non-power-of-2 texture
  - Cube mapping
  - Fast dynamic branching
  - Fast trigonometric functions, including arctangent
  - Full floating-point arithmetic

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- Framebuffer blend with destination alpha
- Indexable texture samples
- Line, quad, triangle and point sprites
- No limit no program length
- Perspective correct texturing
- Point sampling, bilinear, and trilinear filtering
- Programmable mipmap level-of-detail biasing and replacement
- Stencil buffering, 8-bit
- Two-sided stencil
- Unlimited dependent texture reads
- 4-level hierarchical Z and stencil operations
- Up to 512 times Full Scene Anti-Aliasing (FSAA).4x multisampling times 128x supersampling
- 4-bit per texel compressed texture format

- Geometry processor features
  - Programmable vertex shader
  - Flexible input and output formats
  - Autonomous operation tile list generation
  - Indexed and non-indexed geometry input
  - Primitive constructions with points, lines, triangles and quads
- L2 CACHE features
  - 64KB
  - Four sets linked up
  - Supports up to 32 outstanding AXI transmissions
  - Cache line/line fill burst: 64 bytes
  - Supports no cache reading-writing bursts at range of 8-64bytes
  - Limited by the rule of AXI order, hit-under-miss and miss-under-miss are supported
  - Standard pseudo-LRU arithmetic
- Memory management unit

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- Each processor has independent MMU used for controlling and transforming access operations from CPU

- Power management unit
  - Can be controlled by software programming
  - Trigger interrupt when device is awakened

1.5.1.13 NAND FLASH Controller (NFC)

NFC module is the device interface timing controller used to exchange data with peripheral NAND FLASH memory. NFC can be accessed by Cortex-A7 and AP_DMAS.

Features:

- Supports 8-bit/16-bit NAND FLASH memory interface
- Interface timing can be set by programming the register
- 16x16-bit FIFO in transmitting direction and 16x16-bit FIFO in receiving direction as buffer
- Provides AP_DMAS Hardware Handshaking, and data exchange can be performed automatically by AP_DMAS
- Provides 1-bit ECC checkout function for data read/write, which can accomplish up-to 1-bit debug and 2-bit detection per 512 Bytes data. By default, 1-bit ECC checkout is supported.
- Provides 4-bit ECC checkout function for data read/write, which can accomplish up-to 4-bit debug per 512 Bytes data
- Provides 8-bit ECC checkout function for data read/write, which can accomplish up-to 8-bit debug per 512 Bytes data
- Command issuing modes include: FIFO mode and REG mode

1.5.1.14 Security Controller (SECURITY)

SECURITY module is security control module in LC1813, and it contains one 512-Byte Efuse, which accomplishes the functions of storing chip ID, key, function identification, ECC check code, RAM redundancy repair, and ECC check code of redundancy repair; it supplies 4 security control identifications including Cortex-A7 booting location, security enable, JTAG enable and TPZ lock; embedded ECC arithmetic, one-bit checkout of Efuse data; embedded low power module to accomplish low power control; it supplies debug and Cortex-A7 write-permission control signal; it can be accessed by Cortex-A7.

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Features:

- Supplies four security control identifications
  - Supplies 1 bit identification to indicate whether Cortex-A7 is running in Boot ROM or not
  - Supplies 1 bit chip security enable identification for indicating whether chip security is enabled or not
  - Supplies 1 bit JTAG function enable identification for indicating whether JTAG function is closed or not
  - Supplies 1 bit TPZ lock identification for indicating whether configuration of DDR access is locked or not
- Supplies 32 bits chip ID, and each chip ID is unique
- Supplies five 128-bit keys, the same version chips have the same keys
- Supplies 13 bits function identification field for chip functions and characteristics
  - Supplies 1 bit security enable identification for controlling chip's safe mode
  - Supplies 1 bit JTAG function enable identification for controlling JTAG's state
  - Supplies 2 bits recording/video enable identifications for separately controlling MIC's state and Camera's state
  - Supplies 2 bit Cortex-A7 uni/dual/ Quad core identification
  - Supplies 2 bits SDMMC access identification for controlling the accesses of SDMMC0 and SDMMC1 in different modes
  - Supplies 2 bits Cortex-A7 frequency locking identification for controlling Cortex-A7's maximum frequency
  - Supplies 1 bit Function identification for controlling chip to supply HSUPA or not.
- Supplies 24bits ECC checkout code, embedded ECC arithmetic; one-bit checkout of Efuse data
  - Embedded ECC arithmetic of Hamming code checkout, and one-bit checkout of data
  - Generates 24bits ECC checkout value for external data written into Efuse
- Supplies RAM redundancy repair for SHRAM0, SEC_RAM
  - Supplies redundancy repair function of three 64KB RAMs of CP_SHRAM0
  - Supplies redundancy repair function of four 32KB RAMs of AP_SEC_RAM
  - Each of RAMs redundancy repair signals contains two 1bit-enable-signals and two 5bits address signals
- Supplies 24bits ECC checkout code of redundancy repair; one-bit checkout of data in

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RAM redundancy repair

- Supplies the switching of different modes for chip, and controls the access of SDMMC and Efuse in different safe modes
  - Supplies 6 safe states such as boot state, common work state, non-security state, security state and two switching states when switches between non-security state and security state
  - Controls the access of Efuse space in different safe modes
- Supports 32bits AHB slave, and can be accessed by Cortex-A7
- Supports Efuse locked function by external operations. Reading externally and programming Efuse data will be not allowed after package test
- Supplies debugging of Cortex-A7 and CoreSight, control signal of write permission
- Low power control
  - Supports clock is automatically disabled by hardware when AHB slave interface is inactive
  - Supports Efuse power is automatically disabled by harsware after reading the data in Efuse.
  - Supports clocks of related modules with Efuse is disabled when Efuse is not accessed

1.5.1.15 Encryption/Decryption and Digital-signature Module (CIPHER)

CIPHER contains two sub-modules: AES encryption module and SHA signature module, which is used to implement AES encryption/decryption calculation and SHA-1/SHA-256 signature calculation. DMA channels are embedded on CIPHER - one read-only channel for each of SHA and AES, one write-only channel for AES.

This module can be accessed by Cortex-A7.

Features:

- AES encryption module
  - Supports standard AES, AES-CM, AES-F8 algorithms
  - Key size: 128bits, 192bits, 256bits
  - Supports two input modes for packet data: embedded DMA and CPU
  - Standard AES algorithm supports encryption/decryption calculation

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- AES-CM, AES-F8 algorithms support encryption calculation only

- SHA signature module
  - Input message with any size
  - Supports two algorithms: SHA-1 with output size of 160bits and SHA-256 with output size of 256bits
  - supports two input modes: embedded DMA and CPU

1.5.1.16 Universal Serial Bus Controller (USB)

USB is mainly used to exchange large volume of high-speed data with peripheral USB devices/host. It can act as USB host to perform data exchanging with the USB0 device directly, also it can act as USB device to communicate with other host. USB OTG controller has an AHB slave interface and embedded DMA controller, so it can work in both Slave mode and DMA mode. USB OTG supports USB 2.0 high-speed (HS, 480-Mbps), full-speed (FS, 12-Mbps) and low-speed (LS, 1.5-Mbps) modes.

USB OTG controller can be accessed by Cortex-A7.

Features:

- Supports USB 2.0 high-speed, full-speed and low-speed modes
- Supports On-The-Go Supplement to the USB 2.0 Specification(Revision 1.0a)protocol(OTG); supports Host mode and Device mode
- Supports UTMI + Level 3 interface, 16-bit data line
- Supports SRP protocol
- Supports HNP protocol
- Only supports point-to-point transmission
- Supports 15 endpoints in Device mode, including bidirectional endpoint (endpoint 0), IN endpoint (endpoint 1-7), OUT endpoint (endpoint 8-14).The transfer type supported by endpoint can be configured by software
- Supports up to 16 host channels in Host mode, and periodic OUT channel is supported
- Supports packet-based, Dynamic FIFO memory allocation and flexible, efficient use of RAM
- Provides support to change an endpoint's FIFO memory size during transfers
- Total data FIFO RAM size is 5728×32, where RX FIFO (maximum 2880x32), non-periodic TX FIFO (maximum 1024x32), HOST mode periodic TX FIFO (maximum1792x32) shares; the maximum depth of endpoint 0-4 is 256, the maximum depth of endpoint 5-7 is 512.

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- Supports Slave and DMA modes
- Interfaces for the application via the AHB: AHB interface for accessing Control and Status Controller, the Data FIFO

1.5.1.17 SEC_APB

1.5.1.17.1 I2C Interface Controller2 (I2C2)

I2C interface controller mainly accomplishes I2C interface.LC1813 integrates one I2C module which is hung on the SECURE_APB bus, and can be accessed by Cortex-A7.

Features:

- 2-line I2C serial interface
- Transfer speeds
  - Standard mode(100Kbps)
  - Fast mode(400Kbps)
  - High-speed mode(3.4Mbps)
  - Support clock sync
- Work as a I2C Master
- Supports multiple Master mode(bus arbitration)
- 7-bit or 10-bit addressing
- Includes the Transmit FIFO with the width of 8 bits and depth of 16
- Includes the Receive FIFO with the width of 8 bits and depth of 16

1.5.1.17.2 Keyboard Controller (KBS)

KBS supports 8 independent keys. In which, four of 8 independent keys can be used for input as two groups of knob keys(a group of knob key contains two key-value input pins), the module contains two knob key-value detectors, which can control internal knob counter according to input key-value of knob key.

The pins of KBS are multiplexed with other pins of functional modules.

KBS supports matrix keypad, independent keys and knob keys.

It can be accessed by Cortex-A7.

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Features:

- Supports up to 8 independent keys input
- Supports 6 independent keys and one group of knob key input
- Supports 4 independent keys and two groups of knob key input
- Key-value can be read by separate internally module registers at one time
- Each independent key has separate interrupt
- Each pin of independent keys can be configured pull-up respectively
- Supports independent debounce gap detection function, this function can also be disabled by software

1.5.1.17.3 Synchronous Serial Interface Controller 2(SSI2)

SSI is the module used to communicate with external synchronous serial interface.SSI2 supports Motorola's SPI protocol and TI SSP protocol.SSI2 is synchronous serial master device interface.

SSI2 module can be accessed by Cortex-A7.

Features:

- Interrupts enabled respectively
- Users can adjust the data transfer rate. SSI2 master device’s maximum transfer rate is ssi2_mclk/2(the default value of ssi2_mclk is 19.5MHz)
- Users can set the data frame format(4 – 16 bits)
- Depths and width of receiving FIFO and transmitting FIFO are respectively 16 and 16bits
- Supports Motorola SPI protocol and TI SSP protocol
- SSI2 synchronous serial master device
- SSI2 only supports one slave device

1.5.1.17.4 Security Attribute Controller (BP147)

BP147 is a security configuration module, only can be accessed in safe mode. It is used for controlling security zone of AP_SEC_RAM, security property of each layer of LCDC, and security property of each channel of AP_DMAG

BP147 can be accessed by Cortex-A7.

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Features:

- Controls security zone of AP_SEC_RAM
- Controls security property and parameter locking of each layer of LCDC
- Controls security property and parameter locking of AP_DMAG

1.5.1.17.5 SDMMC Interface Controller (SDMMCx)

LC1813 integrates three SDMMC interface controllers at AP side, each SDMMC is hung on SECURE_APB bus of AP side, indicating each of SDMMC controllers supports security access attribute.

Three SDMMC controllers are exactly the same in addition to base address, control clock register of AP_PWR, and pin signal name. Therefore, SDMMC implicitly indicates SDMMC0, SDMMC1, and SDMMC2 except in description referring to base address, control clock register of AP_PWR and pin signal name.

SDMMC interface controller can control data any information exchange between LC1813 and SD memory (SD Memory Card), SDIO (SDIO Card), MMC (MultiMedia Card).

SDMMC can be accessed by Cortex-A7.

Features:

- FIFO width of 32 bits, FIFO depth of 64
- Data lines supported by SDMMC
  - SDMMCx(x=0, 2): up to 4 data lines
  - SDMMC1: up to 8 data lines
- Supports multiple types of memory card:
  - SD card(SD mem – version 3.0)
  - SDIO(SDIO – version 3.0)
  - MMC card(MMC – version 4.41)
- Supports secure access property. When SDMMC secure access property is enabled, each register of SDMMC controller can’t be accessed by Cortex-A7 at Non-secure state
- Provides individual clock control to selectively turn ON or OFF clock to a card
- Supports Command Completion Signal and interrupts to host.
- Supports CRC generation and error detection.
- Supports programmable baud rate.
- Supports clock control

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- SDMMC0 supports card detection and write-protect detection, but SDMMCx(x=1, 2) doesn't
- Supports write protection.
- Supports SDMMC suspend and resume operation.
- Supports SDMMC read wait
- Supports block size of 1 to 65, 535 bytes.
- Embedded DMA

1.5.1.17.6 Memory Security Zone Controller (TPZCTL)

TPZCTL is the TPZ control module in LC1813, and supplies one 32bits APB slave interface. It can be accessed by Cortex-A7, and used for configuring the access of TPZ module to DDR's security zone and generating interrupt according to TPZ module's return signal. TPZCTL provides generation of random number.

Features:

- TPZ control
  - Divides DDR's security zone and attribute
  - Accomplishes DDR access configuration
  - Supports the configuration of security zone locked
  - Random number generation
- Interrupt
  - Interrupt for unauthorized access to DDR
  - Random number generation interrupt
  - Supports interrupt enable and mask

1.5.1.18 DATA_APB

1.5.1.18.1 I2S Interface Controller (I2S)

I2S supports TDM serial interface and standard I2S interface.

Inter-IC sound (I2S) bus is the serial link protocol for digital audio processing. In the interface module, Data Receive FIFO and Data Transmit FIFO are used to cache data and shift between serial data and parallel data, that is, external audio digital signal is converted to parallel data via the shift register and then written to Receive FIFO; internal bus data is

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written to Transmit FIFO, that is, data is converted to serial data via shift register data, and transferred to the external standard digital audio processing chip based on I2S bus protocol.

TDM (Time Division Multiplexed) serial interface transmits audio data via single data line. In the interface module, Data Receive FIFO and Data Transmit FIFO are used to cache data and shift between serial data and parallel data, that is, external audio digital signal is converted to parallel data via the shift register and then written to Receive FIFO; internal bus data is written to Transmit FIFO, that is, data is converted to serial data via shift register data, and transferred to the external standard digital audio processing chip based on TDM protocol.

Features:

- I2S interface
  - Supports standard I2S serial port protocol, and can connect the standard digital audio processing chip supporting I2S protocol.
  - Supports Master(with the control signal given by I2S module) and Slave(with control signal given by external digital audio processing chip) according different sources of control signals
  - The word length of left and right sound tracks are 16bits
- TDM interface(only supported by I2S0 module)
  - Supports TDM serial interface timing and two timing modes, one mode is channel initiation(time slot) aligns with rising edge of frame synchronization signal, the other mode is channel initiation(time slot) delays one SCLK clock cycle than rising edge of frame synchronization signal
  - Support Master(with the control signal given by I2S module) and Slave(with control signal given by external digital audio processing chip)
  - The number of channels (time slot) per frame can be configured; a frame supports 2, 3, 4, 5, 6, 7 or 8 channels.
  - Each channel(time slot)' length is fixed 32 bits
  - Each active channel(time slot)' bit can be configured, and supports 16bits, 18bits, 20bits or 24bits, data left-alignment
- Data interface
  - Receive Data FIFO(32 x 32Bits) buffers external audio digital signal
  - Transmit Data FIFO(32 x 32Bits) buffers internal bus(DATA_APB) data
  - Data transfer supports DMA transfer mode

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1.5.1.18.2 Synchronous Serial Interface Controller (SSI0, SSI1, SSI3)

SSI is the module used to communicate with external synchronous serial interface. SSI supports Motorola's SPI protocol and TI SSP protocol. SSIx(x=0, 1, 3) is synchronous serial master device interface.

SSIx(x=0, 1, 3) module can be accessed by Cortex-A7 and AP_DMAS.

Features:

- Independent enabling of interrupts
- Programmable data transfer rate. SSIx(x=0, 1, 3) master device's maximum transfer rate is ssix_mclk/2(the default value of ssix_mclk is 19.5MHz)
- Programmable data frame format(4 – 16 bits)
- SSI0 depth and width of receiving FIFO and transmitting FIFO are respectively 16 and 16bits
- SSI1 and SSI3 depth and width of receiving FIFO and transmitting FIFO are respectively 32 and 16bits
- Supports Motorola SPI protocol and TI SSP protocol
- SSIx(x=0, 1, 3) synchronous serial master device
- SSIx(x=0, 1, 3) and AP_DMAS's Receive Hardware Handshaking and Transmit Hardware Handshaking
- SSI0 has 2 serial enabled/frame synchronization signal lines, which can be connected with two slave devices; SSI1 and SSI3 both have 1 serial enabled/frame synchronization signal line, which can be connected with one slave device.

1.5.1.18.3 Universal Asynchronous Receiver/Transmitter (UART0, UART1, UART2)

UART is the Universal Asynchronous Receiver/Transmitter used to receive and transmit data between chip and peripheral device. Users can set transfer character length, Baud and parity check, etc.

LC1813 integrates three UART controllers (UART0, UART1 and UART2) which can be accessed by Cortex-A7 and AP_DMAS. Three UARTs all support auto Flow Control.

Features:

- Based on 16550 standard

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- Supports AFC(auto flow control) mode
- Supports programmable THRE interrupt mode
- Depth and width of receiving FIFO and transmitting FIFO are respectively 32 and 8bits
- Programmable FIFO interrupt threshold value
- Enabling and disabling of FIFO
- Programmable serial port baud rate. The default serial port baud rate is 115200, with the maximum baud rate of 19.5M for UART0 and 9.5M for UART1/UART2(UARTx clock needs to be set in AP_PWR module)
- Programmable serial data transfer frame format
- Supports DMAS Hardware Handshaking(by transmitting channel of AP_DMAS)
- Supports clock disabled protection function(enable control in AP_PWR)

1.5.1.19 CTL_APB

1.5.1.19.1 AP Watchdog (AP_WDTx)

AP_WDTx(x=0, 1, 2, 3) separately supervises the corresponding core of Cotex_A7's four cores, and the corresponding WDT will generate system reset signal to AP_PWR once any one of the four cores hangup. Based on the configuration of register, AP_PWR will chooses to reset the whole chip or only A7 to protect the system as long as there is a system reset.

AP_WDT module can be accessed by Cortex-A7.

Features:

- Each core has a corresponding WDT
- 32bits counter
- Supports different work modes
- Counter will time out when it counts down to 0
- Programmable timeout period
- Timeout period can be modified while AP_WDT is working
- Users can restart the counter at any time
- Users can reset AP_WDTx(x=0, 1, 2, 3) by writing the AP_PWR module's reset control register AP_PWR_MOD_RSTCTL2
- User can control system reset or A7 reset by writing AP_PWR module's reset control register AP_PWR_WDTRST_CTL

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- Since system reset signal of AP_WDTx(x=0, 1, 2, 3) is sent to AP_PWR, based on the configuration of register, AP_PWR will chooses to reset the whole chip or only A7 to protect the system as long as there is a system reset.

1.5.1.19.2 AP_Timer (AP_TIMER)

LC1813's AP_TIMER contains seven independent programmable timers: AP_TIMER0, AP_TIMER1, AP_TIMER2, AP_TIMER3, AP_TIMER4, AP_TIMER5, and AP_TIMER6. It can be accessed by Cortex-A7.

Features:

- seven independent programmable timers
- 32bits data width timers
- Two operating modes: free-running mode and user-defined count mode
- Each timer has its own clock
- Each timer has its own interrupt
- It supports simultaneously clearing seven timer interrupts

1.5.1.19.3 I2C Interface Controller (I2C0, I2C1, I2C3)

I2C interface controller mainly accomplish I2C interface.LC1813 contains the same three I2C modules: I2C0, I2C1 and I2C3, which is hung on the CTL_APB bus, and can be accessed by Cortex-A7.

Features:

- 2-line I2C serial interface
- Transfer speeds
  - Standard mode(100Kbps)
  - Fast mode(400Kbps)
  - High-speed mode(3.4Mbps)
  - Support clock sync
- Work as a I2C Master
- Support multiple Master way(bus arbitration)
- 7-bit or 10-bit addressing
- Transmit FIFO with the width of 8bits and depth of 16(Transmit FIFO of the I2C1 with depth of 32

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- Receive FIFO with the width of 8bits and depth of 16(Receive FIFO of the I2C1 with depth of 32

1.5.1.19.4 Pulse Width Modulation Module (PWM)

PWM module is a module in LC1813 used to generate adjustable frequency and variable duty ratio signal.LC1813 integrates two independent programmable PWM modules: PWM0 and PWM1.PWM is mainly used for mobile phones' LCD backlight control, charge control, and the generation of various tones, etc.

PWM can be accessed by Cortex-A7.

Features:

- 8-bit period adjustable counter
- The timing cycle of duty ratio counter is fixed at 100
- PWM clock is adjustable, with the default frequency of 3.25MHz
- The default frequency range of PWM output signal is about 127Hz - 32.5KHz
- It has software reset function
- Three work modes: AM mode, FM mode, FM-AM mode

1.5.1.19.5 AP Clock Power Reset (AP_PWR)

AP_PWR is used to control global power consumption of AP, which generates clock and reset signals for each module, and accomplishes power management for specific modules. It can be accessed by Cortex-A7.

Features:

- Clock management of AP side, including clock generation, clock enabling and disabling for each module
- Accomplish power consumption control for different parts of AP side
- Reset control for each module of AP
- Specific sleep-wake circuit, which is used to process sleep-wake of AP
- Accomplish power management function of AP side(includes Cortex-A7)
- Assists SECURITY module to perform security related functions

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1.5.2 CP Functional Module

1.5.2.1 ARM926

ARM926EJ-S is an integrated processor macro-cell using the ARM9E core. It is a member of the high-performance, 32-bit on-chip system solution ARM9 Thumb family. ARM926EJ-S processor of LC1813 includes the following features.

Features:

- 32-bit address data width
- Support 32-Bit and 16-Bit(Thumb Mode) instruction set
- Support 8-Bit Java Bytecode(Jazelle State)
- 32KB data cache
- 32KB instruction cache
- 8KB instruction Tightly-Coupled Memory
- Memory management unit(MMU)

1.5.2.2 ZSP540

ZSP540 is used to complete GSM/GPRS/EDGE/TD-SCDMA/HSDPA physical layer calculation and control. The main algorithm of HSDPA physical layer is completed by TH, and main algorithm of EDGE is completed by specialized hardware DTC3_0. ZSP540 contains instruction CACHE and data CACHE which are used to cache external memory instructions and data.

Features:

- ZSP540 contains 128KB instruction memory, 32KB Instruction CACHE, 128KB data memory and 16KB data CACHE, with the maximum operating frequency of 156MHz.
- It has three main device interfaces: ZSP540_I_CACHE, ZSP540_D, ZSP540_D_CACHE AHB master interfaces
- It has a slave device interface, by which hosts including ZSP540 can access the instruction and data memory of ZSP540
- Supports part of ZSP TRACE functions
- Prefetchs eight instruction words each clock cycle and execute up to 4 instructions per clock cycle
- Load/store structure

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- Simple and orthogonal RISC instruction set
- 16 universal 16-bit registers
- 2 MAC units

In which, ZSP540_ICACHE has the following features:

- Access to ICACHE register by ZSP540 coprocessor interface
- ICACHE is 2-way set associative
- 32KB instruction CACHE(ICACHE), with each cache line of 512bits
- 256x13bitsx2 of TAG TABLE
- Use of least recently used alternative strategy
- Support the ICACHE loading and FLUSH operation
- When ICACHE is disabled, ICACHE RAM can be used as the instruction RAM, and supports the loading of RAM

ZSP540_DCACHE has the following features:

- Access to DCACHE register by ZSP540 coprocessor interface
- DCACHE is 4-way set associative
- 16KB data CACHE(DCACHE), with each cache line of 256bits
- 128x18bitsx4TAG TABLE
- Use of least recently used alternative strategy
- Support DCACHE FLUSH and CLEAN operations
- Support write back and write through data consistency strategy

ZSP TRACE function has the following features:

- PC monitoring function
  - PC jump monitoring function
  - Instruction bus monitoring function
- Data bus monitoring function

1.5.2.3 ARM926 Interrupt Controller (CP_ICTL0)

ARM926 interrupt controller (CP_ICTL0) is a module used for controlling all the interrupt sources of ARM926 processor. It generates interrupt requests (IRQ) and fast interrupt request (FIQ), and sends them to ARM926 processor and CP_PWR simultaneously.
The main controlling unit which can access to CP_ICTL0 is ARM926.

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Features:

- 27 general interrupt requests(IRQ)
- 1 fast interrupt request(FIQ)
- Software interrupt
- Interrupt enable/mask function
- Programmable 16-level interrupt priorities,
- Vectored interrupts mechanism

1.5.2.4 ZSP540 Interrupt Controller (CP_ICTL1)

LC1813 supplies ZSP540 interrupt controller CP_ICTL1 which is used to control partial ZSP540 interrupt sources. The controller can generate regular interrupt request (IRQ), and send it to ZSP540 maskable interrupt source 3. CP_ICTL1 has a total of 13 interrupt sources, which are simultaneously sent to ZSP540 processor and CP_PWR module.
The main controlling unit which can access CP_ICTL1 is the data accessing unit of ZSP540.

Features:

- 13 general interrupt requests(IRQ)
- Software interrupt
- Interrupt enable/ mask function
- Programmable 16-level interrupt priorities
- Vector interrupts mechanism

1.5.2.5 CP Share RAM0 (CP_SHRAM0)

CP_SHRAM0 is a memory module with 192KB, which supports 8bits (Byte), 16bits (Halfword) and 32bits (Word) read/write operation.
CP_SHRAM0 can map the broken bit line to the redundancy bit line again by working with EFUSE to accomplish self-repair.
CP_SHRAM0 is a shared memory module, which can be used for multi-master data exchange.CP_SHRAM0 can be accessed by ZSP540, CP_DMAC, CP_DMAS, CP_DMAD, and RFIF.

1.5.2.6 CP Share RAM1 (CP_SHRAM1)

CP_SHRAM1 is a memory module with 16KB, which supports 8bits (Byte), 16bits (Halfword) and 32bits (Word) read/write operation.

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CP_SHRAM1 is a share memory module, which can be used for multi-master data exchange.CP_SHRAM1 can be accessed by ARM926, ZSP540, CP_DMAC, CP_DMAS, and CP_DMAD.

1.5.2.7 RF Interface Controller Subsystem (RFIF)

1.5.2.7.1 TD RF Interface Controller (TDIF)

TDIF module is used to complete data processing between the chip and TD RF front-end chip, and control of RF chip. It can be accessed by ARM926, ZSP540.

Features:

- 16-bit frame timer, which can accomplish frame synchronization.10.24MHz clock frequency, adjustable period and phase by software
- 12-bit read only frame number counter
- One Rx data path, each has a Rx FIFO with 24 in depth, 32-bit in width used to buffer data of Rx direction(I way and Q way), and provides embedded DMA interface
- One Tx data path, a Tx FIFO with 24 in depth, 20bits in width used to buffer data of Tx direction(I way and Q way), and provides embedded DMA interface
- Shares SPI interface controller with GSMIF0, support three slave device at most, normal SPI protocol and 4-line protocol of SKYWORKS, and DigRF normal 3-line SPI protocol, 32-bit maximum width, and 30Mbps maximum transfer speed. Tx/Rx Data shares one block of ram with 384 in depth and 32-bit in width
- Supports TD parallel interface
- Provides one Rx and one Tx FIR filters, 65 steps symmetrical filter parameters which can be configured by software, the three filters share one group of parameters
- FIR function can be bypassed, when connection with RF module of internal FIR filter
- Provides one event tables
- Software set and maintains the event table, to trigger and execute the corresponding event regularly. Event table mainly deal with three kind of events as below:
  - Data channel processing，generates timing control signal of Tx/Rx path, enable CP_DMAD channel at specified time point(the corresponding CP_DMAD channel of TDIF Tx/Rx data path), and the timing control signal of GSMIF0 Tx/Rx data path
  - Supports 18 general purpose outputs (GPO), which can be divided into 3 groups, 6 outputs per group. The 18 outputs are multiplexed with general purpose outputs by GSMIF0, supports setting one group general purpose outputs at one time, also support setting up one general purpose output at one time

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- Controls the trigger time and amount of SPI interface data transfer

- Provides a frame interrupt
- Provides four independent non-periodic timer interrupts
- Provides three independent periodic timer interrupts
- Provides an independent time point to startup SPI
- Provides an independent time point to adjust the timer phase
- Provides an independent time point to stop TDIF timer or disable TDIF event table
- Provides an independent time point to enable GSMIF0 timer or reset GSMIF0 timer
- Provides an independent time point to set up general purpose output interface(gpo)
- Supports operating on data path and gpo directly via register
- Supports reading the counter value of TD and GSM timer simultaneously

1.5.2.7.2 GSM RF Interface Controller (GSMIF0)

GSMIF0 module is used to complete data processing between the chip and GSM RF front-end chip, and control of the RF chip. It can be accessed by ARM926，ZSP540.

Features:

- 16-bit frame timer, 1.08MHz clock frequency, and adjustable period and phase by software
- Provides 12-bit read only frame number counter
- Rx FIFO with 12 in depth and 32-bit in width, used to buffer data in Rx direction(I and Q), and provides embedded DMA Interface
- Tx FIFO with 8 in depth and 32-bit in width, used to buffer data in Tx direction(I and Q), and provides embedded DMA Interface
- Supports connection with DIGRF interface
- Shares SPI interface controller with TDIF, support two slave devices at most, normal SPI protocol, 4-line protocol of SKYWORKS, DigRF normal 3-line SPI protocol, 32-bit maximum width, and 30Mbps maximum transfer speed. Tx/Rx Data share one block of ram with 384 in depth and 32-bit in width
- Software set and maintain event table, to trigger and implement the corresponding events. Event table is mainly deal with three kind of events as below:
  - Data path processing, generates timing control signal of Tx/Rx path，enable CP_DMAD channel at specified time point(the corresponding CP_DMAD channel of GSMIF0 Tx/Rx data path)

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- Supports 18 general purpose outputs (GPO), which can be divided into 3 groups, 6 outputs per group. The 18 outputs are multiplexing with general purpose outputs of TDIF, support setting one group general purpose outputs at one time, also support setting one general purpose output at one time
- Control the trigger time and amount of SPI interface data transfer

- Provides a frame interrupt
- Provides an independent non-periodic timer interrupt
- Provides three independent periodic timer interrupts
- Provides an independent time point to adjust the timer phase
- Provides an independent time point to stop GSMIF0 timer or disable GSMIF0 event table
- Provides an independent time point to stop TDIF timer or reset TDIF timer
- Provides an independent time point to set general purpose output(gpo)
- Supports generating Strobe signal on DIGRF interface
- Supports operating on data path and gpo directly via register

1.5.2.7.3 CP System Controller (MAILBOX)

MAILBOX is used for the communication with CPUs, which includes the interrupts between ARM926 and ZSP540 in CP side. It is also responsible for configuring functions of some modules, including ZSP540 control, CP side ICM priority control, low power consumption control, and DMAC interrupt distributing, etc.
MAILBOX can be accessed by ARM926, ZSP540.

Features:

- Interrupts communication for ARM926 and ZSP540
  - Interrupt from ARM926 to ZSP540 (16 interrupt sources)
  - Interrupt from ZSP540 to ARM926 (16 interrupt sources)
  - Interrupt from CP to AP (32 interrupt sources. MAILBOX module only includes interrupt generate register and interrupt set state register from CP to AP. The interrupt enable, interrupt state, the raw state register of interrupt are in CTL module of AP)
  - Interrupt from CP to AP (32 interrupt sources. MAILBOX module only includes interrupt enable, interrupt state, and the raw state register of interrupt. The interrupt generate register is in AP CTL module)

Every interrupt source of the above interrupts has 2bits, and every interrupt is independently

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maskable. The transmitter is set “1” and the reciever is clear. During CP sending interrupt to AP, the clear control signal is return from AP.

Each interrupt between ARM926 and ZSP540 of CP side is controlled by 4 registers, including: interrupt generate register, interrupt enable register, interrupt state register and interrupt raw state register.

- Mode control register
  - ZSP540 control register, controlling interrupt vector addresses and interrupt enable of ZSP540
  - ICM priority control register
- Low power consumption function
  - Control CP bus, ICM and low power mode in partial modules
- DMAC interrupt distribution
  - Distributes the DMAC interrupts to ARM926 and ZSP540, and each CPU has independent DMAC interrupt enable and interrupt state register
- ZSP trace function control

1.5.2.8 CP System Controller (MAILBOX)

MAILBOX is used for the communication with CPUs, which includes the interrupts between ARM926 and ZSP540 in CP side. It is also responsible for configuring functions of some modules, including ZSP540 control, CP side ICM priority control, low power consumption control, and DMAC interrupt distributing, etc.

MAILBOX can be accessed by ARM926, and ZSP540.

Features:

- Interrupts communication for two of ARM926, ZSP0 and ZSP1
  - Interrupt from ARM926 to ZSP540(16 interrupt sources)
  - Interrupt from ZSP540 to ARM926(16 interrupt sources)
- Interrupt from CP to AP (32 interrupt sources, and MAILBOX only includes interrupt generate register and interrupt set state register from CP to AP. The interrupt enable, interrupt state, the raw state register of interrupt are in CTL module of AP)
- Interrupt from CP to AP (32 interrupt sources, and MAILBOX only includes interrupt enable, interrupt state, and the raw state register of interrupt. The interrupt generate register is in AP CTL module)
- interrupt generate register and interrupt set state register from CP to AP, the interrupt enable, interrupt state,

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Each interrupt source is 2 bits and independent maskable. The interrupt is asserted by sender but de-asserted by receiver. The control signal is returned by AP side to clear interrupt from CP to AP.

Each interrupt between ARM926 and ZSP540 of CP side is controlled by 4 registers, including: interrupt generate register, interrupt enable register, interrupt state register and interrupt raw state register.

- Mode control register
  - ZSP540 control register, controlling interrupt vector addresses and interrupt enable of ZSP540
  - ICM priority control register
- Low power consumption function
  - Control CP bus, ICM and low power mode in partial modules
- DMAC interrupt distribution
  - Distributes the DMAC interrupts to ARM926 and ZSP540, and each CPU has independent DMAC interrupt enable and interrupt state register
- ZSP540 trace function control

1.5.2.9 CP Direct Memory Access Controller (CP_DMAC)

CP_DMAC is used as flow controller to transfer massive data. LC1813 integrates a CP_DMAC, which can be used as both master device and slave device. While being used as slave device, CP_DMAC can be accessed by ARM926, and ZSP540; as master device, it can access CP_SHRAM0, CP_SHRAM1, ZSP540 RAM, and DDR, and accomplish the transmission between them.

CP_DMAC supplies three channels with specific registers.

Features:

- Up to three channels, with programmable channel priority, and unidirectional data transfer. Each channel has a FIFO, with the same depth of 64
- One master device interface
- Support 4 types of DMA transmission ways
- Address generation
  - Supports programmable source address, destination address
  - Supports 3 types of address changing
  - Supports 3 types of multi-block transmission

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- Multi-block transmission source and destination are controlled independently
- Source gather/ destination scatter(GATHER/SCATTER)

- Channel control
  - Each channel source address and destination address are programmable
  - Programmable channel transfer type
  - Programmable enable and disable of channel
  - Programmable size of Block
  - Programmable width of Transaction
- Interrupt
  - Support 3 interrupt types
  - Support Interrupt Enable

1.5.2.10 CP Brief Dedicated Memory Access Controller (CP_DMAS)

CP_DMAS provides DMA function, which can automatically transfer the data from peripheral to Memory and from Memory to peripheral under the control of CPU.

It can be accessed by ARM926, ZSP540.

Features:

- 2 peripheral receiving channels and 2 peripheral transmitting channels, with configurable channel priorities.

DMA peripheral receiving channel:

- Fixed source address pointing to peripheral FIFO with width value set of Byte, Halfword and Word
- Successive destination address increment of 1
- Block transfer and variable-length transfer
- Block transfer mode
  - When it is started, DMA will transfer automatically, and return idle state after receiving the set Block length, and then send an interrupt.
  - Programmable Block length in bytes
  - The start address of target buffer is aligned to 4 bytes boundaries, and the buffer size is multiples of 4-byte.

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- Current target buffer address indicates the address of last entered data.

- Variable-length transfer mode
  - When it is started, DMA will automatically detect and receive related peripheral data. When internal buffer data are enough for a 32-byte burst, the data will be written into target buffer;
  - Target buffer supports the circular buffer address mode
  - Current target buffer address directs to the written data address in current target buffer
  - Specific register can be configured by CPU to write data left in internal buffer into target buffer.
  - Support hardware detection of peripheral activity state to perform transfers of data left in internal buffer to target buffer if no data entering in an interval (software programmable) and assert interrupt.

Peripheral DMA transmitting channel:

- Fixed target address pointing to peripheral FIFO with width value set of Byte, Halfword and Word.
- Successive source address increment of 1.
- Target address unchanged
- Support single Block transmit and Block transmit in succession
- Programmable Block Length in byes
- Specific register can be configured by CPU to write data left in internal buffer into target buffer.
- Source buffer's starting address is arbitrary

1.5.2.11 CP Dedicated Memory Access Controller (CP_DMAD)

CP_DMAD provides DMA function, which is used to transfer a large number of data. CP_DMAD has a total of 12 channels, with each channel allocated to a specific module. The transmitting direction is fixed. The 12 channels are divided into three types according to the transfer characteristics: contiguous source and destination address, contiguous source address and fixed destination address and fixed address source and one-dimensional destination. Based on different transfer types, configuration parameters also vary. It can be accessed by ARM926 and ZSP540.

Features:

- Each channel's source and destination address can be configured. Source and

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destination can be in different clock domains

- Block size can be configured, and a maximum of 65, 535 32-bit data can be supported.
- Provides transfer completion interrupt, block transfer completion interrupt, source address and destination address bus error interrupt
- Source and destination addresses grow by the order of + 1
- Data width is fixed at 32 bits
- Supports list way A 2Kbyte memory in the module is used to store the list content
- Supports 12 channels

Channel 0: TDIF receiving (TDIF-> CP_DMAD-> memory) (fixed address source and one-dimensional destination channel)

Channel 1: TDIF transmitting ((memory, THMU) -> CP_DMAD-> TDIF) (contiguous source address and fixed destination address channel)

Channel 2: GSMIF0 receiving (GSMIF0-> CP_DMAD-> memory) (fixed address source and one-dimensional destination channel)

Channel 3: GSMIF0 transmitting (memory -> DMAD-> GSMIF0) (contiguous source address and fixed destination address channel)

Channel 4: THD receiving (THD-> CP_DMAD-> memory) (contiguous source and destination address channel)

Channel 5: THD transmitting (memory -> CP_DMAD-> THD) (contiguous source and destination address channel)

Channel 6: DTC3_0 receiving (DTC3_0-> CP_DMAD-> memory) (fixed address source and one-dimensional destination channel)

Channel 7: DTC3_0 transmitting (memory -> CP_DMAD-> DTC3_0) (contiguous source address and fixed destination address channel)

Channel 8: Memory transmitting 0 (memory -> CP_DMAD-> memory) (contiguous source and destination address channel)

Channel 9: Memory transmitting 1 (memory -> CP_DMAD-> memory) (contiguous source and destination address channel)

Channel 10: THMU receiving (THMU-> CP_DMAD-> memory) (contiguous source and destination address channel)

Channel 11: THMU transmitting (memory-> CP_DMAD-> THMU) (contiguous source and destination address channel)

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1.5.2.12 Audio Enhance Accelerate Operator (AEC_FFT)

AEC_FFT accomplishes the FFT/IFFTfunction of AEC module for the software test, and can saves MIPS of CPU.

AEC_FFT can be accessed by ARM926.

Feature:

- Supports FFT/IFFT of 256-point, 512-point, 320-point and 640-point real number
- Supports exchange between real number and imaginary number, and the function can bypass.
- Supports report of accelerate finish in two ways: interrupt and inquire
- Programmable interrupt priorities: 16 levels
- Vectored interrupts

1.5.2.13 Communication Accelerate Operator (COM_ACC)

1.5.2.13.1 A5_0 Module (A5_0)

A5_0 module is used for accomplish A5-1/2/3 encryption, including A5_0 and KASUMI encryption modules.

A5_0 can be accessed by ZSP540.

Features:

- Supports A5-1/2/3 encryption
- 6x32 bits FIFO for saving the coding operation results
- Dedicated embedded DMA channel for transmitting encryption results

1.5.2.13.2 GEA Module

GEA module is used for accomplish GEA-1/2/3, F8 and KASUMI encryption.

It can be accessed by ARM926.

Features:

- Supports GEA-1/2/3 encryption
- Supports F8 encryption
- Supports KASUMI encryption

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- 6x32 bits FIFO for saving the encryption results
- Dedicated embedded DMA channel for transmitting coding operation results

1.5.2.13.3 SNOW3G Module

SNOW3G is safety process module of LC1813, including UCIA module for TD-SCDMA safety, DCH module for transmitting data, and LPC module for controlling low power consumption. It can access DDR and ZSP540 RAM .

SNOW3G can be accessed by ARM926.

Features:

- UCIA
  - Supports UEA1, UEA2 operation of TD-SCDMA
  - Supports UIA1, UIA2 operation of TD-SCDMA
  - 128bits key length
  - The cipher text and plain text of UEA1, UEA2 are equal with length, support DMA transmission
  - The information authentication code of UIA1, UIA2 operation is 32bits, support DMA transmission and CPU reading
- DCH
  - Provides AHB Master interface
  - Embedded one DMA read channel and one DMA write channel
  - Addresses width is 32-bit, and data width is 32-bit
  - Supports multiple burst data block transmitting, the size of data block can be 1-65, 535 32-bit
- Interrupt
  - Supports operation finish interrupt, FIFO state interrupt, channel finish interrupt, channel error interrupt
  - Supports interrupt enable and interrupt mask
- LPC
  - Supports shut off the clock automatically by hardware when the module is unoccupied

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1.5.2.13.4 DTC3_0 Module (DTC3_0)

There are one DTC3_0 modules in LC1813, to accomplish EDGE channel equalization and Viterbi decoding operation.

DTC3_0 can be accessed by ZSP540.

Features:

- Supports DMAD interface, which is used for data receiving and transmitting
- Supports EDGE channel equalize acceleration
- Supports Viterbi decoding acceleration

1.5.2.13.5 TH Module

1.5.2.13.5.1 THD Core (THD)

THD core is used for accomplishing the downlink data process of TD-SCDMA, which can be accessed by ZSP540.

Features:

- Supports 240MHz main frequency at maximum
- Integrate JD and BRD hardware accelerator
- Supports the characteristics of TD-SCDMA R4/R5
- Supports QPSK/16QAM
- Supports maximum down speed is 2.8Mbps, category 15
- Supports multiple cell channels estimate
- Supports CP_DMAD to access THD register and internal RAM

1.5.2.13.5.2 THMU Core (THMU)

THMU core is used for accomplishing measure work and processing uplink data of TD-SCDMA, and it can be accessed by ZSP540.

Features:

- Supports 156MHz main frequency at maximum
- Integrates M1 and UDP hardware accelerator
- Supports test/detection of 0-127 unknown cells
- Supports DCO cancel
- Supports digital gain adjustment

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- Supports CP_DMAD to access THMU register and internal RAM

1.5.2.14 CP_APB

1.5.2.14.1 CP Clock Power Reset (CP_PWR)

CP_PWR is used to control global power consumption of CP, which generates clock and reset signals for each module, and accomplishes power management for specific modules. It can be accessed by ARM926, ZSP540.

Features:

- Clock management of CP side, including clock generation, clock enabling and disabling for each module
- Accomplish power consumption control for different parts of CP side
- Reset control for each module of CP
- Specific sleep-wake circuit, which is used to process sleep-wake of CP
- Accomplish power management function of CP side(includes Cortex-A7)

1.5.2.14.2 Real-Time Clock (RTC)

LC1813 integrates a real-time clock (RTC) module to display day, hour, minute and second and generate timer interrupt and other functions. RTC module can be accessed by ARM926 and ZSP540.

Features:

- Interrupts can be masked separately
- Long-time and stable operation(support the continuous operation of about 90 years)
- Timing can be accurate to second
- Day, hour, minute and second can be read directly
- Count values within second can be read
- Three independent timer interrupts can be generated
- Interrupts can be set to occur in some day or several days during any given week
- Counter counts upward
- Users can control whether the counter is enabled or not

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1.5.2.14.3 CP Watchdog (CP_WDT)

CP_WDT is used for ARM926 protection. Once ARM926 is down, CP_WDT informs CP_PWR, and CP_PWR accomplishes the reset of ARM926.

CP_WDT module can be accessed by ARM926, ZSP540.

Features:

- 32bits counter
- Supports different work modes
- Counter will time out when it counts down to 0
- Programmable timeout period
- Users can modify the timeout period while CP_WDT is working
- Users can restart the counter at any time
- Users can reset CP_WDT by writing CP_PWR module's reset control register (CP_PWR_APB_SFRSTCTL).

1.5.2.14.4 CP Timer (CP_TIMERx)

CP_TIMER contains four independent configurable timers: CP_TIMER0, CP_TIMER1, CP_TIMER2 and CP_TIMER3.It can be accessed by ARM926, ZSP540.

Features:

- Up to 4 independent programmable timers
- 32bits timers
- Supports two operating modes: free-running mode and user-defined count mode
- Each timer has its own clock
- Each timer has its own interrupt
- Supports simultaneously clearing four timer interrupts

1.5.2.14.5 Smart Card Interface Controller (SIM0, SIM1)

Smart card interface controller is used to implement ISO7816 standard and complete interface with SIM card (smart card). There are two smart card interface controllers in LC1813: SIM0 and SIM1.

Smart card interface controller provides drive interface for SIM cardx(x=0, 1), saves the data sent by processor via the bus to transmitting buffer (transmitting FIFO), and puts the data to

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the external port in the form of signal compatible with ISO7816 standard, as well as receives the data returned from SIM card to store them to the internal receiving buffer (receiving FIFO) and notifies the processor through interrupt.

Meanwhile, the smart card interface controller also controls clock (sim_clk_out) and reset (simx_rst) of SIM cardx(x=0, 1) interface. Users can send to the SIM cardx(x=0, 1) the reset signal, receiving ATR response, prescribed interfaces rate, transmitting commands and receiving response via the module.

It can be accessed by ARM926.

Features:

- Based on ISO7816 protocol standard, complete T = 0, T = 1 protocol
- Implements the function of checking receiving characters
- Supports generation and receiving of retransmission NACK
- Supports standard rate and enhanced rate
- Achieves automatic initial character detection
- Provides a universal timer used to generate the timer function for realizing ATR and receiving test
- Provides 16x10bits FIFO for receiving direction
- Provides 16x8bits FIFO for transmitting direction
- Provides a variety of event interrupts

1.5.3 COM_APB Function Module

1.5.3.1 I2C Interface Controller(COM_I2C)

I2C interface controller mainly accomplish I2C interface, and the module is hung on the bus COM_APB.LC1813 integrates one I2C module COM_I2C which can be shared by AP and CP. It can be accessed by Cortex-A7, ARM926, ZSP540.

Features:

- 2-line I2C serial interface
- Two transfer speeds
  - Standard mode(100Kbps)
  - Fast mode(400Kbps)
  - High speed mode(3.4Mbps)
  - Support clock sync

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- Works as a I2C Master
- Supports multiple Master mode(bus arbitration)
- 7-bit or 10-bit addressing
- Includes the Transmit FIFO with width of 8 bits and depth of 16
- Includes the Receive FIFO with width of 8 bits and depth of 16

1.5.3.2 Synchronous Serial Interface Controller(COM_PCM)

COM_PCM module is a 4-line serial interface to connect audio codec chip or Bluetooth chip.

There are receiving FIFO and transmitting FIFO in the module for caching data. COM_PCM transmits the output data written to transmitting FIFO by AP_DMAS to off-chip device through COM_PCM interface. Data input by COM_PCM interface will be written to receiving FIFO, and read by AP_DMAS to internal memory

This module can be accessed by Cortex-A7, ARM926, and ZSP540.

Features:

COM_PCM

- Supports multi-channel PCM transfers
- The number of receiving channels can be configured as “1” or ”2”, the number of transmitting channels is “1”
  - When the number of receiving channels is “2”, the number of transmitting channels is “1”, 32 clocks per frame correspond to Slot0 and Slot1, and transmitting data repeatedly is transmitted to Slot0 and Slot1.
  - When the number of receiving channels and transmitting channels are both “1”, 16 clocks per frame correspond to Slot only, and transmitting data and receiving data are send to respective slot.
- In receiving dual-channel mode, left channel data is received first, and MSB of right channel data follows LSB of left channel data; left channel data is transmitted first, and MSB of right channel data follows LSB of left channel data(when the number of transmitting channels is “1”, left channel data is repeatedly transmitted twice, it means software needs to copy 16bits data)
- Supports Master mode and Slave mode
  - In Master mode, frame signal and SCLK signal are generated by COM_PCM module
  - In Slave mode, frame signal and SCLK signal are input by pins
- In receiving single-channel mode, two types of frame head format are supported. The rising/falling edge of frame head signal shows the start of a frame

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- Modules configured by software sample and input data at rising/falling edge of SCLK
- Modules configured by software output data at rising/falling edge of SCLK
- When outputting data, high-bit data is first output; when inputting data, high-bit data is also first input (LSB first mode isn't supported).
- In Master mode, if Modules configured by software output data at rising edge of SCLK, the outputting frame signals synchronize with SCLK's rising edge; if Modules configured by software output data at falling edge of SCLK, the outputting frame signals synchronize with SCLK's falling edge
- COM_PCM data size is 16bits, PCM frame size(time interval between frame signals) can be more than 16 SCLK clock cycles
- SCLK phase inversion can be configured, in master mode, phase of output SCLK can be configured as inversion of inner sample or driver output SCLK phase, while in slave mode, input SCLK phase can be reversed by software configuration.
- Read and output first data at next clock of frame head
- Receive Data FIFO(32 x 32-bit) buffers external audio digital signal
- Transmit Data FIFO(32 x 32-bit) buffers internal bus COM_APB data
- Support Transmit and Receive DMA Hardware Handshaking
- COM_PCM interrupt

1.5.3.3 Multiplexed Pin (MUX_PIN)

MUX_PIN module mainly accomplishes function selection of external pins, configuration of Pull-up/Pull-down, configuration of test pins, indication of pins related security, etc.

Features:

- Configurable ports with different functions to external pins
- Configures Pull-up/Pull-down of external pins
- Configures internal signals to be observed by test_pins
- Indication of pins(sec_smc, sec_sw) related security
- Sleeping control for RFIF pins

1.5.3.4 COM_APB Clock Controller (DDR_PWR)

DDR_PWR is located at COM_APB module, and used to generate clock for submodules of COM_APB, reset control and low power management. It can be accessed by Cortex-A7, ARM926, and ZSP540.

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Features:

- Generates clock signals for submodules of COM_APB, including the module's bus clock and clock, and control opening and closing clock
- Supports software reset operations for some submodules of COM_APB
- Controls and inquires low power function of some submodules of COM_APB
- Supports dynamic frequency changing for COM_APB bus clock
- Sleep-wakeup operations through the control of AP_PWR/CP_PWR
- Supports configurable address conversion mode of MEMCTL module
- Supports data access statistics for AXI ports of MEMCTL

1.5.3.5 Universal Asynchronous Receiver/Transmitter (COM_UART)

UART is the Universal Asynchronous Receiver/Transmitter used to receive and transmit data between chip and peripheral device. Users can set transfer character length, Baud and parity check, etc.

LC1813 integrates one UART controller (COM_UART).COM_UART doesn't support auto Flow Control. It can be accessed by Cortex-A7, ARM926, ZSP540, AUDIO_DMAS and CP_DMAS.

Features:

- Based on 16550 standard
- Supports programmable THRE interrupt mode
- Depths and width of receiving FIFO and transmitting FIFO are respectively 32 and 8 bits
- FIFO interrupt threshold value can be set
- FIFO enabled or disabled
- Serial port baud rate can be set. The default serial port baud rate is 115200, with the maximum baud rate of 4M(COM_UART clock needs to be set in DDR_PWR module)
- Serial data transfer frame format can be set
- Supports DMAS Hardware Handshaking(via transmitting channel of AUDIO_DMAS or CP_DMAS, but both cannot be used simultaneously)
- Supports clock disabled protection function(enable control in DDR_PWR)

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1.5.3.6 General Purpose I/O Controller(GPIO0, GPIO1)

The relationship of gpio_d[242:0] with GPIO0 and GPIO1 is listed in *GPIO List*

1.5.3.6.1 General Purpose I/O Controller 0(GPIO0)

- GPIO0 is the general-purpose input-output controller.GPIO0 contains 94 I/O ports.
- GPIO0 module can be accessed by Cortex-A7, ARM926, ZSP540.

Features:

- 94 ports of GPIO0 can be independently configured
- Each port of GPIO0 can be configured as data input, data output, interrupt input
- Supports independently programmable interrupt registers for each port
- GPIO0's interrupt can be output to Cortex-A7, ARM926, and ZSP540, and each of CPUs has own independent interrupt mask register and interrupt status register.
- 94 ports of GPIO0 support multiple types of interrupt signals:
  - HIGH level interrupt
  - LOW level interrupt
  - gpio_clk (32Kclock)rising edge interrupt
  - gpio_clk falling edge interrupt
  - gpio_clk edge interrupt
  - pclk(APB bus clock)rising edge interrupt
  - pclk falling edge interrupt
  - pclk edge interrupt
- External interrupt can be filtered by debounce logic.
  - Filters pulse input less than a gpio_clk (32KHz clock) period
  - 94 ports of GPIO0 can be independently set Whether enable debounce operation or not

1.5.3.6.2 General Purpose I/O Controller 1(GPIO1)

GPIO1 is the general-purpose input-output controller.GPIO1 contains 96 I/O ports.

GPIO1 module can be accessed by Cortex-A7, ARM926, ZSP540.

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Features:

- 96 ports of GPIO1 can be independently configured
- Each port of GPIO1 can be configured as data input, data output, interrupt input
- Supports independently programmable interrupt registers per port
- GPIO1's interrupt can be output to Cortex-A7, ARM926, and ZSP540, and each of CPUs has own independent interrupt mask register and interrupt status register.
- 96 ports of GPIO1 support multiple types of interrupt signals:
  - HIGH/LOW level interrupt
  - gpio_clk (32Kclock)rising edge interrupt
  - gpio_clk falling edge interrupt
  - gpio_clk edge interrupt
  - pclk(APB bus clock)rising edge interrupt
  - pclk falling edge interrupt
  - pclk edge interrupt.
- External interrupt can be filtered by debounce logic.
  - Filters pulse input less than a gpio_clk (32KHz clock) period.
  - 96 ports of GPIO1 can be independently set Whether enable debounce operation or not

1.5.4 External Memory Controller (MEMCTL)

MEMCTL is the module used to transfer data between internal bus and external memory. It mapped the external memory to the address space within the chip. When the internal bus access the address which mapping to external memory, MEMCTL operates the external memory devices.

MEMCTL supports LPDDR2/LPDDR3 memory with 32-bit data width, and 2 chip selections. MEMCTL internal registers and external LPDDR2/LPDDR3 memory locate in different address space. MEMCTL internal registers contains two parts: DDR controller and DDR PHY.

Features:

- 4 standard AXI data bus interfaces and 2 APB register interfaces
- Supports LPDDR2/LPDDR3 memory with the maximum frequency of 400MHz
- Supports auto clock-stop, power-down and self-refresh

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- Supports auto-refresh, refresh interval can be configured by software
- Supports auto pre-charge
- Software and hardware driven self-refresh entry and exit
- Low-power can be entered and exited by ways as follows:
  - Software configures state machine (highest priority).
  - Hardware low-power interface(medium priority)
  - Auto self-refresh(lowest priority)
- Programmable address mapping

1.5.5 Debug and Test Module (DEBUG & TEST)

LC1813 contains one Cortex-A7 Quad-core, one ARM926 core and one ZSP540 core. All cores can be debugged.

- Cortex-A7 can be debugged through APB-AP interface of CORESIGHT subsystem
- ARM926 can be debugged through two mode:
  - Through JTAG-AP interface of CORESIGHT subsystem
  - Through external JTAG interface
- ZSP540 can be debugged through external JTAG interface
- ARM926 and Cortex-A7 transmit Cross Trigger for each other

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2 Chapter2 Pin Allocation and Signal Description

2.1 Pin assignment

For description of LC1813 pin assignment, please see *Figure 2-1.* LC1813 pin assignment (TOP VIEW of bottom pin map).

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	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
A	PVDD2	TDGPO4		TDGPO1	TDD01		TDD04	TDD08		DRFODEN	DRFOSTBE		GSMOGPO1	U2CTS		CS1CLK	GPIO24		GPIO9	TMOD0		U3TXD	PVDD7		PVDD17	PVDD12		PVDD13	PVDD16	A
B	IISODI	PWEN	TDGPO6	TDGPO5	TDGPO3	TDD05	TDD00	TDD06	SPICK	DRFOD	OSCEN0	GSMOGPO2	GSMOGPO3	U2TXD	CS1RXD	GPIO11	GPIO232	GPIO10	GPIO7	TMOD1	BOOTCTL1	BOOTCTL0	U3RXD	MMC2CMD	MMC2CLK	PVDD14	MMC2D0	PVDD11	PVDD5	B
C		ISPSD1	TDGPO7	TDGPO0		TDGPO11	TDD02			SPIDO	SPIDIN			U2RTS	CS1SN			GPIO234	GPIO6			TCK0	TDI0			MMC2D2	MMC2D1	MMCOD1		C
D	OSCIN	IISODO			TDGPO2	GSMOGPO	TDD07	TDD09		SPICSO	TDGPO10		TDGPO8	GSMOGPOO	U2RXD		IICOSCL	GPIO8			BOOTCTL2	TMSO	NTRSO	MMC2D3		S1SN	GPIO3	MMCOD0	MMCOD2	D
E	OSCOUT	IISOCK	IISOWS		GPIO239			TDD03	TDSCK0		TDGPO9	CLK26DI0		SPICS2	GPIO233		CS1TXD	IICOSDA	CLKO1	NTRS1	TDOO			S1RXD		GPIO4	S1TXD	MMCOD3	MMCOCMD	E
F		GPIO240	ISPSDO	CLK26SEL																					S1CLK			MMCOCLK		F
G		RSTON	PRSTN	OSCEN3V	CLK32K								VSS	OSCEN1	CLK26DI1	VSS	VSS	VSS							UORXD	SIM1IO	SIM1RST	KBDKI7	S2SN	G
H	PVDD15	USBOVRES		VSS																					SIM1CLK	UOTXD	UORTS	GPIO12	S2CLK	H
J		USBOVBUS			USBODM																				UOCTS			DPHYREXT		J
K	USBAVDD	KBDKI4	KBDKI5	USBOID	USBODP																				SOSN1	S2TXD		DPHYAVDD	DPHYDNO	K
L	PLLAVDD	PLLDVDD	KBDKI3	KBDKI2	VSS																					S2RXD	DPHYDP1	DPHYCLKN	DPHYDPO	L
M		CSOTXD		KBDKI6								VDDMAIN	VDDMAIN	VDDMAIN	VDDMAIN	VDDMAIN	VDDMAIN	VDDMAIN								SOSNO	DPHYDN1	DPHYCLKP		M
N	CSOCLK	CSOSN			DVFS1							VDDMAIN	VSS	VSS	VSS	VSS	VSS	TDI1							GPIO25			DPHYDN3	DPHYDP2	N
P	CSORXD	CIICSCL	CIICSDA	DVFSO	CLKOO							VDDMAIN	VSS	VSS	VSS	VSS	VSS	TDO1							PWMO	SORXD		DPHYDP3	DPHYDN2	P
R		U1TXD	IIC1SCL	IIC1SDA			CLKO3					VDDA7	VSS	VSS	VSS	VSS	VSS	TMS1					ISPSCLKO			SOCLK	GPIO28			R
T	SECSMC	U1CTS		U1RTS	U1RXD							VDDA7	VSS	VSS	VSS	VSS	VSS	TCK1							VSS	SIMOIO	SIMOCLK	SOTXD	PVDD8	T
U	GPIO2	GPIO5			SECSW							VDDA7	VSS	VDDA7	VSS	VSS	VSS	VSS							SIMORST			ISPPDWN1	PVDD6	U
V		PVDD9	GPIOO	GPIO1								EFUSEVDD	VDDA7	VDDA7	VDDA7	VDDA7	VDDA7	VDDA7								ISPRSTN1		ISPRSTNO		V
W	PVDD10	NANDOEN	NANDWEN	NANDD9																					ISPSD3	ISPSD8	ISPFSINO	ISPFSIN1	ISPPDWNO	W
Y	NANDD7	NANDD8		NANDD3	NANDD4																				ISPSD7	CLKO2	ISPSCLK	ISPSD2	ISPPWM	Y
AA		NANDD6			NANDD14																				ISPSD9			ISPSD4		AA
AB	NANDD5	NANDD12	NANDD11	NANDD13	NANDD10																					ISPSHS		ISPSD6	CPHYODN2	AB
AC	NANDDO	MMC1D7	MMC1D5	MMC1D6	NANDD15								VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ							ISPSVS	ISPSD5	CPHYODN3	CPHYODP3	CPHYODP2	AC
AD		MMC1D4		MMC1D2	MMC1CLK																				ISPSTBE	VSS	ISPSCL	CPHYOCLKP		AD
AE	ZQ	MMC1D3				MMC1CMD	VSS		WEN	RASN		BA2	CKNO			A11		RNK1			RNKO	VSS		VSS	VSS			CPHYOCLK	CPHYODN1	AE
AF		MMC1DO	NANDD2	NANDD1		MMC1D1	VSS	CASN		BA1	A8	A5		CKO	AO	A2		A15	DQO1	DQOO		VSS	RSTO	ATO		VSS	ISPSDA	CPHYODPO	CPHYODP1	AF
AG		DQ31	DQS3	DQ26		DQ12	DQ08			BAO	A6			CSN1		A12		DQO5	DQO4			DQSN2	DQ18			DTO1	VSS	CPHYODNO		AG
AH	DQ29	DQ27	DQ25	DQSN3	DM3	DQ14	DQ13	DQ10	DQSN1	DM1	CKEO	CKE1	CSNO	A3	A4	A13	A14	DQSNO	DQO6	DQO7	DM2	DQ21	DQS2	DQ19	DQ20	DQ16	VSS	VSS	CPHYOREX	AH
AJ	DQ28	DQ30	DQ24		DQ15	DQ11		DQO9	DQS1		A7	A9		A1	A10	VREF	DMO	DQSO		DQO2	DQO3		DQ23	DQ17		DQ22	DTOO		CPHYAVDD	AJ
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	

Figure 2-1 LC1813 Pin Assignment (TOP VIEW of bottom pin map)

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2.2 Symbol Description

- Ball Name: name of BALL corresponding to the package of chip.
- Signal Name: the function signal name of internal function module which this pin corresponds to.
- Description of pin property
  - I: Digital Input
  - O: Digital Output
  - IO: Digital Input/Output
  - AI: Analog Input
  - AO: Analog Output
  - AIO: Analog Input/Output
- Drive Capability: Pin's supporting drive capability, and "d" means default drive capability of power-on reset. The pin's drvie capability can't be seleted except pin of SDMMCx(x=0~2). For detailed configurations of SDMMCx 's drive capability, please refer to pin control register of SDMMCx of Pin Multiplexing and Control chapter.
- Reset Direction: IO pin's default direction after the chip is reset.
- Reset States: output pin's default output state after the chip is reset.
- Pull-up/Pull-down:
- NA: Output pin and its interiors do not connect the input pins of both pull-up resistor and pull-down resistor.
- Signal name/property/ function corresponding to the name of each pin are described as below: default function in the first row, second function in the second row, third function in the third row and fourth function in the fourth row. The first function is by default. For detailed configurations, please refer to System Controller (CTL) Pin Multiplexing and Control chapter in User Manual.

2.3 Package

For description of LC1813 chip package form, please see 6.2.

2.4 Power/Ground

LC1813 chip power ground pin allocation is as shown in *Table 2-1*.

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Table 2-1 LC1813 Power/Ground Pin Allocation Table

Ball Name	Ball Number	Functional Description	Voltage(v)
Digital Power Supply			
VDDMAIN	M12,N12,P12,M13,M14,M15,M16,M17,M18	Core power supply	1.1V
VDDA7	R12,T12,U12,U14,V13,V14,V15,V16,V17,V18	A7 power supply	1.1V
PVDD2	A1	Power supply for TDIF RX0 and GSM0	1.8/3V
PVDD5	B29	Power supply for KBS,PWM,SSI0,SSI2,GPIO12,GPIO28,GPIO25	1.8/3V
PVDD6	U29	Power supply for CAMER RGB	1.8/3V
PVDD7	A23	Power supply for COM_PCM1,UART2,I2C0,GPIO232~GPIO234,GPIO6~11,GPIO24,CLKO1	1.8/3V
PVDD8	T29	Power supply for SIM0	1.8/3V
PVDD9	V2	Power supply for UART1,CLKO2,GPIO0~GPIO2,SECSMC,SECSW,GPIO5,CLKO3,I2C1	1.8/3V
PVDD10	W1	Power supply for NADNFLASH,SDMMC1	1.8/3V
PVDD11	B28	Power supply for SDMMC0	1.8/3V
PVDD12	A26	Power supply for SDMMC2	1.8/3V
PVDD13	A28	Power supply for UART0	1.8/3V
PVDD14	B26	Power supply for SSI1,GPIO3,GPIO4	1.8/3V
PVDD15	H1	power supply for COM_PCM0,I2S0,COM_I2C,PWR,KBS,CLK26MXIN,CLK26MOUT,CLK26SEL,ISPSD1,ISPSD0,GPIO239~GPIO240	1.8/3V
PVDD16	A29	Power supply for SIM1	1.8/3V
PVDD17	A25	Power supply for JTAG,COM_UART, TMOD and BOOTCTL	1.8/3V

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Ball Name	Ball Number	Functional Description	Voltage(v)
PLLDVDD	L2	PLLx(x=0~4)digital power supply	1.1V
VDDQ	AC13,AC14,AC15,AC16,AC17,AC18	VDDQ power supply of LPDDR2/LPDDR3 and core	1.2V
VREF	AJ16	Vref power supply of LPDDR2	0.5*VDDQ
EFUSEVDD	V12	EFUSE power supply	2.5V
Analog Power Supply			
USBAVDD	K1	USB0 OTG power supply	3.3V
CPHYAVDD	AJ29	MIPI RX PHY analog power supply	2.5V
DPHYAVDD	K28	MIPI TX PHY analog power supply	2.5V
PLLAVDD	L1	PLLx(x=0~4)analog power supply	2.5V
Ground			
VSS	AD26,AE7,AE22,AE24,AE25,AF7,AF22,AF26,AG27,AH27,AH28,G13,G16,G17,G18,H4,L5,N13,N14,N15,N16,N17,P13,P14,P15,P16,P17,R13,R14,R15,R16,R17,T13,T14,T15,T16,T17,T25,U13,U15,U16,U17,U18	Ground	

2.5 Analog Signal

LC1813 chip analog signal and pin allocation are as shown in *Table 2-2*.

Table 2-2 LC1813 Analog Signal and Pin Allocation Table

Ball Name	Ball Number	Signal Name	Property	Functional Description
ISP Interface				
Power for the following pins are supplied by CPHYAVDD				
CPHY0REXT	AH29	isp_cphy0_rext	AIO	ISP MIPI CPHY0, external resistance connect with pin; 6. 04KΩ(1%)resistance to ground

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Ball Name	Ball Number	Signal Name	Property	Functional Description
CPHY0CLKP	AD28	isp_cphy0_clkp	AI	ISP MIPI CPHY0, P input of differential clock
CPHY0CLKN	AE28	isp_cphy0_clkn	AI	ISP MIPI CPHY0, N input of differential clock
CPHY0DP3	AC28	isp_cphy0_datap3	AI	ISP MIPI CPHY0 lane 3, P input of differential data
CPHY0DN3	AC27	isp_cphy0_datan3	AI	ISP MIPI CPHY0 lane 3, N input of differential data
CPHY0DP2	AC29	isp_cphy0_datap2	AI	ISP MIPI CPHY0 lane 2, P input of differential data
CPHY0DN2	AB29	isp_cphy0_datan2	AI	ISP MIPI CPHY0 lane 2, N input of differential data
CPHY0DP1	AF29	isp_cphy0_datap1	AI	ISP MIPI CPHY0 lane 1, P input of differential data
CPHY0DN1	AE29	isp_cphy0_datan1	AI	ISP MIPI CPHY0 lane 1, N input of differential data
CPHY0DP0	AF28	isp_cphy0_datap0	AI	ISP MIPI CPHY0 lane 0, P input of differential data
CPHY0DN0	AG28	isp_cphy0_datan0	AI	ISP MIPI CPHY0 lane 0, N input of differential data
DISPLAY DPHY Interface				
Power for the following pins are supplied by DPHYAVDD				
DPHYREXT	J28	mipi_dphy_rext	AIO	LCDC MIPI DPHY, external resistance connect with pin; 6.04KΩ(1%)resistance to ground.
DPHYCLKP	M28	mipi_dphy_clkp	AO	LCDC MIPI DPHY, P output of differential clock
DPHYCLKN	L28	mipi_dphy_clkn	AO	LCDC MIPI DPHY, N output of differential clock
DPHYDP3	P28	mipi_dphy_datap3	AO	LCDC MIPI DPHY lane 3, P output of differential data
DPHYDN3	N28	mipi_dphy_datan3	AO	LCDC MIPI DPHY lane 3, N output of differential data
DPHYDP2	N29	mipi_dphy_datap2	AO	LCDC MIPI DPHY lane 2, P output of differential data

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Ball Name	Ball Number	Signal Name	Property	Functional Description
DPHYDN2	P29	mipi_dphy_datan2	AO	LCDC MIPI DPHY lane 2, N output of differential data
DPHYDP1	L27	mipi_dphy_datap1	AO	LCDC MIPI DPHY lane 1, P output of differential data
DPHYDN1	M27	mipi_dphy_datan1	AO	LCDC MIPI DPHY lane 1, N output of differential data
DPHYDP0	L29	mipi_dphy_datap0	AIO	LCDC MIPI DPHY lane 0, P output of differential data
DPHYDN0	K29	mipi_dphy_datan0	AIO	LCDC MIPI DPHY lane 0, N output of differential data
USB0 OTG Interface				
Power for the following pins are supplied by USBAVDD				
USB0DP	K5	usb0_dp	AIO	USB0's data pin DATA+
USB0DM	J5	usb0_dm	AIO	USB0's data pin DATA -
USB0ID	K4	usb0_id	AIO	Connect to the ID pin on the Mini-type connector
USB0VBUS	J2	usb0_vbus	AIO	Connect to the VBUS pin on the connector
USB0VRES	H2	usb0_vres	AIO	Connect to an external 8.2K (±1%) Ohm resistor for band-gap reference circuit

2.6 Digital Signal

LC1813 chip digital signal and pin allocation are as shown in *Table 2-3*.

The relationship of gpio_d[242:0] with GPIO0 and GPIO1 is listed in *GPIO List.*

Table 2-3 LC1813 Chip Digital Signal and Pin Allocation Table

Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
MEMCTL Interface								
Power for the following pins are supplied by VDDQ								
DQ31	AG2	dmem_d[31]	IO	MEMCTL memory read/write data line [31]	NA	I	Z	NA

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
DQ30	AJ2	dmem_d[30]	IO	MEMCTL memory read/write data line [30]	NA	I	Z	NA
DQ29	AH1	dmem_d[29]	IO	MEMCTL memory read/write data line [29]	NA	I	Z	NA
DQ28	AJ1	dmem_d[28]	IO	MEMCTL memory read/write data line [28]	NA	I	Z	NA
DQ27	AH2	dmem_d[27]	IO	MEMCTL memory read/write data line [27]	NA	I	Z	NA
DQ26	AG4	dmem_d[26]	IO	MEMCTL memory read/write data line [26]	NA	I	Z	NA
DQ25	AH3	dmem_d[25]	IO	MEMCTL memory read/write data line [25]	NA	I	Z	NA
DQ24	AJ3	dmem_d[24]	IO	MEMCTL memory read/write data line [24]	NA	I	Z	NA
DQ23	AJ23	dmem_d[23]	IO	MEMCTL memory read/write data line [23]	NA	I	Z	NA
DQ22	AJ26	dmem_d[22]	IO	MEMCTL memory read/write data line [22]	NA	I	Z	NA
DQ21	AH22	dmem_d[21]	IO	MEMCTL memory read/write data line [21]	NA	I	Z	NA
DQ20	AH25	dmem_d[20]	IO	MEMCTL memory read/write data line [20]	NA	I	Z	NA
DQ19	AH24	dmem_d[19]	IO	MEMCTL memory read/write data line [19]	NA	I	Z	NA
DQ18	AG23	dmem_d[18]	IO	MEMCTL memory read/write data line [18]	NA	I	Z	NA
DQ17	AJ24	dmem_d[17]	IO	MEMCTL memory read/write data line [17]	NA	I	Z	NA
DQ16	AH26	dmem_d[16]	IO	MEMCTL memory read/write data line [16]	NA	I	Z	NA
DQ15	AJ5	dmem_d[15]	IO	MEMCTL memory	NA	I	Z	NA

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
				read/write data line [15]				
DQ14	AH6	dmem_d[14]	IO	MEMCTL memory read/write data line [14]	NA	I	Z	NA
DQ13	AH7	dmem_d[13]	IO	MEMCTL memory read/write data line [13]	NA	I	Z	NA
DQ12	AG6	dmem_d[12]	IO	MEMCTL memory read/write data line [12]	NA	I	Z	NA
DQ11	AJ6	dmem_d[11]	IO	MEMCTL memory read/write data line [11]	NA	I	Z	NA
DQ10	AH8	dmem_d[10]	IO	MEMCTL memory read/write data line [10]	NA	I	Z	NA
DQ09	AJ8	dmem_d[9]	IO	MEMCTL memory read/write data line [9]	NA	I	Z	NA
DQ08	AG7	dmem_d[8]	IO	MEMCTL memory read/write data line [8]	NA	I	Z	NA
DQ07	AH20	dmem_d[7]	IO	MEMCTL memory read/write data line [7]	NA	I	Z	NA
DQ06	AH19	dmem_d[6]	IO	MEMCTL memory read/write data line [6]	NA	I	Z	NA
DQ05	AG18	dmem_d[5]	IO	MEMCTL memory read/write data line [5]	NA	I	Z	NA
DQ04	AG19	dmem_d[4]	IO	MEMCTL memory read/write data line [4]	NA	I	Z	NA
DQ03	AJ21	dmem_d[3]	IO	MEMCTL memory read/write data line [3]	NA	I	Z	NA
DQ02	AJ20	dmem_d[2]	IO	MEMCTL memory read/write data line [2]	NA	I	Z	NA
DQ01	AF19	dmem_d[1]	IO	MEMCTL memory read/write data line [1]	NA	I	Z	NA
DQ00	AF20	dmem_d[0]	IO	MEMCTL memory read/write data line [0]	NA	I	Z	NA

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
A15	AF18	dmem_a[15]	O	MEMCTL memory read/write address line [15]	NA	O	0	NA
A14	AH17	dmem_a[14]	O	MEMCTL memory read/write address line [14]	NA	O	0	NA
A13	AH16	dmem_a[13]	O	MEMCTL memory read/write address line [13]	NA	O	0	NA
A12	AG16	dmem_a[12]	O	MEMCTL memory read/write address line [12]	NA	O	0	NA
A11	AE16	dmem_a[11]	O	MEMCTL memory read/write address line [11]	NA	O	0	NA
A10	AJ15	dmem_a[10]	O	MEMCTL memory read/write address line [10]	NA	O	0	NA
A9	AJ12	dmem_a[9]	O	MEMCTL memory read/write address line [9]	NA	O	0	NA
A8	AF11	dmem_a[8]	O	MEMCTL memory read/write address line [8]	NA	O	0	NA
A7	AJ11	dmem_a[7]	O	MEMCTL memory read/write address line [7]	NA	O	0	NA
A6	AG11	dmem_a[6]	O	MEMCTL memory read/write address line [6]	NA	O	0	NA
A5	AF12	dmem_a[5]	O	MEMCTL memory read/write address line [5]	NA	O	0	NA
A4	AH15	dmem_a[4]	O	MEMCTL memory read/write address line [4]	NA	O	0	NA
A3	AH14	dmem_a[3]	O	MEMCTL memory read/write address line [3]	NA	O	0	NA

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
A2	AF16	dmem_a[2]	O	MEMCTL memory read/write address line [2]	NA	O	0	NA
A1	AJ14	dmem_a[1]	O	MEMCTL memory read/write address line [1]	NA	O	0	NA
A0	AF15	dmem_a[0]	O	MEMCTL memory read/write address line [0]	NA	O	0	NA
CK0	AF14	dmem_ck	O	MEMCTL memory clock signal	NA	O	0	NA
CKN0	AE13	dmem_ckn	O	MEMCTL memory reverse clock signal	NA	O	1	NA
CKE1	AH12	dmem_cke[1]	O	MEMCTL memory clock enable signal, active-HIGH, corresponding to chip select 1	NA	O	0	NA
CKE0	AH11	dmem_cke[0]	O	MEMCTL memory clock enable signal, active-HIGH, corresponding to chip select 0	NA	O	0	NA
CSN1	AG14	dmem_cen[1]	O	MEMCTL memory chip select signal [1], active-LOW	NA	O	1	NA
CSN0	AH13	dmem_cen[0]	O	MEMCTL memory chip select signal [0], active-LOW	NA	O	1	NA
RASN	AE10	dmem_rasn	O	MEMCTL memory Row address select signal, active-LOW	NA	O	1	NA
CASN	AF8	dmem_casn	O	MEMCTL memory Column address select signal, active-LOW	NA	O	1	NA
WEN	AE9	dmem_wen	O	MEMCTLmemory write enable signal, active-LOW	NA	O	1	NA

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
BA2	AE12	dmem_bank[2]	O	MEMCTL memory BANK address line [2]	NA	O	0	NA
BA1	AF10	dmem_bank[1]	O	MEMCTL memory BANK address line [1]	NA	O	0	NA
BA0	AG10	dmem_bank[0]	O	MEMCTL memory BANK address line [0]	NA	O	0	NA
DQS3	AG3	dmem_dqs[3]	IO	MEMCTL memory data strobe signal [3], active-HIGH	NA	I	Z	NA
DQS2	AH23	dmem_dqs[2]	IO	MEMCTL memory data strobe signal [2], active-HIGH	NA	I	Z	NA
DQS1	AJ9	dmem_dqs[1]	IO	MEMCTL memory data strobe signal [1], active-HIGH	NA	I	Z	NA
DQS0	AJ18	dmem_dqs[0]	IO	MEMCTL memory data strobe signal [0], active-HIGH	NA	I	Z	NA
DQSN3	AH4	dmem_dqsn[3]	IO	MEMCTL memory data reverse strobe ignal [3], active-HIGH	NA	I	Z	NA
DQSN2	AG22	dmem_dqsn[2]	IO	MEMCTL memory data reverse strobe ignal [2], active-HIGH	NA	I	Z	NA
DQSN1	AH9	dmem_dqsn[1]	IO	MEMCTL memory data reverse strobe ignal [1], active-HIGH	NA	I	Z	NA
DQSN0	AH18	dmem_dqsn[0]	IO	MEMCTL memory data reverse strobe ignal [0], active-HIGH	NA	I	Z	NA
DM3	AH5	dmem_dm[3]	O	MEMCTL memory data bit [31: 24] write-protect Read Enable signal, active-HIGH	NA	I	Z	NA

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
DM2	AH21	dmem_dm[2]	O	MEMCTL memory data bit [23: 16] write-protect Read Enable signal, active-HIGH	NA	I	Z	NA
DM1	AH10	dmem_dm[1]	O	MEMCTL memory data bit [15: 8] write-protect Read Enable signal, active-HIGH	NA	I	Z	NA
DM0	AJ17	dmem_dm[0]	O	MEMCTL memory data bit [7: 0] write-protect Read Enable signal, active-HIGH	NA	I	Z	NA
RSTO	AF23	dmem_rstn	O	MEMCTLmemory reset signal, active-LOW	NA	O	1	NA
RNK1	AE18	dmem_odt[1]	O	MEMCTL memory On-Die Termination signal [1]	NA	O	0	NA
RNK0	AE21	dmem_odt[0]	O	MEMCTL memory On-Die Termination signal [0]	NA	O	0	NA
DTO1	AG26	dmem_dto[1]	O	MEMCTL memory digital test signal 1	NA	O	0	NA
DTO0	AJ27	dmem_dto[0]	O	MEMCTL memory digital test signal 0	NA	O	0	NA
ATO	AF24	dmem_ato	O	MEMCTL memory analog test signal	NA	O	Z	NA
ZQ	AE1	dmem_zq	O	MEMCTL memory ZQ signal	NA	IO	Z	NA
Note: ZQ is the connective signal of LPDDR2,this PAD pin should be connected through an external 240ohm ± 1% resistor (RZQ) to ground on PCB.								
TDIF RX0 and GSM0 Interface								
Power for the following pins are supplied by PVDD2								
GSM Interface								
CLK26DI	G15	clk26m_in1	I	external 26M crystal	4mA	I	Z	pulldown resistor is

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
1				oscillator 1 digital clock input				internally connected, and pulldown is disabled by default
		gpio_d[32]	IO	General Purpose I/O Port [32]				
OSCEN1	G14	osc_en1	O	external crystal oscillator 1 enabled, HIGH active	8mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[33]	IO	General Purpose I/O Port [33]				
GSM0GPO3	B13	gsm0_sw_gpo[3]	O	GSM General Purpose Output Port [3]	8mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[16]	IO	General Purpose I/O Port [16]				
GSM0GPO2	B12	gsm0_sw_gpo[2]	O	GSM General Purpose Output Port [2]	8mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[17]	IO	General Purpose I/O Port [17]				
GSM0GPO1	A13	gsm0_sw_gpo[1]	O	GSM General Purpose Output Port [1]	8mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[18]	IO	General Purpose I/O Port [18]				
GSM0GPO0	D14	gsm0_sw_gpo[0]	O	GSM General Purpose Output Port [0]	8mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[19]	IO	General Purpose I/O Port [19]				
DRF0D	B10	gsm0_digrf_d	IO	DIGRF Interface 0 receives and transmits data signal	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
DRF0DEN	A10	gsm0_digrf_den	IO	DIGRF Interface 0 receives and transmits valid data signal, active-HIGH	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
DRF0STBE	A11	gsm0_strobe	O	DIGRF Interface 0 strobe sync signal	8mA	O	0	NA
GSM0GPO	D6	gsm0_gpo	O	GSM General Purpose Output Port	8mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
CLK26DI0	E12	clk26m_in0	I	external 26M crystal oscillator 0 digital clock input	4mA	I	Z	NA
OSCEN0	B11	osc_en0	O	external crystal oscillator 0 enabled, HIGH active	8mA	O	0	NA
TDIF RX0 Interface								
TDD09	D8	td_data0[9]	IO	TD parallel interface 0 data [9]	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
TDD08	A8	td_data0[8]	IO	TD parallel interface 0 data [8]	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
TDD07	D7	td_data0[7]	IO	TD parallel interface 0 data [7]	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
TDD06	B8	td_data0[6]	IO	TD parallel interface 0 data [6]	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
TDD05	B6	td_data0[5]	IO	TD parallel interface 0 data [5]	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
TDD04	A7	td_data0[4]	IO	TD parallel interface 0 data [4]	8mA	I	Z	pulldown resistor is internally connected, and pulldown is

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
								disabled by default
TDD03	E8	td_data0[3]	IO	TD parallel interface 0 data [3]	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
TDD02	C7	td_data0[2]	IO	TD parallel interface 0 data [2]	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
TDD01	A5	td_data0[1]	IO	TD parallel interface 0 data [1]	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
TDD00	B7	td_data0[0]	IO	TD parallel interface 0 data [0]	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
TDSCK0	E9	td_sclk0	O	TD analog front-end 0 output 5. 12M clock to sample the card inputs	8mA	O	0	NA
SPIDIN	C11	td_spi_din	I	TD SPI Interface data input	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[44]	IO	General Purpose I/O Port [44]				
SPIDO	C10	td_spi_dout	IO	TD SPI Interface data input	8mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[45]	IO	General Purpose I/O Port [45]				
SPICK	B9	td_spi_clk	O	TD SPI Interface clock Output	8mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[46]	IO	General Purpose I/O Port [46]				
SPICS0	D10	td_spi_cs0	O	TD SPI Interface chip	8mA	O	1	pulldown resistor is

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
				select 0(for TD)				internally connected, and pulldown is disabled by default
		gpio_d[47]	IO	General Purpose I/O Port [47]				
SPICS2	E14	gsm0_spi_cs2	O	TD SPI Interface chip selcect 2(for GSM)	8mA	O	1	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[48]	IO	General Purpose I/O Port [48]				
TDGPO11	C6	td_gpo[11]	O	TD General Purpose Output Port [11]	8mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[59]	IO	General Purpose I/O Port [59]				
TDGPO10	D11	td_gpo[10]	O	TD General Purpose Output Port [10]	8mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[60]	IO	General Purpose I/O Port [60]				
TDGPO9	E11	td_gpo[9]	O	TD General Purpose Output Port [9]	8mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[61]	IO	General Purpose I/O Port [61]				
TDGPO8	D13	td_gpo[8]	O	TD General Purpose Output Port [8]	8mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[62]	IO	General Purpose I/O Port [62]				
TDGPO7	C3	td_gpo[7]	O	TD General Purpose Output Port [7]	8mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[63]	IO	General Purpose I/O Port [63]				
TDGPO6	B3	td_gpo[6]	O	TD General Purpose Output Port [6]	8mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[64]	IO	General Purpose I/O Port [64]				

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
TDGPO5	B4	td_gpo[5]	O	TD General Purpose Output Port [5]	8mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[65]	IO	General Purpose I/O Port [65]				
TDGPO4	A2	td_gpo[4]	O	TD General Purpose Output Port [4]	8mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[66]	IO	General Purpose I/O Port [66]				
TDGPO3	B5	td_gpo[3]	O	TD General Purpose Output Port [3]	8mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[67]	IO	General Purpose I/O Port [67]				
TDGPO2	D5	td_gpo[2]	O	TD General Purpose Output Port [2]	8mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[68]	IO	General Purpose I/O Port [68]				
TDGPO1	A4	td_gpo[1]	O	TD General Purpose Output Port [1]	8mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[69]	IO	General Purpose I/O Port [69]				
TDGPO0	C4	td_gpo[0]	O	TD General Purpose Output Port [0]	8mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[70]	IO	General Purpose I/O Port [70]				
Power for the following pins are supplied by PVDD6								
CAMER RGB Interface								
ISPFSIN0	W27	isp_fsin0	IO	ISP frame sync0 / ISP general control output	8mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[229]	IO	General Purpose I/O Port [229]				
ISPFSIN1	W28	isp_fsin1	IO	ISP frame sync1 / ISP	8mA	O	0	pulldown resistor is

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
				general control output				internally connected, and pulldown is disabled by default
		gpio_d[230]	IO	General Purpose I/O Port [230]				
ISPPWM	Y29	isp_pwm	O	ISP pwm signal to control external image sensor strobe flash / ISP general control output	8mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		pwm[1]	O	PWM output signal 1				
		gpio_d[71]	IO	General Purpose I/O Port [71]				
ISPSCLK0	R23	isp_sclk0	O	ISP output clock signal to external image sensor0/1	8mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[72]	IO	General Purpose I/O Port [72]				
ISPSTBE	AD25	isp_strobe	I	ISP strobe input signal from external image sensor	8mA	I	0	pulldown resistor is internally connected, and pulldown is enabled by default
		gpio_d[73]	IO	General Purpose I/O Port [73]				
ISPSD9	AA25	isp_s_data[9]	I	ISP camera parallel interface data [9]	8mA	I	0	pulldown resistor is internally connected, and pulldown is enabled by default
		gpio_d[80]	IO	General Purpose I/O Port [80]				
ISPSD8	W26	isp_s_data[8]	I	ISP camera parallel interface data [8]	8mA	I	0	pulldown resistor is internally connected, and pulldown is enabled by default
		gpio_d[81]	IO	General Purpose I/O Port [81]				
ISPSD7	Y25	isp_s_data[7]	I	ISP camera parallel interface data [7]	8mA	I	0	pulldown resistor is internally connected, and pulldown is enabled by default
		gpio_d[74]	IO	General Purpose I/O Port [74]				

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
ISPSD6	AB28	isp_s_data[6]	I	ISP camera parallel interface data [6]	8mA	I	0	pulldown resistor is internally connected, and pulldown is enabled by default
		gpio_d[75]	IO	General Purpose I/O Port [75]				
ISPSD5	AC26	isp_s_data[5]	I	ISP camera parallel interface data [5]	8mA	I	0	pulldown resistor is internally connected, and pulldown is enabled by default
		gpio_d[76]	IO	General Purpose I/O Port [76]				
ISPSD4	AA28	isp_s_data[4]	I	ISP camera parallel interface data [4]	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[77]	IO	General Purpose I/O Port [77]				
ISPSD3	W25	isp_s_data[3]	I	ISP camera parallel interface data [3]	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[78]	IO	General Purpose I/O Port [78]				
ISPSD2	Y28	isp_s_data[2]	I	ISP camera parallel interface data [2]	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[79]	IO	General Purpose I/O Port [79]				
ISPSCLK	Y27	isp_sclk	I	ISP camera parallel interface clock signal	8mA	I	0	pulldown resistor is internally connected, and pulldown is enabled by default
		gpio_d[82]	IO	General Purpose I/O Port [82]				
CLKO2 Pin								
CLKO2	Y26	clk_out[2]	O	AP_PWR output signal clkout1	8mA	O	0	NA
		isp_sclk1	O	ISP output clock signal to external image sensor2				
		gpio_d[211]	IO	General Purpose I/O Port [211]				

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
ISP Parallel Interface								
ISPSHS	AB26	isp_s_hsync	I	ISP camera parallel interface video horizontal signal	8mA	I	0	pulldown resistor is internally connected, and pulldown is enabled by default
		gpio_d[83]	IO	General Purpose I/O Port [83]				
ISPSVS	AC25	isp_s_vsync	I	ISP camera parallel interface video vertical signal	8mA	I	0	pulldown resistor is internally connected, and pulldown is enabled by default
		gpio_d[84]	IO	General Purpose I/O Port [84]				
ISPSCL	AD27	isp_i2c_scl	IO	ISP SCCB interface clock signal	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		i2c3_scl	IO	I2C3 clock signal				
		gpio_d[85]	IO	General Purpose I/O Port [85]				
ISPSDA	AF27	isp_i2c_sda	IO	ISP SCCB interface data signal	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		i2c3_sda	IO	I2C3 data signal				
		gpio_d[86]	IO	General Purpose I/O Port [86]				
ISPRSTN0	V28	isp_rst_n0	O	ISP output reset signal to image sensor0/1	8mA	O	0	pulldown resistor is internally connected, and pulldown is enabled by default
		gpio_d[26]	IO	General Purpose I/O Port [26]				
ISPRSTN1	V26	isp_rst_n1	O	ISP output reset signal to image sensor2	8mA	O	0	pulldown resistor is internally connected, and pulldown is enabled by default
		gpio_d[27]	IO	General Purpose I/O Port [27]				
ISPPDW	W29	isp_pdwn_0	O	ISP output power down signal to image sensor0 /	8mA	O	0	Pullup resistor is internally connected,

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
N0				ISP general control output				and pullup is disabled by default
		gpio_d[15]	IO	General Purpose I/O Port [15]				
ISPPDWN1	U28	isp_pdwn_1	O	ISP output power down signal to image sensor1 / ISP general control output	8mA	O	0	Pullup resistor is internally connected, and pullup is disabled by default
		gpio_d[14]	IO	General Purpose I/O Port [14]				
Power for the following pins are supplied by PVDD5								
KBDKI7	G28	kbs_dki[7]	I	KBS direct key in [7]	8mA	I	0	pulldown resistor is internally connected, and pulldown is enabled by default
		dsi_te	I	Tear signal of dsi controller				
		gpio_d[96]	IO	General Purpose I/O Port [96]				
Power for the following pins are supplied by PVDD15								
KBDKI6	M4	kbs_dki[6]	I	KBS direct key in [6]	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[97]	IO	General Purpose I/O Port [97]				
KBDKI5	K3	kbs_dki[5]	I	KBS direct key in [5]	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[98]	IO	General Purpose I/O Port [98]				
KBDKI4	K2	kbs_dki[4]	I	KBS direct key in [4]	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[99]	IO	General Purpose I/O Port [99]				
KBDKI3	L3	kbs_dki[3]	I	KBS direct key in [3]	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[100]	IO	General Purpose I/O Port [100]				
KBDKI2	L4	kbs_dki[2]	I	KBS direct key in [2]	8mA	I	1	Pullup resistor is

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
		gpio_d[101]	IO	General Purpose I/O Port [101]				internally connected, and pullup is enabled by default
PWM,SSI0,SSI2,GPIO25,GPIO28,GPIO12 Interface								
Power for the following pins are supplied by PVDD5								
PWM Interface								
PWM0	P25	pwm[0]	O	PWM output signal 0	8mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[149]	IO	General Purpose IO [149]				
SSI0 Interface								
S0TXD	T28	ssi0_tx	O	SSI0 output data line	4mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[160]	IO	General Purpose I/O Port [160]				
S0RXD	P26	ssi0_rx	I	SSI0 input data line	4mA	I	0	pulldown resistor is internally connected, and pulldown is enabled by default
		gpio_d[161]	IO	General Purpose I/O Port [161]				
S0CLK	R26	ssi0_clk	O	SSI0 output clock signal	4mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[162]	IO	General Purpose I/O Port [162]				
S0SN1	K25	ssi0_ssn[1]	O	SSI0 slave 1 select signal, active-LOW	4mA	O	1	Pullup resistor is internally connected, and pullup is disabled by default
		gpio_d[163]	IO	General Purpose I/O Port [163]				
S0SN0	M26	ssi0_ssn[0]	O	SSI0 slave 0 select signal, active-LOW	4mA	O	1	Pullup resistor is internally connected, and pullup is disabled by default
		gpio_d[164]	IO	General Purpose I/O Port [164]				
SSI2 Interface								

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
S2TXD	K26	ssi2_tx	O	SSI2 output data line	4mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[169]	IO	General Purpose I/O Port [169]				
S2RXD	L26	ssi2_rx	I	SSI2 input data line	4mA	I	0	pulldown resistor is internally connected, and pulldown is enabled by default
		gpio_d[170]	IO	General Purpose I/O Port [170]				
S2CLK	H29	ssi2_clk	O	SSI2 output clock signal	4mA	O	0	Pullup resistor is internally connected, and pullup is disabled by default
		i2c2_scl	IO	I2C2 clock signal				
		gpio_d[171]	IO	General Purpose I/O Port [171]				
S2SN	G29	ssi2_ssn	O	SSI0 slave select signal, active-LOW	4mA	O	1	Pullup resistor is internally connected, and pullup is disabled by default
		i2c2_sda	IO	I2C2 data signal				
		gpio_d[172]	IO	General Purpose I/O Port [172]				
GPIO25	N25	gpio_d[25]	IO	General Purpose I/O Port [25]	8mA	I	0	pulldown resistor is internally connected, and pulldown is enabled by default
GPIO28	R27	usb0_drvvbus	O	usb0 Drive VBUS, Enables driving VBUS to 5 V	8mA	O	0	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[28]	IO	General Purpose I/O Port [28]				
GPIO12	H28	gpio_d[12]	IO	General Purpose I/O Port [12]	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
COM_PCM1,UART2,I2C0,GPIO232~GPIO234,GPIO6~11,GPIO24,CLKO1 Interface								
Power for the following pins are supplied by PVDD7								

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
COM_PCM1 Interface								
CS1TXD	E17	com_pcm1_tx	O	COM_PCM1 data output line	4mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		i2s1_sdout	O	I2S1 data output line				
		gpio_d[177]	IO	General Purpose I/O Port [177]				
CS1RXD	B15	com_pcm1_rx	I	COM_PCM1 data input line	4mA	I	0	pulldown resistor is internally connected, and pulldown is enabled by default
		i2s1_sdin	I	I2S1 data input line				
		gpio_d[178]	IO	General Purpose I/O Port [178]				
CS1CLK	A16	com_pcm1_clk	IO	COM_PCM1 clock signal	4mA	I	0	pulldown resistor is internally connected, and pulldown is enabled by default
		i2s1_sclk	IO	I2S1 clock signal				
		gpio_d[179]	IO	General Purpose I/O Port [179]				
CS1SN	C15	com_pcm1_ssn	IO	COM_PCM1 frame start signal	4mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		i2s1_ws	IO	I2S1 left and right channel select signal				
		gpio_d[180]	IO	General Purpose I/O Port [180]				
UART2 Interface								
U2TXD	B14	uart2_tx	O	UART2 output signal	8mA	O	1	Pullup resistor is internally connected, and pullup is disabled by default
		gpio_d[150]	IO	General Purpose I/O Port [150]				
U2RXD	D15	uart2_rx	I	UART2 input signal	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[151]	IO	General Purpose I/O Port [151]				
U2CTS	A14	uart2_cts	I	UART2 clear-to-send	8mA	I	1	Pullup resistor is

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
				signal, active-Low				internally connected, and pullup is enabled by default
		gpio_d[152]	IO	General Purpose I/O Port [152]				
		uart2_rts	O	UART2 request-to-send signal, active-Low				pulldown resistor is internally connected, and pulldown is disabled by default
U2RTS	C14	gpio_d[153]	IO	General Purpose I/O Port [153]	8mA	O	1	
CLKO1 Pin								
		clk_out[1]	O	AP_PWR output signal clkout0				
CLKO1	E19	gpio_d[212]	IO	General Purpose I/O Port [212]	8mA	O	0	NA
I2C0 Interface								
		i2c0_scl	IO	I2C0 clock signal				Pullup resistor is internally connected, and pullup is enabled by default
IIC0SCL	D17	gpio_d[187]	IO	General Purpose I/O Port [187]	8mA	I	1	
		i2c0_sda	IO	I2C0 data signal				Pullup resistor is internally connected, and pullup is enabled by default
IIC0SDA	E18	gpio_d[188]	IO	General Purpose I/O Port [188]	8mA	I	1	
GPIO232~GPIO234,GPIO6~11,GPIO24 Interface								
GPIO232	B17	gpio_d[232]	IO	General Purpose I/O Port [232]	8mA	I	0	pulldown resistor is internally connected, and pulldown is enabled by default
GPIO233	E15	gpio_d[233]	IO	General Purpose I/O Port [233]	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
GPIO234	C18	gpio_d[234]	IO	General Purpose I/O Port [234]	8mA	I	Z	pulldown resistor is internally connected, and pulldown is

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
								disabled by default
GPIO11	B16	gpio_d[11]	IO	General Purpose I/O Port [11]	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
GPIO10	B18	gpio_d[10]	IO	General Purpose I/O Port [10]	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
GPIO9	A19	gpio_d[9]	IO	General Purpose I/O Port [9]	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
GPIO8	D18	gpio_d[8]	IO	General Purpose I/O Port [8]	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
GPIO7	B19	gpio_d[7]	IO	General Purpose I/O Port [7]	8mA	I	0	pulldown resistor is internally connected, and pulldown is enabled by default
GPIO6	C19	gpio_d[6]	IO	General Purpose I/O Port [6]	8mA	I	0	pulldown resistor is internally connected, and pulldown is enabled by default
GPIO24	A17	gpio_d[24]	IO	General Purpose I/O Port [24]	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
UART1,CLKO2,GPIO0~GPIO2,GPIO22~GPIO23,GPIO5,CLKO3,I2C1 Interface								
Power for the following pins are supplied by PVDD9								
UART1 Interface								
U1TXD	R2	uart1_tx	O	UART1 output signal	8mA	O	1	Pullup resistor is

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
		gpio_d[154]	IO	General Purpose I/O Port [154]				internally connected, and pullup is disabled by default
U1RXD	T5	uart1_rx	I	UART1 input signal	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[155]	IO	General Purpose I/O Port [155]				
U1CTS	T2	uart1_cts	I	UART1 clear-to-send signal, active-LOW	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[156]	IO	General Purpose I/O Port [156]				
U1RTS	T4	uart1_rts	O	UART1 request-to-send signal, active-LOW	8mA	O	1	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[157]	IO	General Purpose I/O Port [157]				
CLKO3 Pin								
CLKO3	R7	clk_out[3]	O	AP_PWR output signal clkout2	8mA	O	0	NA
		gpio_d[210]	IO	General Purpose I/O Port [210]				
GPIO0~GPIO2,SECSMC,SECSW,GPIO5 Interface								
GPIO2	U1	gpio_d[2]	IO	General Purpose I/O Port [2]	8mA	I	0	pulldown resistor is internally connected, and pulldown is enabled by default
GPIO1	V4	gpio_d[1]	IO	General Purpose I/O Port [1]	8mA	I	0	pulldown resistor is internally connected, and pulldown is enabled by default
GPIO0	V3	gpio_d[0]	IO	General Purpose I/O Port [0]	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
SECSMC	T1	sec_smc	I	secure key, control MIC and Camera	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[23]	IO	General Purpose I/O Port [23]				
SECSW	U5	sec_sw	I	secure key, control security mode	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[22]	IO	General Purpose I/O Port [22]				
GPIO5	U2	gpio_d[5]	IO	General Purpose I/O Port [5]	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
I2C1 Interface								
IIC1SCL	R3	i2c1_scl	IO	I2C1 clock signal	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[189]	IO	General Purpose I/O Port [189]				
IIC1SDA	R4	i2c1_sda	IO	I2C1 data signal	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[190]	IO	General Purpose I/O Port [190]				
NADNFLASH,SDMMC1 Interface								
Power for the following pins are supplied by PVDD10								
NANDFLASH Interface								
NANDD15	AC5	nand_io[15]	IO	nandflash data inputs/outputs bit[15]	4mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[109]	IO	General purpose I/O port[109]				
NANDD14	AA5	nand_io[14]	IO	nandflash data inputs/outputs bit[14]	4mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[110]	IO	General purpose I/O port[110]				

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
NANDD13	AB4	nand_io[13]	IO	nandflash data inputs/outputs bit[13]	4mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[111]	IO	General purpose I/O port[111]				
NANDD12	AB2	nand_io[12]	IO	nandflash data inputs/outputs bit[12]	4mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[112]	IO	General purpose I/O port[112]				
NANDD11	AB3	nand_io[11]	IO	nandflash data inputs/outputs bit[11]	4mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[113]	IO	General purpose I/O port[113]				
NANDD10	AB5	nand_io[10]	IO	nandflash data inputs/outputs bit[10]	4mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[114]	IO	General purpose I/O port[114]				
NANDD9	W4	nand_io[9]	IO	nandflash data inputs/outputs bit[15]	4mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[115]	IO	General purpose I/O port[109]				
NANDD8	Y2	nand_io[8]	IO	nandflash data inputs/outputs bit[15]	4mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[116]	IO	General purpose I/O port[109]				
NANDD7	Y1	nand_io[7]	IO	nandflash data inputs/outputs bit[15]	4mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[87]	IO	General purpose I/O port[109]				
NANDD6	AA2	nand_io[6]	IO	nandflash data inputs/outputs bit[6]	4mA	O	0	pulldown resistor is internally connected, and pulldown is
		clkout4	O	DDR_PWR output signal				

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
				clk_out4				disabled by default
		gpio_d[88]	IO	General purpose I/O port[88]				
		nand_io[5]	IO	General purpose I/O port[5]				
		cp_clkout	O	CP_PWR output signal cp_clkout				pulldown resistor is internally connected, and pulldown is disabled by default
NANDD5	AB1	gpio_d[89]	IO	General purpose I/O port[89]	4mA	O	0	
		nand_io[4]	IO	nandflash data inputs/outputs bit[4]				pulldown resistor is internally connected, and pulldown is disabled by default
NANDD4	Y5	gpio_d[90]	IO	General purpose I/O port[90]	4mA	O	0	
		nand_io[3]	IO	nandflash data inputs/outputs bit[3]				pulldown resistor is internally connected, and pulldown is disabled by default
NANDD3	Y4	gpio_d[91]	IO	General purpose I/O port[91]	4mA	O	0	
		nand_io[2]	IO	nandflash data inputs/outputs bit[2]				pulldown resistor is internally connected, and pulldown is disabled by default
NANDD2	AF3	gpio_d[92]	IO	General purpose I/O port[92]	4mA	O	0	
		nand_io[1]	IO	nandflash data inputs/outputs bit[1]				pulldown resistor is internally connected, and pulldown is disabled by default
NANDD1	AF4	gpio_d[93]	IO	General purpose I/O port[93]	4mA	O	0	
		nand_io[0]	IO	nandflash data inputs/outputs bit[0]				pulldown resistor is internally connected, and pulldown is disabled by default
NANDD0	AC1	gpio_d[94]	IO	General purpose I/O port[94]	4mA	O	0	
SDMMC1 Data Port 6 and 7								

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
MMC1D6	AC4	mmc1_data[6]	IO	SDMMC1 card bi-direction data port[6]	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		nand_cle	O	nandflash command latch enable, active-HIGH				
		gpio_d[117]	IO	General purpose I/O port[117]				
MMC1D7	AC2	mmc1_data[7]	IO	SDMMC1 card bi-direction data port[7]	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		nand_ale	O	nandflash address latch enable, active-HIGH				
		gpio_d[118]	IO	General purpose I/O port[118]				
NANDFLASH Interface, WEN and OEN								
NANDWEN	W3	nand_wen	O	nandflash write enable, active-LOW	4mA	O	1	Pullup resistor is internally connected, and pullup is disabled by default
		gpio_d[119]	IO	General purpose I/O port[119]				
NANDOEN	W2	nand_oen	O	nandflash read enable, active-LOW	4mA	O	1	Pullup resistor is internally connected, and pullup is disabled by default
		gpio_d[120]	IO	General purpose I/O port[120]				
SDMMC1 Data Port, CLK and CMD								
MMC1D0	AF2	mmc1_data[0]	IO	SDMMC1 card bi-direction data port[0]	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		nand_rb	I	nandflash ready/busy signal				
		gpio_d[121]	IO	General purpose I/O port[121]				
MMC1D1	AF6	mmc1_data[1]	IO	SDMMC1 card bi-direction data port[1]	8mA	I	1	Pullup resistor is internally connected,

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
		nand_csn1	O	nandflash chip select bit1, active-LOW				and pullup is enabled by default
		gpio_d[122]	IO	General purpose I/O port[122]				
MMC1D2	AD4	mmc1_data[2]	IO	SDMMC1 card bi-direction data port[2]	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		nand_csn0	O	nandflash chip select bit0, active-LOW				
		gpio_d[123]	IO	General purpose I/O port[123]				
MMC1D3	AE2	mmc1_data[3]	IO	SDMMC1 card bi-direction data port[3]	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[126]	IO	General purpose I/O port[126]				
MMC1D4	AD2	mmc1_data[4]	IO	SDMMC1 card bi-direction data port[4]	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[127]	IO	General purpose I/O port[127]				
MMC1D5	AC3	mmc1_data[5]	IO	SDMMC1 card bi-direction data port[5]	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[128]	IO	General purpose I/O port[128]				
MMC1CLK	AD5	mmc1_clk	O	SDMMC1 card clock signal	8mA	O	0	NA
		gpio_d[129]	IO	General Purpose I/O Port [129]				
MMC1CMD	AE6	mmc1_cmd	IO	SDMMC1 card bi-direction command/ response signal	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[130]	IO	General Purpose I/O Port [130]				

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
SDMMC0 Interface								
Power for the following pins are supplied by PVDD11								
MMC0CLK	F28	mmc0_clk	O	SDMMC0 card clock signal	16mA	O	0	NA
		gpio_d[131]	IO	General Purpose I/O Port [131]				
MMC0CMD	E29	mmc0_cmd	IO	SDMMC0 card bi-direction command/ response signal	16mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[132]	IO	General Purpose I/O Port [132]				
MMC0D3	E28	mmc0_data[3]	IO	SDMMC0 card bi-direction data port [3]	16mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[133]	IO	General Purpose I/O Port [133]				
MMC0D2	D29	mmc0_data[2]	IO	SDMMC0 card bi-direction data port [2]	16mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[134]	IO	General Purpose I/O Port [134]				
MMC0D1	C28	mmc0_data[1]	IO	SDMMC0 card bi-direction data port [1]	16mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[135]	IO	General Purpose I/O Port [135]				
MMC0D0	D28	mmc0_data[0]	IO	SDMMC0 card bi-direction data port [0]	16mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[136]	IO	General Purpose I/O Port [136]				
SDMMC2 Interface								
Power for the following pins are supplied by PVDD12								
MMC2CLK	B25	mmc2_clk	O	SDMMC2 card clock signal	8mA	O	0	NA

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
		gpio_d[137]	IO	General Purpose I/O Port [137]				
MMC2CMD	B24	mmc2_cmd	IO	SDMMC2 card bi-direction command/ response signal	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[138]	IO	General Purpose I/O Port [138]				
MMC2D3	D24	mmc2_data[3]	IO	SDMMC2 card bi-direction data port [3]	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[139]	IO	General Purpose I/O Port [139]				
MMC2D2	C26	mmc2_data[2]	IO	SDMMC2 card bi-direction data port [2]	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[140]	IO	General Purpose I/O Port [140]				
MMC2D1	C27	mmc2_data[1]	IO	SDMMC2 card bi-direction data port [1]	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[141]	IO	General Purpose I/O Port [141]				
MMC2D0	B27	mmc2_data[0]	IO	SDMMC2 card bi-direction data port [0]	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[142]	IO	General Purpose I/O Port [142]				
UART0 Interface								
Power for the following pins are supplied by PVDD13								
U0TXD	H26	uart0_tx	O	UART0 output signal	8mA	O	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[145]	IO	General Purpose I/O Port [145]				
		ssi3_tx	O	SSI3 output data line				
U0RXD	G25	uart0_rx	I	UART0 input signal	8mA	I	1	Pullup resistor is

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
		gpio_d[146]	IO	General Purpose I/O Port [146]				internally connected, and pullup is enabled by default
		ssi3_rx	I	SSI3 input data line				
U0CTS	J25	uart0_cts	I	UART0 clear-to-send signal, active-LOW	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[147]	IO	General Purpose I/O Port [147]				
		ssi3_clk	O	SSI3 output clock signal				
U0RTS	H27	uart0_rts	O	UART0 request-to-send signal, active-LOW	8mA	O	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[148]	IO	General Purpose I/O Port [148]				
		ssi3_ssn	O	SSI3 slave select signal, active-LOW				
SSI1,GPIO3,GPIO4 Interface								
Power for the following pins are supplied by PVDD14								
S1TXD	E27	ssi1_tx	O	SSI1 output data line	4mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[165]	IO	General Purpose I/O Port [165]				
S1RXD	E24	ssi1_rx	I	SSI1 input data line	4mA	I	0	pulldown resistor is internally connected, and pulldown is enabled by default
		gpio_d[166]	IO	General Purpose I/O Port [166]				
S1CLK	F25	ssi1_clk	O	SSI1 output clock signal	4mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[167]	IO	General Purpose I/O Port [167]				
S1SN	D26	ssi1_ssn	O	SSI1 slave select signal, active-LOW	4mA	O	1	Pullup resistor is internally connected, and pullup is disabled by default
		gpio_d[168]	IO	General Purpose I/O Port [168]				

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
GPIO3,GPIO4 Interface								
GPIO4	E26	gpio_d[4]	IO	General Purpose I/O Port [4]	8mA	I	0	pulldown resistor is internally connected, and pulldown is enabled by default
GPIO3	D27	gpio_d[3]	IO	General Purpose I/O Port [3]	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
COM_PCM0,I2S0,COM_I2C,PWR,KBS,GPIO20~GPIO21,GPIO239~GPIO240 Interface								
Power for the following pins are supplied by PVDD15								
PRSTNPin								
PRSTN	G3	prst_n	I	chip reset signal, active-LOW	4mA			NA
COM_PCM0 Interface								
CS0TXD	M2	com_pcm0_tx	O	COM_PCM0 data output line	4mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		isp_shutter_0	O	ISP output control signal to external image sensor0's mechanical shutter / ISP general control output				
		gpio_d[173]	IO	General Purpose I/O Port [173]				
		isp_debug_vsync	O	ISP debug interface video vertical signal				
CS0RXD	P1	com_pcm0_rx	I	COM_PCM0 data input line	4mA	I	0	pulldown resistor is internally connected, and pulldown is enabled by default
		isp_frex_0	O	ISP output frame exposure control signal to image sensor0				

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
		gpio_d[174]	IO	General Purpose I/O Port [174]				
		isp_debug_href	O	ISP debug interface video horizontal signal				
CS0CLK	N1	com_pcm0_clk	IO	COM_PCM0 clock signal	4mA	I	0	pulldown resistor is internally connected, and pulldown is enabled by default
		isp_gc0	IO	ISP General Purpose IO 0				
		gpio_d[175]	IO	General Purpose I/O Port [175]				
		isp_debug_pclk	O	ISP debug interface video clock				
CS0SN	N2	com_pcm0_ssn	IO	COM_PCM0 frame start signal	4mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[176]	IO	General Purpose I/O Port [176]				
		isp_debug_y[0]	O	ISP debug interface video data [0]				
I2S0 Interface								
IIS0DI	B1	i2s0_sdin	I	I2S0 data input line	8mA	I	0	pulldown resistor is internally connected, and pulldown is enabled by default
		gpio_d[181]	IO	General Purpose I/O Port [181]				
		isp_debug_y[1]	O	ISP debug interface video data [1]				
IIS0DO	D2	i2s0_sdout	O	I2S0 data output line	8mA	O	0	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[182]	IO	General Purpose I/O Port [182]				
		isp_debug_y[2]	O	ISP debug interface video data [2]				
IIS0CK	E2	i2s0_sclk	IO	I2S0 clock signal	8mA	I	0	pulldown resistor is internally connected, and pulldown is
		gpio_d[183]	IO	General Purpose I/O Port [183]				

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
		isp_debug_y[3]	O	ISP debug interface video data [3]				enabled by default
IIS0WS	E3	i2s0_ws	IO	I2S0 left and right channel select signal	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[184]	IO	General Purpose I/O Port [184]				
		isp_debug_y[4]	O	ISP debug interface video data [4]				
COM_I2C Interface								
CIICSCL	P2	com_i2c_scl	IO	COM_I2C clock signal	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[185]	IO	General Purpose I/O Port [185]				
		isp_debug_y[5]	O	ISP debug interface video data [5]				
CIICSDA	P3	com_i2c_sda	IO	COM_I2C data signal	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[186]	IO	General Purpose I/O Port [186]				
		isp_debug_y[6]	O	ISP debug interface video data [6]				
PWR Interface								
CLKO0	P5	clk_out[0]	O	DDR_PWR output signal clkout	8mA	O	0	NA
		gpio_d[213]	IO	General Purpose I/O Port [213]				
		isp_debug_y[7]	O	ISP debug interface video data [7]				
DVFS1	N5	pmu_dvfs1	O	Cortex-A7 dynamic voltage modulate signal [1] to PMU	8mA	O	0	NA
		gpio_d[214]	IO	General Purpose I/O Port [214]				

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
		isp_debug_y[8]	O	ISP debug interface video data [8]				
DVFS0	P4	pmu_dvfs0	O	Cortex-A7 dynamic voltage modulate signal [0] to PMU	8mA	O	1	NA
		gpio_d[215]	IO	General Purpose I/O Port [215]				
PWEN	B2	pwen	O	power control signal to PMU	8mA	O	0	NA
		gpio_d[209]	IO	General Purpose I/O Port [209]				
CLK32K	G5	clk32k_in	I	32KHz input clock for chip	4mA	I	Z	NA
CLK26MXIN,CLK26MOUT,CLK26SEL,ISPSD1,ISPSD0,GPIO239~GPIO240 Interface								
OSCIN	D1	clk26m_osc_in	I	26MHz crystal oscillator input signal	3mA	I	Z	NA
OSCOUT	E1	clk26m_osc_out	O	26MHz crystal oscillator output signal	3mA	O	Z	NA
CLK26SEL	F4	clk26m_sel	I	26MHz clock select signal	8mA	I	0	pulldown resistor is internally connected, and pulldown is enabled by default
ISPSD1	C2	isp_s_data[1]	I	ISP camera parallel interface data [1]	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[21]	IO	General Purpose I/O Port [21]				
		mmc0_card_det	I	SDMMC0 card detection signal, 0 indicates card inserted				
ISPSD0	F3	isp_s_data[0]	I	ISP camera parallel interface data [0]	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
		gpio_d[20]	IO	General Purpose I/O Port [20]				

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
		mmc0_card_wprt	I	SDMMC0 card write-protect signal, 1 indicates write-protect open				
GPIO239	E5	gpio_d[239]	IO	General Purpose I/O Port [239]	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
GPIO240	F2	gpio_d[240]	IO	General Purpose I/O Port [240]	8mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
RSTON and OSCEN3V Pin								
RSTON	G2	rstn	O	reset signal to PMU	8mA	I	Z	NA
		gpio_d[241]	IO	General Purpose I/O Port [241]				
OSCEN3V	G4	osc_en_3v	O	26MHz OSC enable signal of 3V	8mA	O	0	NA
		gpio_d[242]	IO	General Purpose I/O Port [242]				
SIM0 Interface								
Power for the following pins are supplied by PVDD8								
SIM0CLK	T27	sim0_clk	O	SIM0_CARD Clock	8mA	O	0	NA
		gpio_d[191]	IO	General Purpose IO Port [191]				
SIM0IO	T26	sim0_io	IO	SIM0_CARD data signal	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[192]	IO	General Purpose IO Port [192]				
SIM0RST	U25	sim0_rst	O	SIM0_CARD reset signal, active-LOW	8mA	O	0	NA
		gpio_d[193]	IO	General Purpose IO Port				

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
				[193]				
SIM1 Interface								
Power for the following pins are supplied by PVDD16								
SIM1CLK	H25	sim1_clk	O	SIM1_CARD Clock	8mA	O	0	NA
		gpio_d[194]	IO	General Purpose IO Port [194]				
SIM1IO	G26	sim1_io	IO	SIM1_CARD data signal	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[195]	IO	General Purpose IO Port [195]				
SIM1RST	G27	sim1_rst	O	SIM1_CARD reset signal, active-LOW	8mA	O	0	NA
		gpio_d[196]	IO	General Purpose IO Port [196]				
JTAG Interface,COM_UART, Function Mode Selection, Startup Mode Interface								
Power for the following pins are supplied by PVDD17								
Startup Mode Selection Pin								
BOOTCTL2	D21	boot_ctl[2]	I	chip boot mode control signal [2] to AP_PWR	4mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[226]	IO	General Purpose I/O Port [226]				
		isp_debug_y[9]	O	ISP debug interface video data [9]				
BOOTCTL1	B21	boot_ctl[1]	I	chip boot mode control signal [1] to AP_PWR	4mA	I	0	pulldown resistor is internally connected, and pulldown is enabled by default
		gpio_d[227]	IO	General Purpose I/O Port [227]				
		isp_debug_en	O	ISP dvp debug port enable signal				
BOOTCT	B22	boot_ctl[0]	I	chip boot mode control	4mA	I	0	pulldown resistor is

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
L0				signal [0] to AP_PWR				internally connected, and pulldown is enabled by default
		gpio_d[228]	IO	General Purpose I/O Port [228]				
Notes:BOOTCTL2,BOOTCTL1,BOOTCTL0 =000，NANDFLASH startup mode =100，eMMC startup mode =001，no startup mode, only wake up CP_ARM =101，T-card startup mode =010，USB1.1/COM_UART download mode, enter NANDFLASH startup mode when timeout =011，USB2.0/COM_UART download mode，enter NANDFLASH startup mode when timeout =110，USB1.0/COM_UART download mode，enter eMMC startup mode when timeout =111，USB2.0/COM_UART download mode，enter eMMC startup mode when timeout								
Function Mode Selection								
TMOD1	B20	tmode[1]	I	Function mode selection signal [1]	4mA	I	0	pulldown resistor is internally connected, pulldown is enabled by default and can not disabled
TMOD0	A20	tmode[0]	I	Function mode selection signal [0]	4mA	I	0	pulldown resistor is internally connected, pulldown is enabled by default and can not disabled
Note: Please refer to TEST & DEBUG module for details about function mode selection								
JTAG0 Interface								
TCK0	C22	jtag0_tck	I	JTAG0 clock signal	4mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
		test_pin[9]	O	Test Pin [9]				
		gpio_d[216]	IO	General Purpose I/O Port [216]				

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
TDI0	C23	jtag0_tdi	I	JTAG0 input signal	4mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
		test_pin[8]	O	Test Pin [8]				
		gpio_d[217]	IO	General Purpose I/O Port [217]				
TDO0	E21	jtag0_tdo	O	JTAG0 Output signal	8mA	I	Z	Pullup resistor is internally connected, and pullup is disabled by default
		test_pin[7]	O	Test Pin [7]				
		gpio_d[218]	IO	General Purpose I/O Port [218]				
TMS0	D22	jtag0_tms	I	JTAG0 mode selection signal	4mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
		test_pin[6]	O	Test Pin [6]				
		gpio_d[219]	IO	General Purpose I/O Port [219]				
NTRS0	D23	jtag0_ntrs	I	JTAG0 reset signal, active-LOW	4mA	I	Z	Pullup resistor is internally connected, and pullup is disabled by default
		test_pin[5]	O	Test Pin [5]				
		gpio_d[220]	IO	General Purpose I/O Port [220]				
JTAG1 Interface								
TCK1	T18	jtag1_tck	I	JTAG1 clock signal	4mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
		test_pin[4]	O	Test Pin [4]				
		gpio_d[221]	IO	General Purpose I/O Port [221]				
		sec_sw	I	secure key, control security mode				
TDI1	N18	jtag1_tdi	I	JTAG1 input signal	4mA	I	Z	pulldown resistor is internally connected, and pulldown is disabled by default
		test_pin[3]	O	Test Pin [3]				
		gpio_d[222]	IO	General Purpose I/O Port [222]				

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Ball Name	Ball Number	Signal Name	Property	Functional Description	Drive Capacity	Reset Direction	Reset state	Pullup/ Pulldown
		sec_smc	I	secure key, control MIC and Camera				
TDO1	P18	jtag1_tdo	O	JTAG1 Output signal	8mA	I	Z	Pullup resistor is internally connected, and pullup is disabled by default
		test_pin[2]	O	Test Pin [2]				
		gpio_d[223]	IO	General Purpose I/O Port [223]				
TMS1	R18	jtag1_tms	I	JTAG1 mode selection signal	4mA	I	Z	Pullup resistor is internally connected, and pullup is disabled by default
		test_pin[1]	O	Test Pin [1]				
		gpio_d[224]	IO	General Purpose I/O Port [224]				
		kbs_dki[1]	I	KBS direct key in [1]				
NTRS1	E20	jtag1_ntrs	I	JTAG1 reset signal, active-LOW	4mA	I	Z	Pullup resistor is internally connected, and pullup is disabled by default
		test_pin[0]	O	Test Pin [0]				
		gpio_d[225]	IO	General Purpose I/O Port [225]				
		kbs_dki[0]	I	KBS direct key in [0]				
COM_UART Interface								
U3TXD	A22	com_uart_tx	O	COM_UART output signal	8mA	O	1	Pullup resistor is internally connected, and pullup is disabled by default
		gpio_d[158]	IO	General Purpose I/O Port [158]				
U3RXD	B23	com_uart_rx	I	COM_UART input signal	8mA	I	1	Pullup resistor is internally connected, and pullup is enabled by default
		gpio_d[159]	IO	General Purpose I/O Port [159]				

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3 Chapter3 Address Map

The three processors of LC1813 (Cortex-A7, ARM926, ZSP540) and all DMAs (AP_DMAG, AP_DMAC, AUDIO_DMAS, AP_DMAS, CP_DMAC, CP_DMAS and CP_DMAD) can issue access to function modules. ZSP540 accesses function modules via 24-bit address, and others with 32-bit address.
This chapter describes the address assignment of function modules accessible by them.

3.1 General Address Mapping

Table 3-1 gives the chip's address mapping table. Cortex-A7 and ARM926 can access these modules via following address.

Table 3-1 Address Mapping Table

Module Name		Address Range	Size
DDR Memory		0x0000_0000 ~ 0x7FFF_FFFF	2GB
CP_SHRAM0		0x8100_0000 ~ 0x8102_FFFF	192KB
CP_SHRAM1		0x8103_0000 ~ 0x8103_3FFF	16KB
MAILBOX		0x8400_0000 ~ 0x8400_03FF	1KB
ZSP540_RAM		0x8408_0000 ~ 0x840B_FFFF	256KB
AEC_FFT		0x840C_0000 ~ 0x840C_0FFF	4KB
RFIF	TDIF	0x8410_0000 ~ 0x8410_1FFF	8KB
	GSMIF0	0x8410_2000 ~ 0x8410_2FFF	4KB
CP_DMAC		0x8410_4000 ~ 0x8410_47FF	2KB
CP_DMAS		0x8410_4800 ~ 0x8410_4FFF	2KB
CP_DMAD		0x8410_5000 ~ 0x8410_5FFF	4KB
CP_ICTL0		0x8410_6000 ~ 0x8410_63FF	1KB
CP_ICTL1		0x8410_6400 ~ 0x8410_67FF	1KB
SNOW3G		0x8410_7000 ~ 0x8410_7FFF	4KB
A5_0		0x8410_8000 ~ 0x8410_83FF	1KB
GEA		0x8410_8800 ~ 0x8410_8FFF	2KB

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Module Name		Address Range	Size
DTC3_0		0x8411_0000 ~ 0x8411_7FFF	32KB
CP_APB	SIM0	0x8412_0000 ~ 0x8412_03FF	1KB
	SIM1	0x8412_0400 ~ 0x8412_07FF	1KB
	CP_TIMER	0x8412_1000 ~ 0x8412_13FF	1KB
	CP_WDT	0x8412_1400 ~ 0x8412_17FF	1KB
	CP_PWR	0x8412_2000 ~ 0x8412_27FF	2KB
	CP_RTC	0x8412_3000 ~ 0x8412_33FF	1KB
THD		0x8420_0000 ~ 0x8437_FFFF	1536KB
THMU		0x8438_0000 ~ 0x843F_FFFF	512KB
DEBUG_APB		0x8000_0000 ~ 0x8003_FFFF	256KB
AP_SEC_RAM		0x9FF8_0000 ~ 0x9FF9_FFFF	128KB
AP_DMA	AP_DMAG	0xA000_0000 ~ 0xA000_1FFF	8KB
	AUDIO_DMAS	0xA000_2000 ~ 0xA000_2FFF	4KB
	AP_DMAS	0xA000_3000 ~ 0xA000_3FFF	4KB
	AP_DMAC	0xA000_4000 ~ 0xA000_4FFF	4KB
LCDC		0xA000_8000 ~ 0xA000_87FF	2KB
CTL		0xA006_0000 ~ 0xA006_1000	4KB
NFC		0xA006_1000 ~ 0xA006_13FF	1KB
CTL_APB	AP_WDT0	0xA010_8000 ~ 0xA010_83FF	1KB
	AP_WDT1	0xA010_8400 ~ 0xA010_87FF	1KB
	AP_WDT2	0xA010_8800 ~ 0xA010_8BFF	1KB
	AP_WDT3	0xA010_8C00 ~ 0xA010_8FFF	1KB
	AP_TIMERx	0xA010_9000 ~ 0xA010_93FF	1KB
	I2C1	0xA010_9800 ~ 0xA010_9BFF	1KB
	I2C0	0xA010_9C00 ~ 0xA010_9FFF	1KB
	I2C3	0xA010_A000 ~ 0xA010_A3FF	1KB
	PWM	0xA010_A400 ~ 0xA010_A7FF	1KB

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Module Name		Address Range	Size
	AP_PWR	0xA010_A800 ~ 0xA010_AFFF	2KB
	DSI	0xA011_0000 ~ 0xA011_FFFF	64KB
DATA_APB	I2S0	0xA014_0000 ~ 0xA014_03FF	1KB
	I2S1	0xA014_0800 ~ 0xA014_0BFF	1KB
	SSI0	0xA014_5000 ~ 0xA014_53FF	1KB
	SSI1	0xA014_6000 ~ 0xA014_63FF	1KB
	SSI3	0xA014_6800 ~ 0xA014_6BFF	1KB
	UART0	0xA014_7000 ~ 0xA014_73FF	1KB
	UART1	0xA014_8000 ~ 0xA014_83FF	1KB
	UART2	0xA014_9000 ~ 0xA014_93FF	1KB
ISP		0xA020_0000 ~ 0xA027_FFFF	512KB
USB_OTG		0xA030_0000~0xA033_FFFF	256KB
COM_APB	CTRL_DDR	0xA100_0000 ~ 0xA100_07FF	2KB
	COM_I2C	0xA100_1000 ~ 0xA100_13FF	1KB
	COM_PCM1	0xA100_2800 ~ 0xA100_2BFF	1KB
	MUX_PIN	0xA100_3000 ~ 0xA100_33FF	1KB
	PHY_DDR	0xA100_4000 ~ 0xA100_43FF	1KB
	DDR_PWR	0xA100_5000 ~ 0xA100_53FF	1KB
	COM_UART	0xA100_6000 ~ 0xA100_63FF	1KB
	GPIO0	0xA100_7000 ~ 0xA100_73FF	1KB
	GPIO1	0xA100_7800 ~ 0xA100_7BFF	1KB
	COM_RAM	0xA100_8000 ~ 0xA100_8FFF	4KB
VIDEO_ACC	DECODER	0xA200_0000 ~ 0xA200_03FF	1KB
	ENCODER0	0xA200_1000 ~ 0xA200_13FF	1KB
	ENCODER1	0xA200_1800 ~ 0xA200_1BFF	1KB
GPU		0xA201_0000 ~ 0xA201_FFFF	64KB
SEC_APB	I2C2	0xA300_0000 ~ 0xA300_03FF	1KB

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Module Name		Address Range	Size
	KBS	0xA300_1000 ~ 0xA300_13FF	1KB
	SSI2	0xA300_2000 ~ 0xA300_23FF	1KB
	BP147	0xA300_3000 ~ 0xA300_33FF	1KB
	SDIO0	0xA300_4000 ~ 0xA300_47FF	2KB
	SDIO1	0xA300_5000 ~ 0xA300_57FF	2KB
	SDIO2	0xA300_6000 ~ 0xA300_67FF	2KB
	TIMESTAMP	0xA300_7000~ 0xA300_7FFF	4KB
	TPZCTL	0xA300_8000 ~ 0xA300_83FF	1KB
	GTIMER	0xA300_9000~ 0xA300_9FFF	4KB
CIPHER		0xA400_0000 ~ 0xA400_1FFF	4KB
SECURITY		0xA400_2000 ~ 0xA400_23FF	1KB
DDR_AXI_GPV		0xA410_0000 ~ 0xA41F_FFFF	1MB
PERI_AXI_GPV		0xA420_0000 ~ 0xA42F_FFFF	1MB
A7_AXI_GPV		0xA430_0000 ~ 0xA43F_FFFF	1MB
A7_Private		0xA600_0000 ~ 0xA600_7FFF	32KB
ROM		0xFFFF_0000~ 0xFFFF_FFFF	64KB

3.2 Processors' Access Map

Table 3-2 shows which processors can access LC1813's modules respectively.

Table 3-2 Processors' Access Map

Module Name	ARM926	ZSP0	A7
DDR Memory	√	√	√
CP_SHRAM0		√	
CP_SHRAM1	√	√	
MAILBOX	√	√	
ZSP0_RAM	√	√	
AEC_FFT	√		

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Module Name		ARM926	ZSP0	A7
RFIF	TDIF	√	√	
	GSMIF0	√	√	
CP_DMAC		√	√	
CP_DMAS		√	√	
CP_DMAD		√	√	
CP_ICTL0		√		
CP_ICTL1			√	
SNOW3G		√		
A5_0			√	
GEA		√		
DTC3_0			√	
CP_APB	SIM0	√	√	
	SIM1	√	√	
	CP_TIMER	√	√	
	CP_WDT	√	√	
	CP_PWR	√	√	
	CP_RTC	√	√	
THD			√	
THMU			√	
DEBUG_APB				√
AP_SEC_RAM				√
AP_DMA	AP_DMAG			√
	AUDIO_DMAS			√
	AP_DMAS			√
	AP_DMAC			√
LCDC				√
CTL				√

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Module Name		ARM926	ZSP0	A7
NFC				√
CTL_APB	AP_WDTx			√
	AP_TIMERx			√
	I2C1			√
	I2C0			√
	I2C3			√
	PWM			√
	AP_PWR			√
	DSI			√
DATA_APB	I2S0			√
	I2S1			√
	SSI0			√
	SSI1			√
	SSI3			√
	UART0			√
	UART1			√
	UART2			√
ISP				√
USB_OTG				√
COM_APB	CTRL_DDR	√	√	√
	COM_I2C	√	√	√
	COM_PCM	√	√	√
	MUX_PIN	√	√	√
	PHY_DDR	√	√	√
	DDR_PWR	√	√	√
	COM_UART	√	√	√
	GPIO0	√	√	√

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Module Name		ARM926	ZSP0	A7
	GPIO1	√	√	√
	COM_RAM	√	√	√
VIDEO_ACC	DECODER			√
	ENCODER0			√
	ENCODER1			√
GPU				√
SEC_APB	I2C2			√
	KBS			√
	SSI2			√
	BP147			√
	SDMMC0			√
	SDMMC1			√
	SDMMC2			√
	TIMESTAMP			√
	TPZCTL			√
	GTIMER			√
CIPHER				√
SECURITY				√
DDR_AXI_GPV				√
PERI_AXI_GPV				√
A7_AXI_GPV				√
A7_Private				√
ROM				√

3.3 Address Mapping for ZSP540

The access of ZSP540 is divided into instruction and data, with 24 bits address bus, in 16-bit Word. This 24-bit address with high address configured produces the 32-bit address for ZSP540 to access other modules. (ARM926 use 32 bits bus addresses to

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access external space).This section describes the rules of this address generation.

Instruction spaces are divided into internal space and external space, the external space is remapped to DDR RAM, and its mapping address (in Bytes) is:

[i_base * 225 + 0x4_0000, i_base * 2^{25} + 0x200_0000]

In which, i_base is internal register of ZSP540, with valid range from 0 to 31.

Table 3-3 Instruction Address Mapping Table of ZSP540

Module Name	Address Range	Size
Internal Memory	0x00_0000 ~ 0x00_FFFF	64KW
Outer Memory	0x02_0000 ~ 0xFF_FFFF	

Also, data spaces are divided into internal space and external space, external space is divided into 7 pages, take 2M Word as unit. The addresses of each page can be mapped to different AMBA addresses. Below is a sample of address space:

Table 3-4 Data Address Mapping Table of ZSP540

Module Name	Address Range	Corresponding External Space	Cache Type
Inner RAM	0x00_0000 - 0x00_FFFF	NA	NA
Peripherals	0x20_0000 - 0x3F_FFFF	0x8400_0000 - 0x843F_FFFF	uncacheable
SHRAM0/1	0x40_0000 - 0x5F_FFFF	0x8100_0000~0x8103_3FFF	Cacheable(1)
Outer RAM	0x60_0000 - 0x7F_FFFF	DDR RAM	cacheable
Outer RAM	0x80_0000 - 0x9F_FFFF	DDR RAM	cacheable
Outer RAM	0xA0_0000 - 0xBF_FFFF	DDR RAM	cacheable
Outer RAM	0xC0_0000 - 0xDF_FFFF	DDR RAM	cacheable
Peripherals	0xE0_0000 - 0xFF_FFFF	COM_APB	cacheable

Note:

(1) the type of SHRAM is set to cacheable, in which can set an un-cacheable area for transmitting data with ARM926

ZSP540 has 3 master interfaces of ZSP540_D master interface, ZSP540_D_CACHE master interface and ZSP540_I master interface. The address space accessible by each master interface is different. And ZSP540 can access its own IMEM and DMEM internally. Please refer to *Figure 3-1*.

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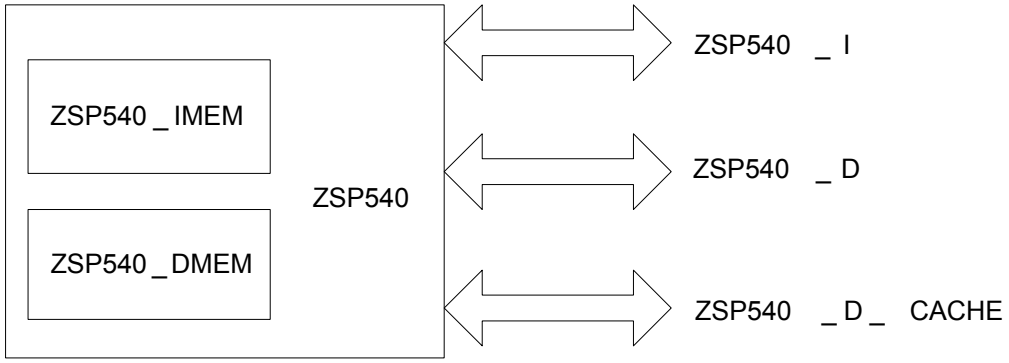

Figure 3-1 ZSP540 interface diagram

Address generation for ZSP_I master interface

Right shifts the 32-bit target address by 1 bit, and takes the lowest 24 bits as the 24-bit address issued by ZSP540.Addresses listed in Table 3-2 are the 24-bit addresses generated this way. Meanwhile, through register HIGH_ADDR, configure the high 7-bit address of 32-bit bus address for ZSP540_I master interface to access external memory.

For example, the 32-bit address to be accessed by ZSP540_I master interface is 0x18080000.

24-bit address is derived from: right shift 0x18080000 by 1 bit, taking the lowest 24 bits to obtain 0x40000, i.e. the 24-bit addressed by ZSP540.

High 7-bit address is derived from: select highest 7 bits of 0x18080000 as 0x0c.

Refer to ZSP540 ICACHE description for information about how ZSP540_I master interface accesses the external address space.

Address generation for ZSP540_D and ZSP540_D_CACHE master interface

ZSP540 accesses external data memory space through ZSP540_D and ZSP540_D_CACHE master interface. Ways to generate addresses are the same for the two interfaces.

Right shift the 32-bit address of ARM926 by 1 bit, and fetch the lowest 24 bits as the 24-bit address accessed by ZSP540. The high 3 bits of 24 bits decide the region mapped the peripheral address space that is accessed by ZSP540，and can be configured to the corresponding high 10 bits address in “DCACHE region control registerx(x= 0, 1, 2, 3)”. The high 10 bits is 10 bits of ARM926’s 32-bit.

For example, the 32-bit address to be accessed by ZSP540_I master interface is 0x8410_4000.

24-bit address is derived from: right shift 0x8410_4000 by 1 bit, fetching the lowest 24 bits to obtain 0x08_2000, i.e. the 24-bit addressed by ZSP540 (*Table 3-5* 24 bits address is derived like this.)

High 10-bit address is derived from: using 0x8410_4000 to fetch the highest 10 bits as 0x210.

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Judging which region the address is mapped: since high 3 bits of address 0x08_2000 is 0, the accessed address is mapped to 0, and user shall configure the 10bit to 0x210 in corresponding REGION0_HIGHADDR of “DCACHE region control register 0.

Additionally, setting the high 3 bits to be 1~7, 24 bits address will be 0x28_2000, 0x48_2000, 0x68_2000……0xE8_2000, the corresponding address will be mapped to region1, 2, 3 …… 7, and user shall configure the high 10 bits to 0x210 in REGION1_HIGHADDR, REGION2_HIGHADDR, REGION3_HIGHADDR … REGION7_HIGHADDR of “DCACHE region control registerx(x= 0, 1, 2, 3)”

Refer to ZSP540 ICACHE description for information about how ZSP540_I master interface accesses the external address space.

Table 3-5 lists the peripheral address space accessible by ZSP540.

Table 3-5 Peripheral Address Space Accessible by ZSP540

Module Name		Address Range	Size
MAILBOX		0x20_0000 ~ 0x20_01FF	512W
ZSP540_RAM		0x24_0000 ~ 0x25_FFFF	128KW
RFIF	TDIF	0x28_0000 ~ 0x28_0FFF	4KW
	GSMIF0	0x28_1000 ~ 0x28_17FF	2KW
CP_DMAC		0x28_2000 ~ 0x28_23FF	1KW
CP_DMAS		0x28_2400 ~ 0x28_27FF	1KW
CP_DMAD		0x28_2800 ~ 0x28_2FFF	2KW
CP_ICTL1		0x28_3200 ~ 0x28_33FF	512W
SNOW3G		0x28_3800 ~ 0x28_3FFF	2KW
A5_0		0x28_4000 ~ 0x28_41FF	512W
DTC3_0		0x28_8000 ~ 0x28_BFFF	16KW
CP_APB	SIM0	0x29_0000 ~ 0x29_01FF	512W
	SIM1	0x29_0200 ~ 0x29_03FF	512W
	CP_TIMER	0x29_0800 ~ 0x29_09FF	512W
	CP_WDT	0x29_0A00 ~ 0x29_0BFF	512W
	CP_PWR	0x29_1000 ~ 0x29_13FF	1KW
	RTC	0x29_1800 ~ 0x29_19FF	512W
THD		0x30_0000 ~ 0x3B_FFFF	768KW

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Module Name		Address Range	Size
THMU		0x3C_0000 ~ 0x3F_FFFF	256KW
COM_APB	CTRL_DDR	0x80_0000 ~ 0x80_03FF	1KW
	COM_I2C	0x80_0800 ~ 0x80_09FF	512W
	COM_PCM	0x80_1400 ~ 0x80_15FF	512W
	MUX_PIN	0x80_1800 ~ 0x80_19FF	512W
	PHY_DDR	0x80_2000 ~ 0x80_21FF	512W
	DDR_PWR	0x80_2800 ~ 0x80_29FF	512W
	COM_UART	0x80_3000 ~ 0x80_31FF	512W
	GPIO0	0x80_3800 ~ 0x80_39FF	512W
	GPIO1	0x80_3C00 ~ 0x80_3DFF	512W
	COM_RAM	0x80_4000~0x80_47FF	2KW

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4 Chapter4 Interrupt System

4.1 ARM926 Interrupt Allocation

ARM926 processor's interrupt requests include fast interrupt request (fiq) and normal interrupt request (irq), both from the ARM926's interrupt controller (CP_ICTL0). All of ARM926 Interrupt sources are first connected to interrupt controller (CP_ICTL0), and after its handling and merger, sent to ARM926 processor. *Table 4-1* is ARM926 interrupt allocation.

Table 4-1 ARM926 interrupt allocation

Interrupt Source	Interrupt Allocation	IRQ Interrupt Priority
FIQ		
MAILBOX		
IRQ		
MAILBOX	0	2
CP_DMAC	1	2
CP_DMAS	2	2
CP_DMAD	3	2
GEA	4	2
SIM0	5	2
SIM1	6	2
RESERVED	7	2
CP_TIMER0	8	2
CP_TIMER1	9	2
CP_TIMER2	10	2
CP_TIMER3	11	2
CP_WDT	12	2
COM_UART	13	2
GPIO0	14	2

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Interrupt Source	Interrupt Allocation	IRQ Interrupt Priority
COM_I2C	15	2
CP_PWR	16	2
DDR	17	2
SNOW3G	18	2
TDIF	19	2
GSMIF0	20	2
AEC_FFT	21	2
RTC	22	2
COM_PCM1	23	2
DDR_PWR	24	2
GPIO1	25	2
CTI	26	2

4.2 ZSP540 Interrupt Allocation

14 maskable interrupt requests (irq) can be connected to ZSP540 processor's interrupt processing unit (ICU). In the ZSP540 of LC1813, non-maskable interrupt is not used, but maskable interrupts 0-8 are used. The unused interrupts(9-13) should be masked. *Table 4-2* is ZSP540 interrupt allocation.

Table 4-2 ZSP540 Interrupt Distribution

Interrupt Source	Interrupt Number	Description
unused	ZSP540 ICU unmaskable interrupt	Non-maskable interrupt
MAILBOX interrupt request	ZSP ICU Maskable Interrupt Source 0	Programmable
TDIF interrupt request	ZSP ICU Maskable Interrupt Source 1	Programmable
GSMIF0 interrupt request	ZSP ICU Maskable Interrupt Source 2	Programmable
CP_ICTL1 interrupt request	ZSP ICU Maskable Interrupt Source 3	Programmable
CP_DMAD interrupt request	ZSP ICU Maskable Interrupt Source 4	Programmable
Reserved	ZSP ICU Maskable Interrupt Source 5	Programmable
Reserved	ZSP ICU Maskable Interrupt Source 6	Programmable

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Interrupt Source	Interrupt Number	Description
THD interrupt request	ZSP ICU Maskable Interrupt Source 7	Programmable
THMU interrupt request	ZSP ICU Maskable Interrupt Source 8	Programmable
Reserved	ZSP ICU Maskable Interrupt Source 9	Programmable
Software reserved	ZSP ICU Maskable Interrupt Source 10	Programmable
Software reserved	ZSP ICU Maskable Interrupt Source 11	Programmable
Software reserved	ZSP ICU Maskable Interrupt Source 12	Programmable
Software reserved	ZSP ICU Maskable Interrupt Source 13	Programmable

As the number of maskable interrupts is limited, LC1813 uses ZSP540 interrupt controller (CP_ICTL1) to control partial ZSP540 interrupt sources. The controller can generate regular interrupt request (IRQ) and send it to ZSP540 Maskable Interrupt Source 3.CP_ICTL1 has a total of 13 Interrupt Sources. See *Table 4-3* CP_ICTL1 interrupt source allocation.

Table 4-3 CP_ICTL1 Interrupt Distribution

CP_ICTL1 Interrupt Allocation	Name	Interrupt Priority	Description
IRQ0	cp_timer2_intr	2	CP_TIMER2 interrupt request
IRQ1	cp_timer3_intr	2	CP_TIMER3 interrupt request
IRQ2	com_gpio0_intr	2	GPIO0 interrupt request
IRQ3	com_pcm1_intr	2	COM_PCM1 interrupt request
IRQ4	com_uart_intr	2	COM_UART interrupt request
IRQ5	cp_pwr_intr	2	CP_PWR interrupt request
IRQ6	cp_A5_0_intr	2	A5_0 interrupt request
IRQ7	zsp0_bus_error_intr	2	ZPS540 BUS ERROR interrupt request
IRQ8	cp_dmac_intr	2	CP_DMAC interrupt request
IRQ9	cp_dmas_intr	2	CP_DMAS interrupt request
IRQ10	dtc3_0_intr	2	DTC3_0 interrupt request
IRQ11	---	2	Reserved
IRQ12	gpio1_intr	2	GPIO1 interrupt request

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4.3 Cortex-A7 Interrupt Allocation

Cortex-A7 adopts embedded Generic Interrupt Controller (GIC) for interrupt management, the GIC meets ARM Generic Interrupt Controller Architecture (V2.0), and its features are shown as follows:

5. Three interrupt typies:SPI, PPI, and SGI
6. The priority of the each interrupt source is programmble; supports 5 bits (0~31) priority in security state and 4 bits (0-15) priority in non-security.
7. Interrupt is maskable. Only when the priority from Distributor is higher than the priority configured by ICCPMR registe, CPU will send the interrupt signal to corresponding processor.
8. Support uni-core/multi-core processors system simultaneously, and any processor has a corresponding interface.
9. Trace interrupt status
10. Support TrusZone security extending. Each interrupt can be configured as security interrupt or non-sucurity interrupt. Security interrupt can generate IRQ or FIQ, and non-security interrupt only can generate IRQ

Cortex-A7 supports 64 SPI interrupt sources, and each interrupt has an interrupt ID number as its unique indication, when an interrupt is generated, software can determine which interrupt occurred by reading interrupt ID number.Cortex-A7's sources are shown below:

Table 4-4 Cortex-A7 interrupt allocation

Interrupt Source	Interrupt Number Allocation	ID Number
CTL|USB_OTG	0	32
AP_DMAG	1	33
AUDIO_DMAS	2	34
AP_DMAS	3	35
SECURITY	4	36
KBS	5	37
AP_TIMER4	6	38
AP_WDT0	7	39
AP_WDT3	8	40
AP_TIMER0	9	41

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Interrupt Source	Interrupt Number Allocation	ID Number
I2C0	10	42
I2C1	11	43
I2C2	12	44
I2C3	13	45
COM_I2C	14	46
AP_PWR	15	47
GPIO0	16	48
DSI	17	49
A7_PMU0	18	50
GPU_GP	19	51
GPU_PP0	20	52
GPU_PP1	21	53
GPU_GPMMU	22	54
GPU_PPMMU0	23	55
GPU_PPMMU1	24	56
GPU_PMU	25	57
A7_CTI0 | I2S0	26	58
A7_CTI1 | I2S1	27	59
SDMMC0	28	60
SDMMC1	29	61
SDMMC2	30	62
SSI0	31	63
SSI1	32	64
SSI2	33	65
A7_PMU1	34	66
UART0	35	67
UART1	36	68

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Interrupt Source	Interrupt Number Allocation	ID Number
UART2	37	69
AP_TIMER5	38	70
COM_UART	39	71
A7_PMU2	40	72
VIDEO_ACC_DECODER	41	73
VIDEO_ACC_ENCODER0	42	74
VIDEO_ACC_ENCODER1	43	75
USB_OTG	44	76
A7_CTI2|AP_DMAC	45	77
A7_CTI3	46	78
LCDC0	47	79
A7_PMU3	48	80
NFC	49	81
ISP	50	82
CIPHER	51	83
A7_TIMER6	52	84
TPZCTL	53	85
SSI3	54	86
AP_TIMER1	55	87
AP_TIMER2	56	88
AP_TIMER3	57	89
COM_PCM	58	90
DDR_PWR	59	91
GPIO1	60	92
AP_WDT2	61	93
AP_WDT3	62	94
nAXIERRIRQ	63	95

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5 Chapter5 Electrical Characteristics

This chapter includes LC1813's electrical absolute maximum ratings and recommended value.

If not specified otherwise, all the relevant AC/DC parameters mentioned in other locations of this article are default values.

5.1 Absolute Maximum Ratings

Prolonged exposure to those listed as absolute maximum ratings may cause permanent damage to the device. Functional operation at these maximum ratings is not implied.

Table 5-1 Absolute Maximum Ratings

Parameter	Min	Max	UNIT
Supply voltage for cores except Cortex-A7 VDDMAIN	-0.5	1.4	V
Supply voltage for Cortex-A7 VDDA7	-0.5	1.5	V
Supply voltage for IO (1) PVDD2, PVDD5, PVDD6, PVDD7, PVDD8, PVDD9, PVDD10, PVDD11, PVDD12, PVDD13, PVDD14, PVDD15, PVDD16, PVDD17	-0.5	2.1 4.0	V
PLLx(x=0-4) Digital supply voltage PLLDVDD	-0.5	1.5	V
PLLx(x=0-4) Analog supply voltage PLLAVDD	-0.5	2.75	V
Supply voltage for LPDDR2 PVDD1	-0.4	2.1	V
Supply voltage for IO VDDQ	-0.5	1.5	V
Supply voltage for Vref of LPDDR2	-0.4	1.5	

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Parameter	Min	Max	UNIT
VREF			
Supply voltage for IO EFUSEVDD, CPHYVDD, DPHYVDD	-0.5	2.75	V
Supply voltage from USB USBAVDD	-0.5	4.0	V
Work temperature	-20	+60	℃
Notes: (1) Parts of LC1813 module's IO voltage support 1.8V/3V dual-voltage. PVDD is the IO pin's power supply voltage.			

5.2 Recommended Operating Conditions

Table 5-2 Recommended Operating Conditions

Parameter	Min	Nom	Max	UNIT
Supply voltage for cores except Cortex-A7 VDDMAIN	0.99	1.1	1.21	V
Supply voltage for Cortex-A7 VDDA7	0.99	1.1	1.21	V
Supply voltage for IO (1) PVDD2, PVDD5, PVDD6, PVDD7, PVDD8, PVDD9, PVDD10, PVDD11, PVDD12, PVDD13, PVDD14, PVDD15, PVDD16,PVDD17	1.62 3.0	1.8 3.3	1.98 3.6	V
PLLx(x=0-4) Digital supply voltage PLLDVDD	0.99	1.1	1.21	V
PLLx(x=0-4) Analog supply voltage PLLAVDD	2.25	2.5	2.75	V
Supply voltage for LPDDR2 PVDD1	1.62	1.8	1.98	V

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Parameter	Min	Nom	Max	UNIT
Supply voltage for IO VDDQ	1.08	1.2	1.32	V
Supply voltage for Vref VREF	0.5*VDDQ	0.5*VDDQ	0.5*VDDQ	
Supply voltage for IO EFUS_VDD, CPHYVDD, DPHYVDD	2.25	2.5	2.75	V
Supply voltage from USB USBAVDD	3.0	3.3	3.6	V
VIL	0		0.2PVDD(2)	V
VIH	0.8PVDD(2)		PVDD(2)	V
Work temperature	-20		+60	℃
Notes: (1) Parts of LC1813 module's IO voltage support 1.8V/3V dual-voltage. (2) PVDD is the IO pin's power supply voltage.				

5.3 I/O Pins AC/DC Characteristics

This section shows I/O pins AC/DC characteristics for MEMCTL, SDMMC0 and other I/O pins separately.

5.3.1 I/O Pins AC/DC Characteristics for MEMCTL

Table 5-3 AC/DC characteristics for MEMCTL

Symbol	Parameters	Min	Nom	Max	UNIT
MEMCTL, AC/DC Operating Conditions(LPDDR2 VDDcore = 1.1V VDDIO = 1.2V Temperature = 25℃)					
VDD	Core supply voltage	0.99	1.10	1.21	V
VDDQ	HSUL output supply voltage	1.14	1.20	1.30	V
VREF	HSUL reference supply voltage	0.49*VDDQ	0.5*VDDQ	0.51*VDDQ	V
VIH(DC)	DC input voltage High	VREF+0.13		VDDQ	V

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Symbol	Parameters	Min	Nom	Max	UNIT
VIL(DC)	DC input voltage Low	VSSQ-0.3		VREF-0.13	V
VIH(AC)	Input logic threshold High	VREF+220mV			mV
VIL(AC)	Input logic threshold Low			VREF-220mV	mV
VOH	DC output logic High	0.9*VDDQ			V
VOL	DC output logic Low			0.1*VDDQ	V
IDDQ	VDDQ standby current		0.02	12.31	uA
IDD	VDD quiescent current		0.02	4.21	uA
IDDQ	Output Low IDDQ DC current		0.30	0.79	mA
IDDQ	Output High IDDQ DC current		0.28	0.76	mA
IDDQ	Input Low IDDQ DC current		0.30	0.79	mA
IDDQ	Input High IDDQ DC current		0.28	0.76	mA
ILL	Input leakage current		0.01	4.51	uA

5.3.2 I/O Pins AC/DC Characteristics for SDMMC0

The following list shows I/O pins AC/DC characteristics for SDMMC0.

Table 5-4 AC/DC characteristics for SDMMC0

Symbol	Parameters	Min	Nom	Max	UNIT
SDMMC, AC/DC Operating Conditions(VDDcore = 1.1V VDD_{IO} = 1.8V Temperature = 25℃)					
V_{IL}	Input Low Voltage	-0.3		0.63	V
V_{IH}	Input High Voltage	1.17		3.6	V
V_T	Threshold Point	0.79	0.88	0.98	V
V_{T+}	Schmitt Trigger Low to High Threshold Point	-	-	-	V
V_{T-}	Schmitt Trigger Low to Low Threshold Point	-	-	-	V
V_{TPU}	Threshold Point with Pull-up Resistor Enabled	-	-	-	V
V_{TPD}	Threshold Point with Pull-down Resistor Enabled	-	-	-	V
$V_T^+{}_{PU}$	Schmitt Trigger Low to High Threshold Point with Pull-up Resistor Enabled	-	-	-	V

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Symbol	Parameters	Min	Nom	Max	UNIT
V_{T^-PU}	Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled	-	-	-	V
V_{T^+PD}	Schmitt Trigger Low to High Threshold Point with Pull-down Resistor Enabled	-	-	-	V
V_{T^-PD}	Schmitt Trigger High to Low Threshold Point with Pull-down Resistor Enabled	-	-	-	V
I_I	Input Leakage Current @ VI=1.8V or 0V			±10μ	A
I_{OZ}	Tri-state Output Leakage Current @ VO=1.8V or 0V			±10μ	A
R_{PU}	Pull-up Resistor	43K	55K	67K	Ω
R_{PD}	Pull-down Resistor	43K	54K	66K	Ω
V_{OL}	Output Low Voltage			0.45	V
V_{OH}	Output High Voltage	1.35			V
I_{OL}	Low Level Output Current @VOL(max) 12mA: 16mA:	 11.3 27.2	 20.4 49.1	 32.8 78.7	mA
I_{OH}	High Level Output Current @VOH(min) 12mA: 16mA:	 7.4 15.4	 17.6 36.6	 34.2 71.3	mA
SDMMC, AC/DC Operating Conditions(VDDcore = 1.1V VDDIO = 3.3V Temperature = 25℃)					
V_{IL}	Input Low Voltage	-0.3		0.8	V
V_{IH}	Input High Voltage	2		3.6	V
V_T	Threshold Point	1.46	1.61	1.79	V
V_{T+}	Schmitt Trigger Low to High Threshold Point	-	-	-	V
V_{T-}	Schmitt Trigger Low to Low Threshold Point	-	-	-	V
V_{TPU}	Threshold Point with Pull-up Resistor Enabled	-	-	-	V
V_{TPD}	Threshold Point with Pull-down Resistor Enabled	-	-	-	V
V_{T^+PU}	Schmitt Trigger Low to High Threshold Point with Pull-up Resistor Enabled	-	-	-	V

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Symbol	Parameters	Min	Nom	Max	UNIT
V_{T^-PU}	Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled	-	-	-	V
V_{T^+PD}	Schmitt Trigger Low to High Threshold Point with Pull-down Resistor Enabled	-	-	-	V
V_{T^-PD}	Schmitt Trigger High to Low Threshold Point with Pull-down Resistor Enabled	-	-	-	V
I_I	Input Leakage Current @ VI=3.3V or 0V			±10μ	A
I_{OZ}	Tri-state Output Leakage Current @ VO=3.3V or 0V			±10μ	A
R_{PU}	Pull-up Resistor	43K	55K	66K	Ω
R_{PD}	Pull-down Resistor	43K	54K	66K	Ω
V_{OL}	Output Low Voltage			0.4	V
V_{OH}	Output High Voltage	2.4			V
I_{OL}	Low Level Output Current @VOL(max) 12mA: 16mA:	 21.3 51.2	 33.0 79.2	 44.7 107.2	mA
I_{OH}	High Level Output Current @VOH(min) 12mA: 16mA:	 29.2 60.8	 57.7 120.2	 97.4 203.0	mA

5.3.3 I/O Pins AC/DC Characteristics for Other Pins

This section describes I/O pins AC/DC characteristics for other I/O pins except MEMCTL and SDMMC0.

Table 5-5 AC/DC Characteristics for other I/O pins

Symbol	Parameters	Min	Nom	Max	UNIT
Other I/O Pins, AC/DC Operating Conditions(VDDcore = 1.1V VDDIO = 1.8V Temperature = 25℃)					
V_{IL}	Input Low Voltage	-0.3		0.63	V
V_{IH}	Input High Voltage	1.17		3.6	V
V_T	Threshold Point	0.77	0.84	0.92	V

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Symbol	Parameters	Min	Nom	Max	UNIT
V_{T+}	Schmitt Trigger Low to High Threshold Point	0.99	1.1	1.19	V
V_{T-}	Schmitt Trigger Low to Low Threshold Point	0.62	0.73	0.82	V
V_{TPU}	Threshold Point with Pull-up Resistor Enabled	0.77	0.84	0.91	V
V_{TPD}	Threshold Point with Pull-down Resistor Enabled	0.77	0.85	0.92	V
$V_T^+{}_{PU}$	Schmitt Trigger Low to High Threshold Point with Pull-up Resistor Enabled	0.99	1.1	1.19	V
$V_T^-{}_{PU}$	Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled	0.62	0.73	0.81	V
$V_T^+{}_{PD}$	Schmitt Trigger Low to High Threshold Point with Pull-down Resistor Enabled	0.99	1.1	1.2	V
$V_T^-{}_{PD}$	Schmitt Trigger High to Low Threshold Point with Pull-down Resistor Enabled	0.62	0.73	0.82	V
I_I	Input Leakage Current @ VI=1.8V or 0V			±10μ	A
I_{OZ}	Tri-state Output Leakage Current @ VO=1.8V or 0V			±10μ	A
R_{PU}	Pull-up Resistor	79K	128K	218K	Ω
R_{PD}	Pull-down Resistor	73K	127K	232K	Ω
V_{OL}	Output Low Voltage			0.45	V
V_{OH}	Output High Voltage	1.35			V
I_{OL}	Low Level Output Current @VOL(max) 12mA: 16mA:	 9.2 11.5	 16.6 20.8	 26.8 33.5	mA
I_{OH}	High Level Output Current @VOH(min) 12mA: 16mA:	 6.3 8.4	 15.0 19.9	 29.1 38.8	mA
Other I/O Pins, AC/DC Operating Conditions(VDDcore = 1.1V VDDIO = 2.5V Temperature = 25℃)					
V_{IL}	Input Low Voltage	-0.3		0.7	V
V_{IH}	Input High Voltage	1.7		3.6	V

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Symbol	Parameters	Min	Nom	Max	UNIT
V_T	Threshold Point	1.03	1.13	1.23	V
V_{T+}	Schmitt Trigger Low to High Threshold Point	1.32	1.45	1.56	V
V_{T-}	Schmitt Trigger Low to Low Threshold Point	0.92	1.01	1.12	V
V_{TPU}	Threshold Point with Pull-up Resistor Enabled	1.03	1.13	1.23	V
V_{TPD}	Threshold Point with Pull-down Resistor Enabled	1.05	1.14	1.23	V
$V_T^+{}_{PU}$	Schmitt Trigger Low to High Threshold Point with Pull-up Resistor Enabled	1.32	1.45	1.55	V
$V_T^-{}_{PU}$	Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled	0.91	1	1.12	V
$V_T^+{}_{PD}$	Schmitt Trigger Low to High Threshold Point with Pull-down Resistor Enabled	1.33	1.46	1.56	V
$V_T^-{}_{PD}$	Schmitt Trigger High to Low Threshold Point with Pull-down Resistor Enabled	0.92	1.01	1.13	V
I_I	Input Leakage Current @ VI=1.8V or 0V			±10μ	A
I_{OZ}	Tri-state Output Leakage Current @ VO=1.8V or 0V			±10μ	A
R_{PU}	Pull-up Resistor	53K	81K	131K	Ω
R_{PD}	Pull-down Resistor	51K	82K	143K	Ω
V_{OL}	Output Low Voltage			0.7	V
V_{OH}	Output High Voltage	1.7			V
I_{OL}	Low Level Output Current @VOL(max) 12mA: 16mA:	 20.1 25.1	 33.8 42.2	 49.8 62.2	mA
I_{OH}	High Level Output Current @VOH(min) 12mA: 16mA:	 17.1 22.8	 34.2 45.7	 59.7 79.6	mA
Other I/O Pins, AC/DC Operating Conditions(VDDcore = 1.1V VDDIO = 3.3V Temperature = 25℃)					
V_{IL}	Input Low Voltage	-0.3		0.8	V

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Symbol	Parameters	Min	Nom	Max	UNIT
V_{IH}	Input High Voltage	2		3.6	V
V_T	Threshold Point	1.34	1.46	1.6	V
V_{T+}	Schmitt Trigger Low to High Threshold Point	1.69	1.83	1.96	V
V_{T-}	Schmitt Trigger Low to Low Threshold Point	1.21	1.32	1.46	V
V_{TPU}	Threshold Point with Pull-up Resistor Enabled	1.33	1.44	1.59	V
V_{TPD}	Threshold Point with Pull-down Resistor Enabled	1.36	1.47	1.6	V
$V_T^+{}_{PU}$	Schmitt Trigger Low to High Threshold Point with Pull-up Resistor Enabled	1.69	1.82	1.94	V
$V_T^-{}_{PU}$	Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled	1.2	1.31	1.45	V
$V_T^+{}_{PD}$	Schmitt Trigger Low to High Threshold Point with Pull-down Resistor Enabled	1.71	1.84	1.97	V
$V_T^-{}_{PD}$	Schmitt Trigger High to Low Threshold Point with Pull-down Resistor Enabled	1.23	1.33	1.46	V
I_I	Input Leakage Current @ VI=3.3V or 0V			±10μ	A
I_{OZ}	Tri-state Output Leakage Current @ VO=3.3V or 0V			±10μ	A
R_{PU}	Pull-up Resistor	41K	60K	91K	Ω
R_{PD}	Pull-down Resistor	43K	63K	103K	Ω
V_{OL}	Output Low Voltage			0.4	V
V_{OH}	Output High Voltage	2.4			V
I_{OL}	Low Level Output Current @VOL(max) 12mA: 16mA:	 17.5 21.9	 27.0 33.8	 36.5 45.7	mA
I_{OH}	High Level Output Current @VOH(min) 12mA: 16mA:	 24.8 33.1	 49.1 65.4	 82.9 110.5	mA

5.4 Clock Characteristics

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This section introduces the characteristics of the clock input signals of LC1813 chip. LC1813 has one 32K clock input signal and three 26MHz clock input signals.

5.4.1 32KHz Clock

The 32.768KHz clock signal of LC1813 is input by external clock input via CLK32K pin, and this pin is powered by PVDD15.

5.4.2 26MHz Clock

LC1813 has three 26MHz clock input signals. A 26MHz clock signal is input from CLK26DI0, the second 26MHz clock signal is input from CLK26DI1，and the last 26MHz clock is input from CLK62MXIN. The detail function of the three clocks is decided by application environment. Refer to AP_PWR module for application description.

5.5 Power-on Timing

This section provides charts of power-on timing, hardware reset timing and significant signals timing when LC1813 is powered on.

Figure 5-1 shows the diagram of power-on reset timing, *Table 5-6* lists the relevant parameters.

Table 5-6 LC1813 Power-on Reset Timing Parameter Table

NO.	Symbol	Description	MIN	MAX	UNIT
RS1	t_w(prst_n)	Pulse duration.prst_n low	N		ns
RS2	t_d(prst_nH-osc_enH)	Delay time.prst_n high to osc_en high		6P	ns
RS3	t_W(26MHz oscillator start-up time)	Pulse duration, 26MHz oscillator start-up time		5	ms
Notes: 1:P=period of 32KHz clock 2:N=32KHz oscillator start-up after stable power					

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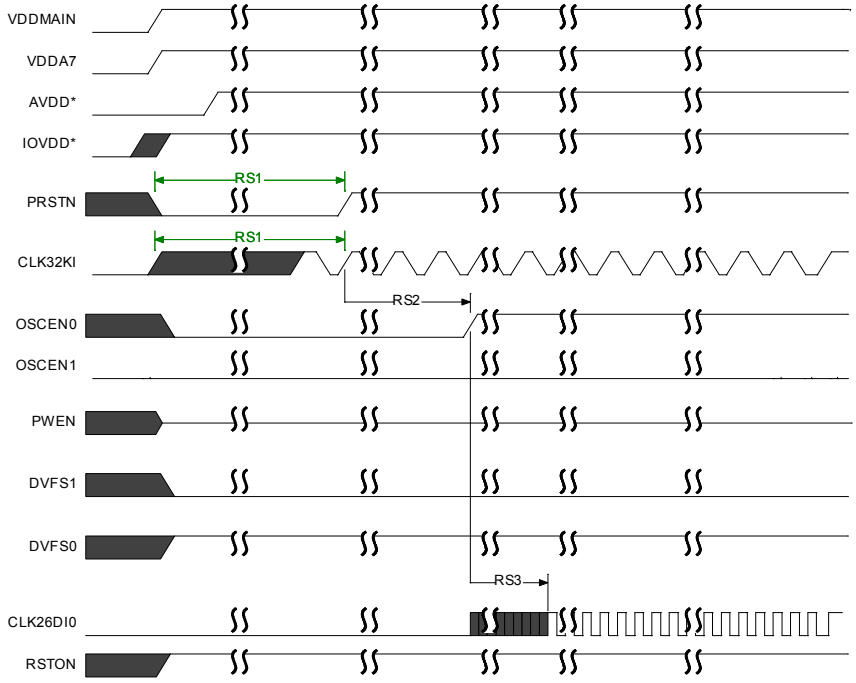

Figure 5-1 LC1813 Power-on Reset Timing Diagram

Notes:

VDDMAIN: Core (except Cortex-A7) power

VDDA7: Core power for Cortex-A7

AVDD *: Represents power DPHYAVDD, CPHYAVDD, PLLAVDD, PLLDVDD, and USBAVDD

IOVDD *: Represents power PVDD2, PVDD5-17, VDD1-2, VDDQ, and VDDCA

PRSTN: off-chip input signal, used as the full-chip power-on reset signal on the chip

RSTON: chip's output signal, asynchronous reset signal RSTON (LOW) generated in AP_PWR, and it is sent out of the chip for the use of other devices that need to be reset simultaneously with the chip.

OSCEN0: chip's output signal, external 26M oscillator (OSC26M0) enable signal

OSCEN1: external OSC26M1's enable signal controlled by CP_PWR. Power-on by default, this signal remains low level.

PWEN: power enable control signal, which is transmitted to power management chip

DVFS0, DVFS1: used for dynamic voltage scaling of Cortex-A7, which are transmitted to power management chip.
LC1813 chip's power supply is divided into 1.1V core power, 1.8/3V IO power, 2.5V power and 3.3V power.

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Core power supply:

- Digital core power (VDDMAIN) is basic core power supplies of the chip, which cannot be turned off after the chip is powered on.
- Digital core power (VDDA7) supplies power for Cortex-A7 based on specific value of DVFS0 and DVFS1; Combined with DVFS0/1 and chip sleep-wake flow, dynamic voltage scaling of Cortex-A7 can be performed.
- Analog core power(DSI DPHY, ISP CPHY, PLL, USB OTG PHY), cannot be turned off after the chip is powered-on, except ISP_CPHY's core power.

IO power supply:

- PVDD2, interface power supply of TDIF RX0 and GSM0
- PVDD5, interface power supply of PWM, SSI0, SSI2, and KBDK17
- PVDD6, interface power supply of CAMER RGB
- PVDD7, interface power supply of COM_PCM1, UART2, I2C0, GPIO232-GPIO234, GPIO6-11, GPIO24, and CLKO1
- PVDD8, interface power supply of SIM0
- PVDD9, interface power supply of UART1, CLKO2, GPIO0-GPIO2, SECSMC , SECSW , GPIO5, CLKO3, I2C1
- PVDD10, interface power supply of NADNFLASH, SDMMC1
- PVDD11, interface power supply of SDMMC0
- PVDD12, interface power supply of SDMMC2
- PVDD13, interface power supply of UART0
- PVDD14, interface power supply of SSI1, GPIO3, GPIO4
- PVDD15, interface power supply of COM_PCM0, I2S0, COM_I2C, PWR, KBS, CLK26SEL, CLK26MOUT, CLK26MXIN, ISPSD1, ISPSD0, and GPIO239-GPIO240
- PVDD16, interface power supply of SIM1
- PVDD17, interface power supply of JTAG interface, COM_UART function mode selection and boot mode selection
- VDDQ: interface power supply of LPDDR2/LPDDR3

PHY, PLL power supply:

- DPHYAVDD: 2.5V analog power supply of MIPI TX PHY
- CPHYAVDD: 2.5V analog power supply of MIPI RX PHY
- PLLAVDD: 2.5V analog power supply of PLL

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- PLLDVDD: 1.1V digital power supply of PLL
- USBAVDD: 3.3V power supply of USB OTG 3.3V

There's no requirement for the power-on order of core power and IO power, but supply of core power must be prior to PHY and PLL.

The effective time of LC1813 chip's power-on asynchronous reset signal PRSTN is decided by 32K clock stable time. To ensure the chip to be in the correct initial state, the PRSTN signal is not de-asserted until 32K clock gets stable. 32K stable time is relative about the load capacitance C_L.

LC1813 chip output signal OSCEN0 is 26M clock control signal to control 26MHz VCXO or CMOS level digital clock's output enable. OSCEN0 signal is LOW in reset state. LOW or HIGH configured by registers in deep-sleep state, and HIGH under the working state (OSCEN0 signal's voltage scope is decided by IO power PVDD2).

OSCEN1 is output from CP module of LC1813. It's high when CP is in working state, and low while CP is in sleep state. OSCEN1 is low by default when chip powers on.

LC1813 outputs asynchronous reset signal RSTON (low active). The signal is in reset state during the whole chip being powed on. RSTON is low in reset state, and keeps low during peripheral 26MHz and inner PLL oscillating. RSTON will becme high a 32k cycle ealier than PLL start oscillating.

As long as the chip power supply, asynchronous reset signal and clock signal meet the above criteria, the chip is turned on to enter the working state; if it is necessary to be shut-down, software needs to have all the switches of the chip off under working state. It is generally recommended to use PMU (Power Management Module) to control the power-on and power-off of LC1813.

The PWEN output by LC1813 chip is power control signal and multiplexed by GPIO. The signal is generally used to connect with that of PMU power. The PWEN signal is not reset, and is in inconclusive the state after power on. However, PWEN can be asserted to HIGH by writing "1" and LOW by writing "0" to APWR_PWEN_CTL.PWEN_CTL. In this chip, PWEN_CTL will be wrote "1" by BOOTROM program and be high when LC1813 powers on.

5.6 Memory Interface Timing

5.6.1 MEMCTL LPDDR2//LPDDR3 Interface Timing

This section describes interface timing of LC1813 MEMCTL connected with peripheral LPDDR2/LPDDR3 through *Figure 5-2* to *Figure 5-3.*

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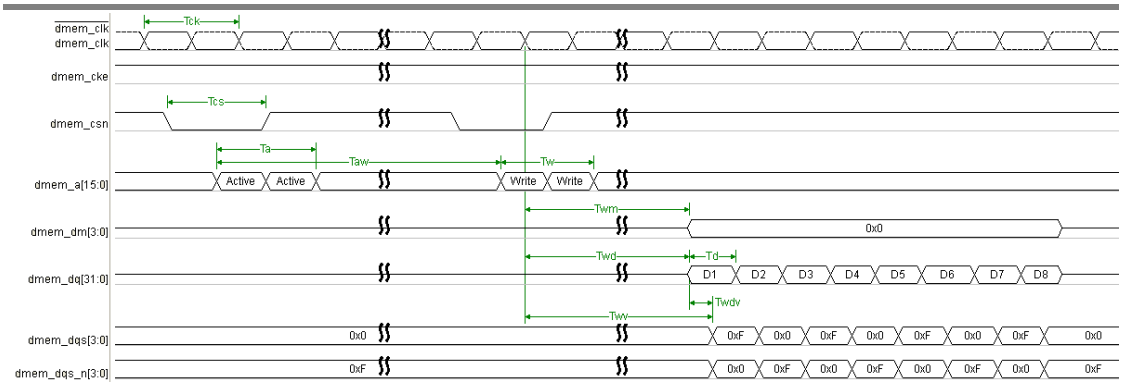

Figure 5-2 LPDDR2/LPDDR3 write burst (BL=8)

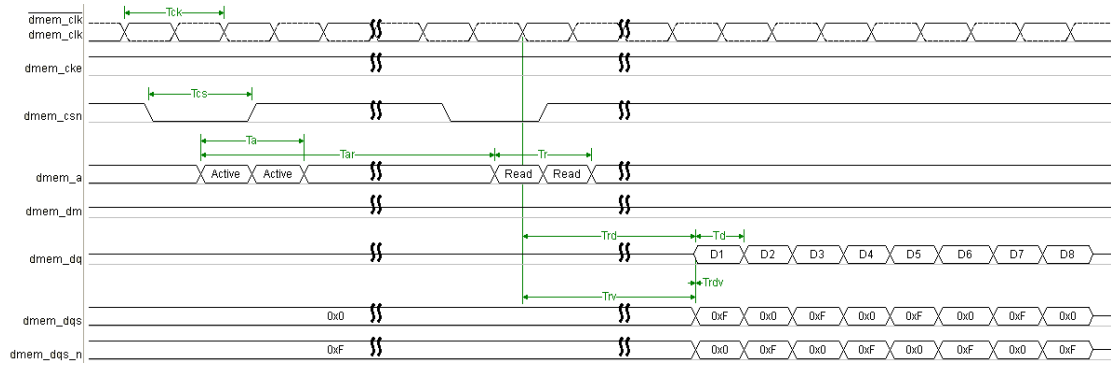

Figure 5-3 LPDDR2/LPDDR3 read burst (BL=8)

Table 5-7 lists LPDDR2/LPDDR3 interface timing parameters.

Table 5-7 LPDDR2/LPDDR3 interface timing parameter table

Symbol	Description	Value
Tck	Working clock cycle of LPDDR2/LPDDR3	Configured by register
Tcs	Valid time of cs_n	Tck
Ta	Time of active instruction	Tck
Tw	Time of write instruction	Tck
Tr	Time of read instruction	Tck
Taw	Delay time from active instruction to write instruction	TRCD*Tck
Tar	Delay time from active instruction to read instruction	TRCD*Tck
Twm	Delay time from write instruction to dm validated	(TCWL+0.75)*Tck
Twd	Delay time from write instruction to data validated of data bus	(TCWL+0.75)*Tck
Trd	Delay time from read instruction to data validated of data bus	(TCL+0.75)*Tck

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Symbol	Description	Value
Twv	Delay time from write instruction to the first rising edge of dqs	(TCWL+1)*Tck
Trv	Delay time from read instruction to the first rising edge of dqs	(TCL+0.75)*Tck
Td	Time cycle of single data validated of data line	0.5Tck
Twdv	Delay time from data validated of data line to the first rising edge of dqs when writing	0.25Tck
Trdv	Delay time from data validated of data line to the first rising edge of dqs when reading	0

5.6.2 NandFLASH Interface Timing

This section introduces LC1813 NAND FLASH interface timing through *Figure 5-4* to *Figure 5-7.*

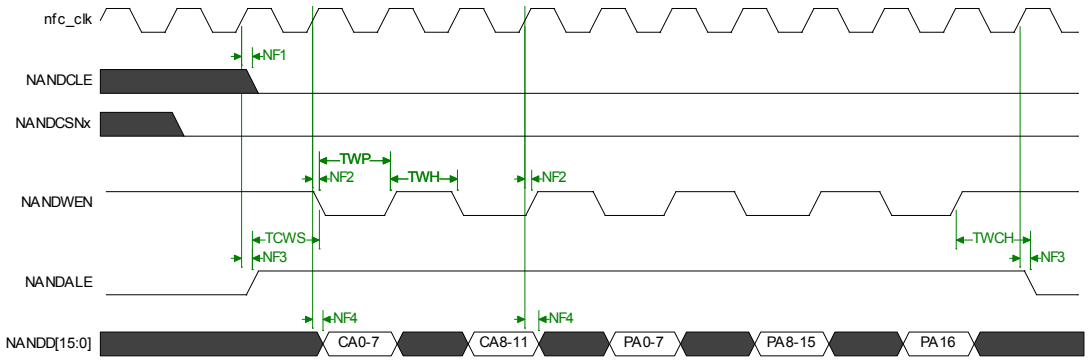

Figure 5-4 NANDFLASH address write timing

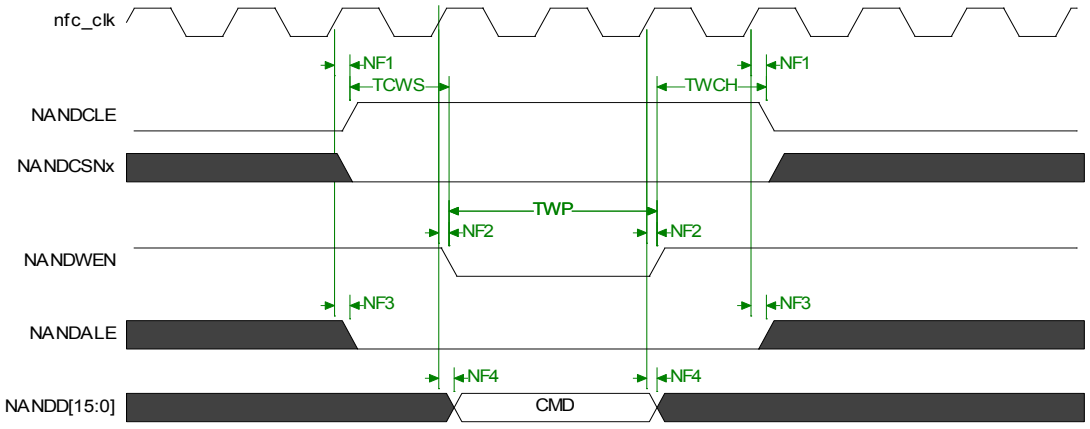

Figure 5-5 NANDFLASH command write timing

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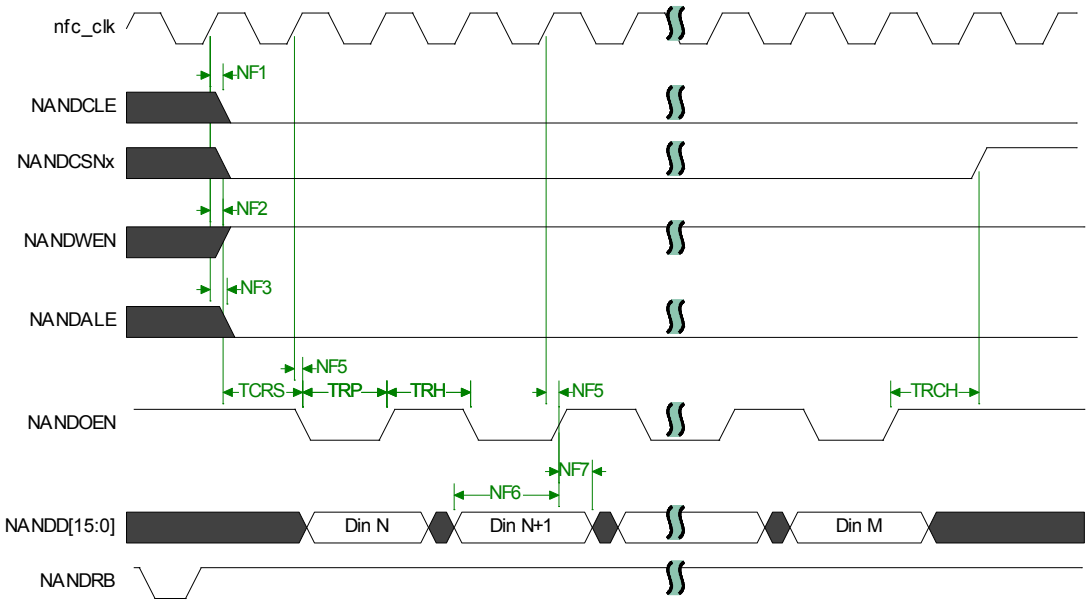

Figure 5-6 NANDFLASH data read timing

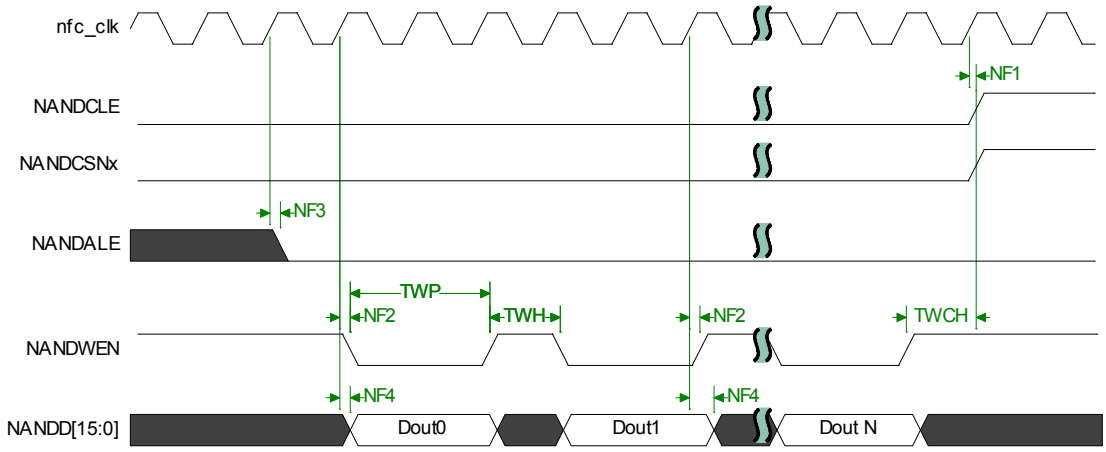

Figure 5-7 NANDFLASH data write timing

Table 5-8 NandFLASH Interface Timing Parameter Table

NO.	Symbol	Description	PVDD10 = 1.8 V Nominal		PVDD10 = 3 V Nominal		UNIT
			MIN	MAX	MIN	MAX	
NF1	td(clkh-clev)	Delay time, internal clock high to nand_cle transition	3	6	3	6	ns
NF2	td(clkh-wev)	Delay time, internal clock high to nand_we transition	4	11	4	11	ns

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NO.	Symbol	Description	PVDD10 = 1.8 V Nominal		PVDD10 = 3 V Nominal		UNIT
			MIN	MAX	MIN	MAX	
NF3	td(clkh-alev)	Delay time, internal clock high to nand_ale transition	3	10	3	10	ns
NF4	td(clkh-iov)	Delay time, internal clock high to nand_io[7: 0] valid	4	5	4	5	ns
NF5	td(clkh-rev)	Delay time, internal clock high to nand_re transition	3	8	3	8	ns
NF6	tsu(iov-reh)	Setup time, nand_io[7: 0] valid to nand_re transition	66	64	66	64	ns
NF7	th(clkh-rev)	Hold time, nand_re transition to nand_io[7: 0] invalid	1T	1T	1T	1T	ns
TWP	Write pulse width		(TWP_REG+3)T	(TWP_REG+3)T	(TWP_REG+3)T	(TWP_REG+3)T	T
TWH	Time between two write pulse		(TWH_REG+1)T	(TWH_REG+1)T	(TWH_REG+1)T	(TWH_REG+1)T	T
TCWS	Delay time, nand_ale, nand_cle and nand_ce valid to nand_we low		(TCWS_REG+3)T	(TCWS_REG+3)T	(TCWS_REG+3)T	(TCWS_REG+3)T	T
TWCH	Delay time, nand_we high to nand_ale, nand_cle and nand_ce invalid		(TWCH_REG+1)T	(TWCH_REG+1)T	(TWCH_REG+1)T	(TWCH_REG+1)T	T
TRP	Read pulse width		(TRP_REG+3)T	(TRP_REG+3)T	(TRP_REG+3)T	(TRP_REG+3)T	T
TRH	Time between two read pulse		(TRH_REG+4)T	(TRH_REG+4)T	(TRH_REG+4)T	(TRH_REG+4)T	T

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NO.	Symbol	Description	PVDD10 = 1.8 V Nominal		PVDD10 = 3 V Nominal		UNIT
			MIN	MAX	MIN	MAX	
TCRS	Time between nand_ce valid and nand_re low		(TCRS_REG+2)T	(TCRS_REG+2)T	(TCRS_REG+2)T	(TCRS_REG+2)T	T
TRCH	Time between nand_ce invalid to nand_re high		(TRCH_REG)T	(TRCH_REG)T	(TRCH_REG+1)T	(TRCH_REG)T	T

Notes:

T= cycle of nfc_clk

TWCH_REG=NFC_TIMR0[7:6]

TCWS_REG=NFC_TIMR0[5:4]

TWH_REG=NFC_TIMR0[3:2]

TWP_REG=NFC_TIMR0[1:0]

TRCH_REG=NFC_TIMR1[7:6]

TCRS_REG=NFC_TIMR0[5:4]

TRH_REG=NFC_TIMR0[3:2]

TRP_REG=NFC_TIMR0[1:0]

5.7 RF Interface Timing

The following sections respectively introduce TD RF interface, and GSM0 RF interface timings supported by LC1813. The following AC parameter's test conditions: T=25℃ /RL=50Ω/CL=50pF/CI=10pF/IO driver-strength=default value.

5.7.1 TDIF

This section introduces LC1813 chip TDx(x=0, 1) RF interface timing through *Figure 5-8* to *Figure 5-10*

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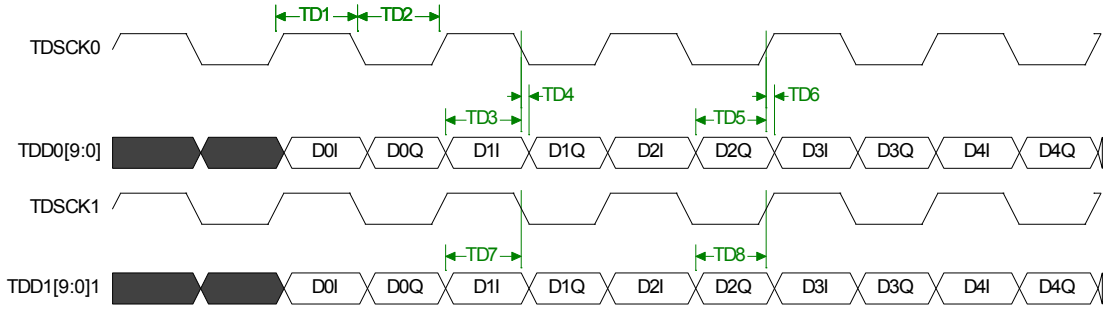

Figure 5-8 TD Rx timing

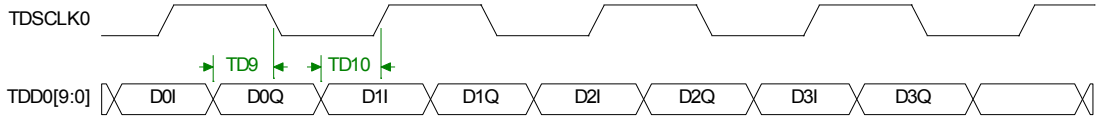

Figure 5-9 TD Tx (DA_CLK_P=1) timing

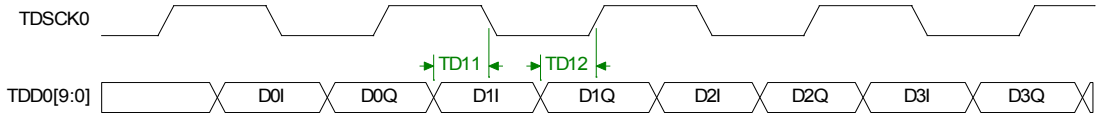

Figure 5-10 TD Tx (DA_CLK_P=0) timing

Table 5-9 TDIF Timing Parameter Table

NO.	Symbol	Description	PVDD2 = 1.8 V Nominal		PVDD2 = 3 V Nominal		UNIT
			MIN	MAX	MIN	MAX	
TD1	Tch	Output clock pulse width high	97.65		97.65		ns
TD2	Tcl	Output clock pulse width low	97.65		97.65		ns
TD3	Tsu	TDD0 Input I data setup time	5.25		5.25		ns
TD4	Thld	TDD0 Input I data hold time	0		0		ns
TD5	Tsu	TDD0 Input Q data setup time	5.25		5.25		ns
TD6	Thld	TDD0 Input Q data hold time	0		0		ns
TD7	Tsu	TDD1 Input I data setup time	9.23		9.23		ns
TD8	Tsu	TDD1 Input Q data setup time	9.23		9.23		ns
TD9	Td	Clk low to Q data delay	39.85	45.66	39.85	45.66	ns
TD10	Td	Clk high to I data delay	39.85	45.66	39.85	45.66	ns
TD11	Td	Clk low to I data delay	39.85	45.66	39.85	45.66	ns

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NO.	Symbol	Description	PVDD2 = 1.8 V Nominal		PVDD2 = 3 V Nominal		UNIT
			MIN	MAX	MIN	MAX	
TD12	Td	Clk high toQ data delay	39.85	45.66	39.85	45.66	ns

5.7.2 GSMIF0

This section describes DigRF V1.12 interface timing supported by GSMIF0 through *Figure 5-11* to *Figure 5-14.*

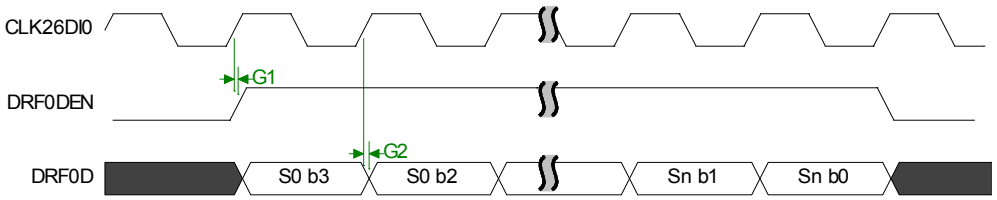

Figure 5-11 GSMIF0 DigRF V1.12 Tx stream/block mode timing

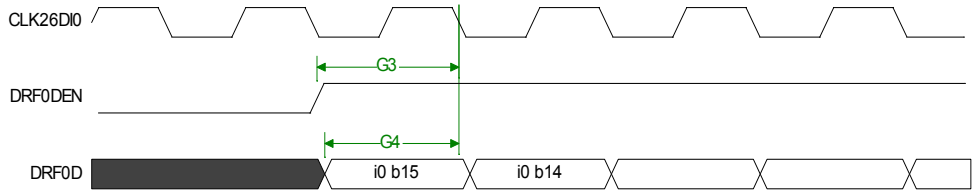

Figure 5-12 GSMIF0 DigRF V1.12 Rx mode timing (negedge)

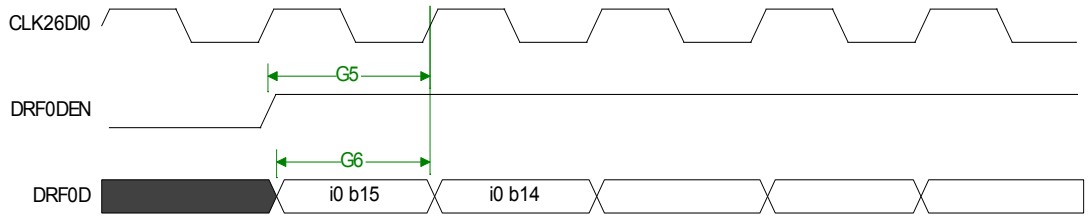

Figure 5-13 GSMIF0 DigRF V1.12 Rx mode timing (posedge)

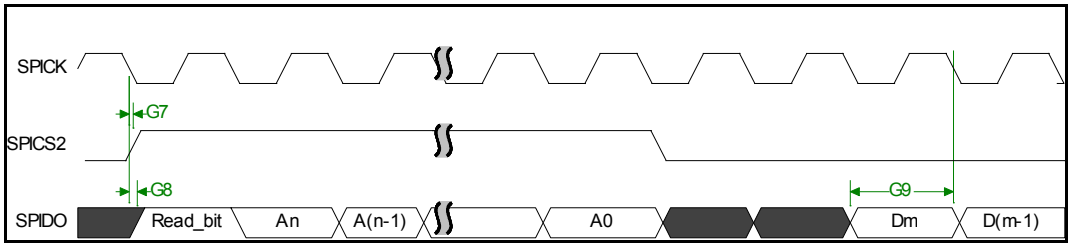

Figure 5-14 GSMIF0 DigRF Ctrl mode timing

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Table 5-10 GSMIF0 DigRF V1.12 Interface Timing Parameter Table

NO.	Symbol	Description	PVDD2 = 3 V Nominal		UNIT
			MIN	MAX	
G1	Td(CLK26M-DRF0DEN)	Output delay time, CLK26M high to DRF0DEN high	1.91	4.67	ns
G2	Td(CLK26M-DRF0D)	Output delay time, CLK26M high to DRF0D valid	2.68	6.12	ns
G3	Tsu(DRF0DEN-CLK26M negedge)	Input DRF0DEN setup time	1.54		ns
G4	Tsu(DRF0D-CLK26M negedge)	Input DRF0D setup time	2.14		ns
G5	Tsu(DRF0DEN-CLK26M posedge)	Input DRF0DEN setup time	1.54		ns
G6	Tsu(DRF0D-CLK26M posedge)	Input DRF0D setup time	2.14		ns
G7	Td(SPICLK - SPICS2)	Output delay time, SPICLK low to SPICS2 high	-10.22	-3.5	ns
G8	Td(SPICLK - SPIDO)	Output delay time, SPICLK low to SPIDO valid	-8.81	-3.11	ns
G9	Tsu(SPIDO - SPICLK)	Input SPIDO setup time	1.34	5.43	ns

5.8 SSI Interface Timing

LC1813 contains four synchronous serial interfaces, which can support SPI and SSP interface protocols. The following section describes the interface timing under various protocols. The following AC parameter's test conditions: T = 25℃/RL = 50Ω/CL = 50pF/CI = 10pF/IO driver-strength=default value.

5.8.1 SPI Protocol Interface Timing

This section introduces the timing of LC1813 chip SSI interface configured as SPI protocol through *Figure 5-16* to *Figure 5-18.*

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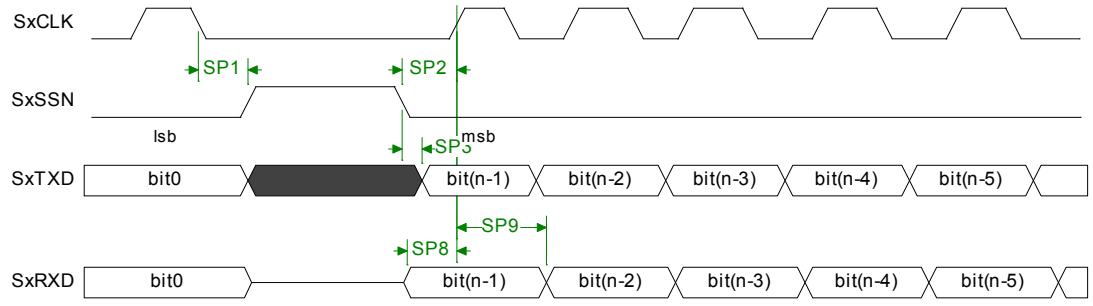

Figure 5-15 SSI as SPI timing (scpol = 0, scph = 0)

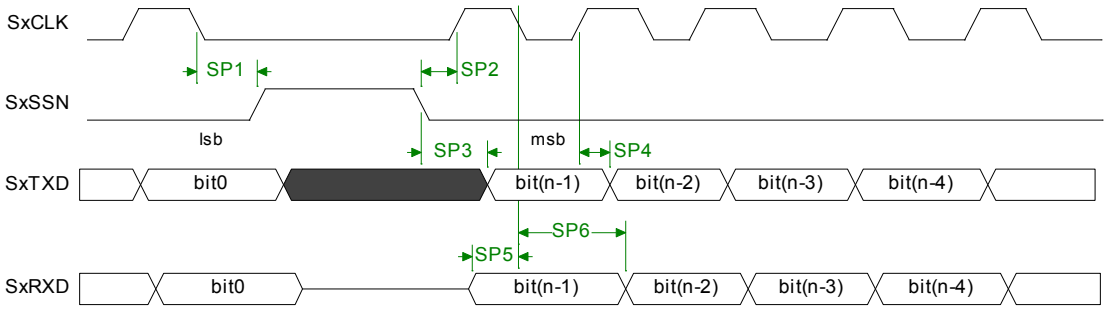

Figure 5-16 SSI as SPI timing (scpol = 0, scph =1)

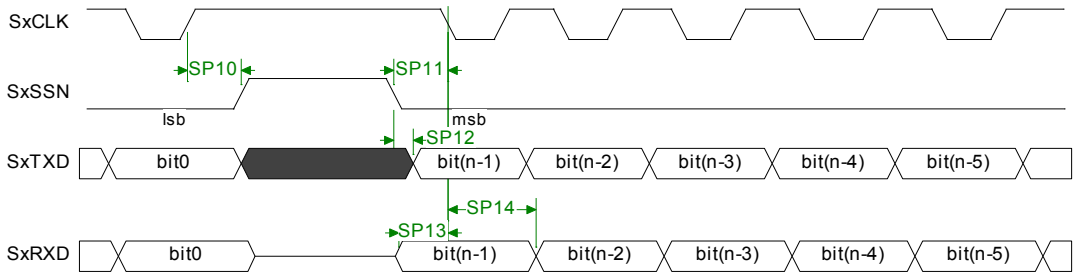

Figure 5-17 SSI as SPI timing (scpol = 1, scph =0)

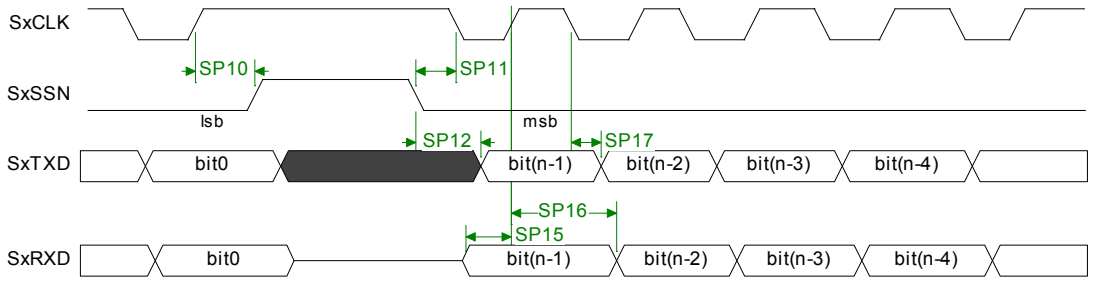

Figure 5-18 SSI as SPI timing (scpol = 1, scph =1)

Table 5-11 SPI Interface Timing Parameter Table

NO.	Symbol	Description	PVDD5 = 3 V Nominal		UNIT
			MIN	MAX	

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NO.	Symbol	Description	PVDD5 = 3 V Nominal		UNIT
			MIN	MAX	
SP1	Th(clkl-ssnh)	hold time, ssn high after clk low		0.5T(1)	ns
SP2	Td(ssnl-clkh)	delay time, ssn low to clk high		0.5T	ns
SP3	Td(ssnl-txdv)	delay time, ssn low to data valid		0	ns
SP4	Td(clkh-txdv)	delay time, clk high to data valid		0	ns
SP5	Tsu(rxdv-clkl)	setup time, data valid before clk low	0.5T		ns
SP6	Th(clkl-rxdv)	hold time, data valid after clk low	0.5T		ns
SP8	Tsu(rxdv-clkh)	setup time, data valid before clk high	0.5T		ns
SP9	Th(clkh-rxdv)	hold time, data valid after clk high	0.5T		ns
SP10	Th(clkh-ssnl)	hold time, ssn low after clk high		0.5T	ns
SP11	Td(ssnl-clkl)	delay time, ssn low to clk low		0.5T	ns
SP12	Td(ssnl-txdv)	delay time, ssn low to data valid		0	ns
SP13	Tsu(rxdv-clkl)	setup time, data valid before clk low	0.5T		ns
SP14	Th(clkl-rxdv)	hold time, data valid after clk low	0.5T		ns
SP15	Tsu(rxdv-clkh)	setup time, data valid before clk high	0.5T		ns
SP16	Th(clkh-rxdv)	hold time, data valid after clk high	0.5T		ns

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NO.	Symbol	Description	PVDD5 = 3 V Nominal		UNIT
			MIN	MAX	
SP17	Td(clkl-rxdv)	delay time, clk low to data valid		0	ns
Note: (1)T = cycle of SxCLK					

5.8.2 SSP Protocol Interface Timing

This section introduces the timing of LC1813 SSI interfaces configured as SSP protocol through *Figure 5-19*

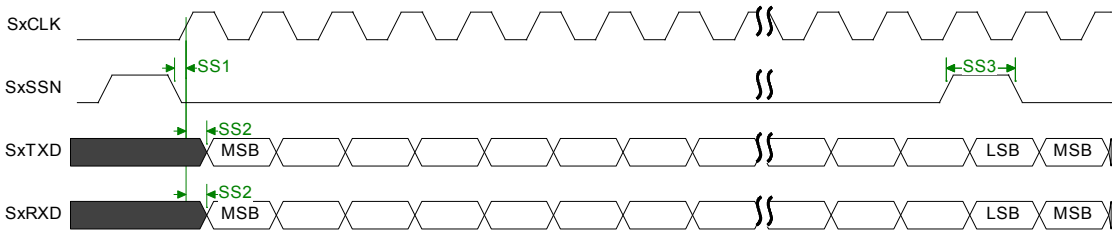

Figure 5-19 SSI as SSP timing

Table 5-12 SSP Interface Timing Parameter Table

NO.	Symbol	Description	PVDD5 = 3.3 VNominal		UNIT
			MIN	MAX	
SS1	Tclk	slave select signal low to clk vaild	0	0	ns
SS2	Tdd	clk high to ssi transmit data vaild	0	0	ns
SS3	tssnw	slave select signal width	1T(1)	1T	ns
Note: (1)T= Cycle of SxCLK					

5.9 PCM Protocol Interface Timing

This section introduces the timing of LC1813 PCM interface through *Figure 5-20* to *Figure 5-23*. *Figure 5-20* and *Figure 5-21* describe interface timing of short frame sync mode in single-channel mode. As well as long frame sync mode; *Figure 5-22* and *Figure 5-23* separately describe interface timings of dual-channel mode configured as DLY_MODE=1 and DLY_MODE=0 when samples input data at clock rising edge and outputs data at clock following edge.

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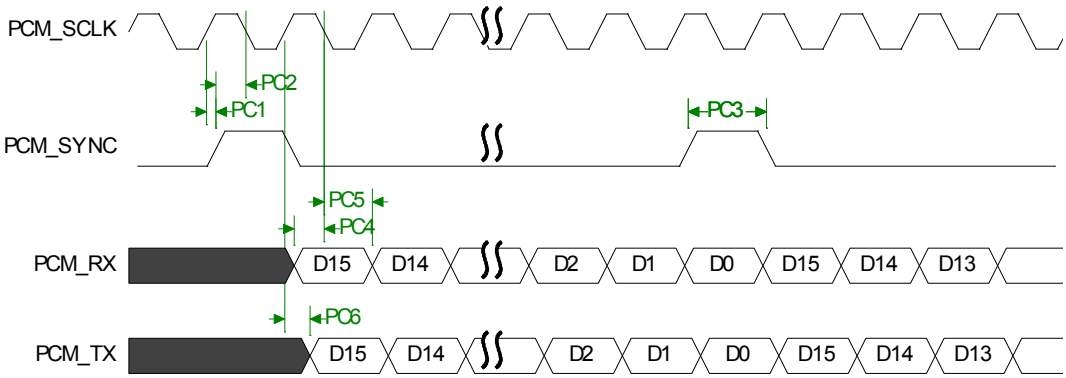

Figure 5-20 PCM short frame sync mode timing (PCM frame length = 16bit)

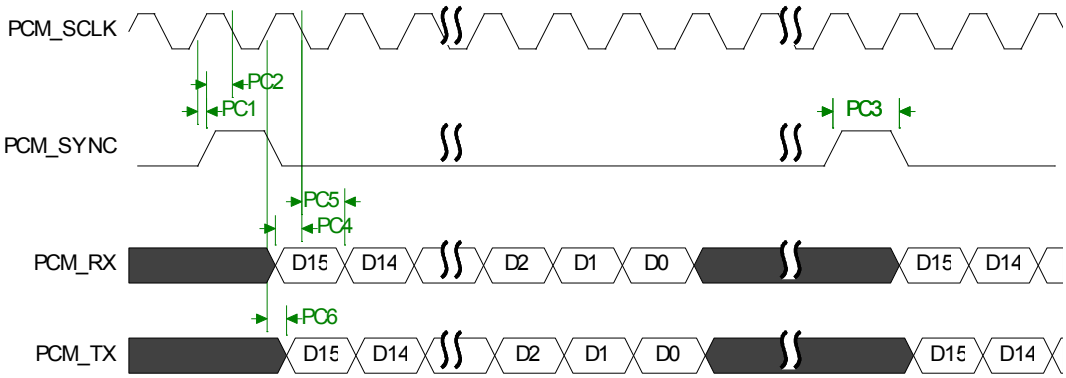

Figure 5-21 PCM short frame sync mode timing(PCM frame length ＞16bit)

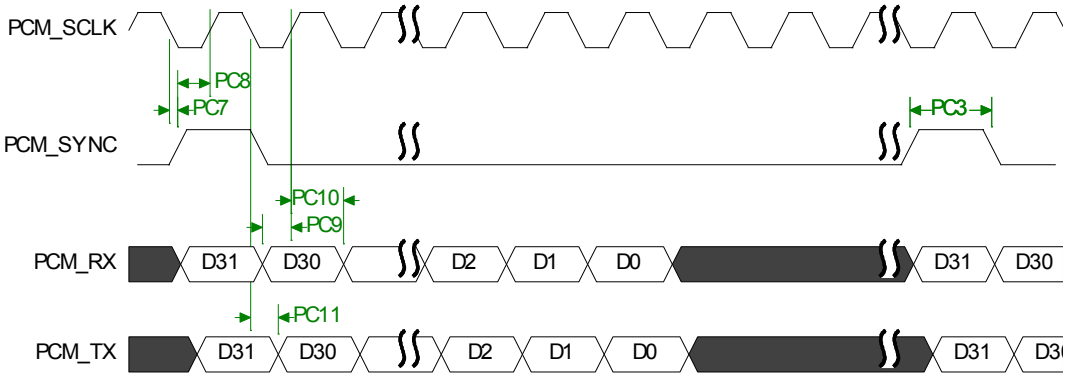

Figure 5-22 PCM dual-channel timing (DLY_MODE=1)

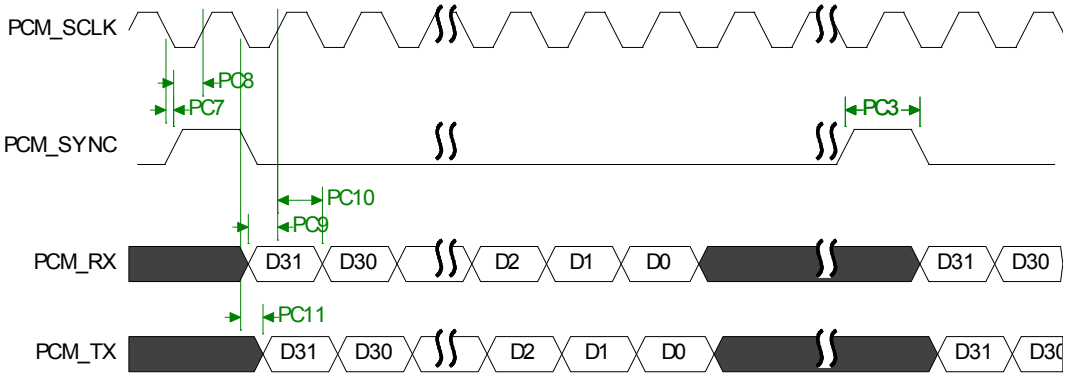

Figure 5-23 PCM dual-channel timing (DLY_MODE=0)

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Table 5-13 PCM Interface Timing Parameter Table

NO.	Symbol	Description	PVDD5 = 3 V Nominal		UNIT
			MIN	MAX	
PC1	td(clkh-syncv)	clk high to PCM SYNC signal valid	0		ns
PC2	tsu(syncv-clkl)	Setup time, PCM SYNC valid beforePCM_SCLK low	3T(1)		ns
PC3	tsyncw	PCM SYNC signal width	T1(2)	T1	ns
PC4	tsu(rxv-clkl)	Setup time, PCM_RX valid before PCM_SCLK low	0		ns
PC5	th(clkl-rxv)	Hold time, PCM_RX valid after PCM_SCLK low	2T		ns
PC6	td(clkh-txv)	clk high to PCM TX data valid	2T		ns
PC7	td(clkl-syncv)	clk low to PCM SYNC signal valid	0		ns
PC8	tsu(syncv-clkh)	Setup time, PCM SYNC valid before PCM_SCLK high	3T		ns
PC9	tsu(rxv-clkh)	Setup time, PCM_RX valid before PCM_SCLK high	0		ns
PC10	th(clkh-rxv)	Hold time, PCM_RX valid after PCM_SCLK high	2T		ns
PC11	td(clkl-txv)	clk low to PCM TX data valid	2T		ns

Notes:

(1)T=Cycle of pcm_mclk

(2)T1=Cycle of pcm_sclk

5.10 I2C Interface Timing

This section introduces the timing of LC1813 I2C interface through Figure 5-24.Five interfaces of I2Cx(x=0-3) and COM_I2C are all the same. The following AC parameter's test conditions: T=25℃/RL=50Ω/CL=50pF/CI=10pF/IO driver-strength=default value.

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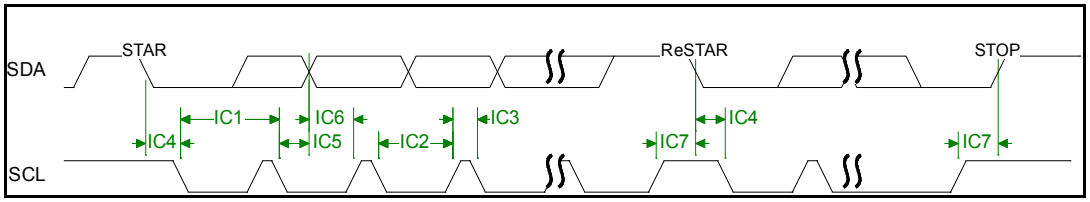

Figure 5-24 I2C timing

Table 5-14 I2C Interface Timing Parameter Table

NO.	Symbol	Description	STANDTARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
IC1	tc(SCL)	Cycle time, I2C.SCL	10		2.5		us
IC2	tw(SCLL)	Pulse duration, I2C.SCL low	4.7		1.3		us
IC3	tw(SCLH)	Pulse duration, I2C.SCL high	4		0.6		us
IC4	th(SCLL-SDAL)	I2C.SCL low after I2C.SDA low(for a START & ReSTART)	4		0.6		us
IC5	th(SDA-SCLL)	Hold time, I2C.SDA valid after I2C.SCL low	1T(1)		1T		ns
IC6	tsu(SDA-SDLH)	Setup time, I2C.SDA valid before I2C.SCL high	250		100		ns
IC7	tsu(SDA-SDLH)	Setup time, I2C.SCL high before I2C.SDA high(for STOP condition)	4		0.6		us
Note: (1)T=Cycle of i2c_mclk							

5.11 I2S Interface Timing

This section introduces the timing of LC1813 chip I2S interface. The following AC parameters' test conditions: T=25 ℃ /RL=50Ω/CL=50pF/CI=10pF/IO driver-strength=default value.

11. I2S standard interface protocol

DLY_MODE can only be configured as 0 when I2S is working in the master mode. In slave mode, DLY_MODE can also be 0 or 1.

When I2S works in slave mode, it must be ensured that there are 16, and only 16 rising edges of i2s_sclk clock in one i2s_wc cycle for both LEFT audio channel and RIGHT audio channel. That is, in the time periods labeled as IS6 in *Figure 5-25* and *Figure 5-26*, i2s_sclk can be HIGH or LOW, but the rising edge of i2s_sclk is not allowed to appear.

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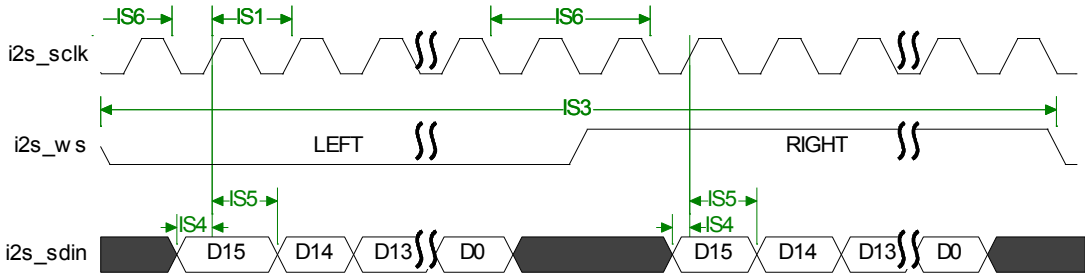

Figure 5-25 I2S master/slave rx timing (DLY_MODE=0)

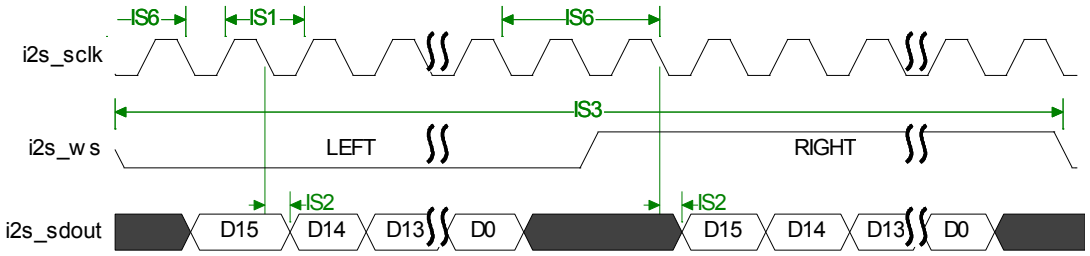

Figure 5-26 I2S master/slave tx timing (DLY_MODE=0)

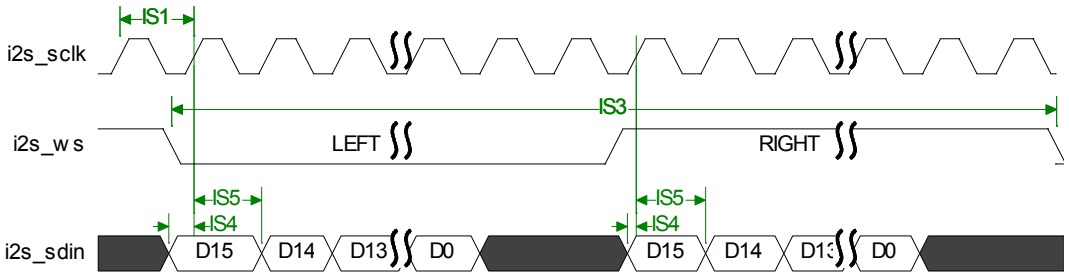

Figure 5-27 I2S slave rx timing (DLY_MODE=1)

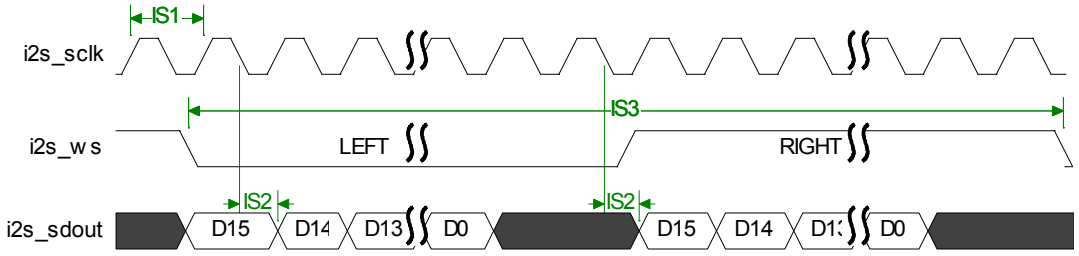

Figure 5-28 I2S slave tx timing (DLY_MODE=1)

Table 5-15 I2S Interface Timing Parameter Table

NO.	Symbol	Description	PVDD5 = 3 V Nominal		UNIT
			MIN	MAX	
IS1	tc(clk)	Cycle time, i2s_sclk	6T(1)		ns
IS2	td(clkl-dv)	i2s_sclk low to i2s_sdout data valid		2T	ns

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NO.	Symbol	Description	PVDD5 = 3 V Nominal		UNIT
			MIN	MAX	
IS3	tc(clk)	Cycle time, i2s_ws	32T1(2)		ns
IS4	tsu(dv_clkh)	Setup time, read data(i2s_sdin) valid before i2s_sclk high	0		ns
IS5	th(clkh-dv)	Hold time, read data(i2s_sdin) valid after i2s_sclk high	2T		ns
IS6	inval	Data invalid time in slave mode, in this period i2s_sclk should be high or low without any rising edges	T1		ns

Notes:

(1) T = Cycle of i2s_mclk

(2) T1 = Cycle of i2s_sclk

12. I2S TDM transmission protocol

TDM interface supports two types of timings: starting of the first channel aligns with rising edge of FSYNC, or is delayed a SCLK clock cycle than rising edge of FSYNC.

The relation between clock frequency and sample rate of SCLK is as below (SCLK is related with channel number per frame, channel block length and sample rate): Fsclk = channel_num * channel_block_length * sample_rate.I2S standard interface is the simplest form of TDM transmission standard, so TDM transmission interface timing can refer to I2S interface timing parameter table.

5.12 SDMMC Interface Timing

This section describes LC1813 chip's SDMMC card interface timing through *Figure 5-29* to *Figure 5-32*.

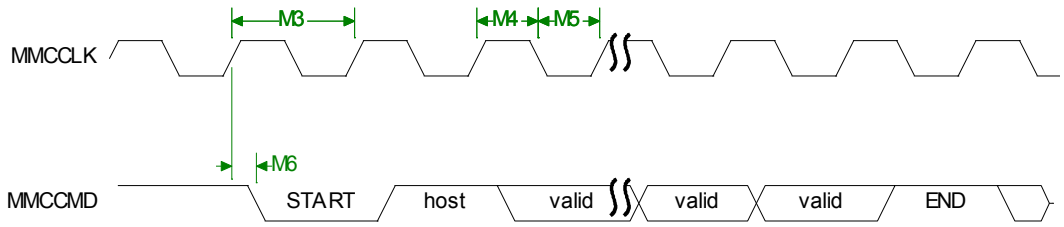

Figure 5-29 SD/MMC host command timing diagram

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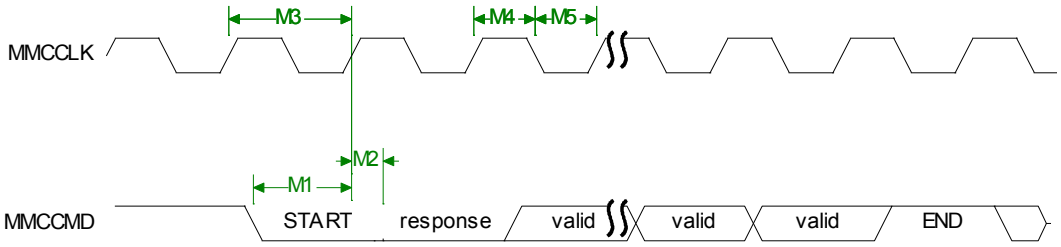

Figure 5-30 SD/MMC response timing

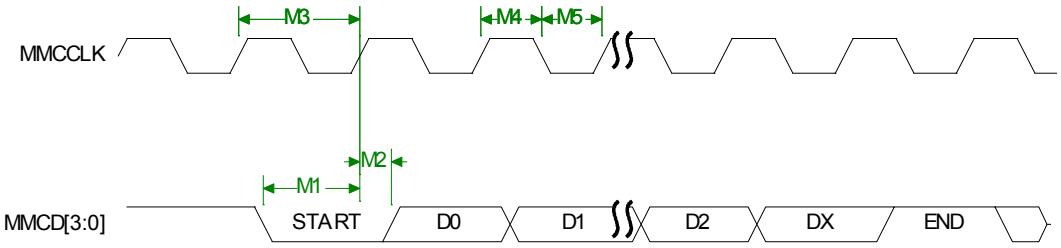

Figure 5-31 SD/MMC read timing

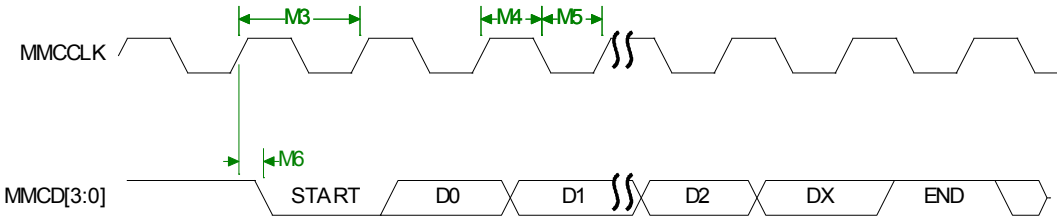

Figure 5-32 SD/MMC write timing

Table 5-16 SD/MMC Timing Parameter Table

NO.	Symbol	Description	PVDD10/PVDD11/PVDD12 = 3 V Nominal		UNIT
			MIN	MAX	
M1	tsu(cmdv-clkh)	Setup time, MMCMD/MMCD valid before MMCCLK high	2		ns
M2	th(clkh-cmdiv)	Hold time, MMCMD/MMCD invalid after MMCCLK high	0		ns
M3	tc(clk)	Cycle time, MMCCLK	1T(1)	2m(3)T	ns
M4	tw(clkh)	Pulse Duration, MMCCLK high	0.5T	mT	ns
M5	tw(clkl)	Pulse Duration, MMCCLK low	0.5T	mT	ns
M6	td(clkh-dv)	Delay time, MMCCLK high to MMCMD/MMCD valid	2.37	6.13+n(4)P(2)	ns

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NO.	Symbol	Description	PVDD10/PVDD11/PVDD12 = 3 V Nominal		UNIT
			MIN	MAX	
Notes: (1) T = cycle of SDMMC (2) P = cycle of clk_afgr (3) m = configuration value of SDMMC_CLKDIV of SDMMC (4) n= configuration value of AP_PWR_SDMMCxCLKCTL.SDMMC_CLK2_DELAY of AP_PWR					

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6 Chapter6 Mechanical Characteristics

This chapter provides the mechanical specifications for LC1813 chip.

6.1 Packaging Materials

Table 6-1 shows the solder ball material list

Table 6-1 Package Materials

Solder Balls	Sn/Ag1.2/Cu0.5/Ni0.05

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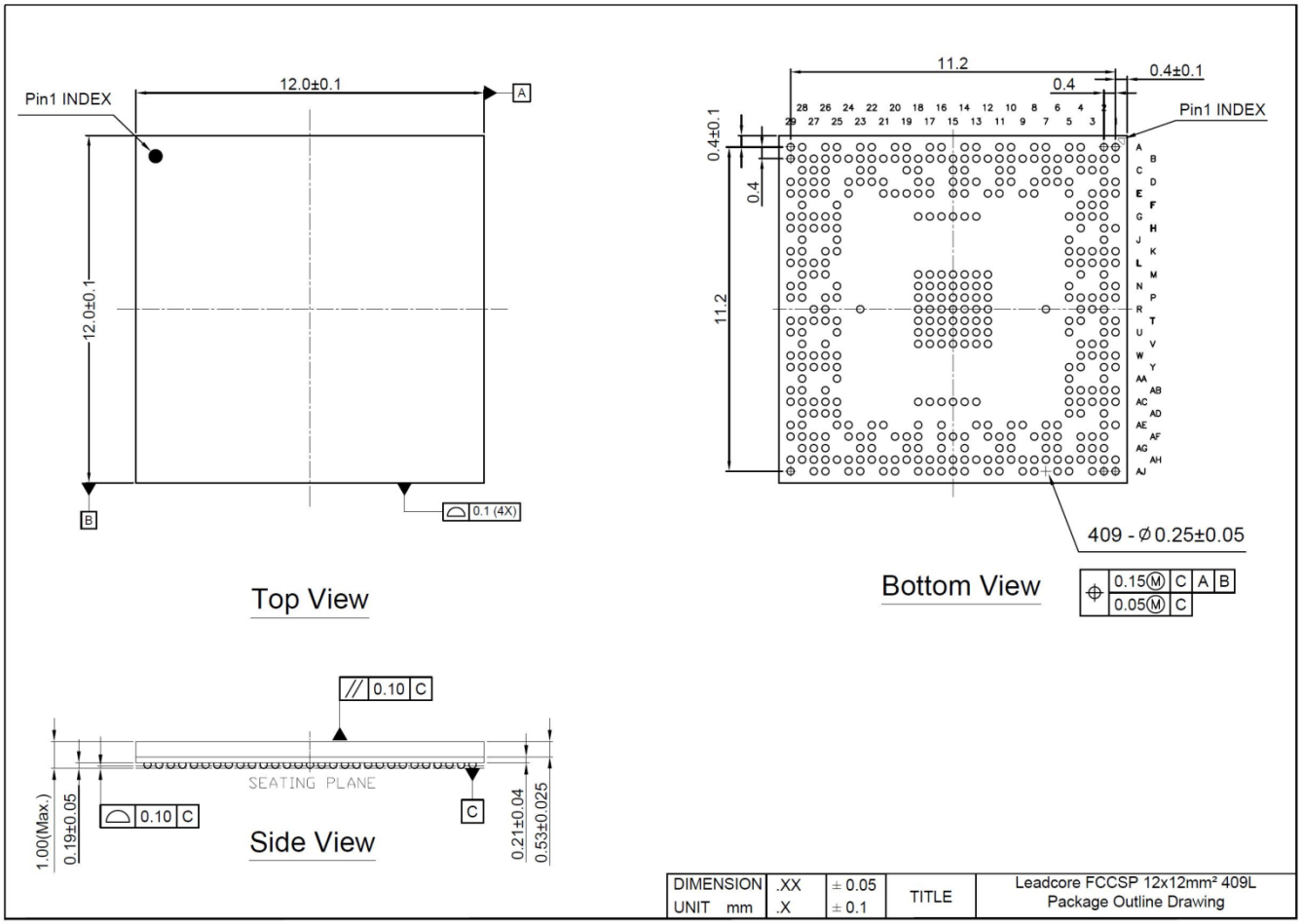
6.2 Packaging Views



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6.3 Classification Profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min(Tsmin) Temperature Max(Tsmax) Time(ts) from(Tsmin to Tsmax)	 150 °C 200 °C 60-120 seconds
Ramp-up rate(TL to Tp)	3 °C/second max.
Liquidous temperature(TL) Time(tL) maintained above TL	217 °C 60-150 seconds
Peak package body temperature(Tp)	≥250°C
Time(tp)* within 5 °C of the specified classification temperature(Tc)	30* seconds
Ramp-down rate(Tp to TL)	6 °C/second max.
Time 25 °C to peak temperature	8 minutes max.

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7 Figure Contents

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8 Table Contents

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9 GPIO List

Module	GPIO	Signal Name
GPIO0	GPIO0_D0	gpio_d[0]
	GPIO0_D1	gpio_d[1]
	GPIO0_D2	gpio_d[2]
	GPIO0_D3	gpio_d[3]
	GPIO0_D4	gpio_d[4]
	GPIO0_D5	gpio_d[5]
	GPIO0_D6	gpio_d[6]
	GPIO0_D7	gpio_d[7]
	GPIO0_D8	gpio_d[8]
	GPIO0_D9	gpio_d[9]
	GPIO0_D10	gpio_d[10]
	GPIO0_D11	gpio_d[11]
	GPIO0_D12	gpio_d[12]
	GPIO0_D14	gpio_d[14]
	GPIO0_D15	gpio_d[15]
	GPIO0_D16	gpio_d[16]
	GPIO0_D17	gpio_d[17]
	GPIO0_D18	gpio_d[18]
	GPIO0_D19	gpio_d[19]
	GPIO0_D20	gpio_d[20]
	GPIO0_D21	gpio_d[21]
	GPIO0_D22	gpio_d[22]
	GPIO0_D23	gpio_d[23]
	GPIO0_D24	gpio_d[24]

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Module	GPIO	Signal Name
	GPIO0_D25	gpio_d[25]
	GPIO0_D26	gpio_d[26]
	GPIO0_D27	gpio_d[27]
	GPIO0_D28	gpio_d[28]
	GPIO0_D32	gpio_d[32]
	GPIO0_D33	gpio_d[33]
	GPIO0_D44	gpio_d[44]
	GPIO0_D45	gpio_d[45]
	GPIO0_D46	gpio_d[46]
	GPIO0_D47	gpio_d[47]
	GPIO0_D48	gpio_d[48]
	GPIO0_D59	gpio_d[59]
	GPIO0_D60	gpio_d[60]
	GPIO0_D61	gpio_d[61]
	GPIO0_D62	gpio_d[62]
	GPIO0_D63	gpio_d[63]
	GPIO0_D64	gpio_d[64]
	GPIO0_D65	gpio_d[65]
	GPIO0_D66	gpio_d[66]
	GPIO0_D67	gpio_d[67]
	GPIO0_D68	gpio_d[68]
	GPIO0_D69	gpio_d[69]
	GPIO0_D70	gpio_d[70]
	GPIO0_D71	gpio_d[71]
	GPIO0_D72	gpio_d[72]
	GPIO0_D73	gpio_d[73]
	GPIO0_D74	gpio_d[74]

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Module	GPIO	Signal Name
	GPIO0_D75	gpio_d[75]
	GPIO0_D76	gpio_d[76]
	GPIO0_D77	gpio_d[77]
	GPIO0_D78	gpio_d[78]
	GPIO0_D79	gpio_d[79]
	GPIO0_D80	gpio_d[80]
	GPIO0_D81	gpio_d[81]
	GPIO0_D82	gpio_d[82]
	GPIO0_D83	gpio_d[83]
	GPIO0_D84	gpio_d[84]
	GPIO0_D85	gpio_d[85]
	GPIO0_D86	gpio_d[86]
	GPIO0_D87	gpio_d[87]
	GPIO0_D88	gpio_d[88]
	GPIO0_D89	gpio_d[89]
	GPIO0_D90	gpio_d[90]
	GPIO0_D91	gpio_d[91]
	GPIO0_D92	gpio_d[92]
	GPIO0_D93	gpio_d[93]
	GPIO0_D94	gpio_d[94]
	GPIO0_D96	gpio_d[96]
	GPIO0_D97	gpio_d[97]
	GPIO0_D98	gpio_d[98]
	GPIO0_D99	gpio_d[99]
	GPIO0_D100	gpio_d[100]
	GPIO0_D101	gpio_d[101]
	GPIO0_D109	gpio_d[109]

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Module	GPIO	Signal Name
	GPIO0_D110	gpio_d[110]
	GPIO0_D111	gpio_d[111]
	GPIO0_D112	gpio_d[112]
	GPIO0_D113	gpio_d[113]
	GPIO0_D114	gpio_d[114]
	GPIO0_D115	gpio_d[115]
	GPIO0_D116	gpio_d[116]
	GPIO0_D117	gpio_d[117]
	GPIO0_D118	gpio_d[118]
	GPIO0_D119	gpio_d[119]
	GPIO0_D120	gpio_d[120]
	GPIO0_D121	gpio_d[121]
	GPIO0_D122	gpio_d[122]
	GPIO0_D123	gpio_d[123]
	GPIO0_D126	gpio_d[126]
	GPIO0_D127	gpio_d[127]
GPIO1	GPIO1_D0	gpio_d[128]
	GPIO1_D1	gpio_d[129]
	GPIO1_D2	gpio_d[130]
	GPIO1_D3	gpio_d[131]
	GPIO1_D4	gpio_d[132]
	GPIO1_D5	gpio_d[133]
	GPIO1_D6	gpio_d[134]
	GPIO1_D7	gpio_d[135]
	GPIO1_D8	gpio_d[136]
	GPIO1_D9	gpio_d[137]
	GPIO1_D10	gpio_d[138]

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Module	GPIO	Signal Name
	GPIO1_D11	gpio_d[139]
	GPIO1_D12	gpio_d[140]
	GPIO1_D13	gpio_d[141]
	GPIO1_D14	gpio_d[142]
	GPIO1_D17	gpio_d[145]
	GPIO1_D18	gpio_d[146]
	GPIO1_D19	gpio_d[147]
	GPIO1_D20	gpio_d[148]
	GPIO1_D21	gpio_d[149]
	GPIO1_D22	gpio_d[150]
	GPIO1_D23	gpio_d[151]
	GPIO1_D24	gpio_d[152]
	GPIO1_D25	gpio_d[153]
	GPIO1_D26	gpio_d[154]
	GPIO1_D27	gpio_d[155]
	GPIO1_D28	gpio_d[156]
	GPIO1_D29	gpio_d[157]
	GPIO1_D30	gpio_d[158]
	GPIO1_D31	gpio_d[159]
	GPIO1_D32	gpio_d[160]
	GPIO1_D33	gpio_d[161]
	GPIO1_D34	gpio_d[162]
	GPIO1_D35	gpio_d[163]
	GPIO1_D36	gpio_d[164]
	GPIO1_D37	gpio_d[165]
	GPIO1_D38	gpio_d[166]
	GPIO1_D39	gpio_d[167]

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Module	GPIO	Signal Name
	GPIO1_D40	gpio_d[168]
	GPIO1_D41	gpio_d[169]
	GPIO1_D42	gpio_d[170]
	GPIO1_D43	gpio_d[171]
	GPIO1_D44	gpio_d[172]
	GPIO1_D45	gpio_d[173]
	GPIO1_D46	gpio_d[174]
	GPIO1_D47	gpio_d[175]
	GPIO1_D48	gpio_d[176]
	GPIO1_D49	gpio_d[177]
	GPIO1_D50	gpio_d[178]
	GPIO1_D51	gpio_d[179]
	GPIO1_D52	gpio_d[180]
	GPIO1_D53	gpio_d[181]
	GPIO1_D54	gpio_d[182]
	GPIO1_D55	gpio_d[183]
	GPIO1_D56	gpio_d[184]
	GPIO1_D57	gpio_d[185]
	GPIO1_D58	gpio_d[186]
	GPIO1_D59	gpio_d[187]
	GPIO1_D60	gpio_d[188]
	GPIO1_D61	gpio_d[189]
	GPIO1_D62	gpio_d[190]
	GPIO1_D63	gpio_d[191]
	GPIO1_D64	gpio_d[192]
	GPIO1_D65	gpio_d[193]
	GPIO1_D66	gpio_d[194]

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Module	GPIO	Signal Name
	GPIO1_D67	gpio_d[195]
	GPIO1_D68	gpio_d[196]
	GPIO1_D81	gpio_d[209]
	GPIO1_D82	gpio_d[210]
	GPIO1_D83	gpio_d[211]
	GPIO1_D84	gpio_d[212]
	GPIO1_D85	gpio_d[213]
	GPIO1_D86	gpio_d[214]
	GPIO1_D87	gpio_d[215]
	GPIO1_D88	gpio_d[216]
	GPIO1_D89	gpio_d[217]
	GPIO1_D90	gpio_d[218]
	GPIO1_D91	gpio_d[219]
	GPIO1_D92	gpio_d[220]
	GPIO1_D93	gpio_d[221]
	GPIO1_D94	gpio_d[222]
	GPIO1_D95	gpio_d[223]
	GPIO1_D96	gpio_d[224]
	GPIO1_D97	gpio_d[225]
	GPIO1_D98	gpio_d[226]
	GPIO1_D99	gpio_d[227]
	GPIO1_D100	gpio_d[228]
	GPIO1_D101	gpio_d[229]
	GPIO1_D102	gpio_d[230]
	GPIO1_D104	gpio_d[232]
	GPIO1_D105	gpio_d[233]
	GPIO1_D106	gpio_d[234]

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Module	GPIO	Signal Name
	GPIO1_D111	gpio_d[239]
	GPIO1_D112	gpio_d[240]
	GPIO1_D113	gpio_d[241]
	GPIO1_D114	gpio_d[242]

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