SingleChip 3-Axis Accelerometer QMA6981



The QMA6981 is a single chip three-axis accelerometer. This surface-mount, small sized chip has integrated acceleration transducer with signal condition ASIC, sensing tilt, motion, shock and vibration, targeted for applications such as screen rotation, step counting, sleep quality, gaming and personal navigation in mobile and wearable smart devices.

The QMA6981 is based on our state-of-the-art, high resolution single crystal silicon MEMS technology. Along with custom-designed 10-bit ADC ASIC, it offers the advantages of low noise, high accuracy, low power consumption, and offset trimming. The I²C serial bus allows for easy interface.

The QMA6981 is in a 2x2x0.95mm3 surface mount 12-pin land grid array (LGA) package.

FEATURES

- 3-Axis Accelerometer in a 2x2x0.95 mm³ Land Grid Array Package (LGA), guaranteed to operate over a temperature range of -40 °C to +85 °C.
- 10 Bit ADC with low noise accelerometer sensor
- I²C Interface with Standard and Fast modes.
- Built-In Self-Test
- Wide range operation voltage (2.4V To 3.6V) and low power consumption (220µA)
- Integrated FIFO with a depth of 32 frames
- RoHS compliant , halogen-free
- Built–in motion algorithm

BENEFIT

- Small size for highly integrated products. Signals have been digitized and factory trimmed.
- High resolution allows for motion and tilt sensing
- High-Speed Interfaces for fast data communications.
 Maximum 2000Hz data output rate
- Enables low-cost functionality test after assembly in production
- Automatically maintains sensor's sensitivity under wide operation voltage range and compatible with battery powered applications
- For higher Data-Read rate
- Environmental protection and wide applications
- Low power and easy applications including step counting, sleep quality, gaming and personal navigation

CONTENTS

CC	NTENTS	2
1	INTERNAL SCHEMATIC DIAGRAM	3
	1.1 Internal Schematic Diagram	3
2	SPECIFICATIONS AND I/O CHARACTERISTICS	4
	2.1 Product Specifications	4
	2.2 Absolute Maximum Ratings	4
	2.3 I/O Characteristics	5
3	PACKAGE PIN CONFIGURATIONS	5
	3.1 Package 3-D View	5
	3.2 Package Outlines	6
4	EXTERNAL CONNECTION	
	4.1 Dual Supply Connection	8
	4.2 Single Supply connection	8
5	BASIC DEVICE OPERATION	9
	5.1 Acceleration Sensors	9
	5.2 Power Management	9
	5.3 Power On/Off Time	9
	5.4 Communication Bus Interface I ² C and Its Addresses	10
	5.5 Internal Clock	10
6	MODES OF OPERATION	10
	6.1 Modes Transition	10
	6.2 Description of Modes	12
7	Functions and interrupts	13
	7.1 POL_INT	13
	7.2 FOB_INT	14
	7.3 STEP/STEP_QUIT INT	14
	7.4 TAP_INT	15
	7.5 LOW-G_INT	17
	7.6 HIGH-G_INT	17
	7.7 DRDY_INT	17
	7.8 FIFO_INT	18
	7.9 Interrupt configuration	19
8	I ² C COMMUNICATION PROTOCOL	20
	8.1 I ² C Timings	20
	8.2 I ² C R/W Operation	20
9	REGISTERS	21
	9.1 Register Map	21
	9.2 Register Definition	24
		33

5

1 INTERNAL SCHEMATIC DIAGRAM

1.1 Internal Schematic Diagram



Figure 1. Block Diagram

Table 1. Block Function

Block	Function
Transducer	3 axis acceleration sensor
CVA	Charge-to-Voltage amplifier for sensor signals
Interrupt	Digital interrupt engine, to generate interrupt signal on data conversion,
	FIFO, and motion function
FIFO	Embedded 32-level FIFO
FSM	Finite state machine, to control device in different mode
12C	Interface logic data I/O
OSC	Internal oscillator for internal operation
Power	Power block, including LDO

2 SPECIFICATIONS AND I/O CHARACTERISTICS

2.1 **Product Specifications**

Table 2. Specifications (* Tested and specified at 25°C except stated otherwise.)

Parameter	Conditions	Min	Тур	Max	Unit]
Supply voltage	AVDD, for internal blocks	2.4	3.3	3.6	V	
I/O voltage	DVDD, for IO only	1.7	3.3	3.6	V	
Standby current	DVDD and AVDD on.		2		μA	
Conversion current	All blocks on, device in run state		220	300	uA	
Sleep current	For analog, AFE is off, BG, Transducer and oscillator are on or in low power mode. For digital, only counter and FSM are on		55	C	uA	
Deep sleep current	For analog, only BG and oscillator are on For digital, only counter and FSM are on	C	26	Л	uA	
BW	Programmable bandwidth		3.9~50 0		Hz	
Data output rate (ODR)	4*BW (ODRH=1)		15.6~2 000		Samples /sec	
Conversion time	in full speed		1/(4*B W)		mS	
Startup time	From the time when VDD reaches to 90% of final value to the time when device is ready for conversion		2		mS	
Wakeup time	From the time device enters into active mode to the time device is ready for conversion		1		mS	
Operating temperature		-40		85	°C	
Acceleration Full Range			+-2 +-4 +-8		G	
Sensitivity	FS=±2g		256		LSB/G	
Sensitivity	FS=±4g		128		LSB/G	
Sensitivity	FS=±8g		64		LSB/G	
Sensitivity Temperature Drift	FS=±2g, Normal VDD Supplies		±0.02		%/K	
Sensitivity tolerance	Gain accuracy		+-5		%	
Zero-g offset	FS=±2g, Normal VDD Supplies		80		mg	
Zero-g offset Temperature Drift	FS=±2g, Normal VDD Supplies		2		mg/K	
Noise density	FS=±2g		800		ug/sqrtHz	
Nonlinearity	FS=±2g, Best fit straight line,		±0.5		%FS	
Cross Axis Sensitivity			1		%	

2.2 Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings (Tested at 25°C except stated otherwise.)

Parameters	Condition	Min	Max	Units
VDD		-0.3	5.4	V
VDDIO		-0.3	5.4	V
ESD	HBM		2	kV
Shock Immunity	Duration < 200uS		10000	Gee
Storage temperature		-50	150	°C

2.3 I/O Characteristics

Table 4. I/O Characteristics

Parameter	Symbol	Pin	Condition	Min.	TYP.	Max.	Unit
Voltage Input	V _{IH} 1	SDA, SCL		0.7*VD		VDDIO+	V
High Level 1				DIO		0.3	
Voltage Input	V _{IL} 1	SDA, SCL		-0.3		0.3*VD	V
Low Level 1						DIO	
Voltage Output	V _{OH}	INT1, INT2	Output Current	0.8*VD			V
High Level			≥-100uA	DIO			
Voltage Output	V _{OL}	INT1, INT2,	Output Current			0.2*VD	V
Low Level		SDA	≤100uA(INT)			DIO	
			Output Current				
			≤1mA (SDA)				

3 PACKAGE PIN CONFIGURATIONS

3.1 Package 3-D View

Arrow indicates direction of G field that generates a positive output reading in normal measurement configuration.



Figure 2. Package 3-D View

Table 5. Pin Configurations

PIN	PIN	I/O	Power	TYPE	Function
No.	NAME		Supply		
1	AD0		VDD	CMOS	LSB of I ² C address
2	SDA	I/O	VLOGIC	CMOS	Serial data for I ² C
3	VDDIO			Power	Power supply for digital interface
4	NC				Not Open to Customer
5	INT1	0	VLOGIC	CMOS	Interrupt 1
6	INT2	0	VLOGIC	CMOS	Interrupt 2
7	VDD			Power	Power supply to internal block
8	GNDIO			Power	Ground for digital interface
9	GND			Power	Ground for internal block
10	NC				Not Open to Customer
11	NC				Not Open to Customer
12	SCK		VLOGIC	CMOS	Serial clock for I ² C

3.2 Package Outlines

3.2.1 Package Type

LGA (Land Grid Array)

3.2.2 Package Outline Drawing:

2.0mm (Length)*2.0mm (Width)*0.95mm (Height)



Figure 3. Package Outline Drawing

0.50

0.225

0.275

BSC

0.325

0.010

е

0.020 BSC

0.012

0.014



Figure 4. Chip Marking

Marking format and specification:

- 1) Laser marking, marking font: Arial
- 2) Marking dimensions: (Unit: mm)

	А	В	С	D	Е	F	G	Н	Pin 1	Letter style
Customer(T)	2	1.4	0.3	0.65	1.175	1.7	2	0.3	0.3	Arial
ChipMOS(T)	2	1.38	0.283	0.662	1.171	1.667	2	0.294	0.296	Arial

3) Offset tolerance: ±0.2mm

4) Marking definition:

Marking Text	Description	Comments
Line 1	Product Name	4 alphanumeric digits stand for product serials, such
		as "6981" stand for QMA6981 serials product.
Line 2	Y: the last digital of year	3 alphanumeric digits, variable to generate mass
	CCC: lot code	production trace-code
Line3	P: Part number S: Sub-con ID	P: 1 alphanumeric digits, fixed to identify part number, such as "A" stand for the part number QMA6981A2. S: 1 alphanumeric digits, variable identify sub-con, such as "C" stand for ChipMOS.
	Pin 1 identifier	Pin1 marking is positioned accordingly with unfilled-corner PIN on substrate.

4 EXTERNAL CONNECTION

4.1 Dual Supply Connection



4.2 Single Supply connection



5 BASIC DEVICE OPERATION

5.1 Acceleration Sensors

The QMA6981 acceleration sensor circuit consists of tri-axial sensors and application specific support circuits to measure the acceleration of device. With a DC power supply is applied to the sensor two terminals, the sensor converts any accelerating incident in the sensitive axis directions to a differential voltage output.

5.2 **Power Management**

Device has two power supply pins. VDD is the main power supply for all of the internal blocks, including analog and digital. VDDIO is a separate power supply, for digital interface only. There is no limitation on the voltage levels of VDD and VDDIO relative to each other, as long as they are within operating range.

The device contains a power-on-reset generator. It generates reset pulse as power on, which can load the register's default value, for the device to function properly.

To make sure the POR block functions well, we should have such constrains on the timing of VDD.

The device should turn-on both power pins in order to operate properly. When the device is powered on, all registers are reset by POR, then the device transits to the standby mode and waits for further commends.

Table 6 provides references for four power states. Transitions between power state 2 and power state 3 are prohibited, due to leakage current concerns.

Power State	VDD	VLOGIC	Power State description			
1	0V	0V	Device Off, No Power Consumption			
2	0V	1.7v~3.6v	Device Off, Unpredictable Leakage Current o VLOGIC due to Floating Node.			
3	2.4v~3.6v	0	Device Off, Same Current as Standby Mode			
4	2.4v~3.6v	1.7v~3.6v	Device On, Normal Operation Mode, Enters Standby Mode after POR			

Table 6: Power States

5.3 Power On/Off Time

After the device is powered on, some time periods are required for the device fully functional. The external power supply requires a time period for voltage to ramp up (PSUP), it is typically 50 milli-second. However it isn't controlled by the device. The Power –On –Reset time period (PORT) includes time to reset all the logics, load values in NVM to proper registers, enter the standby mode and get ready for analogy measurements. The power on/off time related to the device is in Table 7.

Table 7. Time Required for Power On/Off

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
POR	PORT	Time Period After VDD and			350	uS
Completion		VLOGIC at Operating Voltage				
Time		to Ready for I ² C Commend				
		and Analogy Measurement.				
Power off	SDV	Voltage that Device Considers			0.2	V
Voltage		to be Power Down.				
Power on	PINT	Time Period Required for	100			uS
Interval		Voltage Lower Than SDV to				
		Enable Next POR				



Figure 7. Power On/Off Timing

5.4 Communication Bus Interface I²C and Its Addresses

This device will be connected to a serial interface bus as a slave device under the control of a master device, such as the processor. Control of this device is carried out via I²C.

This device is compliant with I²C -Bus Specification, document number: 9398 393 40011. As an I²C compatible device, this device has a 7-bit serial address and supports I²C protocols. This device supports standard and fast speed modes, 100kHz and 400kHz, respectively. External pull-up resistors are required to support all these modes.

There are two I²C addresses selected by connecting pin 1 (AD0) to GND or VDD. The first six MSB are hardware configured to "001001" and the LSB can be configured by AD0.

Table 8. I2C Address Options

AD0 (pin 10)	I ² C Slave Address(HEX)	I ² C Slave Address(BIN)
Connect to GND	12	0010010
Connect to VDD	13	0010011

If more I²C address options are required, please contact factory for metal layer changes.

5.5 Internal Clock

The device has an internal clock for internal digital logic functions and timing management. This clock is not available to external usage.

6 MODES OF OPERATION

6.1 Modes Transition

The device has two different operational modes, controlled by register (11H), mode bit. The main purpose of these modes is for power management. The modes can be transited from one to another, as shown below, through I²C commends of changing mode bits. The default mode is Standby.



Figure 8. Basic operation flow after power-on

The default mode after power on is standby mode. Through I2C instruction, device can switch between standby mode and active mode. With SOFTRESET by writing 0xB6 into register 0x36, all of the registers will get default values. SOFTRESET can be done both in active mode and in standby mode. Also, by writing 1 in NVM_LOAD (0x33<3>) when device is in active mode, the NVM related image registers will get default value from NVM, however, other registers will keep the values of their own.



Figure 9. The work mode transferring

6.2 Description of Modes

6.2.1 Active Mode

In active mode, there are two states, run state, and sleep state.

6.2.1.1 Sleep State

In sleep state, whole signal chain is off, including analog and digital signal conditioning. And the rest blocks are on, including REF and OSC.

6.2.1.2 Run State

In run state, the ADC digitizes the charge signals from transducer, and digital signal processor conditions these signals in digital domain, processes the interrupts, and send data into FIFO (accessible through register 0x3F) and Data registers (0x01~0x06). After the signal conditioning, the signal chain will be off and ASIC enters back into sleep state, leaves timer and FSM on. Also in sleep state, reference and power blocks are on. This mode can also be called as power cycling. The power cycling duty is configurable through state registers SLEEP_DUR (0x11<3:0>). Device can enter into active mode by setting MODE_BIT (0x11<7>) to logic 1.

Besides the power cycling, device can also be configured as FULLRUN, by setting SLEEP_DUR=0000b. In this setting, no sleep state in the active mode, and device consumes most power, deliver the data most frequently.

6.2.1.3 Self-test State

In active mode, when user set SELFTEST_BIT (0x32<7>) to logic 1, ASIC will generate self-test signal onto the transducer, which transfer to electro-static force, to move the transducer. SELF_TEST_SIGN (0x32<2>) is used to set the force to negative.

For proper function of self-test, user should set SELFTEST_BIT to logic 1 for at least 4mS, for the settling of transducer due to self-test force.

User can compare the data before self-test with that after self-test. If the difference between these two data is larger than value listed in following, the device functions well. Also, please make sure that no external acceleration is added on the device.

	X axis	Y axis	Z axis			
Effective self-test signal	0.3g	0.3g	0.3g			

After done the self-test, please set the SELFTEST_BIT back to logic 0.

6.2.2 Standby Mode

In standby mode, most of the blocks are off, while device is ready for access through I2C. Standby mode is the default mode after power on or soft reset. Device can enter into this mode by set the soft reset register (0x36) to 0xB6 or set the MODE_BIT (0x11<7>) to logic 0.

Besides the above two modes, device also contains NVM loading state. This state is used to reset the value of the NVM related image registers. There are two bits related to this state. When NVM_LOAD (0x33<3>) is set to 1, NVM loading starts. When device is in NVM loading state, NVM_RDY (0x33<2>) is set to logic 0 by device. After NVM loading finished, NVM_RDY (0x33<2>) is set back to logic 1 by device, and NVM_LOAD is reset to 0 by device automatically. NVM loading can only happen when NVM_LOAD is set to 1 in active mode. If user set this NVM_LOAD bit to 1 in standby mode, device will not take the action until the device enters into active state by setting MODE_BIT (0x11<7>) to logic 1.

After loading NVM, the device will enter into standby mode directly. The loading time for NVM is about 100uS.

7 Functions and interrupts

ASIC support interrupts, such as POL_INT, FOB_INT (4D/6D), FLAT_INT, FF_INT, TAP_INT, SHK_INT, SLO_NO_MOT_INT, DRDY_INT, FIFO_INT, LPF, etc. (these functions are first priority) Also we support SLOPE_INT, HPF, high-g?, low-g, I2C watch dog timer, etc. (these functions are second priority) If necessary, we support Master I2C and FIFO for mag. (these are third priority) And, if necessary, we support SPI. (this is fourth priority)

7.1 POL_INT

The POL _INT stands for Portrait or Landscape interrupt, responses to the device in portrait direction or landscape direction. It includes 4 different event types, left, right, up and down events. The different type event stored and can be read from register ORIENT (0x0D<2:0>).

POLA(0x0D<2:0>)	Left	Right	Down	Up	comments
000	0	0	0	0	unknown
001	1	0	0	0	Left/Landscape
010	0	1	0	0	Right/Landscape
101	0	0	1	0	Down/portrait
110	0	0	0	1	Up/portrait

All different event can be detected by comparing the threshold set by register UD_X_TH(0x2D),RL_Y_TH(0x2F) with the sensor data , also have dependency on comparing result between the Z sensor readings and the register UD_Z_TH(0x2C) and RL_Z_TH(0x2E). Hysteresis can be introduced to the angle by decreasing a small offset for the threshold registers. All angle data inside the Hysteresis area will be regarded as unknown status in the orient status register (0x0D<2:0>).

Below Table shows the condition for kinds of orient events generation, the default threshold for X, Y is set to 40 degrees

Event	Х		Y		Z
Up	X >UD_X_TH X	(<0			Z <ud_z_th< th=""></ud_z_th<>
Down	X >UD_X_TH X	(>0			Z <ud_z_th< th=""></ud_z_th<>
Right			Y >RL_Y_TH	Y <0	Z <rl_z_th< th=""></rl_z_th<>
Left			Y >RL_Y_TH	Y >0	Z <rl_z_th< th=""></rl_z_th<>

For the registers settings, all the orient events threshold 1 LSB bit stand for 3.9mg. For Z axis, it is 8-bit signed 2's complement number ranged from 0.3g to 1.29g, default value 0 as stands for 0.8g. X, Y axis are unsigned data, default value A4 stands for 640mg which angel be regards as 40 degree ,there will be around 10 degree dead band left. The degree value for event can be calculated by the equal $\arcsin(0.0039^* rl_y_th)$.

The related interrupt status bit is ORIENT_INT (0x09<6>). When the POL status changed, the value of ORIENT_INT will be set to logic 1, and this will be cleared after the interrupt status register is read by user. ORIENT_EN (0x16<6>) is the enable bit for the POL_INT. Also, to get this interrupt on PIN_INT1 and/or PIN_INT2, we need to set INT1_ORIENT (0x19<6>) or INT2_ORIENT (0x1B<6>) to logic 1, to map the interrupt to the interrupt PINs.

7.2 FOB_INT

The Front/back event detected by comparing Z axis data with a low g value, ranged from 0.1g to 0.6g, which is defined by FB_Z_TH(0x30). The comparing condition shows below:

Event	X	Y	Z
Front			Z >FB_TH Z>0
Back			Z >FB_TH Z<0

The 2 different type events are stored and can be read from register ORIENT (0x0D<4:3>)

FOB(0x0D<4:3>)	status
00	unknown
01	Front
10	Back
11	Reserved

Angle between the Z-axis and g can have the relationship:

Acc_Z=1g X cos(theta).

Each threshold will introduce a dark area, which the Front/Back status cannot be recognized, the dark area angel is +/- (90-theta).

When the threshold register value is 0x00, the default value stands for 0.1g, and 1 LSB is 2mg. the minimum angel between sensor and g direction should be 84 degree, so the dark area should be \pm -6 degree. When the value is 0xFF, the dark area should be \pm -37 degree.

The related interrupt status bit is FOB_INT (0x09<7>). When the FOB status changed, the value of FOB_INT will be set to logic 1, and this will be cleared after the interrupt status register is read by user. FOB_EN (0x16<6>) is the enable bit for the FOB_INT. Also, to get this interrupt on PIN_INT1 and/or PIN_INT2, we need to set INT1_FOB (0x19<7>) or INT2_FOB (0x18<7>) to logic 1, to map the internal interrupt to the interrupt PINs.

7.3 STEP/STEP_QUIT INT

The STEP/STEP_QUIT detect that the user is entering/exiting step mode. When the user enter into step mode, at least one axis sensor data will vary periodically, by numbering the variation periods the step counter can be calculated.



Figure 10. STEP/STEP_QUIT

Median data (max+min) /2 is called dynamic threshold, the max and min data can be updated by certainly samples, the sample number can be set by register STEP_SAMPLE_CNT (0x12). When the sensor data decreasing (or increasing) through the dynamic threshold, a user run step is detected.

Register STEP_PRECISION (0x13) is used as threshold when updating the new collected sensor data. Sensor data below the threshold will be discarded, this helps removing unstable variations causing failed detection. The run step event happened at certain interval timing. All of the events outside the timing window will not be regarded as a run step and the step counter will not counted. The timing window can be set by register STEP_TIME_UP(0x15) and STEP_TIME_LOW(0x14), the conversion ODR numbers ranged from STEP_TIME_LOW *ODR to 8* STEP_TIME_UP*ODR . Also if no new run step event detected until the up limited timing threshold, STEP_QUIT INT will generation.

To remove unstable variation which will cause failing STEP event detection, only after 4 continuous step detected, it will be considered as valid step events, also the step counter register STEP_CNT_LSB/ STEP_CNT_MSB (0x1C,0x1D) will updated immediately by value 4, interrupt STEP is generated as well.

The related interrupt status bit is STEP_INT (0x0A<4 >) and STEP_QUIT_INT (0x0A<3>). When the interrupt is generated, the value of STEP_INT/ STEP_QUIT_INT will be set to logic 1, and this will be cleared after the interrupt status register is read by user. STEP_EN/STEP_QUIT_EN (0x16<3>/0x16<2>) is the enable bit for the STEP_INT/STEP_QUIT_INT. Also, to get this interrupt on PIN_INT1 and/or PIN_INT2, we need to set INT1_STEP (0x1A<3>)/INT1_STEP_QUIT (0x19<2>) or INT2_STEP (0x1A<4>) /INT2_STEP_QUIT (0x1B<2>) to logic 1, to map the interrupt to the interrupt PINs.

7.4 TAP_INT

Tap detection allows the device to detect the events such as clicking or double clicking of a touch-pad. A tap event is detected if a pre-defined slope (absolute value of acceleration difference) of the acceleration of at least one axis is exceeded. The tap detection includes single tap (TAPS) and double tap (TAPD). A 'Single tap' is a single event within a certain time, followed by a certain quiet time. A 'double tap' consists of a first such event followed by a second event within a defined time frame.

Single tap interrupt can be enabled (disabled) by setting '1' ('0') to bit (0x16) S_TAP_EN. The double tap detection can be enabled (disabled) by setting '1' ('0') to (0x16) D_TAP_EN.

The status of single tap interrupt is stored in (0x0A) S_TAP_INT, the status of double tap interrupt is stored in (0x0A) D_TAP_INT.

The slope threshold for detecting a tap event is set by register (0x2B) TAP_TH. The meaning of an LSB of (0x2B) TAP_TH depends on the selected g-range: 1 LSB of the (0x2B) TAP_TH is 62.5mg in 2g-range, 125mg in 4g-range, 250mg in 8g-range.

In figure the timing for single tap and double tap is visualized:



Figure 11. Timing of tap detction

The parameters (0x2A) TAP_SHOCK and (0x2A) TAP_QUIET are effect in both single tap and double tap detection, while (0x2A) TAP_DUR is effect in double tap detection only. Within the duration of (0x2A) TAP_SHOCK, any slope exceeding (0x2B) TAP_TH after the first event will be ignored. Contrary to this, within duration of (0x2A) TAP_QUIET, no slope exceeding (0x2B) TAP_TH must occur, otherwise the first event will be cancelled. A single tap interrupt is generated after the combined duration of (0x2A) TAP_SHOCK and (0x2A) TAP_QUIET. The interrupt is cleared after a delay of 12.5ms.

A double tap interrupt is generated if an event fulfilling the conditions for a single tap occurs within the duration defined by (0x2A) TAP_DUR after the completion of the first tap event. The interrupt is cleared after a delay of 12.5ms.

For each of parameter (0x2A) TAP_SHOCK and (0x2A) TAP_QUIET two values are selectable. By writing '0' ('1') to bit (0x2A) TAP_SHOCK, the duration of (0x2A) TAP_SHOCK is set to 50ms (75ms). By writing '0' ('1') to bit (0x2A) TAP_QUIET, the duration of (0x2A) TAP_QUIET is set to 30ms (20ms). The duration of (0x2A) TAP_DUR can be set by (0x2A) TAP_DUR bits:

TAP_DUR	Duration of TAP_DUR
000	50ms
001	100ms
010	150ms
011	200ms
100	250ms
101	375ms
110	500ms
111	700ms

The axis which triggered the interrupt is indicated by bits (0x0B) TAP_FIRST_X, (0x0B) TAP_FIRST_Y, and (0x0B) HIGH_FIRST_Z. The bit corresponding to the triggering axis contains a '1' while the other bits hold a '0'. These bits hold until new interrupt is triggered.

The sign of the triggering acceleration is stored in bit (0x0B) TAP_SIGN. If the (0x0C) HIGH_SIGN = '0' ('1'), the sign is positive (negative). This bit holds until new interrupt is triggered.

7.5 LOW-G_INT

The low-g interrupt is based on the comparison of acceleration data against a low-g threshold for the detection of free-fall.

The low-g interrupt is enabled (disabled) by writing logic '1' ('0') to bits (0x17) LOW_EN. There are two modes available, 'single' mode and 'sum' mode. In 'single' mode, the acceleration of each axis is compared with the threshold; in 'sum' mode, the sum of absolute value of all accelerations $|acc_x| + |acc_y| + |acc_z|$ is compared with the threshold. The mode is selected by the contents of the (0x24) LOW_MODE bit: '0' means 'single' mode, '1' means 'sum' mode.

The low-g threshold is set through the (0x23) LOW_TH register. 1 LSB of (0x23) LOW_TH always corresponds to an acceleration of 7.81mg (increment is independent from g-range setting).

A hysteresis can be set with the (0x24) LOW_HYST bits. 1 LSB of (0x24) LOW_HYST always corresponds to an acceleration of 125mg (as well, increment is independent from g-range setting).

The low-g interrupt is generated if the absolute values of the acceleration of all axes ('and' relation, in case of 'single' mode) or their sum (in case of 'sum' mode) are lower than the threshold for at least the time defined by the (0x22) LOW_DUR register. The interrupt is reset if the absolute value of the acceleration of at least one axis ('or' relation, in case of 'single' mode) or the sum of absolute values (in case of 'sum' mode) is higher than the threshold plus the hysteresis for at least one data acquisition. The relation between the content of (0x25) LOW_DUR and the actual delay of the interrupt generation is delay = $[(0x22) LOW_DUR+1]^*2ms$. The interrupt status is stored in bit (0x0B) LOW_INT.

7.6 HIGH-G_INT

The high-g interrupt is based on the comparison of acceleration data against a high-g threshold for the detection of shock or other high-acceleration events.

The high-g interrupt is enabled (disabled) per axis by writing logic '1' ('0') to bits (0x17) HIGH_EN_X, (0x17) HIGH_EN_Y, and (0x17) HIGH_EN_Z, respectively. The high-g threshold is set through the (0x26) HIGH_TH register. The meaning of an LSB of (0x26) HIGH_TH depends on the selected g-range: it corresponds to 7.81mg in 2g-range (15.63mg in 4g-range, 31.25mg in 8g-range).

A hysteresis can be set with the (0x24) HIGH_HYST bits. Analogously to the (0x26) HIGH_TH, the meaning of an LSB of (0x24) HIGH_HYST depends on the selected g-range: it corresponds to 125mg in 2g-range (250mg in 4g-range, 500mg in 8g-range).

The high-g interrupt is generated if the absolute value of the acceleration data of at least one of the enabled axes ('or' relation) is higher than the threshold for at least the time defined by the (0x25) HIGH_DUR register. The interrupt is reset if the absolute value of the acceleration of all enabled axes ('and' relation) is lower than the threshold minus the hysteresis. The relation between the content of (0x25) HIGH_DUR and the actual delay of the interrupt generation is delay = [(0x25) HIGH_DUR+1]*2ms.

The interrupt status is stored in bit (0x09) HIGH_INT. The axis which triggered the interrupt is indicated by bits (0x0C) HIGH_FIRST_X, (0x0C) HIGH_FIRST_Y, and (0x0C) HIGH_FIRST_Z. The bit corresponding to the triggering axis contains a '1' while the other bits hold a '0'. These bits hold until new interrupt is triggered. The sign of the triggering acceleration is stored in bit (0x0C) HIGH_SIGN. If the (0x0C) HIGH_SIGN = '0' ('1'), the sign is positive (negative). This bit holds until new interrupt is triggered.

7.7 DRDY_INT

The width of the acceleration data is 10 bits, in two's complement representation. The data of each axis is split into 2 parts, the MSB part (one byte contains bit 11 to bit 4) and the LSB part (one byte contains bit 3 to bit 0). Reading data should start with LSB part. When user is reading the LSB byte of data, to ensure the integrity of the acceleration data, the content of MSB can be locked, by setting SHADOW_DIS (0x21<6>) to logic 0. This lock function can be disabled by setting SHADOW_DIS to logic 1. Without lock, the MSB and LSB content will be updated by new value immediately. The bit NEW_DATA in the LSB byte is the flag of the new data. If new data is updated, this NEW_DATA flag will be 1, and will be cleared when corresponding MSB or LSB is read by user. Also user should note that, even with SHADOW_DIS=0, the data of 3 axes are not guaranteed from the same time point. If user need all of the 3 axes data from the same time point, please use FIFO. Detailed information, user can refer to 6.8.

If SLEEP_DUR is set to be 0000, then the data can be filtered by low-pass filter, with bandwidth is set by BW (0x10<4:0>). If SLEEP_DUR is set to be other values, the data also can be averaged in different way (set by BW). In any conditions, the data stored in data registers are offset-compensated.

The device supports four different acceleration measurement ranges. The range is setting through RANGE (0x0F<3:0>), and the details as following:

	<u> </u>	
RANGE	Acceleration	Resolution
	range	
0001	2g	3.9mg/LSB
0010	4g	7.8mg/LSB
0100	8g	15.6mg/LSB
Others	Reserved	0.98mg/LSB

The interrupt for the new data serves for the synchronous data reading for the host. It is generated after storing a new value of z-axis acceleration data into data register. This interrupt will be cleared automatically when the next data conversion cycle starts, when SLEEP_DUR is not set to 0000b. When device is in full run (SLEEP_DUR=0000), the interrupt will be effective about 128us, and automatically cleared. The interrupt mode for the new data is fixed to be non-latched.

7.8 FIFO_INT

The device has integrated FIFO memory, capable of storing up to 32 frames, with each frame contains three 10 bits words, for acceleration data of x, y, and z axis. All of the 3 axes acceleration are sampled at same point in time line.

The FIFO can be configured as three modes, FIFO mode, STREAM mode, and BYPASS mode. FIFO mode.

In FIFO mode, the acceleration data of selected axes are stored in the buffer memory. If enabled, a watermark interrupt can be triggered when the buffer filled up to the defined level. The buffer will continuously be filled until the fill level reaches to 32. When the buffer is full, data collection stops, and the new data will be ignored. Also, FIFO FULL interrupt will be triggered when enabled.

STREAM mode

In STREAM mode, the acceleration data of selected axes will be stored into the buffer until the buffer is full. The buffer's depth is 31 now. When the buffer is full, data collection continues, and the oldest data is discarded. If enabled, a watermark interrupt will be triggered when the fill level reached to the defined level. Also, when buffer is full, FIFO_FULL interrupt will be triggered if enabled. If any old data is discarded, the FIFO_OR (0x0E<7>) will be set to be logic 1.

BYPASS mode

In BYPASS mode, only the current acceleration data of selected axes can be read out from the FIFO. The FIFO acts like the STREAM mode with a depth of 1. Compare to reading directly from data register, this mode has the advantage of ensuring the package of xyz data are from same point of time line. The data registers are updated sequentially and have chance for the xyz data sampled in different time. Also, if any old data is discarded, the FIFO_OR will be set to be logic 1, similar as that in stream mode.

The FIFO mode can be configured by setting FIFO_MODE (0x3E<7:6>).

FIFO_MODE	Mode
00	BYPASS
01	FIFO
10	STREAM
11	FIFO

User can select the acceleration data of which axes to be stored in the FIFO. This configuration can be done by setting FIFO_CH (0x3E<1:0>), where '00b' for x-, y-, and z-axis, '01b' for x-axis only, '10b' for y-axis only, '11b' for z-axis only.

If all the 3 axes data are selected, the format of data read from 0x3F is as follows

	XLSB	XMSB	YLSB	YMSB	ZLSB	ZMSB				
		,								
Tho	sa comprisa ona	frame								

I hese comprise one frame

If only one axis is enabled, the format of data read from 0x3F is as follows

YLSB YMSB

These comprise one frame

If the frame is not read completely, the remaining parts of the frame will be discarded.

If the FIFO is read beyond the FIFO fill level, all zeroes will be read out.

FIFO_FRAME_COUNTER (0x0E<6:0>) reflects the current fill level of the buffer. If additional data frames are written into the buffer when the FIFO is full (in Stream mode or Bypass mode), then, FIFO_OR (0x0E<7>) is set to 1. This FIFO_OR can be considered as flag of discarding old data.

When a write access to one of the FIFO configuration registers (0x3E) or (0x31) occurs, the FIFO buffer will be cleared, the FIFO fill level indication register FIFO_FRAME_COUNTER (0x0E<6:0>) will be cleared, and the FIFO_OR (0x0E<7>) will be cleared.

As mentioned, FIFO controller contains two interrupts, FIFO_FULL interrupt, and watermark interrupt. These two interrupts are functional in all the FIFO operating modes.

The watermark interrupt is triggered when the fill level of buffer reached to the level that is defined by register FIFO_WM_TRIGGER (0x31<5:0>), if the interrupt is enabled by setting INT_FWM_EN (0x17<6>) to logic 1 and INT1_FWM (0x1A<1>) or INT2_FWM (0x1A<6>) is set.

The FIFO_FULL interrupt is triggered when the buffer has been fully filled. In FIFO mode, the fill level is 32, and in STREAM mode the fill level is 31, in BYPASS mode the fill level is 1. To enable the FIFO_FULL interrupt, INT_FFULL (0x17<5>) should be set to 1, and INT1_FFULL (0x1A<2>) or INT2_FFULL (0x1A<7>) should be set to 1.

The status of watermark interrupt and fifo full interrupt can be read through INT_STAT (0x0A). After soft-reset, the watermark interrupt and FIFO full interrupt are disabled.

For the FIFO to recollect the data, user should reconfigure the register FIFO_MODE. (consult with app team)

7.9 Interrupt configuration

The device has the above 8 interrupt engines. Each of the interrupts can be enabled and configured independently. If the trigger condition of the enabled interrupt fulfilled, the corresponding interrupt status bit will be set to logic 1, and the mapped interrupt pin will be activated. The device has two interrupt PINs, INT1 and INT2. Each of the interrupts can be mapped to either PIN or both PINs.

The interrupt status registers update when a new data word is written into the data registers. If an interrupt is disabled, the related active interrupt status bit is disabled immediately.

The interrupt sequence is like the following

New data conversion, with or without filtering, judge the interrupt condition, new data written to data register, update interrupt status registers, trig associated interrupts, set mapped interrupt PINs, clear interrupts (depending on the interrupt mode), waiting for next data conversion.

Device supports 2 interrupt modes, non-latched, and latched mode. The interrupt modes are set through LATCH_INT (0x21<0>).

In non-latched mode, the interrupt status bit and the mapped interrupt pin are cleared as soon as the associated conditions are no more valid, or read operation to the INT_STAT (0x09~0x0b). Exceptions to this are the new data, orientation, and flat interrupts, which are automatically reset after a fixed time.

In latched mode, the clearings of the interrupt status and selected pin are determined by INT_RD_CLR (0x21<7>). If INT_RD_CLR=0, read operation to the INT_STAT will clear the interrupt and the selected pin. If INT_RD_CLR=1, any read operation to the device will clear the interrupt and the selected pin.

If the condition for trigging the interrupt still holds, the interrupt status will be set again with the next change of the data registers.

Mapping the interrupt pins can be set by INT_MAP (0x19~0x1B).

The electrical interrupt pins can be set INT_PIN_CONF (0x20<3:0>). The active logic level can be set to 1 or 0, and the interrupt pin can be set to open-drain or push-pull.

If the interrupt mode is configured as latched mode, the interrupt can also be cleared by I2C reading any of the interrupt status register (0x09 ~ 0x0c). (should confirm with application team, check 0x21<7>)

8 I²C COMMUNICATION PROTOCOL

8.1 I²C Timings

Below table and graph describe the I²C communication protocol times

Table 9. I2C Timings

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
SCL Clock	f _{scl}		0		400	kHz
SCL Low Period	t _{low}		1			μS
SCL High Period	t _{high}		1			μS
SDA Setup Time	t _{sudat}		0.1			μS
SDA Hold Time	t _{hddat}		0		0.9	μS
Start Hold Time	t _{hdsta}		0.6			μS
Start Setup Time	t _{susta}		0.6			μS
Stop Setup Time	t _{susto}		0.6			μS
New Transmission Time	t _{buf}		1.3			μS
Rise Time	t _r					μS
Fall Time	t _f					μS



Figure 12. I²C Timing Diagram

8.2 I²C R/W Operation

8.2.1 Abbreviation

Table 10. Abbreviation

SACK	Acknowledged by slave
MACK	Acknowledged by master
NACK	Not acknowledged by master
RW	Read/Write

8.2.2 Start/Stop/Ack

START: Data transmission begins with a high to transition on SDA while SCL is held high. Once I²C transmission starts, the bus is considered busy.

STOP: STOP condition is a low to high transition on SDA line while SCL is held high.

ACK: Each byte of data transferred must be acknowledged. The transmitter must release the SDA line during the acknowledge pulse while the receiver mush then pull the SDA line low so that it remains stable low during the high period of the acknowledge clock cycle.

NACK: If the receiver doesn't pull down the SDA line during the high period of the acknowledge clock cycle, it's recognized as NACK by the transmitter.

8.2.3 I²C Write

 I^2C write sequence begins with start condition generated by master followed by 7 bits slave address and a write bit (R/W=0). The slave sends an acknowledge bit (ACK=0) and releases the bus. The master sends the one byte register address. The slave again acknowledges the transmission and waits for 8 bits data which shall be written to the specified register address. After the slave acknowledges the data byte, the master generates a stop signal and terminates the writing protocol.

Table 11. I2C Write



8.2.4 I²C Read

 I^2C write sequence consists of a one-byte I^2C write phase followed by the I^2C read phase. A start condition must be generated between two phase. The I^2C write phase addresses the slave and sends the register address to be read. After slave acknowledges the transmission, the master generates again a start condition and sends the slave address together with a read bit (R/W=1). Then master releases the bus and waits for the data bytes to be read out from slave. After each data byte the master has to generate an acknowledge bit (ACK = 0) to enable further data transfer. A NACK from the master stops the data being transferred from the slave. The slave releases the bus so that the master can generate a STOP condition and terminate the transmission.

The register address is automatically incremented and more than one byte can be sequentially read out. Once a new data read transmission starts, the start address will be set to the register address specified in the current I^2C write command.

Table 12. I2C Read



9 REGISTERS

9.1 Register Map

The table below provides a list of the 8-bit registers embedded in the device and their respective function and addresses

Table 13. Register Map

Addr	Name	Description	B7	B6	B5	B4	B3	B2	B1	B0	Defa ult	R/ W
0x00	CHIP_ID	CHIP ID	For produ	For product version							0xB0	RW
0x01	DXL	LSB of X data	DX<1:0>							NEW_ DATA_ X	0x00	R

0x02	DXM	MSB of X	DX<9:2>								0x00	R	
0.00	DVI	data	DV (1)0		1	1			1		0.00	_	
0x03	DIL	LSB of Y	DY<1:0>							DATA_	0x00	R	
0.01	DVM		DV -0.25							Y	000	D	
0x04	DTM	MSB OF Y	D1<3.2>								000	ĸ	
0x05	DZL	LSB of Y	DZ<1:0>							NEW_	0x00	R	
0,00		data								DATA_	0,000	IX.	
0x06	DZM	MSB of Y	DZ<9:2>							2	0x00	R	
UNU U		data									0,000		
0x07	STEP_C	LSB	STEP_C	NT_LSB							0x00	RW	
0x08	NI	MSB	STEP_C	NT_MSB							0x00	RW	
0x09	INT_STA										0xFF	R	
0x0a	1		FOB_I	ORIEN	S_TAP	D_TAP	STEP_	STEP_	STEP_		0x00	R	
				1_1111				NT	ILAR				
0x0b				FIFO_ WM_I	FIFO_	DATA_	LOW_I	HIGH_			0x00	R	
				NT	INT								
0x0c			TAP_S IGN	TAP_F IRST	TAP_F IRST	TAP_F IRST	HIGH_ SIGN	HIGH_ FIRST	HIGH_ FIRST	HIGH_ FIRST	0x00	R	
	_			Z	Y	X		_Z	Y	_X			
0x0d			STEP_ CNT			FOB<1:0)>	ORIENT	<2:0>		0x00	R	
			OVFL										
0x0e	FIFO_ST AT		FIFO_ OR	FIFO_FF	RAME_COU	JNTER<6:0	>				0x00	R	
0x0f	RANGE						RANGE	<3:0>			0x00	RW	
0x10	BW				ODRH	BW<4:0>	>				0x00	RW	
0x11	POWER		MODE	DSLP	PRESET	<1:0>	SLEEP_	DUR<3:0>			0x00	RW	
0v12	STEP C		_BII STEP			STEP S	AMPLE CO	OUNT<4:0>			0×00	RW/	
0.12	ONF		STAR								0,00	1	
0x13	_		I STEP	STEP P	RECISION	<6:0>					0x00	RW/	
0,10											0,000		
0x14			STEP_T	ME_LOW	-						0x00	RW	
0x15			STEP_T						OTED	ł	0xFF	RW	
0x16			EN	T_EN	_EN	_EN	EN	QUIT_	UNSIM		0x00	RW	
								EN	ILAR_				
0x17				INT_F	INT_F	DATA_	LOW_	HIGH_	HIGH_	HIGH_	0x00	RW	
0, TT				WM_E	FULL_	EN	EN	EN_Z	EN_Y	EN_X	0,000		
0x18				INT_S	INT_S	INT_S					0x00	RW	
				RC_S	RC_D	RC_T							
0x19	INT_MAP		INT1_	INT1_	INT1_	INT1_	INT1_	INT1_	INT1_		0x00	RW	
UX I U			FOB	ORIEN T	S_TAP	D_TAP	STEP	STEP_	STEP_		0,000		
				1				QUIT	IL				
0x1A				INT1_	INT1_	INT1_	INT1_	INT1_			0x00	RW	
0x1B	_		INT2_	INT2_	INT2_	INT2_	INT2_	INT2_	INT2_		0x00	RW	
0/112			FOB	ORIEN T	S_TAP	D_TAP	STEP	STEP_	STEP_		ence e		
				I				QUII	IL				
0x1C				INT2_ FWM	INT2_ FFUU	INT2_ DATA	INT2_	INT2_ HIGH			0x00	RW	
0x1D					, I ULL	DAIA			1	ı	0x00	RW	
0x1E			PEAK_B	PEAK_B<5:0> STEP_MISMATC								RW	
			VALLEY	H_B<1:0>								D\//	
0x1F	INTPIN C	Interrupt DIM			1	1	INT2	INT2	INT1	INT1	0x00		
0,20	FG	configuration					OD	LVL	OD	LVL	0,000	1.1.1.1	
0x21	INT_CFG	Interrupt	INT_R	SHAD	INT_P	ł	<u> </u>	<u> </u>	ł	LATC	0x00	RW	
		configuration	D_CL R	OW_D	ULSE					H_INT			
0x22	LOW_HI		LOW_DU	JR	1	1	1	1	1	1	0x09	RW	
0x23	GH_G		LOW_TH	1							0x30	RW	
0x24	1		HIGH_H	YST<1:0				LOW_	LOW_H	/ST<1:0>	0x81	RW	
0.05	-		> MODE									DW	
0x25	-											KVV DVV	
0x20	OS CUS												
0x21	T			ST Y							0x00		
0x20	1		OS CUS	T_Z							0x00	R\//	
0x24	TAP		TAP.	TAP. S				TAP DU	R<2:0>		0x04	RW/	
	1		QUIET	HOCK	1	1	1	0	-		0.04	1.1.1	1

0x2B					TAP_TH	<4:0>			0x0A	RW
0x2C	4D6D		PL_Z_TH						0x00	RW
0x2D			UD_X_TH						0xA4	RW
0x2E			RL_Z_TH						0x00	RW
0x2F			RL_Y_TH						0xA4	RW
0x30			ORIEN FB_Z_T T_DB_ DIS	H<6:0>					0x00	RW
0x31	FIFO_WT MK	FIFO water mark level		FIFO_W	'TMK_LVL<	5:0>			0x00	RW
0x32	ST_CFG		SELFT EST_B IT		SELFT EST_A MP/EN _PK_V LY	SINGL E_EN_ STEP	SELFT ESET_ SIGN	SELFTEST_AXIS <1:0>	0x00	RW
0x33	NVM_CF G		UNLO CK_3F			NVM_ LOAD	NVM_ RDY	NVM_ PROG	0x04	RW
0x34			VALLEY_A<5:0>						0x00	RW
0x35			PEAK_A<5:0>					STEP_MISMATC H_A<1:0>	0x00	RW
0x36	SR	Soft reset	SOFT_RESET: 0x	36, NVM_U	NLOCK: 0xl	B3			0x00	RW
0x37	TRIM		OFFSET_X<10:8>		GAIN_Z∢	<9:8>	OFFSET	_Y<10:8>	NVM	RW
0x38			OFFSET_X<7:0>						NVM	RW
0x39			OFFSET_Y<7:0>						NVM	RW
0x3A			OFFSET_Z<7:0>						NVM	RW
0x3B			GAIN_X						NVM	RW
0x3C			GAIN_Y						NVM	RW
0x3D			GAIN_Z<7:0>						NVM	RW
0x3E	FIFO_CF G	FIFO	FIFO_MODE<1:0					FIFO_CH<1:0>	0x00	RW
0x3F	FIFO	FIFO register	FIFO_DATA	_ I	-				0x00	R

Register Definition 9.2

Product Discrete Bits Bits Bits Bits Bits Bits Bits Bits Bits RW Default is register is used to identify the device is register (0.01 - 0.02 (DXL, DXM) RV NEWDAT R 0.x00 K 10 Bits Bits Bits Bits Bits R 0.x00 K-d:2> 1 10bits acceleration data of x-channel. This data is in two's complement. R 0.x00 WDATA_X: 1. acceleration data of x-channel has been updated since last reading 0.acceleration data of x-channel has not been updated since last reading 0.acceleration data of y-channel. This data is in two's complement. R 0.x00 Y(*1:0> 1 Bits Bits Bits Bits Bits 0.x00 Y(*1:0> 1. acceleration data of y-channel has been updated since last reading 0.x00 0.x00 0.x00 Y(*1:0> 1. acceleration data of y-channel has been updated since last reading 0.x00 X/Y R 0.x00 Y(*1:0) 1. acceleration data of z-channel. This data is in two's complement. NEWDAT R										
evice ID RW is register is used to identify the device agister 0x01 - 0x02 (DXL, DXM) V Bit6 Bit3 Bit4 Bit3 Bit2 Bit1 Bit0 R/W Default K:10- A X R 0x00 A.X R 0x00 K:10- IObits acceleration data of x-channel has been updated since last reading 0, acceleration data of x-channel has been updated since last reading 0, acceleration data of x-channel has been updated since last reading 0, acceleration data of x-channel has been updated since last reading 0, acceleration data of y-channel has been updated since last reading 0, acceleration data of y-channel has not been updated since last reading 0, acceleration data of y-channel has not been updated since last reading 0, acceleration data of y-channel has not been updated since last reading 0, acceleration data of y-channel has not been updated since last reading 0, acceleration data of y-channel has not been updated since last reading 0, acceleration data of y-channel has not been updated since lared and y-channel. R 0x00 Y Isit6 Bit6 Bit4 Bit3 Bit2 Bit1 Bit0 R/W Default V scceleration data of y-channel has not been updated since	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
is register is used to identify the device agister 0x01 - 0x02 (DXL, DXM) Y X Bit6 Bit5 Bit	Device ID								RW	
BigIst Dx01 - 0x02 (DXL, DXM) Hit Bits <	This register	r is used to id	entify the devi	се						
IP Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 Bit0 R/W Default K<10-	Register 0x()1 ~ 0x02 (D>	(L, DXM)							
K<1:0> NEWDAT R 0x00 X<3:2> 10bits acceleration data of x-channel. This data is in two's complement. R 0x00 K: 10bits acceleration data of x-channel has been updated since last reading 0. acceleration data of x-channel has not been updated since last reading 0. acceleration data of x-channel has been updated since last reading egister 0x03 - 0x04 (DYL, DYM) If Bit6 Bit3 Bit2 Bit1 Bit0 R/W Default Y1:0> Iobits acceleration data of y-channel. This data is in two's complement. R 0x00 0x00 Y1:0> Iobits acceleration data of y-channel has been updated since last reading 0. acceleration data of y-channel has not been updated since last reading 0. acceleration data of x-channel has not been updated since last reading 0. acceleration data of x-channel has not been updated since last reading 0. acceleration data of x-channel. This data is in two's complement. R 0.000 Ze3-2 Iobits acceleration data of x-channel. This data is in two's complement. R 0.000 Ze3-2 Iobits acceleration data of x-channel. This data is in two's complement. R 0.000 Ze3-2 Iobits acceleration data of x-channel. This data is in two's complement. R 0.000 Ze1-2 Io	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
Xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx	DX<1:0>								R	0x00
King 10bits acceleration data of x-channel. This data is in two's complement. 17 1000 EWDATA_X: 1 acceleration data of x-channel has been updated since last reading 0, acceleration data of x-channel has not been updated since last reading 9 ggister 0x03 - 0x04 (DYL, DYM). Image: transmit in two's complement. NEWDAT R 0x00 Y<:1:0:-	DX<9.2>							A_A	R	0x00
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Z<9:2> I <td>231.02</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>A Z</td> <td></td> <td>0,00</td>	231.02							A Z		0,00
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TEP_INT: 1, step valid interrupt is active 0, step valid interrupt is inactive TEP_QUIT_INT: 1, step quit interrupt is active 0, step quit interrupt is inactive 0, step quit interrupt is inactive 0, step quit interrupt is active 0, step quit interrupt is inactive rEP_UNSIMILAR: 1, step unsimilar interrupt is active 0, step unsimilar interrupt is inactive agister 0x0b (INT_STAT1) t7 Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 Bit0 R/W Default t7 Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 Bit0 R/W Default tis register indicates interrupt status related to data ready, FIFO watermark, and FIFO full. Image: the status related to data ready, FIFO full. Terrupt full	OB_INT OB_INT: ORIENT_IN S_TAP_INT D_TAP_INT	Bito ORIENT_I NT 1 0 T: 1 : 1 0 : 1 0 : 1	Bit5 S_TAP_I NT , front-back im orient interru orient interru single tap int single tap int double tap in	D_TAP_I NT terrupt active pt active pt inactive errupt active errupt active terrupt active	BIT3 STEP_IN T e	STEP_Q UIT_INT	Bit1 STEP_UN SIMILAR	BitO	R/W R	Default 0x00
is tep valid interrupt is inactive TEP_QUIT_INT: 1, step quit interrupt is active 0, step quit interrupt is inactive TEP_UNSIMILAR: 1, step unsimilar interrupt is active 0, step unsimilar interrupt is inactive agister 0x0b (INT_STAT1) t7 Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 Bit0 R/W Default t7 Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 Bit0 R/W Default trip LI_INT T T NOV R 0x00 is register indicates interrupt status related to data ready, FIFO watermark, and FIFO full. Image: Status related to data ready in the status r	FOB_INT FOB_INT: DRIENT_IN S_TAP_INT D_TAP_INT	Bito ORIENT_I NT 1 0 T: 1 0 : 1 0 : 1 0	Bit5 S_TAP_I NT , front-back in , front-back in orient interru orient interru single tap int double tap in double tap in	DITAP_I NT terrupt active pt active pt inactive errupt active errupt active terrupt active terrupt inactive	BIT3 STEP_IN T e	STEP_Q UIT_INT	Bit1 STEP_UN SIMILAR	BitO	R/W R	Default 0x00
iter_goin_intri iter put interrupt is active 0, step quit interrupt is inactive iter_goin_intri it	OB_INT OB_INT: DRIENT_IN S_TAP_INT D_TAP_INT STEP_INT:	Bito ORIENT_I NT 1, 0, T: 1, 0; 1, 0; 1, 0; 1, 0; 1, 0; 1, 0, 1, 0, 1, 0, 1, 0, 1, 0, 1,	Bit5 S_TAP_I NT front-back in orient interru orient interru single tap int double tap int double tap in step valid int	DITAP_I NT terrupt active terrupt inactive pt inactive errupt active errupt active terrupt active terrupt inactive terrupt is active	BIT3 STEP_IN T e e	STEP_Q UIT_INT	Bit1 STEP_UN SIMILAR	BitO	R/W R	Default 0x00
TEP_UNSIMILAR: 1, step unsimilar interrupt is inactive 0, step unsimilar interrupt is active egister 0x0b (INT_STAT1) t7 Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 Bit0 R/W Default t7 Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 Bit0 R/W Default INT LL_INT T T NO00 R 0x00 is register indicates interrupt status related to data ready, FIFO watermark, and FIFO full. Image: Content of the status related to data ready. T T	OB_INT OB_INT: DRIENT_IN S_TAP_INT D_TAP_INT STEP_INT:	Bito ORIENT_I NT 1, 0, 1, 0, 1, 0, 1, 0, 1, 0, 1, 0, 1, 0, 1, 0, 1, 0, 1, 0, 1, 0, 1, 0, 1, 0, 1, 0, 1, 0, 1, 0, 1, 0, 1, 0, 1, 0, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1,	Bit5 S_TAP_I NT front-back in orient interru orient interru single tap int double tap in double tap in step valid int step valid int	DITAP_I NT terrupt active terrupt inactive pt inactive errupt active errupt active terrupt active terrupt inactive terrupt is active errupt is active	BIT3 STEP_IN T e e ve e ve e	STEP_Q UIT_INT	Bit1 STEP_UN SIMILAR	BitO	R/W R	Default 0x00
O, step unsimilar interrupt is inactive agister 0x0b (INT_STAT1) t7 Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 Bit0 R/W Default t7 Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 Bit0 R/W Default t7 Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 Bit0 R/W Default t1 FIFO_WM FIFO_FU DATA_IIN LOW_INT HIGH-INT R 0x00 is register indicates interrupt status related to data ready, FIFO watermark, and FIFO full. Status related to data ready. FIFO full.	FOB_INT FOB_INT: DRIENT_IN S_TAP_INT D_TAP_INT STEP_INT: STEP_QUIT	Bito ORIENT_I NT 1, T: 1, 0: 1,	Bit5 S_TAP_I NT , front-back in , front-back in , orient interru , orient interru , single tap int , single tap int , double tap in , double tap in , step valid int , step valid int , step quit inter , step quit inter	DITAP_I D_TAP_I NT terrupt active terrupt inactive pt inactive errupt active errupt active terrupt active terrupt active terrupt is active errupt is active rrupt is active rrupt is active	BIT3 STEP_IN T e e ve e ve	STEP_Q UIT_INT	Bit1 STEP_UN SIMILAR	BitO	R/W R	Default 0x00
egister 0x0b (INT_STAT1) t7 Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 Bit0 R/W Default FIFO_WM FIFO_FU DATA_IIN LOW_INT HIGH-INT R 0x00 _INT LL_INT T T I R R 0x00 is register indicates interrupt status related to data ready, FIFO watermark, and FIFO full.	OB_INT OB_INT: ORIENT_IN S_TAP_INT D_TAP_INT STEP_INT: STEP_QUIT STEP_UNS	Bito ORIENT_I NT 1, 0, T: 1, 0; 1, 0, 1, 0, 1, 0, 1, 0, 1, 0, 1, 0, 1, 0, 1, 0, 1, 0, 1, 0, 1, 0, 1, 0, <td>Bit5 S_TAP_I NT , front-back in , front-back in , orient interru , orient interru , single tap int , single tap int , double tap in , double tap in , step valid int , step valid int , step quit inte , step quit inte , step quit inte , step unsimila</td> <td>DIL4 D_TAP_I NT terrupt active terrupt inactive pt inactive errupt active errupt active terrupt active terrupt inactive terrupt is active errupt is inactive rrupt is inactive rrupt is inactive rrupt is inactive rrupt is inactive</td> <td>BIT3 STEP_IN T e e ve e ve active</td> <td>STEP_Q UIT_INT</td> <td>Bit1 STEP_UN SIMILAR</td> <td>BitO</td> <td>R/W R</td> <td>Default 0x00</td>	Bit5 S_TAP_I NT , front-back in , front-back in , orient interru , orient interru , single tap int , single tap int , double tap in , double tap in , step valid int , step valid int , step quit inte , step quit inte , step quit inte , step unsimila	DIL4 D_TAP_I NT terrupt active terrupt inactive pt inactive errupt active errupt active terrupt active terrupt inactive terrupt is active errupt is inactive rrupt is inactive rrupt is inactive rrupt is inactive rrupt is inactive	BIT3 STEP_IN T e e ve e ve active	STEP_Q UIT_INT	Bit1 STEP_UN SIMILAR	BitO	R/W R	Default 0x00
egister 0x0b (INT_STAT1) t7 Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 Bit0 R/W Default FIFO_WM FIFO_FU DATA_IIN LOW_INT HIGH-INT R 0x00 _INT LL_INT T T T N R 0x00 vis register indicates interrupt status related to data ready, FIFO watermark, and FIFO full. FIFO full. FIFO full. FIFO full.	FOB_INT FOB_INT: DRIENT_IN S_TAP_INT D_TAP_INT STEP_INT: STEP_UNS	Bito ORIENT_I NT 1 0 T: 1 0 : 1 0 : 1 0 : 1 0 : 0 : 0 : 0 IMILAR: 0	Bit5 S_TAP_I NT , front-back im , front-back in , orient interru , orient interru , single tap int , single tap int , double tap in , double tap in , step valid int , step valid int , step quit inte , step quit inte , step unsimila	DIL4 D_TAP_I NT terrupt active terrupt inactive pt inactive errupt active errupt active terrupt active terrupt inactive terrupt is active errupt is active errupt is inactive rrupt is inactive interrupt is a t interrupt is in	BIT3 STEP_IN T e e ve active inactive	STEP_Q UIT_INT	Bit1 STEP_UN SIMILAR	BitO	R/W R	Default 0x00
t7 Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 Bit0 R/W Default FIFO_WM FIFO_FU DATA_IIN LOW_INT HIGH-INT R 0x00 _INT LL_INT T T r R 0x00	FOB_INT FOB_INT: DRIENT_IN S_TAP_INT D_TAP_INT STEP_INT: STEP_UNS	Bito ORIENT_I NT 1 0 T: 1 0 : 1 0 : 1 0 : 1 0 : 0 : 0 : 0 IMILAR: 0	Bit5 S_TAP_I NT , front-back im , front-back in , orient interru , orient interru , single tap int , single tap int double tap in , step valid int , step valid int , step valid int , step quit inte , step unsimila , step unsimila	DIL4 D_TAP_I NT terrupt active terrupt inactive pt inactive errupt active errupt active errupt active terrupt inactive terrupt is active errupt is active errupt is active errupt is inactive rrupt is inactive rrupt is inactive rrupt is inactive is is inactive is inactive is is inactive is inact	e e e e ve e ve active inactive	STEP_Q UIT_INT	Bit1 STEP_UN SIMILAR	BitO	R/W R	Default 0x00
FIFO_WM FIFO_FU DATA_IIN LOW_INT HIGH-INT R 0x00 INT LL_INT T T VI	FOB_INT FOB_INT: DRIENT_IN S_TAP_INT D_TAP_INT STEP_INT: STEP_UNS Register 0x0	Bito ORIENT_I NT 1 0 T: 1 0 : 1 0 : 1 0 : 1 0 : 0 : 0 : 0 : 0 MILAR: 0 Db (INT_STAT	Bit5 S_TAP_I NT , front-back in , front-back in , orient interru , orient interru , single tap int , single tap int double tap in , step valid int , step valid int , step valid int , step quit inte , step unsimila , step unsimila , step unsimila	DIL4 D_TAP_I NT terrupt active terrupt inactive pt inactive errupt active errupt active errupt active terrupt is active terrupt is active errupt is active errupt is inactive rrupt is inactive rrupt is inactive rrupt is inactive rrupt is inactive interrupt is active interrupt is active	BIt3 STEP_IN T e e ve e ve active inactive	STEP_Q UIT_INT	Bit1 STEP_UN SIMILAR	BitO	R/W R	Default 0x00
INT LL_INT T T	TOB_INT TOB_INT: DRIENT_IN S_TAP_INT D_TAP_INT TEP_INT: STEP_UNS STEP_UNS Register 0x0 Sit7	Bito ORIENT_I NT 1 0 T: 1 0 T_INT: 1 0 IMILAR: 1 0b Db INT_STAT	Bit5 S_TAP_I NT , front-back im , front-back im , orient interru , orient interru , single tap int , single tap int , double tap in , double tap in , step valid int , step valid int , step quit inte , step quit inte , step unsimila , step unsimila , step unsimila	DIL4 D_TAP_I NT terrupt active terrupt inactive pt inactive errupt active errupt active errupt active terrupt is active errupt is active errupt is active errupt is active errupt is inactive rrupt is inactive in interrupt is a ar interrupt is in Bit4	BIt3 STEP_IN T e e ve e ve active inactive Bit3	Bit2	Bit1 STEP_UN SIMILAR Bit1	Bit0	R/W R R/W	Default 0x00 Default
his register indicates interrupt status related to data ready, FIFO watermark, and FIFO full.	OB_INT OB_INT: ORIENT_IN TAP_INT TAP_INT TEP_INT: TEP_UNS egister 0x0 it7	Bito ORIENT_I NT 1 0 T: 1 0 T: 1 0 T: 1 0 T: 1 0 T. 1 0 T_INT: 1 0 IMILAR: 1 0b FIFO_WM	Bit5 S_TAP_I NT , front-back in , front-back in , orient interru , orient interru , single tap int , single tap int , double tap in , double tap in , step valid int , step valid int , step quit inte , step quit inte , step unsimila , step unsimila , step Unsimila , step Unsimila	DIL4 D_TAP_I NT terrupt active terrupt inactive pt inactive errupt active errupt active errupt active terrupt is active errupt is active errupt is active errupt is active errupt is inactive ar interrupt is a at interrupt is a	BIt3 STEP_IN T e e ve e ive s ve active inactive Bit3 LOW_INT	Bit2 STEP_Q UIT_INT Bit2 HIGH-INT	Bit1 STEP_UN SIMILAR Bit1	BitO	R/W R R/W R	Default 0x00 Default 0x00
	OB_INT OB_INT: ORIENT_IN _TAP_INT _TAP_INT TEP_INT: TEP_UNS egister 0x0 it7	Bito ORIENT_I NT 1 0 T: 1 0 T: 1 0 : 1 0 : 1 0 : 1 0 : 0 : 0 IMILAR: 1 0b INT_STAT Bit6 FIFO_WM INT	Bit5 S_TAP_I NT , front-back in , front-back in , orient interru , orient interru , single tap int , single tap int , double tap in , double tap in , step valid int , step valid int , step quit inte , step quit inte , step unsimila , step unsimila , step Unsimila	DIL4 D_TAP_I NT terrupt active terrupt inactive pt inactive errupt active errupt active errupt active terrupt is active errupt is active errupt is active errupt is active errupt is active errupt is inactive ar interrupt is a minterrupt is a minterrupt is active ar interrupt is active ar interrupt is active ar interrupt is active DATA_IIN T T	Bit3 STEP_IN T e e ve e ive e ve active inactive Bit3 LOW_INT	Bit2 STEP_Q UIT_INT Bit2 HIGH-INT	Bit1 STEP_UN SIMILAR Bit1	BitO	R/W R R/W R	Default 0x00 Default 0x00
	OB_INT OB_INT: IRIENT_IN TAP_INT TAP_INT TEP_INT: TEP_UNS egister 0x0 it7 his register	Bito ORIENT_I NT 1 0 T: 1 0 T_INT: 0 IMILAR: 0 Db (INT_STAT Bit6 FIFO_WM INT	Bit5 S_TAP_I NT , front-back in , front-back in , orient interru , orient interru , single tap int , single tap int , double tap in , step valid int , step valid int , step valid int , step unsimila , step Unsimila	DIL4 D_TAP_I NT terrupt active terrupt inactive pt inactive errupt active errupt active errupt active terrupt is active errupt is active errupt is active errupt is inactive errupt is inactive errupt is inactive ar interrupt is a at interrupt is a Bit4 DATA_IIN T T elated to data	Bit3 STEP_IN T e e ve active inactive Bit3 LOW_INT a ready, FIFO	Bit2 STEP_Q UIT_INT Bit2 HIGH-INT watermark, an	Bit1 STEP_UN SIMILAR Bit1 d FIFO full.	BitO	R/W R R/W R	Default 0x00 Default 0x00

- 1, FIFO full interrupt active
- 0, FIFO full interrupt inactive
- DATA_INT: 1, data ready interrupt active
 - 0, data ready interrupt inactive

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LOW_INT:	1, low-g interrupt active
	0, low-g interrupt inactive
HIGH_INT:	 high-g interrupt active
	0, high-g interrupt inactive

Register 0x0c (INT_STAT2)

		··,							
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
TAP_SIG	TAP_FIR	TAP_FIR	TAP_FIR	HIGH_SI	HIGH_FI	HIGH_FI	HIGH_FI	R	0x00
Ν	ST_Z	ST_Y	ST_X	GN	RST_Z	RST_Y	RST_X		
TAP_SIGN:		1, sign of tap tr	iggering is ne	gative					
		0, sign of tap tr	iggering signa	al is positive					
TAP_FIRST	Г_Z:	1, tap interrupt	is triggered b	y Z axis					
		0, tap interrupt	is not triggere	ed by Z axis					
TAP_FIRST	Г_Ү:	1, tap interrupt	is triggered b	y Y axis					
		0, tap interrupt	is not triggere	ed by Y axis					
TAP_FIRST	Г_Х:	1, tap interrupt	is triggered b	y X axis					
		0, tap interrupt	is not triggere	ed by X axis					
HIGH_SIGN	N:	1, sign of high-	g triggering si	ignal is negati	ve				
		0, sign of high-	g triggering si	ignal is positiv	e				
HIGH_FIRS	ST_Z:	1, high-g interr	upt is triggere	d by Z axis					
		0, high-g interr	upt is not trigg	gered by Z axi	S				
HIGH_FIRS	ST_Y:	1, high-g interr	upt is triggere	d by Y axis					
		0, high-g interr	upt is not trigg	gered by Y axi	S				
HIGH_FIRS	ST_X:	1, high-g interr	upt is triggere	d by X axis					
		0, high-g interr	upt is not trigg	gered by X axi	S				

Register 0x0d (INT_STAT3)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_CN			FOB<1:0>		ORIENT<2:0	0>		R	0x00
T_OVFL									
0755 0117									
STEP_CNI	_OVFL:	1, step counter	is over-flowed						
		0, step counter	is not over-flo	owed					
FOB<1.0>		00 device is in	unknown orie	entation					
1000		01, device is in	front orientati	on					
		10, device is in	back orientat	ion					
		11, reserved							
ORIENT<2:	0>:	000, device is i	n unknown ori	ientation					
		001, device is i	n left orientati	on					
		010, device is i	n right orienta	tion					
		011, reserved	0						
		100, reserved							
		101, device is i	n down orient	ation					
		110. device is i	n up orientatio	on					
		111. reserved							
		,							

Register 0x0e (FIFO_STATE)

		=/							
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
FIFO_OR	FIFO_FRAM	AE_COUNT<	6:0>					R	0x00
		FIED							

FIFO_OR: 1, FIFO over run occurred

0, FIFO over run not occurred

FIFO_FRAME_COUNT<6:0>:

Fill level of FIFO buffer. An empty FIFO corresponds to 0x00. The frame counter can be cleared by reading out all of the frames, or by writing register 0x3e (FIFO_CFG1) or 0x31.

Register 0x0f (RANGE)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
				RANGE<3:0)>			RW	0x00
RANGE<3:0)>: se	et the full scale	e of the accele	erometer. Sett	ting as followi	ng			

RANGE<3:0>	Acceleration range	Resolution
0001	2g	3.9mg/LSB
0010	4g	7.8mg/LSB
0100	8g	15.6mg/LSB
Others	Reserved	0.98mg/LSB

Register 0x10 (BW)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
		ODRH	BW<4:0>					RW	0x00
	1	higher output	data rata	$D = 4 \times E = D M$					

JURII.	i, nigher output uata rate	, ODK = 4 T	
	0. lower output data rate.	ODR = 2*F	BW

BW<4:0>: bandwidth setting, as following

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BW<4:0>	F_BW (Bandwidth)	ODR (0x10<5>=0)	ODR (0x10<5>=1)
xx000	3.9Hz	7.8Hz	15.6Hz
xx001	7.8Hz	15.6Hz	31.2Hz
xx010	15.6Hz	31.2Hz	62.5Hz
xx011	31.2Hz	62.5Hz	125Hz
xx100	62.5Hz	125Hz	250Hz
xx101	125Hz	250Hz	500Hz
xx110	250Hz	500Hz	1000Hz
xx111	500Hz	1000Hz	2000Hz

Even if unfiltered data is used, the ODR is still set by BW value.

Register 0x11 (POWER)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
MODE BI	DSLP	PRESET<1:	0>	SLEEP D	JR<3:0>	2.11	2.10	RW	0x00
Τ			•						
MODE_BIT:		1, set device in	to active mo	de					
		0, set device in	to standby r	node					
DSLP:		1, enable deep	sleep. This	action can low	er down the p	ower consi	umption more		
		0, disable deep	sleep						
PRESET<1:	:0>:	Preset time set	ting. The pr	eset time is res	served for CIC	; filter in dig	ital		
		11, Tpreset=20	48us						
		10, Tpreset=76	8us						
		01, Tpreset=96	us						
	D. 0.0	00, 1preset=12	US 						
SLEEP_DU	R<3:0>:	Set the sleep til	ne, when a	evice is in pow	er cycling pol	ver saving.	-		
		SLEEP_DU	JR<3:0>	Siee	o time i si	6			
		0000		NO P	ower cycling /	tuli speed			
		0001~0101		0.5m	S				
		0110		1ms					
		0111		2ms			_		
		1000		4ms					
		1001		6mS			2		
		1010		10m	5				
		1011		25m	6				
		1100		50m	3				
		1101		100n	ıS				
		1110		500n	าร				
		1111		1s					

Register 0x12 (STEP CONF0)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_ST			STEP_SAM	PLE_COUNT	<4:0>			RW	0x0C
ART									

STEP_START: start step counter, this bit should be set when using step counter

STEP_SAMPLE_COUNT<4:0>:

sample count setting for dynamic threshold calculation. The actual value is STEP_SAMPLE_COUNT<4:0>*4, default is 0xC, 48 sample count

Register 0x13 (STEP_CONF1)

<u> </u>									
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_CL	STEP_PRE	CISION<6:0>						RW	0x00
R									

STEP_CLR: clear step count in register 0x7 and 0x8

STEP_PRECISION<6:0>:

threshold for acceleration change of two successive sample which is used to update sample_new register in step counter, the actual g value is TEP_PRECISION<6:0>*3.9mg

Register 0x14 (STEP_CONF2)

i i giotto i di		/							
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_TIME	LOW							RW	0x00

STEP_TIME_LOW: the short time window for a valid step, the actual time is STEP_TIME_LOW<7:0>*ODR

Register 0x15 (STEP_CONF3)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_TIME	E_UP							RW	0x00
OTED TIME	- LID- +ia	ma window for	auitting aton	counter the c	otual tima ia	OTED TI		*0*ODD	

STEP_TIME_UP: time window for quitting step counter, the actual time is STEP_TIME_UP<7:0>*8*ODR

Register 0x16 (INT_EN0)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
FOB_EN	ORIENT_ EN	S_TAP_E N	D_TAP_E N	STEP_EN	STEP_Q UIT_EN	STEP_UN SIMILAR_ EN		RW	0x00

1, enable front-and-back orientation interrupt
0, disable front-and-back orientation interrupt
1, enable 4D orientation interrupt
0, disable 4D orientation interrupt
1, enable single tap interrupt
0, disable single tap interrupt
1, enable double tap interrupt
0, disable double tap interrupt
1, enable step valid interrupt
0, disable step valid interrupt
1, enable step quit interrupt
0, disable step quit interrupt
N:
1, enable step unsimilar interrupt
0, disable step unsimilar interrupt

Register 0x17 (INT_EN1)

	1 0	, enable step , disable step	unsimilar inter unsimilar inte	rupt rrupt						
Register 0x1	17 (INT_EN1))								
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default	
	INT_FWM	INT_FFU	DATA_EN	LOW_EN	HIGH_EN	HIGH_EN	HIGH_EN	RW	0x00	
	_EN	LL_EN			_Z	_Y	_X			
INT_FWM_B	EN: 1	, enable FIFO	watermark in	terrupt						
	0	, disable FIFO	watermark ir	nterrupt						
INT_FFULL	_EN: 1	, enable FIFO	full interrupt							
	0	, disable FIFO	full interrupt							
DATA_EN:	1	, enable data	ready interrup	ot						
	0	, disable data	ready interrup	ot						
LOW_EN:	1	, enable low-g	interrupt							
	0	, disable low-g	g interrupt							
HIGH_EN_2	<u> </u>	, enable high-	g interrupt on							
	0	, disable high-	g interrupt on	Z axis						
HIGH_EN_1	r: 1	, enable high-	g interrupt on	Y axis						
	() ()	, disable nign-	g interrupt on	Y axis						
HIGH_EN_/	K: 1	, enable high-	g interrupt on	X axis						
	0	, uisable nigh-	g menupi on	~ axis						

Register 0x18 (INT_SRC)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
	INT_SRC	INT_SRC	INT_SRC	Ý.				RW	0x00
	_STEP	_DATA	_TAP						
INT_SRC_STEP: 1, select unfiltered data for step counter									
0, select filtered data for step counter									
INT_SRC_E	DATA: 1	, select unfilte	red data for n	ew data interr	rupt and FIFO				
	0	, select filtered	d data for new	data interrup	t and FIFO				
INT_SRC_TAP: 1, select unfiltered data for TAP interrupt									
0, select filtered data for TAP interrupt									

Register 0x19 (INT_MAP0)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
INT1_FO	INT1_ORI	INT1_S_T	INT1_D_T	INT1_ST	INT1_ST	INT1_ST		RW	0x00
В	ENT	AP	AP	EP	EP_QUIT	EP_UNSI			
						MILAR			
INT1_FOB:	1,	map FOB int	errupt to INT1	pin					
	0,	not map FOE	3 interrupt to I	NT1 pin					
INT1_ORIENT: 1, map ORIENT interrupt to INT1 pin									
0, not map ORIEN			ENT interrupt	to INT1 pin					
INIT1 S TAP 1 man single to			n interrunt to	INIT1 nin					

INT1_S_TAP:	1, map single tap interrupt to INT1 pin
	0, not map single tap interrupt to INT1 pin
INT1_D_TAP:	1, map double tap interrupt to INT1 pin
	0, not map double tap interrupt to INT1 pin
INT1_STEP:	1, map step valid interrupt to INT1 pin
	0, not map step valid interrupt to INT1 pin
INT1_STEP_QUIT:	1, map step quit interrupt to INT1 pin
	0, not map step quit interrupt to INT1 pin
INITA OTED LINIONAL	

INT1_STEP_UNSIMILAR:

1, map step unsimilar interrupt to INT1 pin 0, not map step unsimilar interrupt to INT1 pin

Register 0x1a (INT_MAP1)

		.)							
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
	INT1_FW	INT1_FF	INT1_DA	INT1_LO	INT1_HIG			RW	0x00
	Μ	ULL	TA	W	Hs				

INT1_FWM:	1,	map FIFO wa	atermark inter	rupt to INT1 p	oin T1 pip			
INT1_FFULI	L: 1,	map FIFO fu	ll interrupt to I	NT1 pin	прп			
INT1 DATA	0, : 1,	not map FIF(map data rea	D full interrupt ady interrupt to	to INT1 pin INT1 pin				
	0,	0, not map data ready interrupt to INT1 pin						
INT1_LOW:	1, 0.	map low-g in not map low-	a interrupt to IN I	1 pın INT1 pin				
INT1_HIGH:	1,	map high-g i	nterrupt to INT	Γ1 pin				
Register 0x1	0, B (INT MAP	not map high 2)	i-g interrupt to	INT1 pin				
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1		

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default			
INT2_FO	INT2_ORI	INT2_S_T	INT2_D_T	INT2_ST	INT2_ST	INT2_ST		RW	0x00			
В	ENT	AP	AP	EP	EP_QUIT	EP_UNSI						
						MILAR						
INT2_FOB: 1, map FOB interrupt to INT2 pin												
	0	, not map FOE	3 interrupt to I	NT2 pin								
INT2_ORIE	NT: 1	, map ORIEN⊺	T interrupt to I	NT2 pin								
	0, not map ORIENT interrupt to INT2 pin											
INT2_S_TA	.P: 1	, map single ta	ap interrupt to	INT2 pin								
	0	, not map sing	le tap interrup	ot to INT2 pin								
INT2_D_TA	P: 1	, map double t	tap interrupt to	o INT2 pin								
	0	, not map dou	ble tap interru	pt to INT2 pin	1							
INT2_STEP	P: 1,	map step val	id interrupt to	INT2 pin								
	0	, not map step	valid interrup	ot to INT2 pin								
INT2_STEP	P_QUIT: 1	, map step qui	it interrupt to I	NT2 pin								
	0	, not map step	o quit interrupt	to INT2 pin								
INT2_STEP	P_UNSIMILAR	2:										

1, map step unsimilar interrupt to INT2 pin 0, not map step unsimilar interrupt to INT2 pin

Register 0x1c (INT_MAP3)

		- /							
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
	INT2_FW	INT2_FUL	INT2_DA	INT1_ST	INT2_LO	INT2_HIG		RW	0x00
	Μ	L	TA	EP	W	H			
INT2_FWM:	1,	map FIFO wa	atermark inter	rupt to INT2 p	bin		*		
	0,	not map FIFO	D watermark i	nterrupt to IN	T2 pin				
INT2_FULL:	: 1,	map FIFO fu	Il interrupt to I	NT2 pin					
	0,	not map FIFO	D full interrupt	to INT2 pin					
INT2_DATA	.: 1,	map data rea	ady interrupt to	o INT2 pin					
	0,	not map data	ready interru	pt to INT2 pin					
INT2_LOW:	1,	map low-g	interrupt to IN	T2 pin					
	0,	not map low-	g interrupt to	o INT2 pin					
INT2_HIGH	: 1,	map high-g	interrupt to IN	VT2 pin					
	0,	not map high	-g interrupt	to INT2 pin					
			-						

Register	0x1e	(VALL	FY	B)

t

riegieter en									
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
VALLEY_B<	<5:0>							RW	0x00
	5.0								

valley value of one axis which is used for step valley match VALLEY_B<5:0>:

Register 0x1f (PEAK_B)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
PEAK_B<5:	0>					STEP_MISN 1:0>	/ATCH_B<	RW	0x00
DEAK D.C.	0	a alu u alu a af a	والمأوانين مأريتم ومور	in up and fam at	معمم بالمماد	L-			

PEAK_B<5:0>: peak value of one axis which is used for step peak match

STEP_MISMATCH_B<1:0>:

- precision for step peak and valley match 00, match VALLEY_B<5:1> and PEAK_B<5:1>
- 01, match VALLEY_B<5:2> and PEAK_B<5:2>
- 10, match VALLEY_B<5:3> and PEAK_B<5:3> 11, match VALLEY_B<5:4> and PEAK_B<5:4>

Register 0x20 (INTPIN_CFG)
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<u> </u>									
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
				INT2_OD	INT2_LVL	INT1_OD	INT1_LVL	RW	0x05
INT2_OD:	1,	open-drain fo	or INT2 pin						

1, open-drain for INT2 pin 0, push-pull for INT2 pin

INT2_LVL:

1, logic high as active level for INT2 pin

0, logic low as active level for INT2 pin

INT1_OD:

INT1_LVL:

- 1, open-drain for INT1 pin 0, push-pull for INT1 pin 1, logic high as active level for INT1 pin 0, logic low as active level for INT1 pin

Register 0x21 (INT_CFG)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default	
INT_RD_	SHADOW	INT_PUL					LATCH_I	RW	0x00	
	_DIS	SE	ntormunto la l-	tobod model.	when any rate	d operation (-	NT this device			
INT_RD_CL	.R: 1, 0, n(, clear all the i , clear all the i on-latched-mo	nterrupts in la nterrupts, only ode	y when read t	when any rea he register IN	d operation to T_STAT (0x0)	A~0x0B), no r	matter the inte	rrupts in latch	ed-mode, or in
SHADOW_[DIS: 1,	disable the s	hadowing fun	ction for the a	cceleration da	ata				
	0, lo T	, enable the sl cked, when c bo MSR will b	hadowing fund orresponding	ction for the a LSB of the da	cceleration da ita is reading.	ta. When sha This can ensi	dowing is ena ure the integri	abled, the MSE ty of the accel	B of the accele eration data c	eration data is luring the reading
INT PULSE	: 1.	data ready ir	terrupt is kep	t until next co	nversion starts	s, in power cy	cling			
	0,	pulse of data	ready interru	pt is fixed to b	be 128us	-, , ,	5			
LATCH_INT	: 1, 0,	interrupt is in interrupt is in	i latch mode i non-latch mo	ode						
Register 0x2	22 (LOW_HIG	H_G_0)								l
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default	
LOW_DUR	10	w-a interrunt	triagered dela	v the actual t	ime is (LOW)*2ms: the de	ERVV	0x09 me is 20ms	
LOW_DOK.	10	w-g interrupt	linggereu uela	y, the actual t		001(<1.02+1) zhis, the de	lault delay ti	1110 13 201113	
Register 0x2	23 (LOW_HIG	6H_G_1)								
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default	
LOW_TH		u a intorrunt i	thraphald tha	actual a valu		1.7.0.)*7.0m	ay the default i	RW	0x30	
LOW_IH:	10	w-g interrupt	uneshold, the	actual g valu		i<≀.∪>)″≀.୪m(y, the default	value is 375m	y	
Register 0x2	24 (LOW HIG	6H_G_2)						/		
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default	
HIGH_HYS	T<1:0>				LOW_MO	LOW_HYST	T<1:0>	RW	0x81	
	T 1.0	veteresis of hi	ala a interneta		DE)*405			*0 <u>50</u>
HIGH_HYS	I<1:0>: n	ysteresis of hi	gn-g interrupt	, the actual g	value is (HIG	H_HYSI<1:0	i>)~125mg(2g	range), (HIGF	HYSI<1:0>	•)*250mg
	[4 F· Io	w-a interrunt	mode 0. sina	le-axis mode	1: sum mode					
LOW HYST		vsteresis of lo	w-a interrupt .	the actual a	value is (LOW	HYST<1:0>)*125ma. inde	ependent of th	e selected a r	ange
2011_11101	S1.02. 11		n g inton upt ;	the dotadi g			, 120mg, mac		e colocica g i	ango
Register 0x2	25 (LOW_HIG	6H_G_3)								
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default	
HIGH_DUR								RW	0x0F	
HIGH_DUR:	: hi	gh-g interrupt	triggered del	ay, the actual	time is (HIGH	I_DUR<7:0>+	1)*2ms; the d	efault delay	time is 32ms	
Pogistor 0v										
Register 02	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default	l
HIGH TH	Bito	Dito	Bitt	Bito	BILL	Bitt	Bito	RW	0xC0	
HIGH TH:	hi	ah-a interrupt	threshold, the	e actual q valu	ue is (HIGH T		ng(2g range),	(HIGH TH<7	:0>)*15.6mg(4	lg range).
	(H	IGH_TH<7:0	>)*31.2mg(8g	range)	·	, ,	5.5 5-7		,	
Register 0x2	27 (OS_CUST	_X)	Ditt	D:10	Dito	Ditt	Dite	DAA	Defends	I
Bit/	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default	
	X X· of	feet calibratio	n of X avis for	rusar tha I SI	B depends on	full-scale of t	he device whi	Chis 3 9mg in	0000	and in 4d range
05_0031_		5.6mg in 8g rs	nde			iuii-scaie UI l		on is starting If	i ∠y ianye, 7.0	ang in 4 g range,
Register 0x2	28 (OS_CUST	[_Y]								
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default	
OS_CUST_	Y							RW	0x00	
OS_CUST_	Y: of	fset calibratio	n of Y axis for	r user, the LSI	B depends on	full-scale of t	he device whi	ch is 3.9mg in	2g range, 7.8	3mg in 4g range,
	1	5.6mg in 8g ra	ange							
Register Ov		7)								
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default	l
OS CUST	Z			2.0	2.12		2.00	RW	0x00	
OS_CUST	Z: of	fset calibratio	n of Z axis for	user, the LSI	B depends on	full-scale of t	he device whi	ch is 3.9ma in	2g range, 7.8	3mg in 4g range.
	1	5.6mg in 8g ra	ange	,0					J J-, I	J JJo,
_			-							
Register 0x2	2a (TAP_CON	IFO)								I
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default	
IAP_QUI	TAP_SH				IAP_DUR<	2:0>		RW	0x04	
			1.30ma 0.00)me	I			1	I	l
TAP SHOC	. ta K: t≏	ip quiet time, " ip shock time	1:50ms 0.7	/ms						
	oration			0110						
war oorp	JUIALIUII									

TAP_DUR<2:0>:

the time window of the second tap event for double tap

TAP_DUR<2:0>	Duration of TAP_DUR
000	50ms
001	100ms
010	150ms
011	200ms
100	250ms
101	375ms
110	500ms
111	700ms

eaister 0x2	2b (TAP C								
it7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
			TAP_TH<4:	0>				RW	0x00
AP_TH<4:(0>:	threshold of sin TAP_TH<4:0>*	igle/double ta 250mg(8g rai	p interrupt, the nge)	e actual g val	ue is TAP_TH	l<4:0>*62.5mg	g (2g range)	, TAP_TH<4:0>*125mg(4g r
egister 0x2	2c (4D6D_	CONF0)							
t7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
D_Z_TH								RW	0x00
D_Z_1H:		Up/down z axis	s threshold, th	e actual g vali	ue is UD_Z_1	H<7:0>*3.91	mg+0.1g, inde	pendent of	the selected g range
egister 0x2	2d (4D6D_	CONF1)	_	-		_			
t7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
<u>)_X_IH</u>			thrachold th			5LL -7:0: *2.01	ma independe	RW	UXA4
J_A_IN.		the default valu	ie is 0.64g, co	e actual g val	o 40 degree	11<1.0> 3.91	ing, independe		necieu y range,
gister 0x2	2e (4D6D_	CONF2)	D'4	Dia	D:40		Dite	DAM	
7 11	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
Z_IH 7 тш.		Pight/loft z ovic	thrachold th			U ~ 7.0 + 2 01r	ng 0 1g indo	RVV	0x00
		Righthen 2 axis	s unesnoia, un	e actual y van		11<7.02 3.911	ng+0. rg, inde		ne selected y lange
gister 0x2	2f (4D6D_0	CONF3)	-				-		
t7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
<u>Y_TH</u>								RW	0xA4
_Y_IH:		the default valu	ie is 0.64g, co	e actual g van prresponding t	to 40 degree	H<7:0>"3.911	ng, independ	dent of the s	selected g range,
gister ux3	30 (4D6D_	CONF4)	Bit/	Bit2	Bit2	Bi+1	BitO	D/\//	Dofault
			DII4	DILO	DILZ	DILI	ЫЮ		
	10_2_11	1<0.0>						1	0,000
	B_DIS:	1: disable orien	t denounce ti	me					
B_Z_TH<6	B_DIS: 3:0>:	1: disable orien 0: enable orien Front/back z ax	nt denounce ti t denounce tir kis threshold, t	me ne the actual g va	alue is FB_Z_	_TH<7:0>*3.9	1mg+0.1g, ind	ependent o	f the selected g range
B_Z_TH<6	3_DIS: 5:0>: 31 (FIFO_V	1: disable orien 0: enable orien Front/back z ax VTMK)	t denounce ti t denounce tir kis threshold, t	me ne the actual g va	alue is FB_Z_	_TH<7:0>*3.9	1mg+0.1g, ind	ependent o	f the selected g range
B_Z_TH<6	3_DIS: 5:0>: 31 (FIFO_V Bit6	1: disable orien 0: enable orien Front/back z ax VTMK) Bit5	t denounce ti t denounce tir kis threshold, t Bit4 K I VI <5:0>	me ne the actual g va Bit3	alue is FB_Z_ Bit2	_TH<7:0>*3.9 Bit1	1mg+0.1g, ind Bit0	ependent o	f the selected g range
B_Z_TH<6 egister 0x3 t7 FO_WTMI	3_DIS: 5:0>: 31 (FIFO_V Bit6 K_LVL<5:(1: disable orien 0: enable orien Front/back z ax VTMK) Bit5 FIFO_WTM D>:	t denounce tir t denounce tir tis threshold, t Bit4 K_LVL<5:0>	me ne the actual g va Bit3	alue is FB_Z_ Bit2	_TH<7:0>*3.9 Bit1	1mg+0.1g, ind	ependent o	f the selected g range Default 0x00
A Constant Sector Secto	3_DIS: 31 (FIFO_V <u>Bit6</u> K_LVL<5:(32 (ST_CC	1: disable orien 0: enable orien Front/back z ax VTMK) Bit5 FIFO_WTM bit5 FIFO_WTMK_I DNF) Diff	t denounce tir t denounce tir tis threshold, t Bit4 K_LVL<5:0> vater mark lev _VL<5:0>. Wh	me ne the actual g va Bit3 el. Interrupt w en the value	alue is FB_Z_ Bit2 ill be generat of this registe	_TH<7:0>*3.9 Bit1 ed, when the er is changed,	1mg+0.1g, ind Bit0 number of ent the FIFO_FR/	Pependent o	f the selected g range Default 0x00 IFO exceeds NTER is reset to 0.
Egister 0x3	3_DIS: 31 (FIFO_V Bit6 K_LVL<5:(32 (ST_CC Bit6	1: disable orien 0: enable orien Front/back z ax VTMK) Bit5 FIFO_WTM bit5 defines FIFO w FIFO_WTMK_I PNF) Bit5	t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir bit4 K_LVL<5:0> vater mark lev _VL<5:0>. Wh Bit4	me ne the actual g va Bit3 el. Interrupt w en the value Bit3	alue is FB_Z_ Bit2 ill be generat of this register	_TH<7:0>*3.9 Bit1 ed, when the er is changed, Bit1	1mg+0.1g, ind Bit0 number of ent the FIFO_FR/	ependent o R/W RW ries in the F AME_COUN	f the selected g range Default 0x00 IFO exceeds NTER is reset to 0. Default 0x00
ELETES	3_DIS: 31 (FIFO_V <u>Bit6</u> K_LVL<5:(32 (ST_CC <u>Bit6</u>	1: disable orien 0: enable orien Front/back z ax VTMK) Bit5 FIFO_WTM bit5 defines FIFO w FIFO_WTMK_I NF) Bit5 Bit5	t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir bit4 K_LVL<5:0> vater mark lev _VL<5:0>. Where the terms _VL<5:0>. Where terms _T_AMP/F	me ne the actual g va Bit3 el. Interrupt w hen the value Bit3 SingleEn_ Sten	alue is FB_Z_ Bit2 ill be generat of this register Bit2 SELFTES T_SIGN	_TH<7:0>*3.9 Bit1 ed, when the er is changed, Bit1 SELFTEST	1mg+0.1g, ind Bit0 number of ent the FIFO_FR/ Bit0 AXIS<1:0>	ependent o R/W RW ries in the F AME_COUN R/W RW	f the selected g range Default 0x00 IFO exceeds NTER is reset to 0. Default 0x00
FO_WTMI	3_DIS: 31 (FIFO_V <u>Bit6</u> K_LVL<5:(32 (ST_CC <u>Bit6</u>	1: disable orien 0: enable orien Front/back z ax VTMK) Bit5 FIFO_WTM bit5 defines FIFO w FIFO_WTMK_I NF) Bit5 Bit5	t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir Bit4 K_LVL<5:0> VL<5:0>. Wr SELFTES T_AMP/E n Peak V	me ne the actual g va Bit3 el. Interrupt w hen the value Bit3 SingleEn_ Step	alue is FB_Z_ Bit2 ill be generat of this registe Bit2 SELFTES T_SIGN	_TH<7:0>*3.9 Bit1 ed, when the er is changed, Bit1 SELFTEST	1mg+0.1g, ind Bit0 number of ent the FIFO_FR/ Bit0 _AXIS<1:0>	ependent o R/W RW ries in the F AME_COUN R/W RW	f the selected g range Default 0x00 IFO exceeds NTER is reset to 0. Default 0x00
G_Z_TH<6 gister 0x3 7 FO_WTMI gister 0x3 7 ELFTES BIT	3_DIS: 31 (FIFO_V <u>Bit6</u> K_LVL<5:(32 (ST_CC <u>Bit6</u>	1: disable orien 0: enable orien Front/back z ax VTMK) Bit5 FIFO_WTM >: defines FIFO w FIFO_WTMK_I NF) Bit5	t denounce tir t denounce t denounce tir t denounce t denounce tir t denounce t denounce tir t denounce t denounce	me ne the actual g va Bit3 el. Interrupt w hen the value Bit3 SingleEn_ Step	alue is FB_Z_ Bit2 ill be generat of this registe Bit2 SELFTES T_SIGN	_TH<7:0>*3.9 Bit1 ed, when the er is changed, Bit1 SELFTEST	1mg+0.1g, ind Bit0 number of ent the FIFO_FR/ Bit0 _AXIS<1:0>	ependent o R/W RW ries in the F AME_COUN R/W RW	f the selected g range Default 0x00 IFO exceeds NTER is reset to 0. Default 0x00
CENT_DE gister 0x3 7 FO_WTMI gister 0x3 7 CLFTES BIT CLFTEST_	B_DIS: 31 (FIFO_V Bit6 K_LVL<5:(32 (ST_CC Bit6 _BIT:	1: disable orien 0: enable orien Front/back z ax VTMK) Bit5 FIFO_WTM bit5 Bit5 Bit5 DNF) Bit5 1, self-test enal	t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir K_LVL<5:0> vater mark lev LVL<5:0>. Wh SELFTES T_AMP/E n_Peak_V alley bled. When se	me ne the actual g va Bit3 el. Interrupt w nen the value Bit3 SingleEn_ Step	alue is FB_Z_ Bit2 ill be generat of this registe Bit2 SELFTES T_SIGN ed, a delay of	_TH<7:0>*3.9 Bit1 ed, when the rr is changed, Bit1 SELFTEST 3ms is necess	1mg+0.1g, ind Bit0 number of ent the FIFO_FR/ Bit0 AXIS<1:0>	ependent o R/W RW ries in the F AME_COUN R/W RW	f the selected g range Default 0x00 IFO exceeds NTER is reset to 0. Default 0x00
ALERT DE B_Z_TH<6 egister 0x3 7 FO_WTMI egister 0x3 ELFTES BIT ELFTEST_	B_DIS: 31 (FIFO_V Bit6 K_LVL<5:(32 (ST_CC Bit6 _BIT:	1: disable orien 0: enable orien Front/back z ax VTMK) Bit5 FIFO_WTM bit5 Bit5 Bit5 DNF) Bit5 1, self-test enal 0, normal	t denounce tir t denounce t denounce tir t denounce t denounce tir t denounce t denounce tir t denounce t de	me ne the actual g va Bit3 el. Interrupt w nen the value Bit3 SingleEn_ Step	Bit2 Bit2 Bit2 Bit2 Bit2 Bit2 SELFTES T_SIGN d, a delay of	_TH<7:0>*3.9 Bit1 ed, when the rr is changed, Bit1 SELFTEST 3ms is necess	1mg+0.1g, ind Bit0 number of ent the FIFO_FR/ Bit0 _AXIS<1:0>	ependent o R/W RW ries in the F AME_COUN R/W RW	f the selected g range Default 0x00 IFO exceeds NTER is reset to 0. Default 0x00
ELFTEST_	3_DIS: 31 (FIFO_V <u>Bit6</u> K_LVL<5:(<u>32 (ST_CC</u> <u>Bit6</u> _BIT: _AMP/En_	1: disable orien 0: enable orien Front/back z ax VTMK) Bit5 FIFO_WTM bit5 Bit5 Bit5 DNF) Bit5 1, self-test enal 0, normal Peak_Valley:	t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir K_LVL<5:0> vater mark lev LVL<5:0>. Whe LVL<5:0>. When see n_Peak_V alley	me ne the actual g va Bit3 el. Interrupt w nen the value Bit3 SingleEn_ Step	alue is FB_Z_ Bit2 ill be generat of this register Bit2 SELFTES T_SIGN id, a delay of	_TH<7:0>*3.9 Bit1 ed, when the rr is changed, Bit1 SELFTEST 3ms is necess	1mg+0.1g, ind Bit0 number of ent the FIFO_FR/ Bit0 _AXIS<1:0>	ependent o R/W RW ries in the F AME_COUN R/W RW	f the selected g range Default 0x00 IFO exceeds NTER is reset to 0. Default 0x00
ELFTEST_	B_DIS: 31 (FIFO_V Bit6 K_LVL<5:(32 (ST_CC Bit6 _BIT: _AMP/En_1	1: disable orien 0: enable orien Front/back z ax VTMK) Bit5 FIFO_WTMK)>: defines FIFO w FIFO_WTMK_I PNF) Bit5 1, self-test enal 0, normal Peak_Valley: This bit is multi When we do here	t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir K_LVL<5:0> vater mark lev LVL<5:0>. Whe LVL<5:0>. Whe SELFTES T_AMP/E n_Peak_V alley bled. When se	me ne the actual g va Bit3 el. Interrupt w nen the value Bit3 SingleEn_ Step elf-test enable	alue is FB_Z_ Bit2 ill be generat of this register Bit2 SELFTES T_SIGN id, a delay of MP and En_P	_TH<7:0>*3.9 Bit1 ed, when the rr is changed, Bit1 SELFTEST 3ms is necess eak_Valley,	1mg+0.1g, ind Bit0 number of ent the FIFO_FR/ Bit0 _AXIS<1:0>	ependent o R/W RW ries in the F AME_COUN R/W RW	f the selected g range Default 0x00 IFO exceeds NTER is reset to 0. Default 0x00
ELFTEST_	3_DIS: 31 (FIFO_V <u>Bit6</u> K_LVL<5:(<u>32 (ST_CC</u> <u>Bit6</u> _BIT: _AMP/En_	1: disable orien 0: enable orien Front/back z ax VTMK) Bit5 FIFO_WTMK bit5 Bit5 Content of the second of t	t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir K_LVL<5:0> vater mark lev LVL<5:0>. Wr Bit4 SELFTES T_AMP/E n_Peak_V alley bled. When set SELFTEST_/	me ne the actual g va Bit3 el. Interrupt w nen the value Bit3 SingleEn_ Step elf-test enable ELFTEST_AN AMP: test force	alue is FB_Z_ Bit2 ill be generat of this registe Bit2 SELFTES T_SIGN id, a delay of MP and En_P	_TH<7:0>*3.9 Bit1 ed, when the rr is changed, Bit1 SELFTEST 3ms is necess reak_Valley,	1mg+0.1g, ind Bit0 number of ent the FIFO_FR/ Bit0 _AXIS<1:0>	ependent o R/W RW ries in the F AME_COUN R/W RW	f the selected g range Default 0x00 IFO exceeds ITER is reset to 0. Default 0x00
ALERT_DE 3_Z_TH<6 2gister 0x: t7 FO_WTMI 2gister 0x: T ELFTES ELFTEST_ ELFTEST_	3_DIS: 31 (FIFO_V <u>Bit6</u> K_LVL<5:(<u>32 (ST_CC</u> <u>Bit6</u> _BIT: _AMP/En_	1: disable orien 0: enable orien Front/back z ax VTMK) Bit5 FIFO_WTMK bit5 Bit5 0.5: defines FIFO w FIFO_WTMK_I 0.5: 0, normal Peak_Valley: This bit is multi When used as 1, set high amp 0, set low ampd	t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir K_LVL<5:0> vater mark lev LVL<5:0>. Whe VL<5:0>. Whe SELFTES T_AMP/E n_Peak_V alley bled. When set ple used by S SELFTEST_/ plitude for set	me ne the actual g va Bit3 el. Interrupt w nen the value Bit3 SingleEn_ Step elf-test enable ELFTEST_AN AMP: -test force rest force	alue is FB_Z_ Bit2 ill be generat of this register Bit2 SELFTES T_SIGN ed, a delay of MP and En_P	_TH<7:0>*3.9 Bit1 ed, when the rr is changed, Bit1 SELFTEST 3ms is necess reak_Valley,	1mg+0.1g, ind Bit0 number of ent the FIFO_FR/ Bit0 _AXIS<1:0>	ependent o R/W RW ries in the F AME_COUN R/W RW	f the selected g range Default 0x00 IFO exceeds NTER is reset to 0. Default 0x00
ELFTEST_	3_DIS: 31 (FIFO_V <u>Bit6</u> K_LVL<5:(32 (ST_CC Bit6 _BIT: _AMP/En_	1: disable orien 0: enable orien Front/back z ax VTMK) Bit5 FIFO_WTMK >: defines FIFO w FIFO_WTMK_I PNF) Bit5 1, self-test enal 0, normal Peak_Valley: This bit is multi When used as 1, set high amp 0, set low ampl When used as	t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir K_LVL<5:0> vater mark lev LVL<5:0>. Wr Ditude State SELFTES T_AMP/E n_Peak_V alley bled. When se ple used by S SELFTEST_/ plitude for self-t tirude for self-t En Peak Val	me ne the actual g va Bit3 el. Interrupt w nen the value Bit3 SingleEn_ Step elf-test enable ELFTEST_AN AMP: -test force test force lev:	alue is FB_Z_ Bit2 ill be generat of this register Bit2 SELFTES T_SIGN ed, a delay of MP and En_P	_TH<7:0>*3.9 Bit1 ed, when the rr is changed, Bit1 SELFTEST 3ms is necess reak_Valley,	1mg+0.1g, ind Bit0 number of ent the FIFO_FR/ Bit0 _AXIS<1:0>	ependent o R/W RW ries in the F AME_COUN R/W RW	f the selected g range Default 0x00 IFO exceeds NTER is reset to 0. Default 0x00
ELFTEST_	3_DIS: 31 (FIFO_V <u>Bit6</u> K_LVL<5:(32 (ST_CC <u>Bit6</u> _BIT: _AMP/En_1	1: disable orien 0: enable orien Front/back z ax VTMK) Bit5 FIFO_WTMK)>: defines FIFO w FIFO_WTMK_I PNF) Bit5 1, self-test enal 0, normal Peak_Valley: This bit is multi When used as 1, set high amp 0, set low ampl When used as 1, enable Peak	t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir K_LVL<5:0> vater mark lev LVL<5:0>. Wr Ditude for self-t En_Peak_Val and Valley m	me ne the actual g va bit3 el. Interrupt w nen the value Bit3 SingleEn_ Step elf-test enable ELFTEST_AN AMP: -test force ley: atch in step c	alue is FB_Z_ Bit2 ill be generat of this register Bit2 SELFTES T_SIGN ed, a delay of MP and En_P	_TH<7:0>*3.9 Bit1 ed, when the rr is changed, Bit1 SELFTEST 3ms is necess reak_Valley,	1mg+0.1g, ind Bit0 number of ent the FIFO_FR/ Bit0 _AXIS<1:0>	ependent o R/W RW ries in the F AME_COUN R/W RW	f the selected g range Default 0x00 IFO exceeds NTER is reset to 0. Default 0x00
ELFTEST_	3_DIS: 31 (FIFO_V <u>Bit6</u> K_LVL<5:(32 (ST_CC Bit6 _BIT: _AMP/En_1	1: disable orien 0: enable orien Front/back z ax VTMK) Bit5 FIFO_WTMK)>: defines FIFO w FIFO_WTMK_I PNF) Bit5 1, self-test enal 0, normal Peak_Valley: This bit is multi When used as 1, set high amp 0, set low ampl When used as 1, enable Peak 0, disable Peak	t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir K_LVL<5:0> vater mark lev _VL<5:0>. Whe VL<5:0>. Whe SELFTES T_AMP/E n_Peak_V alley bled. When set ple used by S SELFTEST_/ blitude for self-t En_Peak_Val and Valley m c and Valley m	me ne the actual g va bit3 el. Interrupt w nen the value Bit3 SingleEn_ Step elf-test enable ELFTEST_AN AMP: -test force test force ley: atch in step c natch in step c	alue is FB_Z_ Bit2 ill be generat of this register <u>Bit2</u> SELFTES T_SIGN ed, a delay of MP and En_P	_TH<7:0>*3.9 Bit1 ed, when the rr is changed, Bit1 SELFTEST 3ms is necess reak_Valley,	1mg+0.1g, ind Bit0 number of ent the FIFO_FR/ Bit0 _AXIS<1:0>	ependent o R/W RW ries in the F AME_COUN R/W RW	f the selected g range Default 0x00 IFO exceeds NTER is reset to 0. Default 0x00
ALENT_DE B_Z_TH<6 egister 0x: t7 FO_WTMI egister 0x: t7 ELFTES BIT ELFTEST_ ELFTEST_	B_DIS: 31 (FIFO_V Bit6 K_LVL<5:(32 (ST_CC Bit6 _BIT: _AMP/En_1 tep:	1: disable orien 0: enable orien Front/back z ax VTMK) Bit5 FIFO_WTMK Solution FIFO_WTMK_I NF) Bit5 I, self-test enal 0, normal Peak_Valley: This bit is multi When used as 1, set high amp 0, set low ampl When used as 1, enable Peak 0, disable Peak 1, enable Peak	t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir K_LVL<5:0> vater mark lev LVL<5:0>. Whe SELFTES T_AMP/E n_Peak_V alley bled. When set ple used by S SELFTEST_/ blitude for self-t En_Peak_Val and Valley m c and Valley m	me ne the actual g va bit3 el. Interrupt w nen the value Bit3 SingleEn_ Step elf-test enable ELFTEST_AN AMP: -test force test force ley: atch in step c o step counter	alue is FB_Z_ Bit2 ill be generat of this register SELFTES T_SIGN ed, a delay of MP and En_P	_TH<7:0>*3.9 Bit1 ed, when the rr is changed, Bit1 SELFTEST 3ms is necess reak_Valley,	1mg+0.1g, ind Bit0 number of ent the FIFO_FR/ Bit0 _AXIS<1:0>	ependent o R/W RW ries in the F AME_COUN R/W RW	f the selected g range Default 0x00 IFO exceeds NTER is reset to 0. Default 0x00
ALENT_DE B_Z_TH<6 egister 0x: t7 FO_WTMI egister 0x: t7 ELFTES BIT ELFTEST_ ELFTEST_ ngleEn_St	B_DIS: 31 (FIFO_V Bit6 K_LVL<5:(32 (ST_CC Bit6 BIT: _AMP/En_1 tep:	1: disable orien 0: enable orien Front/back z ax VTMK) Bit5 FIFO_WTMK Solution FIFO_WTMK_I NF) Bit5 I, self-test enal 0, normal Peak_Valley: This bit is multi When used as 1, set high amp 0, set low ampl When used as 1, enable Peak 0, disable Peak 1, enable Single 0, disable single	t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir K_LVL<5:0> vater mark lev LVL<5:0>. Whe SELFTES T_AMP/E n_Peak_V alley bled. When set ple used by S SELFTEST_/ alley bled. When set tirude for self-t En_Peak_Val and Valley m c and Valley m c axis mode ir e axis mode i	me ne the actual g va bit3 el. Interrupt w nen the value Bit3 SingleEn_ Step elf-test enable ELFTEST_AN AMP: -test force lest force lest force lest force o step counter n step counter	alue is FB_Z_ Bit2 ill be generat of this register SELFTES T_SIGN ed, a delay of MP and En_P counter counter	_TH<7:0>*3.9 Bit1 ed, when the rr is changed, Bit1 SELFTEST 3ms is necess reak_Valley,	1mg+0.1g, ind Bit0 number of ent the FIFO_FR/ Bit0 AXIS<1:0>	ependent o R/W RW ries in the F AME_COUN R/W RW	f the selected g range Default 0x00 IFO exceeds NTER is reset to 0. Default 0x00
B_Z_TH<6 egister 0x: it7 IFO_WTMI egister 0x: it7 ELFTES _BIT ELFTEST_ ELFTEST_ ngleEn_St ELFTEST_	B_DIS: 31 (FIFO_V Bit6 K_LVL<5:(32 (ST_CC Bit6 BIT: _AMP/En_1 tep: _SIGN:	1: disable orien 0: enable orien Front/back z ax VTMK) Bit5 FIFO_WTMK)>: defines FIFO w FIFO_WTMK_I PNF) Bit5 1, self-test enal 0, normal Peak_Valley: This bit is multi When used as 1, set high amp 0, set low ampl When used as 1, enable Peak 0, disable Peak 1, enable Peak 1, enable Single 0, disable single 0, disable single 1, set self-test enal	t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir K_LVL<5:0> vater mark lev LVL<5:0>. Whe SELFTES T_AMP/E n_Peak_V alley bled. When set SELFTEST_/ blitude for self-f tirude for self-f tirude for self-f tirude for self-f tirude for self-f tirude for self-f tirude for self-f en_Peak_Val and Valley m c and Valley m c axis mode in excitation position	me ne the actual g va bit3 el. Interrupt w nen the value Bit3 SingleEn_ Step ELFTEST_AN AMP: -test force test force ley: atch in step counter n step counter tive	alue is FB_Z_ Bit2 ill be generat of this register <u>Bit2</u> SELFTES T_SIGN ed, a delay of MP and En_P counter counter	_TH<7:0>*3.9 Bit1 ed, when the rr is changed, Bit1 SELFTEST 3ms is necess reak_Valley,	1mg+0.1g, ind Bit0 number of ent the FIFO_FR/ Bit0 AXIS<1:0>	ependent o R/W RW ries in the F AME_COUN R/W RW	f the selected g range Default 0x00 IFO exceeds NTER is reset to 0. Default 0x00
INCENT_DE B_Z_TH<6 egister 0x: it7 IFO_WTMI egister 0x: it7 ELFTES _BIT ELFTEST_ ELFTEST_ ST Corp	B_DIS: 31 (FIFO_V Bit6 S2 (ST_CC Bit6 Bit6 BIT: _AMP/En_1 tep: _SIGN: poration	1: disable orien 0: enable orien Front/back z ax VTMK) Bit5 FIFO_WTMK Solution FIFO_WTMK_I NF) Bit5 I, self-test enal 0, normal Peak_Valley: This bit is multi When used as 1, set high amp 0, set low ampl When used as 1, enable Peak 0, disable Peak 1, enable Peak 1, enable Single 0, disable single 1, set self-test enal 1, set self-test enal	t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir t denounce tir K_LVL<5:0> vater mark lev _VL<5:0>. Whe SELFTES T_AMP/E n_Peak_V alley bled. When set SELFTEST_/ blitude for self-f tirude for self-f tirude for self-f tirude for self-f tirude for self-f en_Peak_Val and Valley m c and Valley m c axis mode ir excitation position	me ne the actual g va bit3 el. Interrupt w nen the value Bit3 SingleEn_ Step elf-test enable ELFTEST_AN AMP: -test force test force lley: natch in step counter n step counter tive	alue is FB_Z_ Bit2 ill be generat of this register <u>Bit2</u> SELFTES T_SIGN ed, a delay of MP and En_P counter counter	_TH<7:0>*3.9 Bit1 ed, when the rr is changed, Bit1 SELFTEST 3ms is necess reak_Valley,	1mg+0.1g, ind Bit0 number of ent the FIFO_FR/ Bit0 _AXIS<1:0>	ependent o	f the selected g range Default 0x00 IFO exceeds UTER is reset to 0. Default 0x00

0, set self-test excitation negative

SELFTEST_AXIS<1:0>:

These two bits are used to select axis for selftest or step counter When SELFTEST_BIT (0x32<7>) is enabled: 00, x axis 01, y axis 10, z axis 11, z axis When STEP_EN (0x16<3>) is enabled, 00, x axis 01, y axis 10, z axis 11. z axis When STEP_EN (0x16<3>) and SingleEn_Step (0x32<3>) is enabled, 00, x axis 01, y axis 10, z axis 11, z axis

Register 0x34 (VALLEY_A)

0	. –	/							
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
VALLEY_A	<5:0>							RW	0x00
	F O	II		and the last state of the second state of the	d fam at an inell	and a second set			

VALLEY_A<5:0>: valley value of one axis which is used for step valley match

Register 0x1f (PEAK A)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
PEAK_A<5:0)>					STEP_MISM 1:0>	/ATCH_A<	RW	0x00

PEAK_A<5:0>: peak value of one axis which is used for step peak match

STEP_MISMATCH_A<1:0>:

precision for step peak and valley match

00, match VALLEY_A<5:1> and PEAK_A<5:1> 01, match VALLEY_A<5:2> and PEAK_A<5:2>

10, match VALLEY_A<5:3> and PEAK_A<5:3>

11, match VALLEY_A<5:4> and PEAK_A<5:4>

Register	0x33 ((NVM
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	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default		
ſ	UNLOCK				NVM_LO	NVM_RD	NVM_PR		RW	0x04	1	
	_3F				AD	Y	OG				1	
	UNLOCK_3F: 1, unlock the burst-reading of FIFO. The burst-reading can access registers behind 0x3F. This option is reserved for internal test.											
		0	, lock the burs	t-reading of F	IFO. The regi	ster address v	will be locked	at 0x3F, for ne	ormal use.			
	NVM_LOAD): 1	, trigger loadin	g register from	m NVM							
		0	, not trigger lo	ading register	form NVM							
			Thi	s bit is cleared	d when NVM I	oading is don	e					
	NVM_RDY: 1, NVM is ready, loading or programing NVM is done											
	0, NVM is not ready, loading or programming NVM is in progress.											
	NVM_RDY is read-only to customer.											
	NVM_PROG: 1, trigger programing NVM											
	0, not trigger programming NVM											
	This bit is cleared when NVM programming is done											

Register 0x	36 (SR)								
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
SOFT_RES	RW	0x00							
SOFT_RESET: 0xB6, reset all of the registers 0xB3, unlock NV/M for programming (not open to customer)									

This register is cleared when reset or NVM programming is done

Register 0x37 (OFFSET_XY)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default]
OFFSET_X	<10:8>		GAIN_Z<9:	3>	OFFSET_Y	<10:8>		RW	NVM	
OFFSET_X	<10:8>:	8>: offset value of x-channel. This data is the trimming data for x channel in FT phase, together with OFFSET_X<7:0>								7:0> in 0x38
GAIN_Z<9:8	8>:	sensitivity trimming bits for z channel, together with GAIN_Z<7:0> in 0x3D (total 10 bits).								

OFFSET_Y<10:8>: offset value of y-channel. This data is the trimming data for y channel in FT phase, together with OFFSET_Y<7:0> in 0x39.

Register 0x38 (OFFSET_X)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
OFFSET_X	<7:0>							RW	NVM
OFFSET_X	<7:0>:	offset value of >	-channel. Thi	s data is the t	rimming data f	for x channel	in FT phase, t	together with (DFFSET_X<10

offset value of x-channel. This data is the trimming data for x channel in FT phase, together with OFFSET_X<10:8> in 0x37<7:5>. The trimming LSB is 4mg, the full trimming range in digital domain is +-4g

User can perform read-modify-write access, to change the register value. However, when device is re-power-on, or soft-reset, this value will be updated to default again.

Register 0x39 (OFF	SET_Y)							
Bit7 Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
FSET_Y<7:0>							RW	NVM
FSET_Y<7:0>:	offset value The trimmin User can pe this value wi	of y-channel. g LSB is 4mg, rform read-mo ill be updated	This data is th the full trimm odify-write act to default aga	ne trimming da ning range in c cess, to chang ain.	ita for y chan ligital domain le the registe	nel in FT phase i is +-4g r value. Howev	e, together wir rer, when dev	th OFFSET_Y<
gister 0x3a (OFF	SET_Z)							
it7 Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
FFSET_Z<7:0>						··· ·	RW	NVM
	The trimmin User can pe this value wi	g LSB is 4mg, rform read-mo ill be updated	the full trimm odify-write act to default aga	hing range in c cess, to chang ain.	ligital domain e the registe	r value. Howev	e, together wi ver, when dev	ice is re-power-
agister 0x3b (GAII	N_X) not open to	Bit/	Bit3	Bit2	Bit1	Bit0	R/M	Default
	Dito	DIG	Dito	Ditz	Ditt	Dito	RW	NVM
egister 0x3c (GAII	Gain_total = Gain rang is J_Y) not open to	from 1 to 2, the customer	_X) / 256 ne worst gain	accuracy is 1,	/256 ~= 0.4%			
7 Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
N_Y							RW	NVM
egister 0x3d (GAII it7 Bit6	Gain rang is <u>N_Z) not open to</u> Bit5	from 1 to 2, th	ne worst gain	accuracy is 1, Bit2	/256 ~= 0.4%	Bit0	R/W	Default
IN_Z<7:0>		-					RW	NVM
AIN_2: egister 0x3e (FIFC t7 Bit6 F0_MODE<1:0>	sensitivity tri Gain_total = Gain rang is D_CFG) Bit5	Imming bits for (128 + GAIN_ from 0.5 to 4. Bit4	r z channel, te _Z) / 256 5, the worst g 	ogetner with G gain accuracy Bit2	is 1/128 ~= 0 Bit1 FIFO_C	IN 0x37<4:3> 0.8% Bit0 H<1:0>	R/W	Default 0x00
	FIFO_MOD	E defines FIFO	D mode of the	e device. Settir	ngs as followi	ing		ł
FIFO CH<1:0>:	FIFO_MC 11 10 01 00 FIFO_CH de	DDE<1:0> M F S F E E fines which c	Aode TFO TREAM TFO SYPASS hannel data b	be stored in FI	FO buffer. Se	etting as followi	ng	
	11, only z ax 10, only y ax 01, only x ax 00, all axes	kis data be sto kis data be sto kis data be sto data be stored	red in FIFO b red in FIFO b red in FIFO b in FIFO buff	ouffer ouffer ouffer ouffer er			5	
egister 0x3f (FIFO	_DATA)							
7 Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
EO DATA							IR	0x00

FIFO_DATA: FIFO read out data. User can read out FIFO data through this register. Data format depends on the setting of FIFO_CH (0x3e<1:0>).

When the FIFO data is the LSB part of acceleration data, and if FIFO is empty, then FIFO_DATA<0> is 0. Otherwise if FIFO is not empty and the data is effective, FIFO_DATA<0> is 1 when reading LSB of acceleration.

ORDERING INFORMATION

Ordering Number	Temperature Range	Package	Packaging
QMC6981-TR	-40℃~85℃	LGA-12	Tape and Reel: 5k pieces/reel



CAUTION: ESDS CAT. 1B

FIND OUT MORE

For more information on QST's Accelerometer Sensors contact us at 86-21-50497300.

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ISO9001 : 2008

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China Patents 201510000399.8, 201510000425.7, 201310426346.3, 201310426677.7, 201310426729.0, 201210585811.3 and 201210553014.7 apply to the technology described.

QST First Floor, Building No.2,



Rev1.0, released Apr. 2015 QST Corporation



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>>QST Corporation(矽容)