0.1-3.0GHz SP6T Antenna Switch

Product ID： VC1616

Version： V1.0

Vanchip Technologies

Preliminary Datasheet
Vanchiptech Confidential

Revision History

Version	Date	Author	Modify Description
1.0	Jan. 2015	Vanchip	Released

VC1616
0.1-3.0GHz SP6T Antenna Switch

Package size：QFN , 14pin , 2 x 2 x 0.6mm

Description

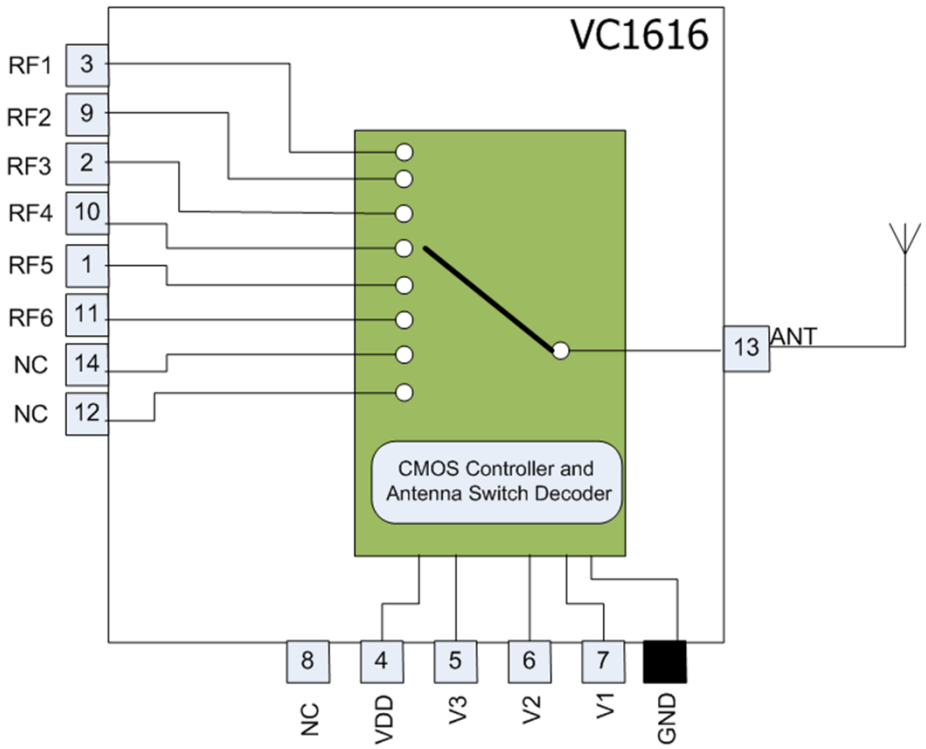
The VC1616 is a SP6T with low insertion loss and high isolation. It can be used to support band switching and mode switching in antenna diversity systems for 2G/3G/4G, data cards and tablets. The symmetrical design of internal ports provides a flexibility in applications, making it convenient for PCB routing and adjustment of receive and transmit signals. The mode switching is realized by the GPIO pins as referenced in the chip block diagram and the control logic.

The VC1616 is provided in a compact 2 x 2 x0.6mm ，14-Pin QFN package.

Key features

- Frequency range：0.1~3GHz
- Low insertion loss:0.7 dB typ. @ 2.7 GHz
- High isolation：>20 dB @ 2.7 GHz
- Internal supply voltage regulator and logic control，NO DC blocking capacitors required.
- Internal ESD protection circuit at Antenna part
- Low power consumption
- Small package: QFN，14-pin，2mm x 2mm x 0.6mm
- Process: CMOS/SOI

Chip block diagram



Absolute Maximum Ratings

Parameter	Max	Units
Supply voltage	5.0	V
Control voltage（V3/2/1）	3.0	V
Max RF input power	37.5	dBm
ESD（HBM）	1000	V
Operating temperature	-40 to +90	℃
Storage temperature	-55 to +150	℃

Recommended operating condition

DC specifications

Parameter	Symbol	Min	Typ.	Max	Units	Test condition
Supply voltage	V_{DD}	2.5	3.0	4.8	V	
Supply current	I_{DD}		55	70	uA	
Logic low voltage V3/2/1	V_{X_L}	0		0.3	V	
Logic high voltage V3/2/1	V_{X_H}	1.2	1.8	2.4	V	
Control current	I_{CTL}	0	0.5	1.5	uA	Vx=1.8V
Leakage current	I_L		5	10	uA	Vx=1.8V
Turn-on switching time	T_{ON}		1.7	2.8	uS	

RF Specifications

Parameter	Symbol	Min	Typ.	Max	Units	Test condition
Insertion loss (ANT to RF1~6)	IL		0.52		dB	0.1~1.0GHz
			0.58		dB	1.0~2.0GHz
			0.72		dB	2.0~2.7GHz
Isolation (ANT to RF1~6)	I_{SO}	30			dB	0.1~1.0GHz
		25			dB	1.0~2.0GHz
		22			dB	2.0~2.7GHz

RF specifications						
Parameter	**Symbol**	**Min**	**Typ.**	**Max**	**Units**	**Test Condition**
Input return loss （ANT to RF1~6）	RL		-20		dB	0.1~1.0GHz
			-20		dB	1.0~2.0GHz
			-18		dB	2.0~2.7GHz
2nd harmonics （ANT to RF1~6）	$2f_O$		-65		dBm	Pin=+26dBm 0.1~3.0GHz
3rd harmonics （ANT to RF1~6）	$3f_O$		-65		dBm	Pin=+26dBm 0.1~3.0GHz
0.1dB Compression point （ANT to RF1~6）	$P_{0.1dB}$		37.5		dBm	0.8 GHz~3.0 GHz
3rd Order input intercept	I_{IP3}		66		dBm	@ 2.0 GHz, PIN = +26 dBm, Δf = 1 MHz

Control logic

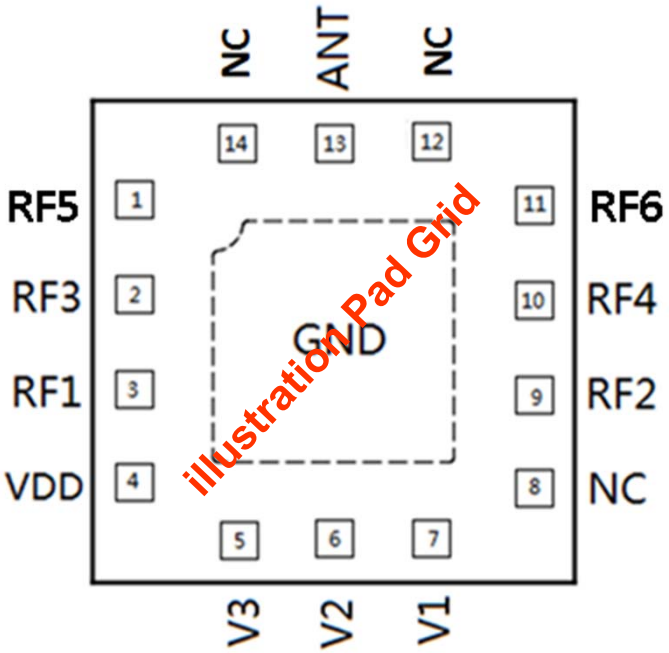
Logic Control Table			“ON” RF Path					
V1	V2	V3	RF1	RF2	RF3	RF4	RF5	RF6
0	0	0	On	X	X	X	X	X
0	0	1	X	On	X	X	X	X
0	1	0	X	X	On	X	X	X
0	1	1	X	X	X	On	X	X
1	0	0	X	X	X	X	On	X
1	0	1	X	X	X	X	X	On

* Control pin 1 stands for high voltage, 0 stands for low voltage; “ON” path stands for “ON”， X stands for “OFF”.

Port isolation

Port	Freq. (GHz)	Isolation (dB)					
		RF1	RF2	RF3	RF4	RF5	RF6
Ant-Port							
RF1	1	-	-43	-46	-40	-40	-37
RF1	2	-	-38	-36	-35	-32	-31
RF1	2.7	-	-33	-32	-31	-29	-28
RF2	1	-43	-	-40	-47	-36	-40
RF2	2	-37	-	-34	-38	-30	-33
RF2	2.7	-34	-	-31	-33	-27	-29
RF3	1	-47	-43	–	-40	-48	-37
RF3	2	-36	-37	–	-34	-35	-31
RF3	2.7	-33	-33	–	-31	-29	-28
RF4	1	-43	-48	-40	–	-36	-48
RF4	2	-36	-39	-34	–	-31	-36
RF4	2.7	-33	-34	-31	–	-28	-30
RF5	1	-51	-43	-43	-41	–	-38
RF5	2	-38	-36	-34	-35	–	-32
RF5	2.7	-33	-32	-31	-31	–	-28
RF6	1	-43	-49	-40	-44	-37	–
RF6	2	-36	-39	-34	-35	-31	–
Port-Port							
RF1	1	–	-44	-33	-48	-44	-53
RF1	2	–	-36	-27	-39	-34	-39
RF1	2.7	–	-32	-24	-34	-30	-34
RF2	1	-44	–	-48	-33	-52	-44
RF2	2	-36	–	-39	-27	-38	-35
RF2	2.7	-32	–	-34	-24	-33	-30
RF3	1	-33	-44	–	-47	-34	-53
RF3	2	-27	-37	–	-39	-27	-39
RF3	2.7	-24	-32	–	-34	-24	-33
RF4	1	-45	-33	-48	–	-52	-34
RF4	2	-37	-28	-39	–	-38	-28
RF4	2.7	-33	-24	-34	–	-33	-24
RF5	1	-38	-44	-32	-46	–	-50
RF5	2	-32	-37	-26	-38	–	-38
RF5	2.7	-29	-36	-23	-34	–	-32
RF6	1	-45	-39	-47	-32	-51	–
RF6	2	-37	-33	-39	-26	-37	–
RF6	2.7	-39	-29	-34	-23	-32	–

Pin definition

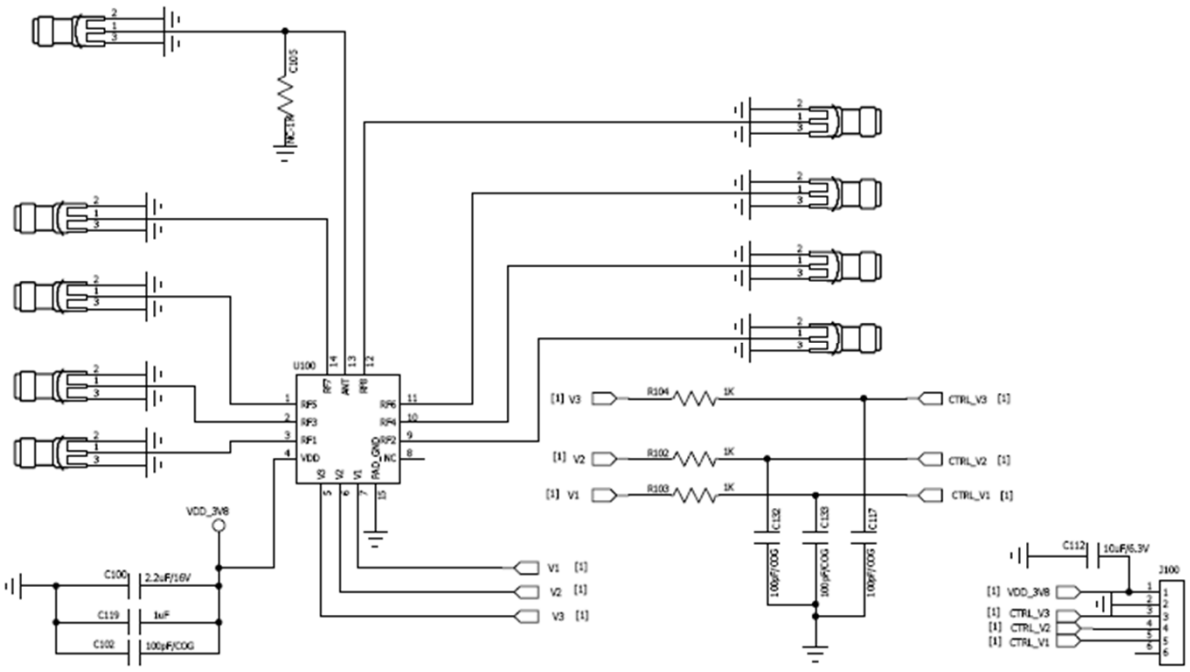


*Pad layout as seen from Top View looking through package

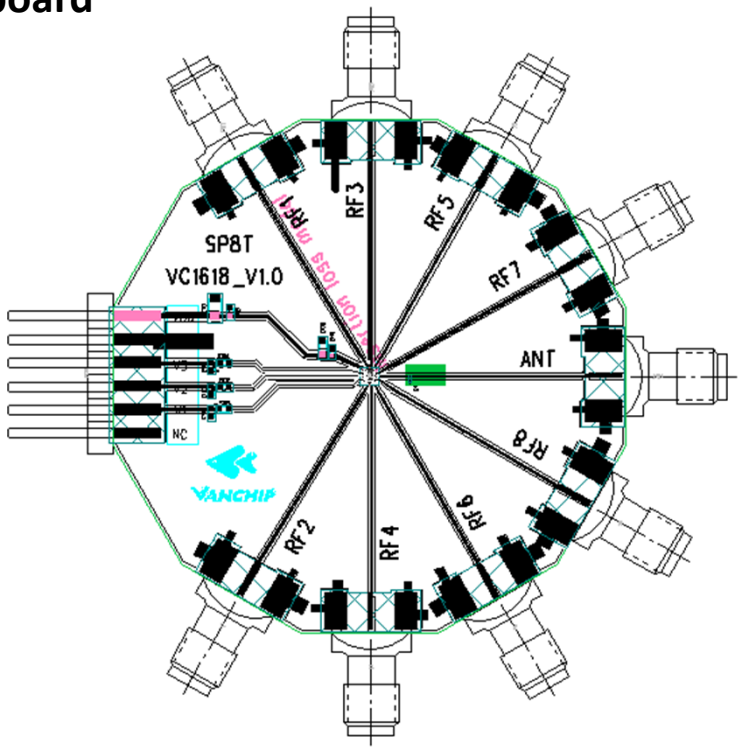
Pin	Name	Description	Pin	Name	Description
1	RF5	RF I/O Port 5	8	NC	Not used
2	RF3	RF I/O Port 3	9	RF2	RF I/O Port 2
3	RF1	RF I/O Port 1	10	RF4	RF I/O Port 4
4	VDD	DC supply	11	RF6	RF I/O Port 6
5	V3	Control logic 3	12	NC	Not used
6	V2	Control logic 2	13	ANT	Antenna Port
7	V1	Control logic 1	14	NC	Not used

Bottom Ground PAD must be connected to ground.

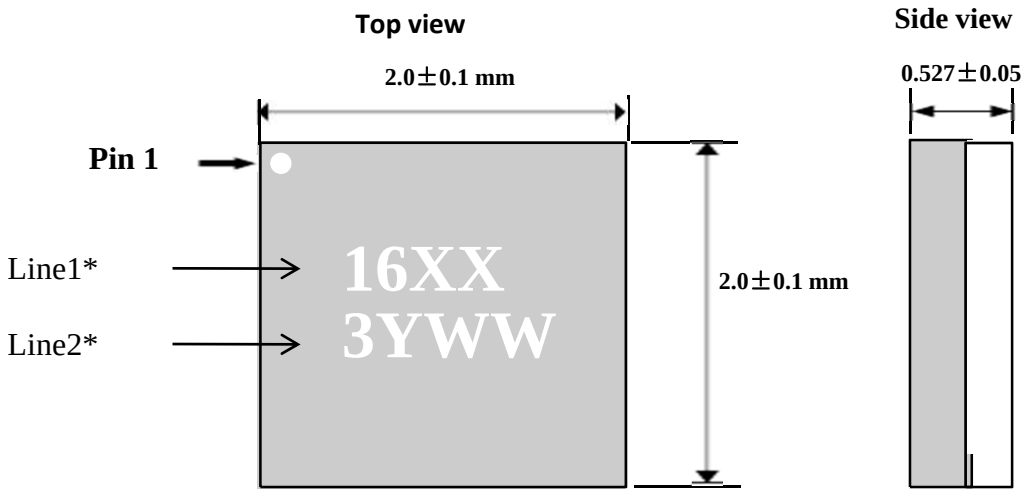
Application circuit



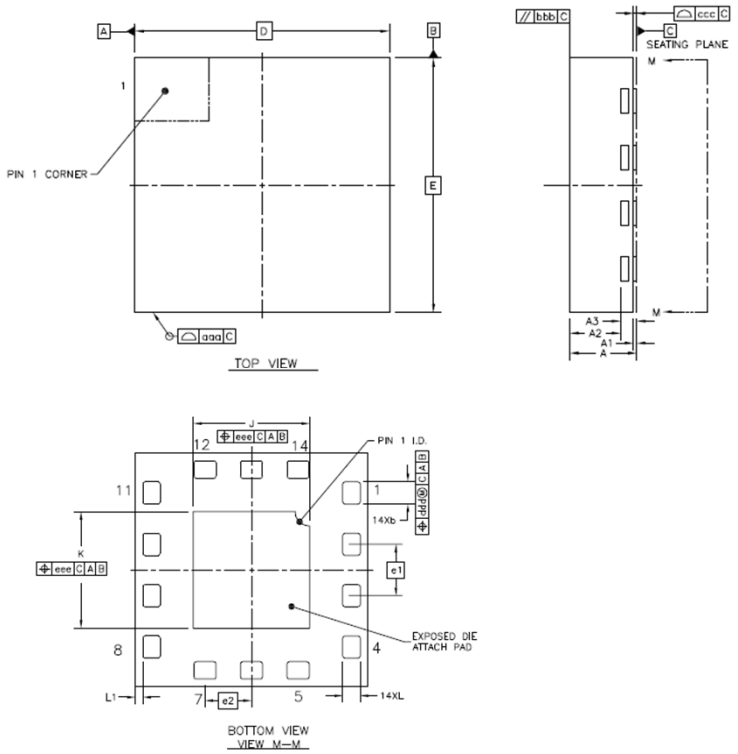
Evaluation board



Package Dimensions （Unit: mm）

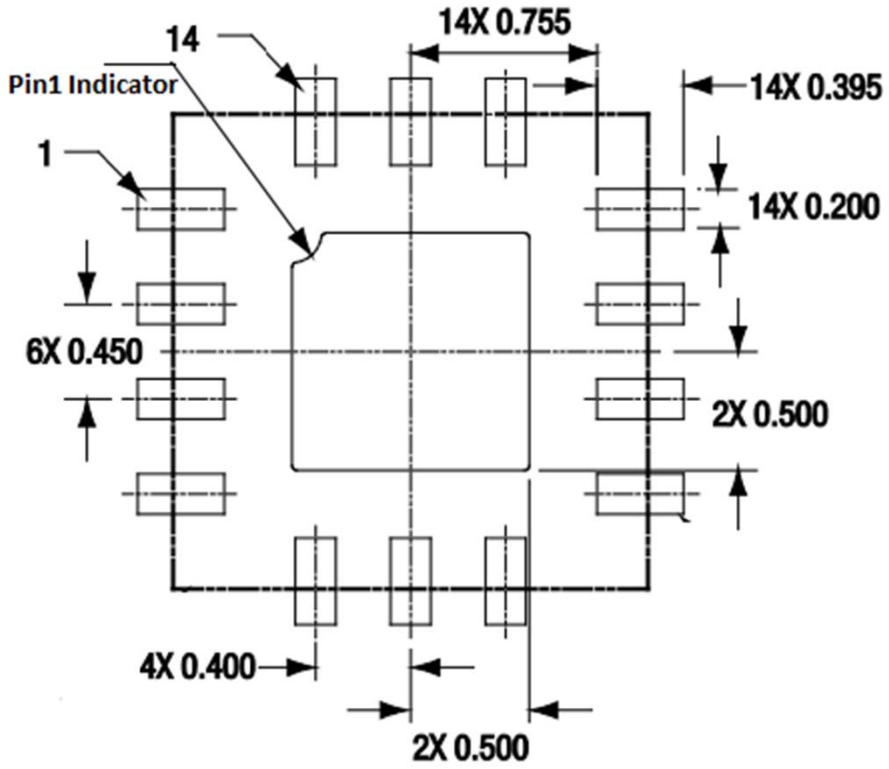


Line1*:	16	VC1616
	XX	Trace Code
Line2*:	3	Assy house Code
	YWW	Date Code



DESCRIPTION		SYMBOL	MILLIMETER		
			MIN	NOM	MAX
TOTAL THICKNESS		A	0.477	0.527	0.577
STAND OFF		A1	0.00	---	0.05
MOLD THICKNESS		A2	0.35	0.40	0.45
L/F THICKNESS		A3	0.127REF		
LEAD WIDTH		b	0.14	0.19	0.24
BODY SIZE	X	D	1.95	2.00	2.05
	Y	E	1.95	2.00	2.05
LEAD PITCH		e1	0.44 REF		
		e2	0.40 REF		
EP SIZE	X	J	0.95	1.00	1.05
	Y	K	0.95	1.00	1.05
LEAD LENGTH		L	0.10	0.15	0.20
		L1	0.065REF		
PACKAGE EDGE TOLERANCE		aaa	0.05		
MOLD FLATNESS		bbb	0.05		
COPLANARITY		ccc	0.05		
LEAD OFFSET		ddd	0.05		
EXPOSED PAD OFFSET		eee	0.05		

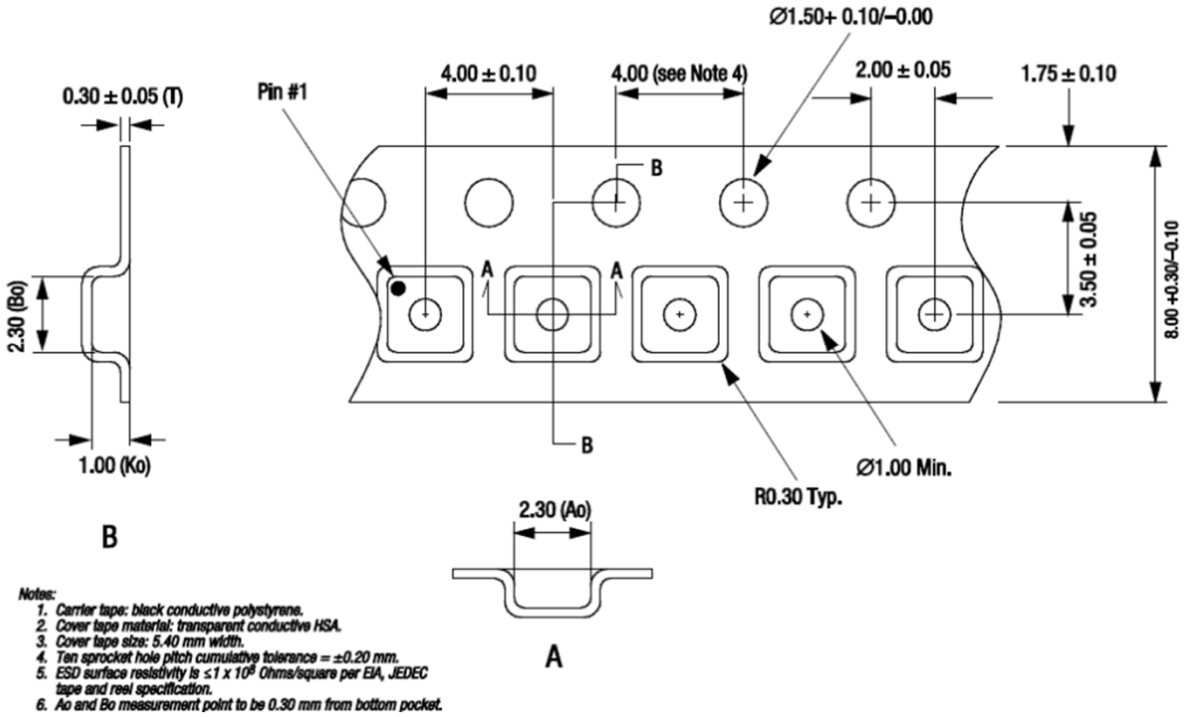
PCB Layout Footprint Recommendation



Tape and Reel

VC1616 carrier tape basic dimensions are based on EIA 481. The pocket is designed to hold the part for shipping and loading onto SMT manufacturing equipment, while protecting the body and the solder terminals from damaging stresses.

Prior to shipping, moisture sensitive parts (MSL level 2a-5a) are baked and placed into the pockets of the carrier tape. A cover tape is sealed over the top of the entire length of the carrier tape. The reel is sealed in a moisture barrier ESD bag with the appropriate units of desiccant and a humidity indicator card, which is placed in a cardboard shipping box. It is important to note that unused moisture sensitive parts need to be resealed in the moisture barrier bag. If the reels exceed the exposure limit and need to be rebaked, most carrier tape and shipping reels are not rated as bakeable at 125°C.



Notes:
1. Carrier tape: black conductive polystyrene.
2. Cover tape material: transparent conductive HSA.
3. Cover tape size: 5.40 mm width.
4. Ten sprocket hole pitch cumulative tolerance = ±0.20 mm.
5. ESD surface resistivity is ≤1 x 10^9 Ohms/square per EIA, JEDEC tape and reel specification.
6. Ao and Bo measurement point to be 0.30 mm from bottom pocket.