# XC9201 Series

## PWM Controlled Step-Down DC/DC Controllers

## ■GENERAL DESCRIPTION

The XC9201 series are step-down multiple current and voltage feedback DC/DC controller ICs. Current sense, clock frequencies and amp feedback gain can all be externally regulated.

A stable power supply is possible with output currents of up to 3.0A. With output voltage fixed internally, output voltage is selectable in 100mV increments (semi-custom) within a 1.2V ~ 16.0V range. (±2.5%).

For output voltages outside this range, we recommend the FB version which has a 0.9V internal reference voltage. Using this version, the required output voltage can be set-up using 2 external resistors.

Switching frequencies can also be set-up externally within a range of 100kHz~600kHz and therefore frequencies suited to your particular application can be selected.

With the current sense function, peak currents (which flow through the driver transistor and the coil) can be controlled. Soft-start time can be adjusted using external resistors and capacitors.

During shutdown (CE pin =L), consumption current can be reduced to as little as $0.5\mu A$ (TYP.) or less and with U.V.L.O. (Under Voltage Lock Out) built-in, the external transistor will be automatically shut off below the regulated voltage.

## ■APPLICATIONS

● Mobile, Cordless phones
● Palm top computers, PDAs
● Portable games
● Cameras, Digital cameras
● Notebook computers

## ■FEATURES

**Stable Operations via Current & Voltage Multiple Feedback**
**Unlimited Options for Peripheral Selection**
**Current Protection Circuit**
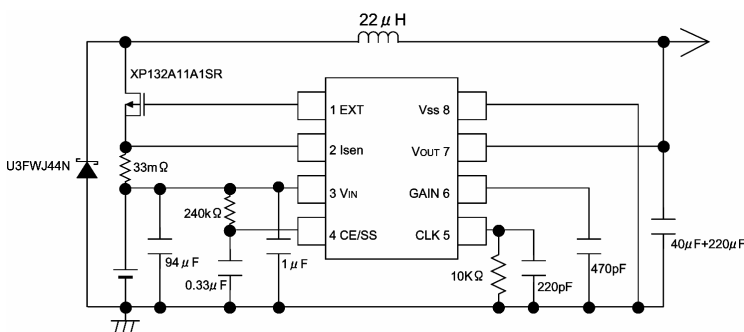**Ceramic Capacitor Compatible**
**Input Voltage Range** : 2.5V ~20V
**Output Voltage Range** : 1.2V ~ 16V
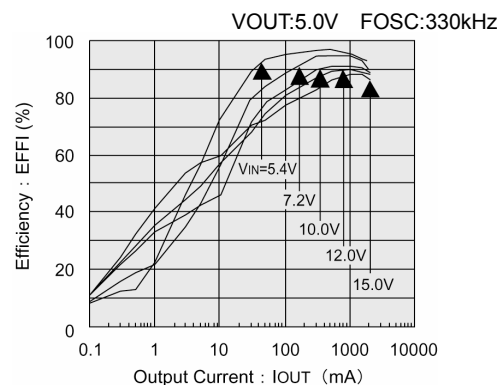**Oscillation Frequency Range** : 100kHz ~ 600kHz
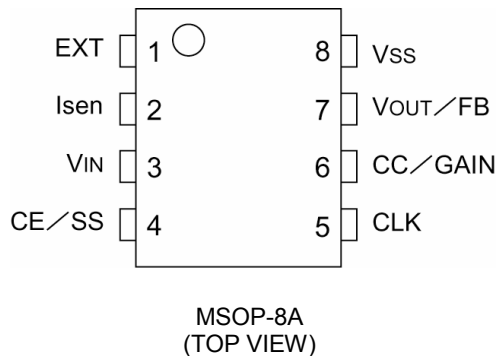**Output Current** : Up To 3.0A
**Package** : MSOP-8A

## ■TYPICAL APPLICATION CIRCUIT



## ■TYPICAL PERFORMANCE CHARACTERISTICS

# XC9201 Series

## ■PIN CONFIGURATION

```
        ┌───────────────┐
 EXT ─┤1  ◯          8├─ VSS
Isen ─┤2             7├─ VOUT／FB
 VIN ─┤3             6├─ CC／GAIN
CE／SS─┤4             5├─ CLK
        └───────────────┘
```

MSOP-8A
(TOP VIEW)

## ■PIN ASSIGNMENT

| PIN NUMBER | PIN NAME | FUNCTION |
|---|---|---|
| 1 | EXT | Driver |
| 2 | $I_{SEN}$ | Current Sense |
| 3 | $V_{IN}$ | Power Input |
| 4 | CE / SS | CE/Soft Start |
| 5 | CLK | Clock Input |
| 6 | CC / GAIN | Phase Compensation |
| 7 | $V_{OUT}$ / FB | Voltage Sense |
| 8 | $V_{SS}$ | Ground |

## ■PRODUCT CLASSIFICATION

●Ordering Information

XC9201 ①②③④⑤⑥

| DESIGNATOR | DESCRIPTION | SYMBOL | DESCRIPTION |
|---|---|---|---|
| ① | Type of DC/DC Controller | C | : $V_{OUT}$ (Fixed Voltage Type), Soft-start externally set-up |
| | | D | : FB voltage, Soft-start externally set-up |
| ② ③ | Output Voltage | Integer | : e.g. $V_{OUT}$=2.3V → ②=2, ③=3<br>FB products → ②=0, ③=9 fixed |
| | | A ~ H | : Voltage above 10V<br>→ 10=A, 11=B, 12=C, 13=D, 14=E, 15=F, 16=H<br>e.g. $V_{OUT}$=13.5V → ②=D, ③=5 |
| ④ | Oscillation Frequency | A | : Adjustable |
| ⑤ | Package | K | : MSOP-8A |
| ⑥ | Device Orientation | R | : Embossed tape, standard feed |
| | | L | : Embossed tape, reverse feed |

The standard output voltages of the XC9201C series are 2.5V, 3.3V, and 5.0V.

Voltages other than those listed are semi-custom.

# ■BLOCK DIAGRAM
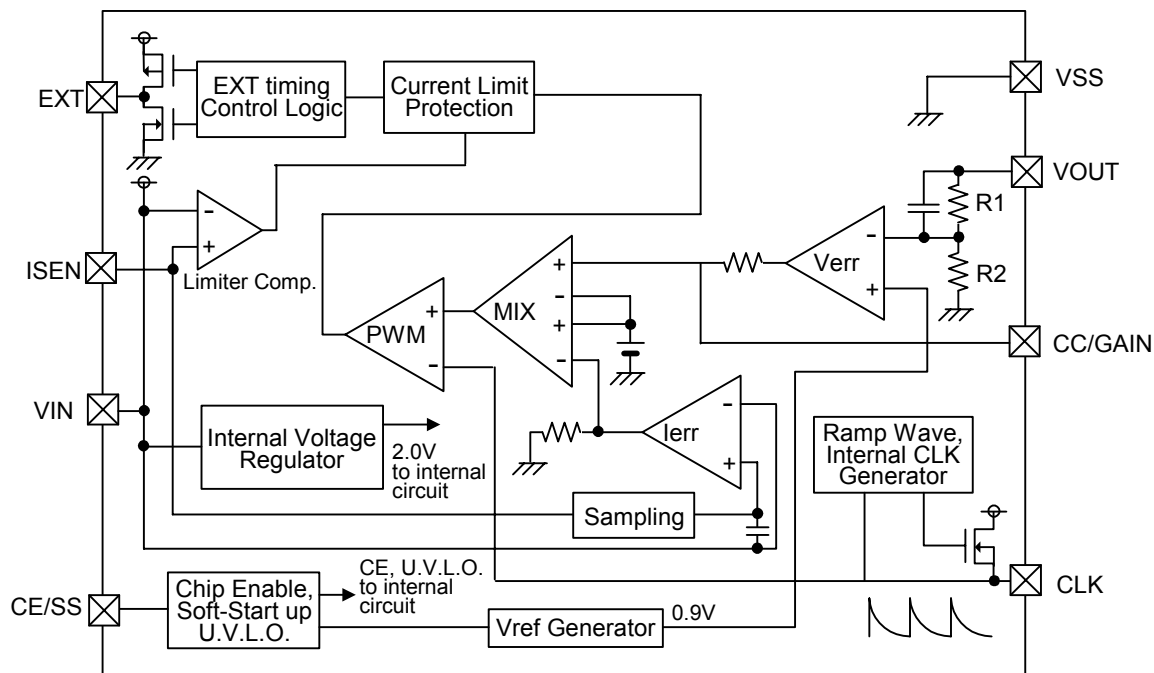


# ■ABSOLUTE MAXIMUM RATINGS

Ta = 25℃

| PARAMETER | SYMBOL | RATINGS | UNITS |
|-----------|--------|---------|-------|
| EXT Pin Voltage | VEXT | -0.3~VDD+0.3 | V |
| ISEN Pin Voltage | VISEN | -0.3~+22 | V |
| VIN Pin Voltage | VIN | -0.3~+22 | V |
| CE/ SS Pin Voltage | VCE | -0.3~+22 | V |
| CLK Pin Voltage | VCLK | -0.3~VDD+0.3 | V |
| CC/ GAIN Pin Voltage | VCC | -0.3~VDD+0.3 | V |
| VOUT/ FB Pin Voltage | VOUT/FB | -0.3～+22 | V |
| EXT Pin Current | IEXT | ±100 | mA |
| Power Dissipation | Pd | 150 | mW |
| Operating Ambient Temperature | Topr | -40~+85 | ℃ |
| Storage Temperature | Tstg | -55~+125 | ℃ |

TOREX

3/24

## ■ELECTRICAL CHARACTERISTICS

XC9201C25AKR                                                                                    Ta=25°C

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS | CIRCUITS |
|---|---|---|---|---|---|---|---|
| Output Voltage | $V_{OUT}$ | $I_{OUT}$=300mA | 2.438 | 2.500 | 2.562 | V | ① |
| Maximum Operating Voltage | $V_{INmax}$ | | 20 | - | - | V | ① |
| Minimum Operating Voltage | $V_{INmin}$ | | - | - | 2.200 | V | ① |
| U.V.L.O. Voltage | $V_{UVLO}$ | EXT voltage = High | 1.0 | 1.4 | 2.0 | V | ⑤ |
| Supply Current 1 | $I_{DD1}$ | $V_{IN}$=3.75V, CE=$V_{IN}$=$V_{OUT}$ | - | 115 | 220 | $\mu$A | ② |
| Supply Current 2 | $I_{DD2}$ | $V_{IN}$=20.0V, CE=$V_{IN}$, $V_{OUT}$=$V_{SS}$ | - | 130 | 235 | $\mu$A | ② |
| Stand-by Current | $I_{STB}$ | $V_{IN}$=3.75V, CE=$V_{OUT}$=$V_{SS}$ | - | 0.5 | 2.0 | $\mu$A | ② |
| CLK Oscillation Frequency | $F_{OSC}$ | RT=10.0k$\Omega$, CT=220pF | 280 | 330 | 380 | kHz | ③ |
| Frequency Input Stability | $\frac{\Delta F_{OSC}}{\Delta V_{IN} \cdot F_{OSC}}$ | $V_{IN}$=2.5V～20V | - | ±5 | - | % | ③ |
| Frequency Temperature Fluctuation | $\frac{\Delta F_{OSC}}{\Delta T_{OPR} \cdot F_{OSC}}$ | $V_{IN}$=3.75V Topr=-40～+85°C | - | ±5 | - | % | ③ |
| Maximum Duty Cycle | MAXDTY | $V_{OUT}$=$V_{SS}$ | 100 | - | - | % | ④ |
| Minimum Duty Cycle | MINDTY | $V_{OUT}$=$V_{IN}$ | - | - | 0 | % | ④ |
| Current Limiter Voltage | $I_{LIM}$ | $V_{IN}$ pin voltage - $I_{SEN}$ pin voltage | 90 | 150 | 220 | mV | ⑥ |
| $I_{SEN}$ Current | $I_{ISEN}$ | $V_{IN}$=3.75V, $I_{SEN}$=3.75V | 4.5 | 7.0 | 13.0 | $\mu$A | ⑥ |
| CE "High" Current | $I_{CEH}$ | CE=$V_{IN}$=20.0V, $V_{OUT}$=0V | -0.1 | 0 | 0.1 | $\mu$A | ⑤ |
| CE "Low" Current | $I_{CEL}$ | CE=0V, $V_{IN}$=20.0V, $V_{OUT}$=0V | -0.1 | 0 | 0.1 | $\mu$A | ⑤ |
| CE "High" Voltage | $V_{CEH}$ | CLK Oscillation start, $V_{OUT}$=0V, CE：Voltage applied | 0.6 | - | - | V | ⑤ |
| CE "Low" Voltage | $V_{CEL}$ | CLK Oscillation stop, $V_{OUT}$=0V, CE：Voltage applied | - | - | 0.2 | V | ⑤ |
| EXT "High" ON Resistance | $R_{EXTH}$ | EXT=$V_{IN}$－0.4V, CE=$V_{OUT}$=$V_{IN}$ (*1) | - | 27 | 40 | $\Omega$ | ④ |
| EXT "Low" ON Resistance | $R_{EXTL}$ | EXT=0.4V, CE=$V_{IN}$, $V_{OUT}$=$V_{SS}$ (*1) | - | 24 | 33 | $\Omega$ | ④ |
| Efficiency (*2) | EFFI | | - | 93 | - | % | ① |
| Soft-start Time | $T_{SS}$ | Connect $C_{SS}$ and $R_{SS}$, CE：0V→3.75V | 5 | 10 | 20 | ms | ① |
| CC/GAIN Pin Output Impedance | $R_{CCGAIN}$ | | - | 400 | - | k$\Omega$ | ⑦ |

Unless otherwise stated, $V_{IN}$=3.75V

NOTE:

   *1: On resistance = 0.4V / measurement current

   *2: EFFI = {[(output voltage) x (output current)] / [(input voltage) x (input current)]} x 100

   *3: The capacity range of the condenser used to set the external CLK frequency is 180 ~ 300pF

# ■ELECTRICAL CHARACTERISTICS (Continued)

XC9201C33AKR                                                                        Ta=25℃

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS | CIRCUITS |
|---|---|---|---|---|---|---|---|
| Output Voltage | $V_{OUT}$ | $I_{OUT}$=300mA | 3.218 | 3.300 | 3.382 | V | ① |
| Maximum Operating Voltage | $V_{INmax}$ | | 20 | - | - | V | ① |
| Minimum Operating Voltage | $V_{INmin}$ | | - | - | 2.200 | V | ① |
| U.V.L.O. Voltage | $V_{UVLO}$ | EXT voltage = High | 1.0 | 1.4 | 2.0 | V | ⑤ |
| Supply Current 1 | $I_{DD1}$ | $V_{IN}$=5.0V, CE=$V_{IN}$=$V_{OUT}$ | - | 115 | 220 | $\mu$A | ② |
| Supply Current 2 | $I_{DD2}$ | $V_{IN}$=20.0V, CE=$V_{IN}$, $V_{OUT}$=$V_{SS}$ | - | 130 | 235 | $\mu$A | ② |
| Stand-by Current | $I_{STB}$ | $V_{IN}$=5.0V, CE=$V_{OUT}$=$V_{SS}$ | - | 0.5 | 2.0 | $\mu$A | ② |
| CLK Oscillation Frequency | $F_{OSC}$ | RT=10.0kΩ, CT=220pF | 280 | 330 | 380 | kHz | ③ |
| Frequency Input Stability | $\frac{\Delta F_{OSC}}{\Delta V_{IN}\cdot F_{OSC}}$ | $V_{IN}$=2.5V～20V | - | ±5 | - | % | ③ |
| Frequency Temperature Fluctuation | $\frac{\Delta F_{OSC}}{\Delta T_{OPR}\cdot F_{OSC}}$ | $V_{IN}$=5.0V Topr=-40～+85℃ | - | ±5 | - | % | ③ |
| Maximum Duty Cycle | MAXDTY | $V_{OUT}$=$V_{SS}$ | 100 | - | - | % | ④ |
| Minimum Duty Cycle | MINDTY | $V_{OUT}$=$V_{IN}$ | - | - | 0 | % | ④ |
| Current Limiter Voltage | $I_{LIM}$ | $V_{IN}$ pin voltage - $I_{SEN}$ pin voltage | 90 | 150 | 220 | mV | ⑥ |
| $I_{SEN}$ Current | $I_{ISEN}$ | $V_{IN}$=5.0V, $I_{SEN}$=5.0V | 4.5 | 7 | 13 | $\mu$A | ⑥ |
| CE "High" Current | $I_{CEH}$ | CE=$V_{IN}$=20.0V, $V_{OUT}$=0V | -0.1 | 0 | 0.1 | $\mu$A | ⑤ |
| CE "Low" Current | $I_{CEL}$ | CE=0V, $V_{IN}$=20.0V, $V_{OUT}$=0V | -0.1 | 0 | 0.1 | $\mu$A | ⑤ |
| CE "High" Voltage | $V_{CEH}$ | CLK Oscillation start, $V_{OUT}$=0V, CE : Voltage applied | 0.6 | - | - | V | ⑤ |
| CE "Low" Voltage | $V_{CEL}$ | CLK Oscillation stop, $V_{OUT}$=0V, CE : Voltage applied | - | - | 0.2 | V | ⑤ |
| EXT "High" ON Resistance | $R_{EXTH}$ | EXT=$V_{IN}$－0.4V, CE=$V_{OUT}$=$V_{IN}$ (*1) | - | 24 | 33 | Ω | ④ |
| EXT "Low" ON Resistance | $R_{EXTL}$ | EXT=0.4V, CE=$V_{IN}$, $V_{OUT}$=$V_{SS}$ (*1) | - | 22 | 31 | Ω | ④ |
| Efficiency (*2) | EFFI | | - | 93 | - | % | ① |
| Soft-start Time | $T_{SS}$ | Connect $C_{SS}$ and $R_{SS}$, CE : 0V→5.0V | 5 | 10 | 20 | ms | ① |
| CC/GAIN Pin Output Impedance | $R_{CCGAIN}$ | | - | 400 | - | kΩ | ⑦ |

Unless otherwise stated, $V_{IN}$=5.0V

NOTE:

*1: On resistance = 0.4V / measurement current
*2: EFFI = {[(output voltage) x (output current)] / [(input voltage) x (input current)]} x 100
*3: The capacity range of the condenser used to set the external CLK frequency is 180 ~ 300pF

## ■ELECTRICAL CHARACTERISTICS (Continued)

XC9201C50AKR                                                                                                  Ta=25℃

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS. | CIRCUITS |
|---|---|---|---|---|---|---|---|
| Output Voltage | $V_{OUT}$ | $I_{OUT}$=300mA | 4.875 | 5.000 | 5.125 | V | ① |
| Maximum Operating Voltage | $V_{INmax}$ | | 20 | - | - | V | ① |
| Minimum Operating Voltage | $V_{INmin}$ | | - | - | 2.200 | V | ① |
| U.V.L.O. Voltage | $V_{UVLO}$ | EXT voltage = High | 1.0 | 1.4 | 2.0 | V | ⑤ |
| Supply Current 1 | $I_{DD1}$ | $V_{IN}$=7.5V, CE=$V_{IN}$=$V_{OUT}$ | - | 115 | 220 | $\mu$A | ② |
| Supply Current 2 | $I_{DD2}$ | $V_{IN}$=20.0V, CE=$V_{IN}$, $V_{OUT}$=$V_{SS}$ | - | 130 | 235 | $\mu$A | ② |
| Stand-by Current | $I_{STB}$ | $V_{IN}$=7.5V, CE=$V_{OUT}$=$V_{SS}$ | - | 0.5 | 2.0 | $\mu$A | ② |
| CLK Oscillation Frequency | $F_{OSC}$ | RT=10.0k$\Omega$, CT=220pF | 280 | 330 | 380 | kHz | ③ |
| Frequency Input Stability | $\dfrac{\Delta F_{OSC}}{\Delta V_{IN} \cdot F_{OSC}}$ | $V_{IN}$=2.5V～20V | - | ±5 | - | % | ③ |
| Frequency Temperature Fluctuation | $\dfrac{\Delta F_{OSC}}{\Delta T_{OPR} \cdot F_{OSC}}$ | $V_{IN}$=7.5V $T_{opr}$=-40～+85℃ | - | ±5 | - | % | ③ |
| Maximum Duty Cycle | MAXDTY | $V_{OUT}$=$V_{SS}$ | 100 | - | - | % | ④ |
| Minimum Duty Cycle | MINDTY | $V_{OUT}$=$V_{IN}$ | - | - | 0 | % | ④ |
| Current Limiter Voltage | $I_{LIM}$ | $V_{IN}$ pin voltage - $I_{SEN}$ pin voltage | 90 | 150 | 220 | mV | ⑥ |
| $I_{SEN}$ Current | $I_{ISEN}$ | $V_{IN}$=7.5V, $I_{SEN}$=7.5V | 4.5 | 7.0 | 13.0 | $\mu$A | ⑥ |
| CE "High" Current | $I_{CEH}$ | CE=$V_{IN}$=20.0V, $V_{OUT}$=0V | -0.1 | 0 | 0.1 | $\mu$A | ⑤ |
| CE "Low" Current | $I_{CEL}$ | CE=0V, $V_{IN}$=20.0V, $V_{OUT}$=0V | -0.1 | 0 | 0.1 | $\mu$A | ⑤ |
| CE "High" Voltage | $V_{CEH}$ | CLK Oscillation start, $V_{OUT}$=0V, CE : Voltage applied | 0.6 | - | - | V | ⑤ |
| CE "Low" Voltage | $V_{CEL}$ | CLK Oscillation stop, $V_{OUT}$ =0V, CE : Voltage applied | - | - | 0.2 | V | ⑤ |
| EXT "High" ON Resistance | $R_{EXTH}$ | $V_{EXT}$=$V_{IN}$－0.4V, CE= $V_{OUT}$ =$V_{IN}$ (*1) | - | 21 | 29 | $\Omega$ | ④ |
| EXT "Low" ON Resistance | $R_{EXTL}$ | $V_{EXT}$=0.4V, CE=$V_{IN}$, $V_{OUT}$ =$V_{SS}$ (*1) | - | 20 | 27 | $\Omega$ | ④ |
| Efficiency [*2] | EFFI | | - | 93 | - | % | ① |
| Soft-start Time | Tss | Connect Css and Rss, CE : 0V→7.5V | 5 | 10 | 20 | ms | ① |
| CC/GAIN Pin Output Impedance | $R_{CCGAIN}$ | | - | 400 | - | k$\Omega$ | ⑦ |

Unless otherwise stated, $V_{IN}$=7.5V

NOTE:

　*1: On resistance = 0.4V / measurement current
　*2: EFFI = {[(output voltage) x (output current)] / [(input voltage) x (input current)]} x 100
　*3: The capacity range of the condenser used to set the external CLK frequency is 180 ~ 300pF

# ■ELECTRICAL CHARACTERISTICS (Continued)

XC9201D09AKR                                                                 Ta=25℃

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS | CIRCUITS |
|---|---|---|---|---|---|---|---|
| Output Voltage | $V_{OUT}$ | $I_{OUT}$=300mA | 0.8775 | 0.9000 | 0.9225 | V | ① |
| Maximum Operating Voltage | $V_{INmax}$ | | 20 | - | - | V | ① |
| Minimum Operating Voltage | $V_{INmin}$ | | - | - | 2.200 | V | ① |
| U.V.L.O. Voltage | $V_{UVLO}$ | EXT voltage = High | 1.0 | 1.4 | 2.0 | V | ⑤ |
| Supply Current 1 | $I_{DD1}$ | $V_{IN}$=4.0V, CE=$V_{IN}$=FB | - | 115 | 220 | $\mu$A | ② |
| Supply Current 2 | $I_{DD2}$ | $V_{IN}$=20.0V, CE=$V_{IN}$, FB=$V_{SS}$ | - | 130 | 235 | $\mu$A | ② |
| Stand-by Current | $I_{STB}$ | $V_{IN}$=4.0V, CE=FB=$V_{SS}$ | - | 0.5 | 2.0 | $\mu$A | ② |
| CLK Oscillation Frequency | $F_{OSC}$ | RT=10.0k$\Omega$, CT=220pF | 280 | 330 | 380 | kHz | ③ |
| Frequency Input Stability | $\dfrac{\Delta F_{OSC}}{\Delta V_{IN} \cdot F_{OSC}}$ | $V_{IN}$=2.5V～20V | - | ±5 | - | % | ③ |
| Frequency Temperature Fluctuation | $\dfrac{\Delta F_{OSC}}{\Delta T_{OPR} \cdot F_{OSC}}$ | $V_{IN}$=4.0V Topr=-40～+85℃ | - | ±5 | - | % | ③ |
| Maximum Duty Cycle | MAXDTY | FB=$V_{SS}$ | 100 | - | - | % | ④ |
| Minimum Duty Cycle | MINDTY | FB=$V_{IN}$ | - | - | 0 | % | ④ |
| Current Limiter Voltage | $I_{LIM}$ | $V_{IN}$ pin voltage - $I_{SEN}$ pin voltage | 90 | 150 | 220 | mV | ⑥ |
| $I_{SEN}$ Current | $I_{ISEN}$ | $V_{IN}$=4.0V, $I_{SEN}$=4.0V | 4.5 | 7 | 13 | $\mu$A | ⑥ |
| CE "High" Current | $I_{CEH}$ | CE=$V_{IN}$=20.0V, $V_{OUT}$=0V | -0.1 | 0 | 0.1 | $\mu$A | ⑤ |
| CE "Low" Current | $I_{CEL}$ | CE=0V, $V_{IN}$=20.0V, $V_{OUT}$=0V | -0.1 | 0 | 0.1 | $\mu$A | ⑤ |
| CE "High" Voltage | $V_{CEH}$ | CLK Oscillation start, $V_{OUT}$=0V, CE：Voltage applied | 0.6 | - | - | V | ⑤ |
| CE "Low" Voltage | $V_{CEL}$ | CLK Oscillation stop, $V_{OUT}$=0V, CE：Voltage applied | - | - | 0.2 | V | ⑤ |
| EXT "High" ON Resistance | $R_{EXTH}$ | EXT=$V_{IN}$－0.4V, CE=FB=$V_{IN}$ (*1) | - | 27 | 40 | $\Omega$ | ④ |
| EXT "Low" ON Resistance | $R_{EXTL}$ | EXT=0.4V, CE=$V_{IN}$, FB=$V_{SS}$ (*1) | - | 24 | 34 | $\Omega$ | ④ |
| Efficiency [*2] | EFFI | | - | 93 | - | % | ① |
| Soft-start Time | Tss | Connect Css and Rss, CE：0V→4.0V | 5 | 10 | 20 | ms | ① |
| CC/GAIN Pin Output Impedance | $R_{CCGAIN}$ | | - | 400 | - | k$\Omega$ | ⑦ |

Unless otherwise stated, $V_{IN}$=4.0V

NOTE:

*1: On resistance = 0.4V / measurement current
*2: EFFI = {[(output voltage) x (output current)] / [(input voltage) x (input current)]} x 100
*3: The capacity range of the condenser used to set the external CLK frequency is 180 ~ 300pF

## ■TYPICAL APPLICATION CIRCUITS

XC9201C33AKR
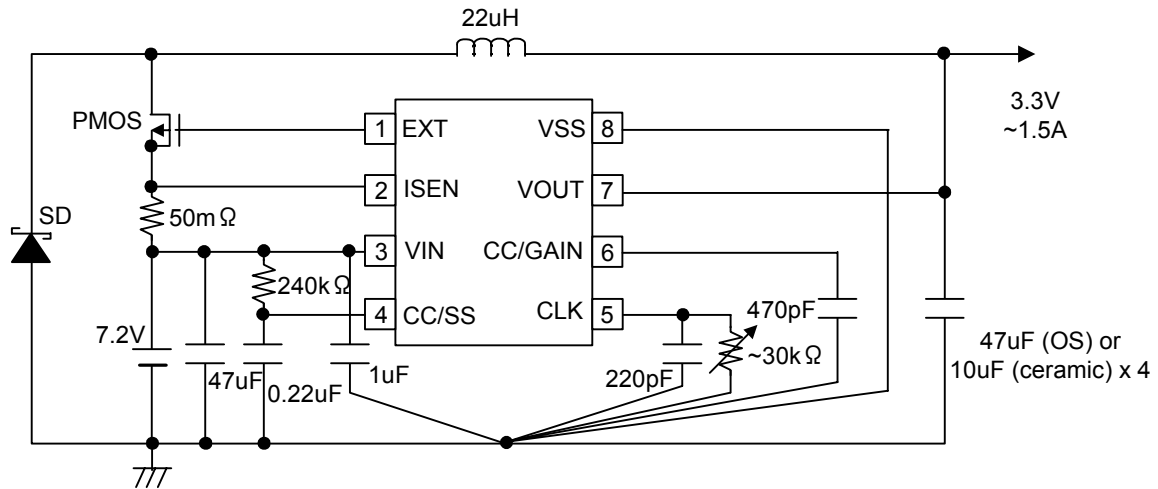


PMOS      : XP132A11A1SR (TOREX)
Coil        : 22 $\mu$ H (CR105 SUMIDA)
Resistor   : 50m $\Omega$ for I$_{SEN}$ (NPR1 KOA), 30k $\Omega$ (trimmer) for CLK, 240k $\Omega$ for SS
Capacitors : 220pF (ceramic) for CLK, 470pF (ceramic) for CC/GAIN, 0.22 $\mu$ F (any) for SS,1 $\mu$ F (ceramic) for Bypass
              47 $\mu$ F (OS) or 10 $\mu$ F (ceramic) x 4 for C$_L$, 47 $\mu$ F (tantalum) for C$_{IN}$
SD          : U3FWJ44N (TOSHIBA)


XC9201C50AKR
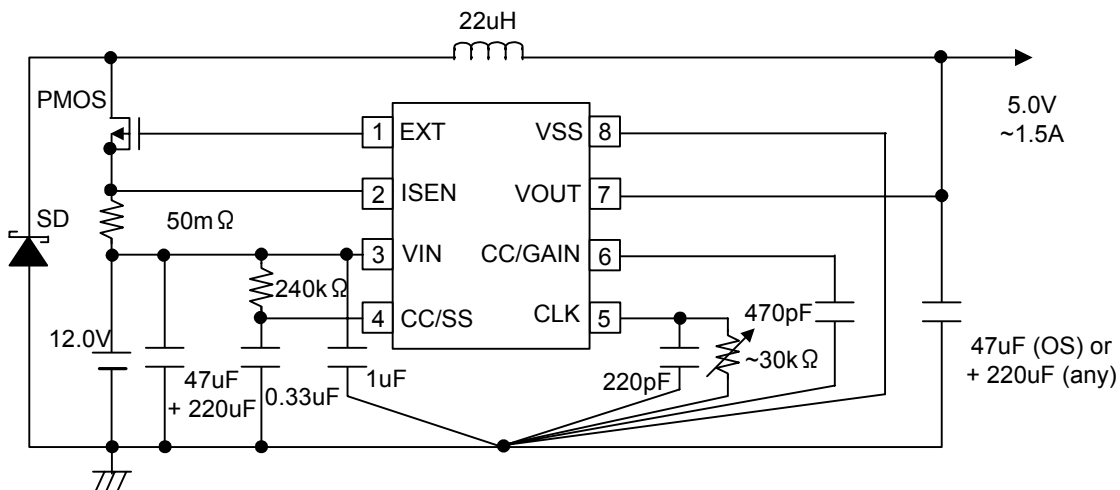


PMOS      : XP132A11A1SR (TOREX)
Coil        : 22 $\mu$ H (CDRH127 SUMIDA)
Resistor   : 20m $\Omega$ for I$_{SEN}$ (NPR1 KOA), 30k $\Omega$ (trimmer) for CLK, 240k $\Omega$ for SS
Capacitors : 220pF (ceramic) for CLK, 470pF (ceramic) for CC/GAIN, 0.33 $\mu$ F (any) for SS, 1 $\mu$ F (ceramic) for Bypass
              47 $\mu$ F (OS) + 220 $\mu$ F (any) for C$_L$, 47 $\mu$ F (tantalum) + 220 $\mu$ F (any) for C$_{IN}$
SD          : U3FWJ44N (TOSHIBA)

# ■TYPICAL APPLICATION CIRCUITS (Continued)

XC9201D09AKR
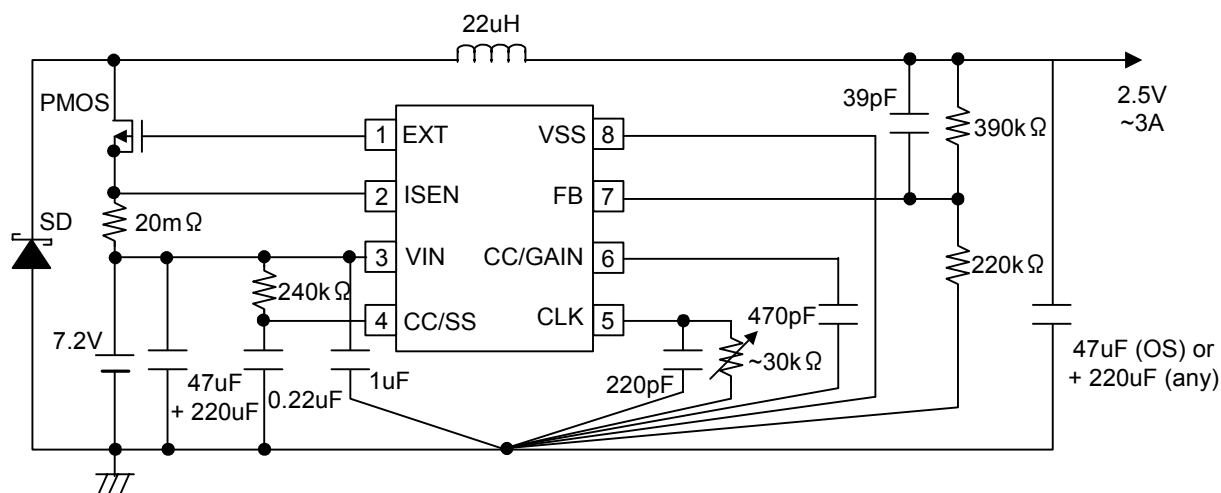


PMOS      : XP132A11A1SR (TOREX)
Coil       : 22$\mu$H (CDRH127 SUMIDA)
Resistors  : 20m$\Omega$ for I$_{SEN}$ (NPR1 KOA), 30k$\Omega$ (trimmer) for CLK, 240k$\Omega$ for SS, 390k$\Omega$ for Output Voltage
             220k$\Omega$ for Output Voltage
Capacitors : 220pF (ceramic) for CLK, 470pF (ceramic) for CC/GAIN, 0.22$\mu$F (any) for SS, 1$\mu$F (ceramic) for Bypass
             39pF (ceramic) for FB, 47$\mu$F (OS) for C$_L$, 47$\mu$F (tantalum) + 220$\mu$F(any) for C$_{IN}$
SD         : U3FWJ44N (TOSHIBA)

XC9201D09AKR
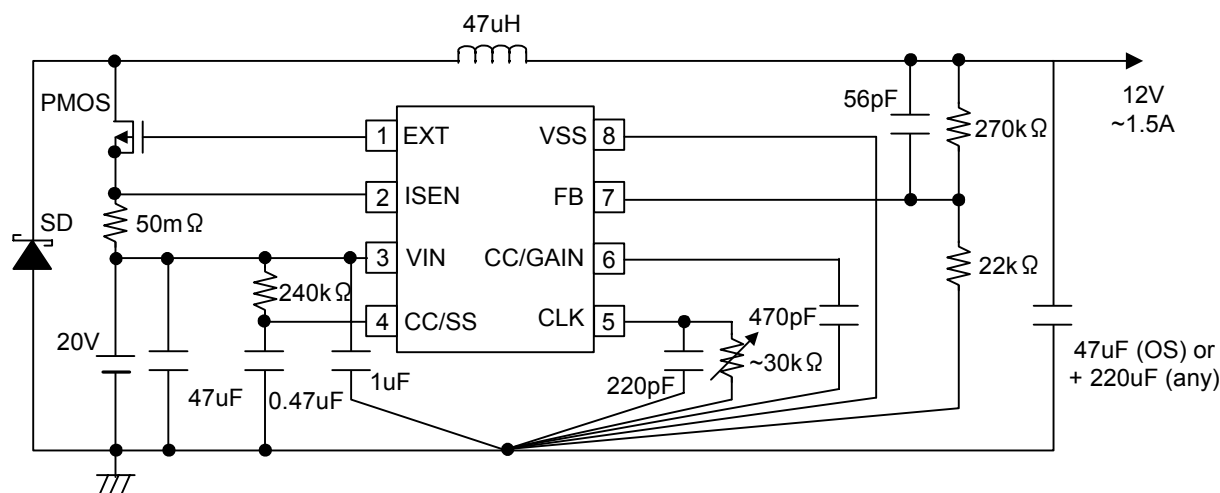


PMOS      : XP132A11A1SR (TOREX)
Coil       : 47$\mu$H (CR105 SUMIDA)
Resistor   : 50m$\Omega$ for I$_{SEN}$ (NPR1 KOA), 30k$\Omega$ (trimmer) for CLK, 240k$\Omega$  for SS, 270k$\Omega$ for Output Voltage
             22k$\Omega$ (trimmer) for Output Voltage
Capacitors : 220pF (ceramic) for CLK, 470pF (ceramic) for CC/GAIN, 0.47$\mu$F (any) for SS, 1$\mu$F (ceramic) for Bypass
             56pF (ceramic) for FB, 47$\mu$F (OS) + 20$\mu$F (any) for C$_L$, 47$\mu$F (tantalum) + 220$\mu$F (any) for C$_{IN}$
SD         : U3FWJ44N (TOSHIBA)

## ■OPERATIONAL EXPLANATION

Step-down DC/DC converter controllers of the XC9201series carry out pulse width modulation (PWM) according to the multiple feedback signals of the output voltage and coil current.

The internal circuits consist of different blocks that operate at $V_{IN}$ or the stabilized power (2.0V) of the internal regulator. The output setting voltage of type C controller and the FB pin voltage (Vref=0.9 V) of type D controller have been adjusted and set by laser-trimming.

<Clock>
With regard to clock pulses, a capacitor and resistor connected to the CLK pin generate ramp waveforms whose top and bottom are 0.7V and 0.15V, respectively. The frequency can be set within a range of 100 to 600 kHz externally (refer to the "Functional Settings" section for further information). The clock pulses are processed to generate a signal used for synchronizing internal sequence circuits.

<Verr Amplifier>
The Verr amplifier is designed to monitor the output voltage. A fraction of the voltage applied to internal resistors R1, R2 in the case of a type C controller, and the voltage of the FB pin in the case of a type D controller, are fed back and compared with the reference voltage. In response to feedback of a voltage lower than the reference voltage, the output voltage of the Verr amplifier increases.

The output of the Verr amplifier enters the mixer via resistor (RVerr). This signal works as a pulse width control signal during PWM operations. By connecting an external capacitor and resistor through the CC/GAIN pin, it is possible to set the gain and frequency characteristics of Verr amplifier signals (refer to the "Functional Settings" section for further information).

<Ierr Amplifier>
The Ierr amplifier monitors the coil current. The potential difference between the $V_{IN}$ and $I_{SEN}$ pins is sampled at each switching operation. Then the potential difference is amplified or held, as necessary, and input to the mixer. The Ierr amplifier outputs a signal ensuring that the greater the potential difference between the $V_{IN}$ and $I_{SEN}$ pins, the smaller the switching current. The gain and frequency characteristics of this amplifier are fixed internally.

<Mixer and PWM>
The mixer modulates the signal sent from Verr by the signal from Ierr. The modulated signal enters the PWM comparator for comparison with the saw-tooth pulses generated at the CLK pin. If the signal is greater than the saw-tooth waveforms, a signal is sent to the output circuit to turn on the external switch.

<Current Limiter>
The current flowing through the coil is monitored by the limiter comparator via the $V_{IN}$ and $I_{SEN}$ pins. The limiter comparator outputs a signal when the potential difference between the $V_{IN}$ and $I_{SEN}$ pins reaches 150mV or more. This signal is converted to a logic signal and handled as a DFF reset signal for the internal limiter circuit. When a reset signal is input, a signal is output immediately at the EXT pin to turn off the MOS switch. When the limiter comparator sends a signal to enable data acceptance, a signal to turn on the MOS switch is output at the next clock pulse. If at this time the potential difference between the $V_{IN}$ and $I_{SEN}$ pins is large, operation is repeated to turn off the MOS switch again. DFF operates in synchronization with the clock signal of the CLK pin.
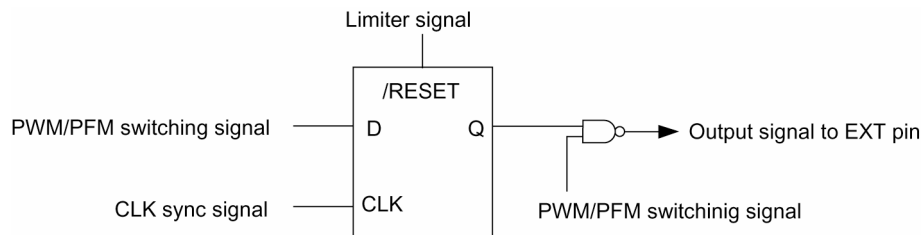
<Soft-Start>
The soft start function is made available by attaching a capacitor and resistor to the CE/SS pin. The Vref voltage applied to the Verr amplifier is restricted by the start-up voltage of the CE/SS pin. This ensures that the Verr amplifier operates with its two inputs in balance, thereby preventing the ON-TIME signal from becoming stronger than necessary. Consequently, soft start time needs to be set sufficiently longer than the time set to CLK. The start-up time of the CE/SS pin equals the time set for soft start (refer to the "Functional Settings" section for further information).

The soft start function operates when the voltage at the CE/SS pin is between 0V to 1.55V. If the voltage at the CE/SS pin doesn't start from 0V but from a mid level voltage when the power is switched on, the soft start function will become ineffective and the possibilities of large inrush currents and ripple voltages occurring will be increased.

Under Voltage Lock Out (U.V.L.O.) is also provided. This function is activated to turn off the MOS switch attached to the EXT pin when the input voltage ($V_{IN}$) decreases to approximately 1.4 V or below. The purpose of this function is to keep the external MOS switch from turning on when a voltage at which the IC operates unstably is applied. U.V.L.O. also restricts signals during soft start so that the external MOS switch does not turn on until the internal circuitry becomes stable.

# ■OPERATIONAL EXPLANATION (Continued)

●Functional Settings

1. Soft-Start

CE and soft-start (SS) functions are commonly assigned to the CE/SS pin.   The soft start function is effective until the voltage at the CE pin reaches approximately 1.55V rising from 0V.   Soft start time is approximated by the equation below according to values of Vcont, Rss, and Css.
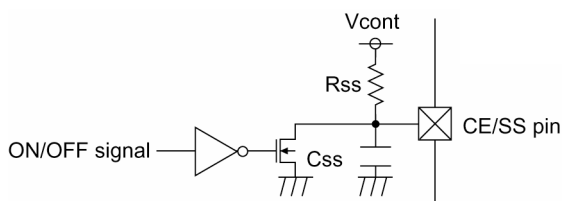
$$T = -Css \times Rss \times ln((Vcont-1.55)/Vcont)$$

Example: When Css=0.1$\mu$F, Rss=470k$\Omega$, and Vcont=5V, $T = -0.1 \times 10^{-6} \times 470 \times 10^{3} \times ln((5-1.55)/5)=17.44ms$.
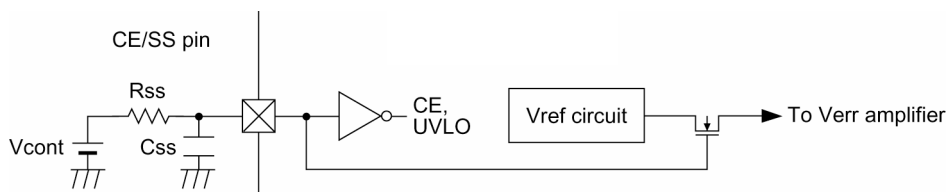
Set the soft-start time to a value sufficiently longer than the period of a clock pulse.

> Circuit example 1: N-ch open drain

> Circuit example 2: CMOS logic (low current dissipation)
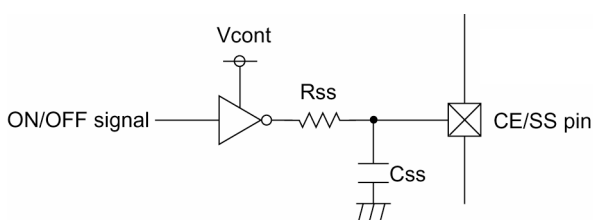
> Circuit example 3: CMOS logic (low current dissipation)
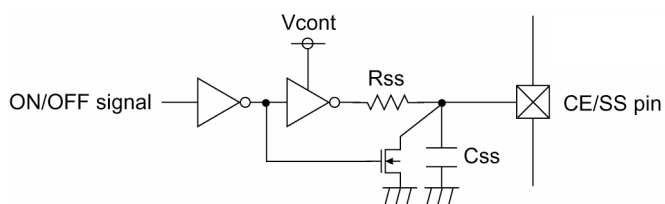
# ■OPERATIONAL EXPLANATION (Continued)

●Functional Settings (Continued)

### 2. Oscillation Frequency

The oscillation frequency of the internal clock generator is approximated by the following equation according to the values of the capacitor and resistor attached to the CLK pin.   To stabilize the IC's operation, set the oscillation frequency within a range of 100kHz to 600kHz.   Select a value for Cclk within a range of 180pF to 300pF and fix the frequency based on the value for Rclk.

$$f = 1/ (-Cclk \times Rclk \times ln\ 0.26)$$

Example: When Cclk = 220pF and Rclk = 10 kΩ, $f = 1/(- 220 \times 10^{-12} \times 10 \times 10^3 \times ln(0.26)) = 337.43\ kHz$.
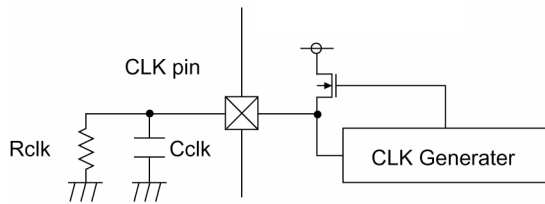


### 3. Gain and Frequency Characteristics of the Verr Amplifier

The gain at output and frequency characteristics of the Verr amplifier are adjusted by the values of capacitor and resistor attached to the CC/GAIN pin.   It is generally recommended to attach a C_GAIN of 220 to 1,000pF without an R_GAIN.   The greater the C_GAIN value, the more stable the phase and the slower the transient response.   When using the IC with R_GAIN connected, it should be noted that if the R_GAIN resistance value is too high, abnormal oscillation may occur during transient response time.   The size of R_GAIN should be carefully determined and connected.
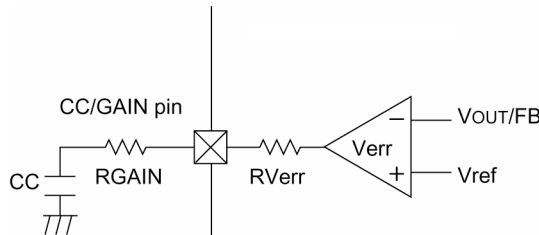


### 4. Current Limit

The current limit value is approximated by the following equation according to resistor $R_{SEN}$ inserted between the $V_{IN}$ and $I_{SEN}$ pins.   Double function, current FB input and current limit, is assigned to the $I_{SEN}$ pin.   The current limit value is approximated by the following equation according to the value for $R_{SEN}$.

$$ILpeak\_limit = 0.15 / R_{SEN}$$

Example: When $R_{SEN}$ = 100 mΩ, $ILpeak\_limit = 0.15 / 0.1 = 1.5\ A$
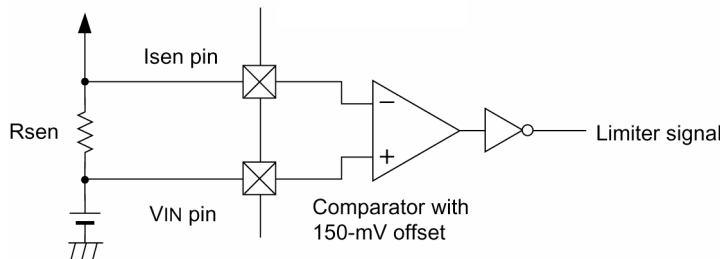


Because of the feedback at the internal error amp with this IC (which is brought about as a result of the phase compensation of the voltage generated at $R_{SEN}$, which is in turn caused by current flowing through the coil when the PMOS is working.), should the value of the $R_{SEN}$ resistor be too large, the feedback signal will also increase and intermittent oscillation may occur.   We therefore recommend that you carefully check the value for $R_{SEN}$ should you have a problem with oscillation. During normal operations, a voltage will be generated at RSEN as a result of the coil's peak current.   Please ensure that this voltage is less than the current limit voltage, which is 90mV (min.).
For $R_{SEN}$ resistor's rated power, please refer to NOTES ON USE, External Components, RSENSE Resistor.

# ■OPERATIONAL EXPLANATION (Continued)

● Functional Settings (Continued)

5. FB Voltage and $C_{FB}$

With regard to the XC9201D series, the output voltage is set by attaching externally divided resistors. The output voltage is determined by the equation shown below according to the values of $R_{FB1}$ and $R_{FB2}$. In general, the sum of $R_{FB1}$ and $R_{FB2}$ should be 1 MΩ or less.
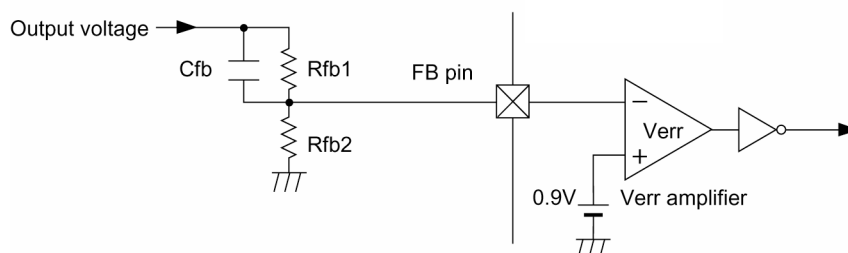
$$V_{OUT} = 0.9 \times (R_{FB1} + R_{FB2}) / R_{FB2}$$

The value of $C_{FB}$ (phase compensation capacitor) is approximated by the following equation according to the values of $R_{FB1}$ and fzfb. The value of fzfb should be 10 kHz, as a general rule.

$$C_{FB} = 1/(2 \times \pi \times R_{FB1} \times fzfb)$$

Example: When $R_{FB1}$ = 455 kΩ and $R_{FB2}$ = 100 kΩ : $V_{OUT}$ = 0.9 x (455 k + 100 k)/100 k = 4.995 V

: $C_{FB}$= 1/(2 x $\pi$ x 455 k x 10 k) = 34.98 pF.



# ■APPLICATION NOTES

1. The XC9201 series are designed for use with an output ceramic capacitor. If, however, the potential difference between input and output is too large, a ceramic capacitor may fail to absorb the resulting high switching energy and oscillation could occur on the output side. If the input-output potential difference is large, connect an electrolytic capacitor in parallel to compensate for insufficient capacitance.

2. The EXT pin of the XC9201 series is designed to minimize the through current that occurs in the internal circuitry. However, the gate drive of external PMOS has a low impedance for the sake of speed. Therefore, if the input voltage is high and the bypass capacitor is attached away from the IC, the charge/discharge current to the external PMOS may lead to unstable operations due to switching operation of the EXT pin.
As a solution to this problem, place the bypass capacitor as close to the IC as possible, so that voltage variations at the $V_{IN}$ and $V_{SS}$ pins caused by switching are minimized. If this is not effective, insert a resistor of several to several tens of ohms between the EXT pin and PMOS gate. Remember that the insertion of a resistor slows down the switching speed and may result in reduced efficiency.

3. A PNP transistor can be used in place of PMOS. If using a PNP transistor, insert a resistor ($R_B$) and capacitor ($C_B$) between the EXT pin and the base of the PNP transistor in order to limit the base current without slowing the switching speed. Adjust $R_B$ in a range of 500Ω to 1kΩ according to the load and hFE of the transistor. Use a ceramic capacitor for $C_B$, complying with $C_B \leqq 1/( 2 \times \pi \times R_B \times F_{OSC} \times 0.7)$, as a rule.
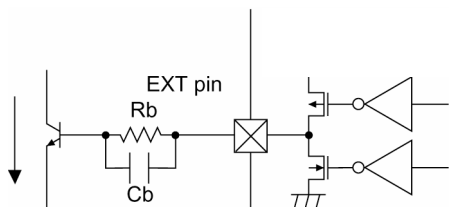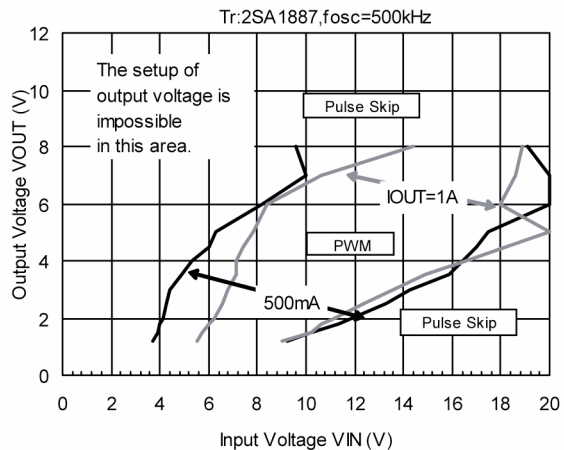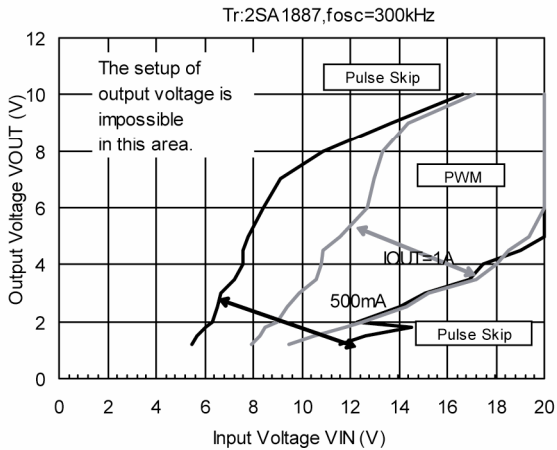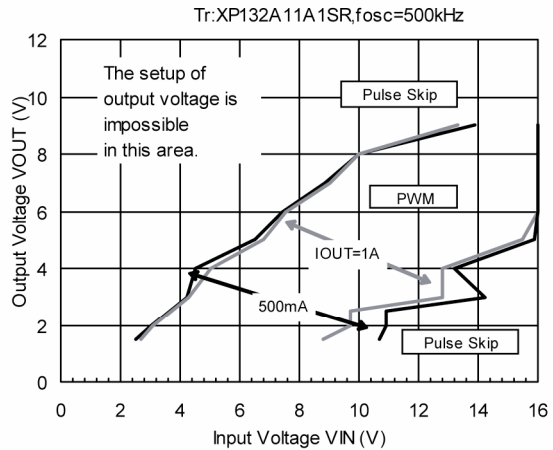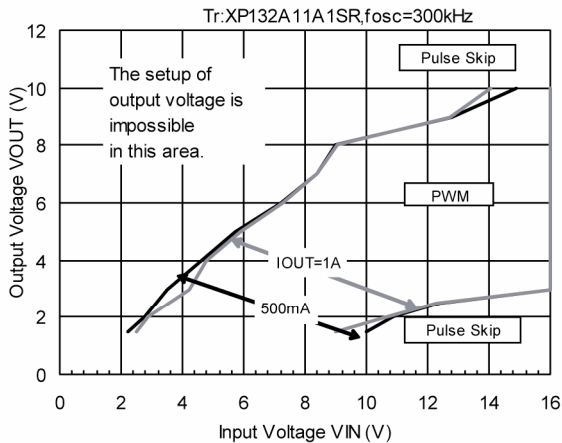


4. This IC incorporates a limit comparator to monitor the voltage produces across the $R_{SEN}$ resistor at the current peak of the coil. It functions as a limiter when, for example, the output is short-circuited. In such a case, the limit comparator senses that the voltage across the $R_{SEN}$ resistor has reached a current-limiting voltage (typically 150mV) and outputs a signal to turn off the external transistor. After sensing a current-limit voltage, the limit comparator typically takes 200nsec (TYP.) before it turns off the external resistor. During this time, the voltage across the $R_{SEN}$ resistor can exceed the current-limit voltage, especially when the difference between the input voltage and the output voltage is large and the coil inductance is small. Therefore, exercise great care in selecting absolute maximum ratings of the external transistor, coil, and Schottky diode.

5. If the difference between the input voltage and the output voltage is large or small, the switching ON time or OFF time of this IC becomes short and actual operation can be critically influenced by values of peripheral components 'inductance of coil, resistance of CLK connection, capacitance of capacitor, etc.) Before use, it is recommended to evaluate this IC thoroughly with an actual unit.

**TOREX**

## ■APPLICATION NOTES (Continued)

6. The series are designed to operate in PWM control.   However, there is the possibility that some cycles may be skipped depending on the operational conditions.   Please use the following output voltage vs. input voltage characteristics for reference.   Verification using actual devices is recommended.   It should be noted that when $C_{CLK}$ is connected to $V_{IN}$, the influence of noise is lessened and the input and output voltage ranges as well as the output current range in which stable operation is possible is widened.   It is recommended that you refer to the "Oscillation Frequency" Functional Settings for setting up the oscillation frequency.   If using a MOSFET, please pay particular attention to the gate breakdown voltage.   In the following graphs, because the gate breakdown voltage of the MOSFET used was 20V, input voltages over 16V were not measured.   Please use a bipolar transistor in applications where higher input voltages are required.

● Operational Control Characteristics

○ XC9201D09AKR      $C_{CLK}$ $V_{IN}$ Connection



SD:  D1FH3
L:  CDRH127 / LD-220 (22uH)
$C_{IN}$:  TMK432BJ106KM (25V / 10uF) x 3
$C_L$:  JMK325BJ226MM (6.3V / 22uF) x 3
$C_{DD}$:  UMK325BJ105KH (50V / 1uF)
$R_{SEN}$:  50m$\Omega$
$R_{CLK}$:  11k$\Omega$  (300kHz), 6.8k$\Omega$  (500kHz)
$C_{CLK}$:  220pF
$C_{CC}$:  330pF
$R_{CC}$:  0$\Omega$
$R_B$(2SA1887):  7k$\Omega$  (300kHz), 16k$\Omega$  (500kHz)
$R_{SS}$:  1M$\Omega$
$C_{SS}$:  0.1uF
$R_{FB1}$:  330k$\Omega$
$C_{FB}$:  47pF
$R_{FB2}$:  0.9 x $R_{FB1}$ / ($V_{OUT}$-0.9V)

CCLK VIN Connection Circuit

# ■APPLICATION NOTES (Continued)

● Operational Control Characteristics (Continued)
○ XC9201D09AKR  C_CLK GND Connection

Tr:XP132A11A1SR,fosc=300kHz

The setup of
output voltage is
impossible
in this area.

Pulse Skip

PWM

IOUT=1A

500mA

Pulse Skip

Tr:XP132A11A1SR,fosc=500kHz

The setup of
output voltage is
impossible
in this area.

Pulse Skip

PWM

IOUT=1A

500mA

Pulse Skip

Tr:2SA1887,fosc=300kHz

The setup of
output voltage is
impossible
in this area.

Pulse Skip

PWM

IOUT
=1A

500mA

Pulse Skip

Tr:2SA1887,fosc=500kHz

The setup of
output voltage is
impossible
in this area.

Pulse Skip

IOUT=1A

PWM

500mA

Pulse Skip

C_CLK GND Connecton Circuit

SD:    D1FH3
L:    CDRH127 / LD-220 (22uH)
C_IN:    TMK432BJ106KM (25V / 10uF) x 3
C_L:    JMK325BJ226MM (6.3V / 22uF) x 3
C_DD:    UMK325BJ105KH (50V / 1uF)
R_SEN:    50mΩ
R_CLK:    11kΩ  (300kHz), 6.8kΩ  (500kHz)
C_CLK:    220pF
C_CC:    330pF
R_CC:    0Ω
R_B(2SA1887):    7kΩ  (300kHz), 16kΩ  (500kHz)
R_SS:    1MΩ
C_SS:    0.1uF
R_FB1:    330kΩ
C_FB:    47pF
R_FB2:    0.9V x R_FB1 / (V_OUT-0.9V)

TOIREX

# ■INSTRUCTION ON PATTERN LAYOUT

①In order to stabilize VDD's voltage level, we recommend that a by-pass condenser (CDD) be connected as close as possible to the VIN & VSS pins.

②In order to stabilize the GND voltage level which can fluctuate as a result of switching, we suggest that C_CLK's, R_CLK's & C_GAIN's GND be separated from Power GND and connected as close as possible to the VSS pin (by-pass condenser, CDD).   Please use a multi layer board and check the wiring carefully.

**Pattern Layout Examples**

**XC9201 Series (D Series)**

2 layer Evaluation Board
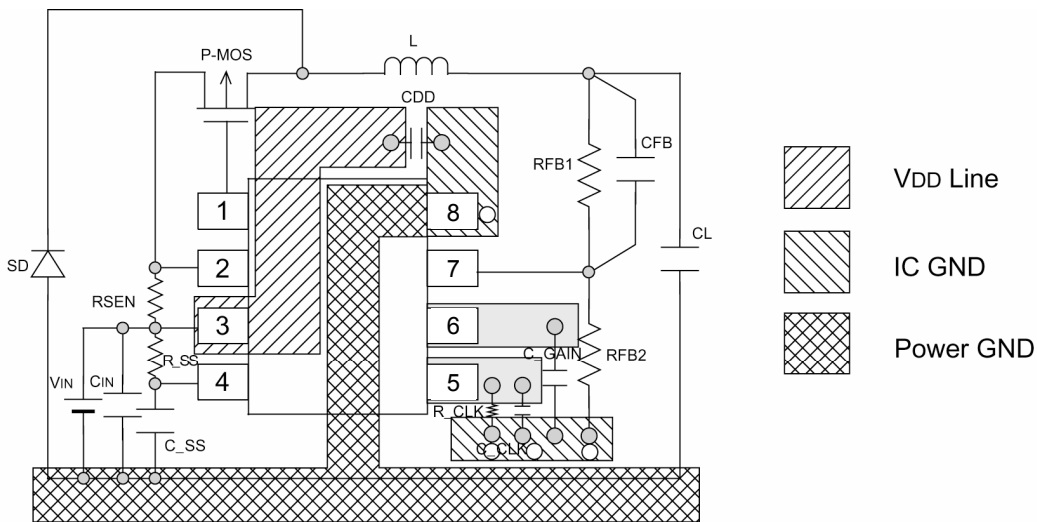


○   Through Hole
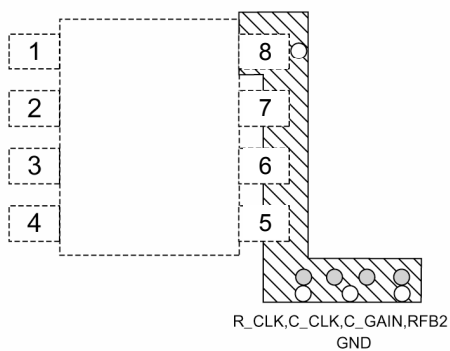


○   Through Hole

# ■INSTRUCTION ON PATTERN LAYOUT (Continued)

1 layer Evaluation Board
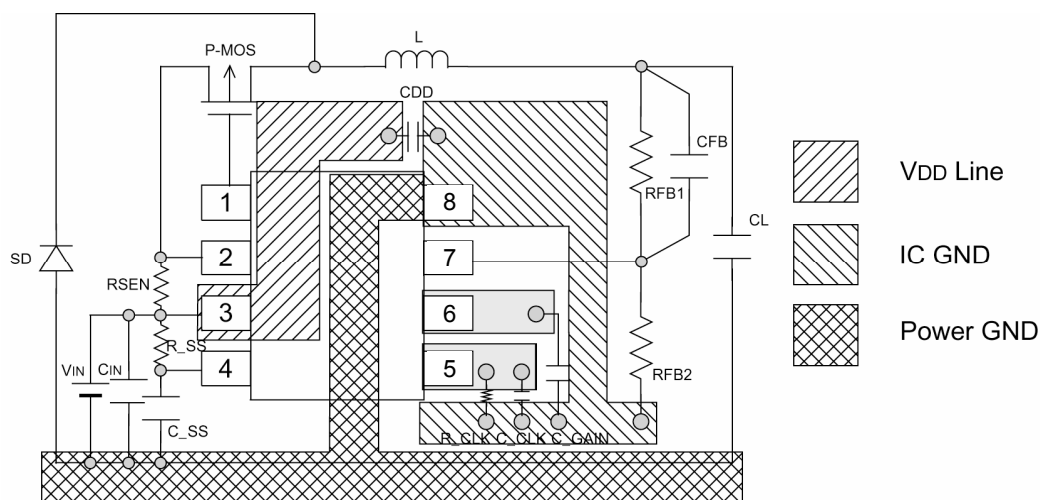


# ■NOTES ON USE

Ensure that the absolute maximum ratings of the external components and the XC9201 DC/DC IC itself are not exceeded. We recommend that sufficient counter measures are put in place to eliminate the heat that may be generated by the external P-ch MOSFET as a result of switching losses.

Try to use a P-ch MOSFET with as small a gate capacitance as possible in order to avoid overly large output spike voltages that may occur (such spikes occur in proportion to gate capacitance). The performance of the XC9201 DC/DC converter is greatly influenced by not only its own characteristics, but also by those of the external components it is used with. We recommend that you refer to the specifications of each component to be used and take sufficient care when selecting components.

Wire external components as close to the IC as possible and use thick, short connecting wires to reduce wiring impedance. In particular, minimize the distance between the by-pass capacitor and the IC.

Make sure that the GND wiring is as strong as possible as variations in ground potential caused by ground current at the time of switching may result in unstable operation of the IC. Specifically, strengthen the ground wiring in the proximity of the Vss pin.

●External Components

RSENSE Resistor

A low value resistor is defined as a resistor with a 10Ω value or lower. For RSENSE, the XC9201 series uses a resistor with a value of either 50mΩ or 100mΩ. Although resistors for RSENSE are classified as low resistance chip resistors or current limit resistors (which may give the impression that the RSENSE resistor is expensive), it is not necessary to use expensive low resistance chip resistors as general purpose chip resistors with values of 50mΩ or 100mΩ will do the job just as well.

When choosing the RSENSE resistor, it is important to confirm the resistor's power consumption, which can be done using the following equation:

$$W \text{ (Power Consumption)} = I \text{ (Current)} \times V \text{ (Voltage)}$$

$$= I \text{ (Current)} \times I \text{ (Current)} \times R \text{ (Resistance)}$$

It is recommended that a resistor which has a power rating of more than 3 times the power consumption of RSENSE be selected (refer to the example given below):

*(ex.)   RSENSE = 100mΩ, I = 1A*

I = 1A  ⟶

RSENSE = 100mΩ (0.1Ω)

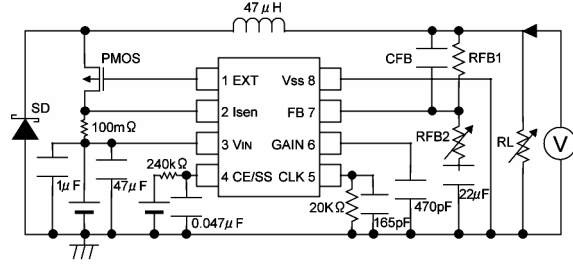*Power supply W = 1 x 1 x 0.1 = 0.1 [W]*        0.5W, 100mΩ  resistor should be used

## ■TEST CIRCUITS

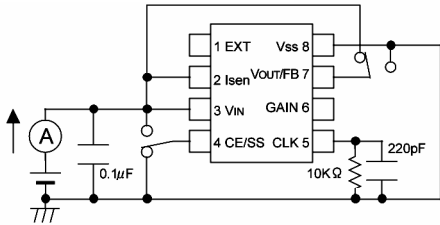### Circuit ① (VOUT Type)
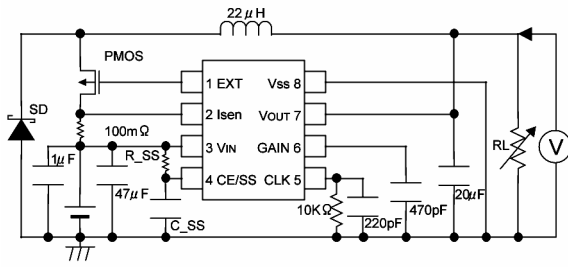


XC9201C25A  R_SS : 188kΩ  C_SS : 0.1μF
XC9201C33A  R_SS : 270kΩ  C_SS : 0.1μF
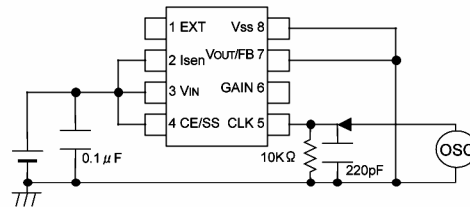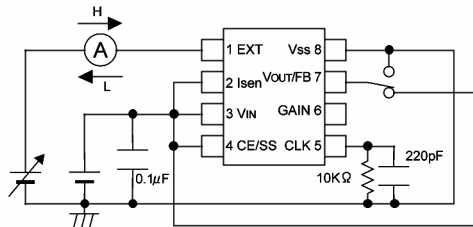XC9201C50A  R_SS : 430kΩ  C_SS : 0.1μF
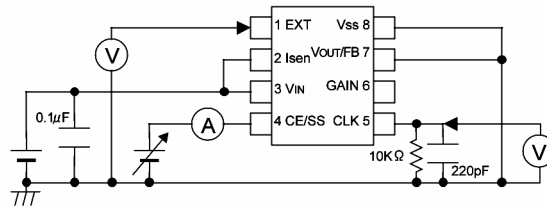
### Circuit ① (FB Type)



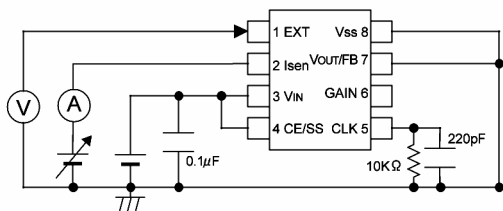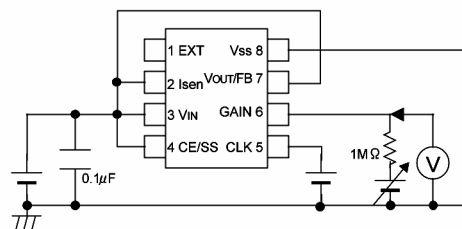### Circuit ②



### Circuit ③



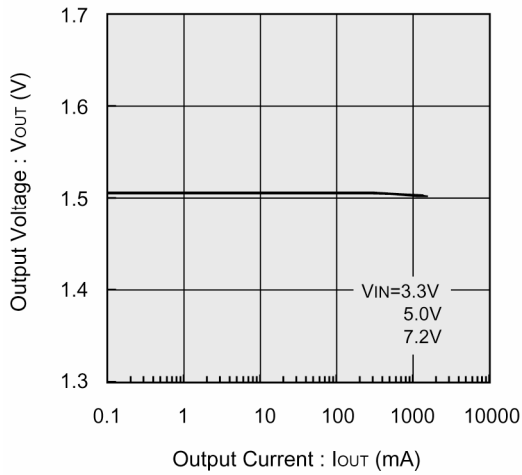### Circuit ④



### Circuit ⑤



### Circuit ⑥



### Circuit ⑦

# ■TYPICAL PERFORMANCE CHARACTERISTICS

XC9201D09AKR

(1) Output Voltage vs. Output Current
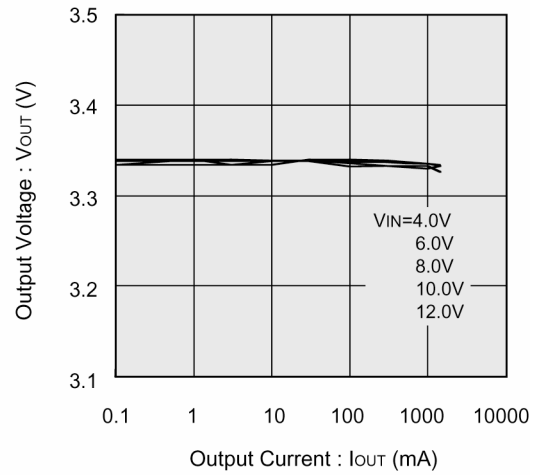
V$_{OUT}$ 1.5V, F$_{OSC}$ : 330kHz

L=22$\mu$H, C$_L$=40$\mu$F (Ceramic), C$_{IN}$=30$\mu$F (Ceramic)
R$_{SEN}$=50m$\Omega$, C$_{DD}$=1$\mu$F (Ceramic), SD:U3FWJ44N
C$_{GAIN}$=470pF (Ceramic), Tr:XP162A11C0PR

V$_{OUT}$ 3.3V, F$_{OSC}$ : 330kHz

L=22$\mu$H, C$_L$=40$\mu$F (Ceramic), C$_{IN}$=30$\mu$F (Ceramic)
R$_{SEN}$=50m$\Omega$, C$_{DD}$=1$\mu$F (Ceramic), SD:U3FWJ44N
C$_{GAIN}$=470pF (Ceramic), Tr:XP162A11C0PR

V$_{OUT}$ 5.0V, F$_{OSC}$ : 330kHz

L=22$\mu$H, C$_L$=40$\mu$F (Ceramic), C$_{IN}$=30$\mu$F (Ceramic)
R$_{SEN}$=50m$\Omega$, C$_{DD}$=1$\mu$F (Ceramic), SD:U3FWJ44N
C$_{GAIN}$=470pF (Ceramic), Tr:XP162A11C0PR

V$_{OUT}$ 12.0V, F$_{OSC}$ : 100kHz

L=68$\mu$H, C$_L$=40$\mu$F (Ceramic), C$_{IN}$=30$\mu$F (Ceramic)
R$_{SEN}$=50m$\Omega$, C$_{DD}$=10$\mu$F (Ceramic), SD:U3FWJ44N
C$_{GAIN}$=470pF (Ceramic), Tr:XP132A11C0PR

# ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)
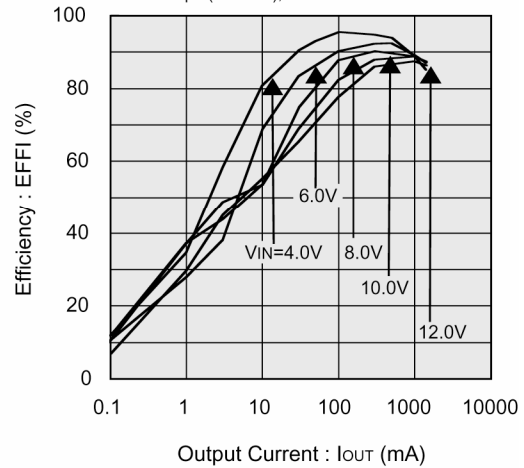
(2) Efficiency vs. Output Current

V$_{OUT}$ 1.5V, F$_{OSC}$ : 330kHz

L=22$\mu$H, C$_L$=40$\mu$F (Ceramic), C$_{IN}$=30$\mu$F (Ceramic)
R$_{SEN}$=50m$\Omega$, C$_{DD}$=1$\mu$F (Ceramic), SD:U3FWJ44N
C$_{GAIN}$=470pF (Ceramic), Tr:XP162A11C0PR



V$_{OUT}$ 3.3V, F$_{OSC}$ : 330kHz

L=22$\mu$H, C$_L$=40$\mu$F (Ceramic), C$_{IN}$=30$\mu$F (Ceramic)
R$_{SEN}$=50m$\Omega$, C$_{DD}$=1$\mu$F (Ceramic), SD:U3FWJ44N
C$_{GAIN}$=470pF (Ceramic), Tr:XP162A11C0PR



V$_{OUT}$ 5.0V, F$_{OSC}$ : 330kHz

L=22$\mu$H, C$_L$=40$\mu$F (Ceramic), C$_{IN}$=30$\mu$F (Ceramic)
R$_{SEN}$=50m$\Omega$, C$_{DD}$=1$\mu$F (Ceramic), SD:U3FWJ44N
C$_{GAIN}$=470pF (Ceramic), Tr:XP162A11C0PR



V$_{OUT}$ 12.0V, F$_{OSC}$ : 100kHz

L=68$\mu$H, C$_L$=40$\mu$F (Ceramic), C$_{IN}$=30$\mu$F (Ceramic)
R$_{SEN}$=50m$\Omega$, C$_{DD}$=10$\mu$F (Ceramic), SD:U3FWJ44N
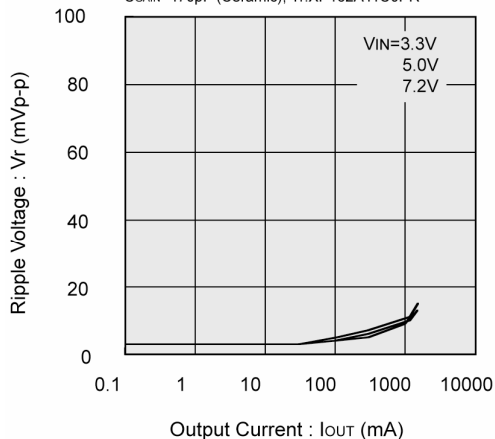C$_{GAIN}$=470pF (Ceramic), Tr:XP132A11C0PR



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# ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)
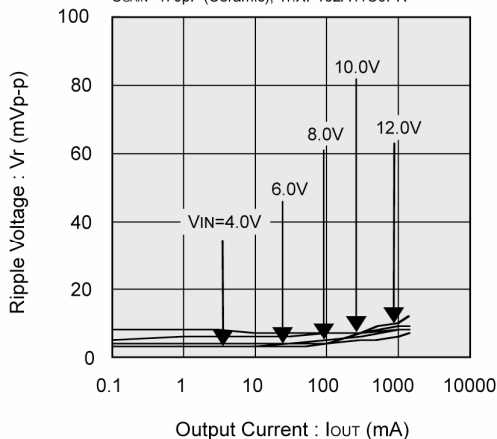
(3) Ripple Voltage vs. Output Current

V$_{OUT}$ 1.5V, F$_{OSC}$ : 330kHz

L=22$\mu$H, C$_L$=40$\mu$F (Ceramic), C$_{IN}$=30$\mu$F (Ceramic)
R$_{SEN}$=50m$\Omega$, C$_{DD}$=1$\mu$F (Ceramic), SD:U3FWJ44N
C$_{GAIN}$=470pF (Ceramic), Tr:XP162A11C0PR



V$_{OUT}$ 3.3V, F$_{OSC}$ : 330kHz

L=22$\mu$H, C$_L$=40$\mu$F (Ceramic), C$_{IN}$=30$\mu$F (Ceramic)
R$_{SEN}$=50m$\Omega$, C$_{DD}$=1$\mu$F (Ceramic), CD:U3FWJ44N
C$_{GAIN}$=470pF (Ceramic), Tr:XP162A11C0PR



V$_{OUT}$ 5.0V, F$_{OSC}$ : 330kHz

L=22$\mu$H, C$_L$=40$\mu$F (Ceramic), C$_{IN}$=30$\mu$F (Ceramic)
R$_{SEN}$=50m$\Omega$, C$_{DD}$=1$\mu$F (Ceramic), SD:U3FWJ44N
C$_{GAIN}$=470pF (Ceramic), Tr:XP162A11C0PR
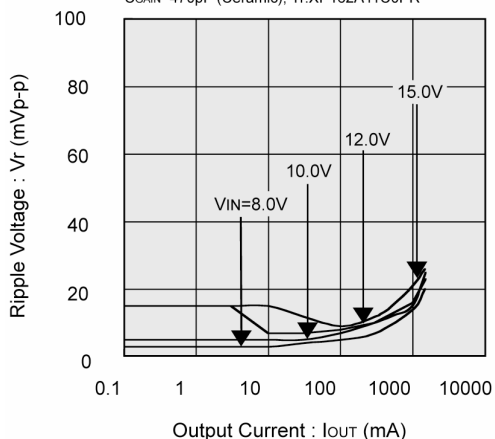


V$_{OUT}$ 12.0V, F$_{OSC}$ : 100kHz

L=68$\mu$H, C$_L$=40$\mu$F (Ceramic), C$_{IN}$=30$\mu$F (Ceramic)
R$_{SEN}$=50m$\Omega$, C$_{DD}$=10$\mu$F (Ceramic), SD:U3FWJ44N
C$_{GAIN}$=470pF (Ceramic), Tr:XP132A11C0PR
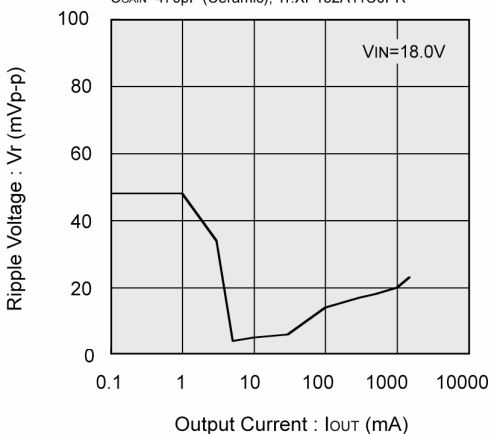


V$_{OUT}$ 1.5V, F$_{OSC}$ : 330kHz

L=22$\mu$H, C$_L$=47$\mu$F (Tantalum), C$_{IN}$=47$\mu$F (Tantalum)
R$_{SEN}$=50m$\Omega$, C$_{DD}$=1$\mu$F (Ceramic), SD:U3FWJ44N
C$_{GAIN}$=470pF (Ceramic), Tr:XP162A11C0PR
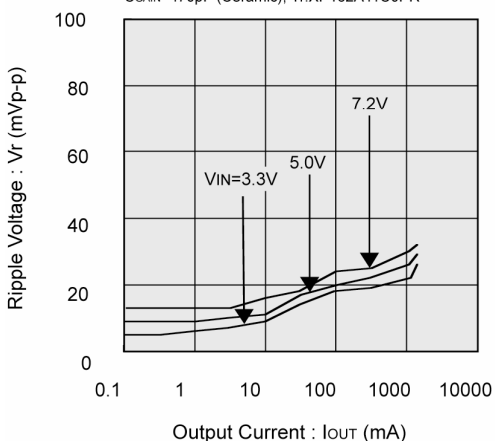


V$_{OUT}$ 3.3V, F$_{OSC}$ : 330kHz

L=22$\mu$H, C$_L$=47$\mu$F (Tantalum), C$_{IN}$=47$\mu$F (Tantalum)
R$_{SEN}$=50m$\Omega$, C$_{DD}$=1$\mu$F (Ceramic), SD:U3FWJ44N
C$_{GAIN}$=470pF (Ceramic), Tr:XP162A11C0PR
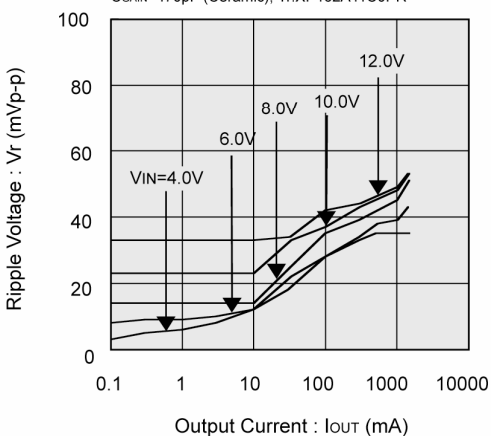


*Note: If the input and output voltage differential is large or small, the time of ON and OFF switching will be shorten.
This gives external components such as inductance value of coil, connecting a resistor to CLK, capacitor, will critically influence the actual operation.

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## ■PACKAGING INFORMATION

●MSOP-8A



0.15 $^{+0.08}_{-0.02}$

0.53±0.13

3.00±0.10

4.90±0.10

3.00±0.10

0.86 $^{+0.11}_{-0.10}$

1.02 $^{+0.20}_{-0.21}$

0.30 $^{+0.08}_{-0.02}$

(0.65)

0.00～0.20

0～6°
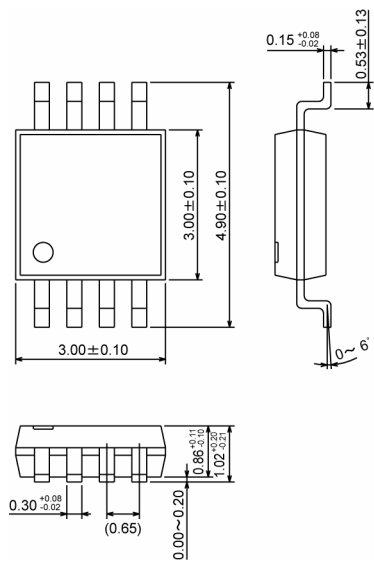
# ■MARKING RULE

●MSOP-8A

MSOP-8A
(TOP VIEW)

①Represents product series

| MARK | PRODUCT SERIES |
|---|---|
| 1 | XC9201xxxAKx |

②Represents product type, DC/DC controller
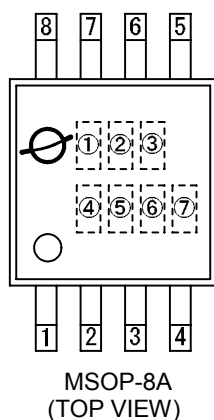
| MARK | TYPE | PRODUCT SERIES |
|---|---|---|
| C | $V_{OUT}$, CE PIN | XC9201CxxAKx |
| D | FB, CE PIN | XC9201C09AKx |

③Represents integral number of output voltage or FB type

| MARK | VOLTAGE | PRODUCT SERIES |
|---|---|---|
| 1 | 1.x | XC9201C1xAKx |
| 2 | 2.x | XC9201C2xAKx |
| 3 | 3.x | XC9201C3xAKx |
| 4 | 4.x | XC9201C4xAKx |
| 5 | 5.x | XC9201C5xAKx |
| 6 | 6.x | XC9201C6xAKx |
| 7 | 7.x | XC9201C7xAKx |
| 8 | 8.x | XC9201C8xAKx |
| 9 | 9.x | XC9201C9xAKx |
| 0 | FB products | XC9201D09AKx |
| A | 10.x | XC9201CAxAKx |
| B | 11.x | XC9201CxAKx |
| C | 12.x | XC9201CCxAKx |
| D | 13.x | XC9201CDxAKx |
| E | 14.x | XC9201CExAKx |
| F | 15.x | XC9201CFxAKx |
| H | 16.x | XC9201CHxAKx |

④Represents decimal number of output voltage

| MARK | VOLTAGE | PRODUCT SERIES |
|---|---|---|
| 0 | x.0 | XC9201Cx0AKx |
| 3 | x.3 | XC9201Cx3AKx |
| 9 | FB products | XC9201D09AKx |

⑤Represents oscillation frequency's control type

| MARK | VOLTAGE | PRODUCT SERIES |
|---|---|---|
| A | Adjustable Frequency | XC9201xxxxAKx |

⑥⑦Represents production lot number
 0 to 9,A to Z repeated (G, I, J, O, Q, W excepted).
 Note: No character inversion used.

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