

## 2-Bit Bidirectional Voltage-Level Translator for Open-Drain and Push-Pull Applications

### FEATURES

- Voltage Level Translator Without Direction-Control Signal
- Maximum Data Rates
  - 24Mbps (Push Pull)
  - 2Mbps (Open Drain)
- Power Supply Range:
  - A Port and VCCA: 1.65 V to 3.6 V
  - B Port and VCCB: 2.3 V to 5.5 V
  - $V_{CCA} \leq V_{CCB}$
- Pull Up Resistors are Integrated in A Port and B Port
- No Power-Supply Sequencing Required: Either VCCA or VCCB Can be Ramped First
- Support Ultra-Low Power Consumption Mode with OE Pin is Low Voltage Level
- I/O Pin ESD:
  - A Port: 2.5 kV (HBM)
  - B Port: 6 kV (HBM)
- Latch -Up Performance Exceeds  $\pm 200\text{mA}$  Under JESD 78 Standard
- DFN 1.4mm $\times$ 1.0mm $\times$ 0.37mm-8L Package

### APPLICATIONS

- I<sup>2</sup>C / SMBus
- UART
- GPIO
- Handheld Devices Interface

### GENERAL DESCRIPTION

AW39102 is a 2-bit high-performance voltage-level translator without direction control signal, which is a non-inverting converter and can be used to convert digital signal with mixed-voltage systems. It needs two separate power supply rails, with the A ports tracks the V<sub>CCA</sub> ranging from 1.65 V to 3.6 V, and the B ports tracks the V<sub>CCB</sub> ranging from 2.3 V to 5.5 V. This makes the chip has capabilities of support both lower and higher logic signal levels translation between any of the 1.8 V, 2.5 V, 3.3 V, and 5 V voltage nodes.

If the voltage level of output-enable (OE) pin is low, the chip works in the high-impedance state, which costs ultra-low power-supply quiescent current. And the OE input circuit is supplied by VCCA. Meanwhile, OE is recommended to be tied to GND through a pull-down resistor to ensure the high-impedance state during power up or power down.

No power supply sequencing requirements means either VCCA or VCCB can be powered up first, and OE should be enabled after both VCCA and VCCB are established.

## APPLICATION CIRCUIT

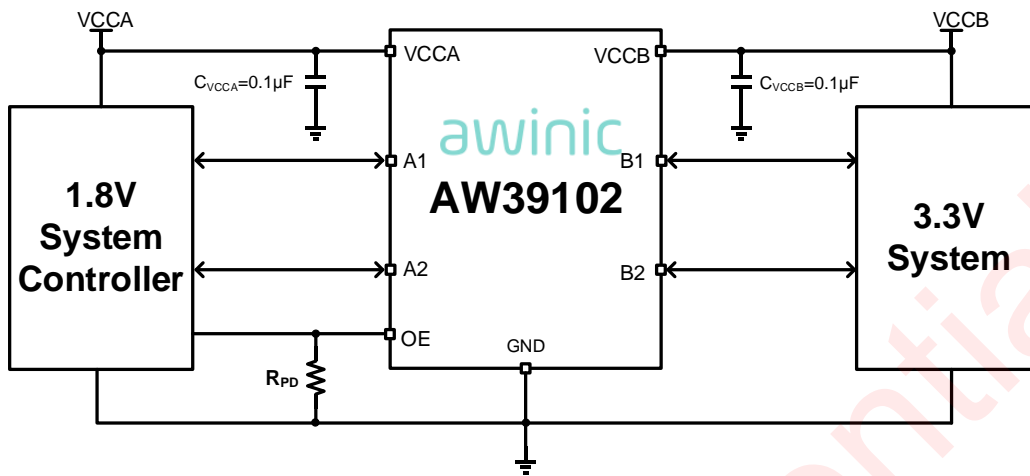
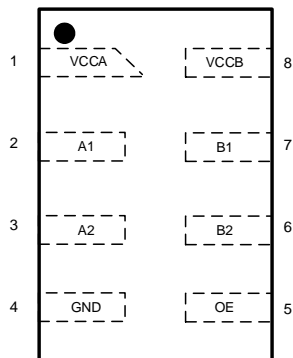


Figure 1 Typical Application Circuit of AW39102

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## PIN CONFIGURATION AND TOP MARK

AW39102DNR PIN Configuration  
(Top View)AW39102DNR Marking  
(Top View)

X5G – AW39102DNR

XX – Production Tracing Code

Figure 2 Pin Configuration and Top Mark

## PIN DEFINITION

Pin No.	Pin Name	Description
1	VCCA	A-port supply voltage. $1.65\text{ V} \leq V_{CCA} \leq 3.6\text{ V}$ , $V_{CCA} \leq V_{CCB}$ .
2	A1	Input/output A1.
3	A2	Input/output A2.
4	GND	Ground.
5	OE	Output enable.
6	B2	Input/output B2.
7	B1	Input/output B1.
8	VCCB	B-port supply voltage. $2.3\text{ V} \leq V_{CCB} \leq 5.5\text{ V}$ .

## FUNCTIONAL BLOCK DIAGRAM

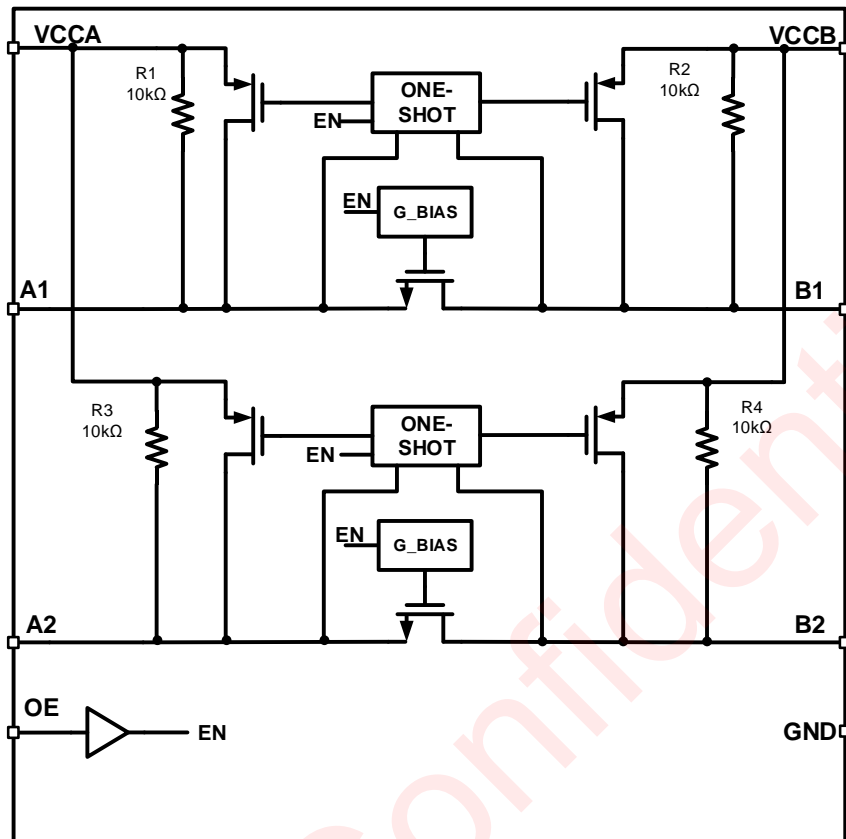


Figure 3 AW39102 Function Block

## TYPICAL APPLICATION CIRCUITS

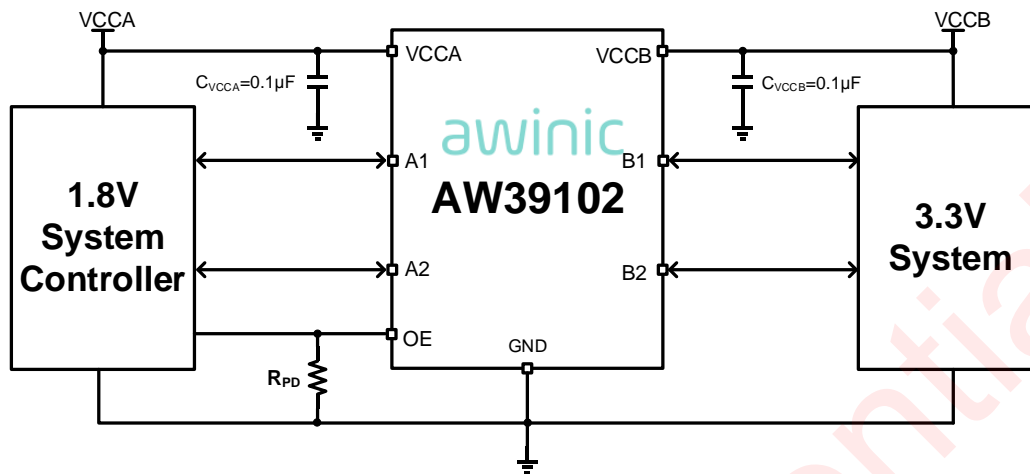


Figure 4 AW39102 Application Circuit

## ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW39102DNR	-40°C~85°C	DFN 1.4mm×1.0mm-8L	X5G	MSL1	ROHS+HF	3000 units/ Tape and Reel

**ABSOLUTE MAXIMUM RATINGS**(NOTE1)

PARAMETERS		MIN	MAX	UNIT
Supply voltage range $V_{CCA}$ (NOTE2)		-0.5	5	V
Supply voltage range $V_{CCB}$ (NOTE2)		-0.5	6.5	V
Input voltage range, $V_I$ (NOTE2)	A port	-0.5	5	V
	B port	-0.5	6.5	V
Output voltage range in high or low state, $V_O$ (NOTE2)	A port	-0.5	5	V
	B port	-0.5	6.5	V
Operating free-air temperature range		-40	85	°C
Operating junction temperature $T_J$		-40	125	°C
Storage temperature $T_{STG}$		-65	150	°C
Lead temperature (Soldering 10 seconds)			260	°C

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: With respect to GND

**ESD RATING AND LATCH UP**

PARAMETERS	VALUE	UNIT
B Port HBM (Human Body Model) (NOTE 3)	±6	kV
Other PINS HBM (Human Body Model)	±2.5	kV
CDM(NOTE 4)	±1.5	kV
Latch-Up(NOTE 5)	+IT: 200 -IT: -200	mA

NOTE3: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017

NOTE4: Test method: ESDA/JEDEC JS-002-2014

NOTE5: Test method: JESD78E

## RECOMMENDED OPERATING CONDITIONS

VCCI is the VCC associated with the input port

PARAMETERS		CONDITIONS		MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage for A port			1.65	3.6	V
V <sub>CCB</sub>	Supply voltage for B port			2.3	5.5	V
V <sub>IH</sub>	High-level input voltage	A-port	V <sub>CCA</sub> =1.65V~3.6V V <sub>CCB</sub> =2.3V~5.5V	V <sub>CCI</sub> -0.4	V <sub>CCI</sub>	V
		B-port	V <sub>CCA</sub> =1.65V~3.6V V <sub>CCB</sub> =2.3V~5.5V	V <sub>CCI</sub> -0.4	V <sub>CCI</sub>	V
		OE input	V <sub>CCA</sub> =1.65V~3.6V V <sub>CCB</sub> =2.3V~5.5V	V <sub>CCA</sub> ×0.65	5.5	V
V <sub>IL</sub>	Low-level input voltage	A-port	V <sub>CCA</sub> =1.65V~3.6V V <sub>CCB</sub> =2.3V~5.5V	0	0.4-I <sub>OL</sub> ×R <sub>NPASS</sub> (NOTE6)	V
		B-port	V <sub>CCA</sub> =1.65V~3.6V V <sub>CCB</sub> =2.3V~5.5V	0	0.4-I <sub>OL</sub> ×R <sub>NPASS</sub> (NOTE6)	V
		OE input	V <sub>CCA</sub> =1.65V~3.6V V <sub>CCB</sub> =2.3V~5.5V	0	V <sub>CCA</sub> ×0.35	V
Δt/ΔV	Input transition rise or fall rate	A-port (NOTE 7)	V <sub>CCA</sub> =1.65V~3.6V V <sub>CCB</sub> =2.3V~5.5V		10	ns/V
		B-port (NOTE7)	V <sub>CCA</sub> =1.65V~3.6V V <sub>CCB</sub> =2.3V~5.5V		10	ns/V
		Control input	V <sub>CCA</sub> =1.65V~3.6V V <sub>CCB</sub> =2.3V~5.5V		10	ns/V
T <sub>A</sub>	Operating junction temperature T <sub>A</sub>			-40	85	°C

NOTE6: I<sub>OL</sub> is the current from external resistor to output port, R<sub>NPASS</sub> is equal internal resistor of NMOSFET between A port and B port.

NOTE7: The parameter is defined for push-pull driving.

## THERMAL INFORMATION

PARAMETERS	VALUE	UNIT
Junction-to-ambient thermal resistance θ <sub>JA</sub>	246	°C /W

## ELECTRICAL CHARACTERISTICS

## DC Electrical Characteristics

Operating under recommended conditions,  $V_{CCA} \leq V_{CCB}$ ,  $T_A = 25^\circ\text{C}$  for typical values (unless otherwise noted)

PARAMETER		TEST CONDITION	$V_{CCA}(V)$	$V_{CCB}(V)$	MIN	TYP	MAX	UNIT
$V_{OHA}$	Port A output high voltage	$I_{OH} = -20\mu A$ $V_{IA} \geq V_{CCA} - 0.4V$	1.65~3.6	2.3~5.5	$V_{CCA} \times 0.67$			V
$V_{OLA}$	Port A output low voltage	$I_{OL} = 1mA$ $V_{IA} \leq 0.15V$	1.65~3.6	2.3~5.5			0.4	V
$V_{OHB}$	Port B output high voltage	$I_{OH} = -20\mu A$ $V_{IB} \geq V_{CCB} - 0.4V$	1.65~3.6	2.3~5.5	$V_{CCB} \times 0.67$			V
$V_{OLB}$	Port B output low voltage	$I_{OL} = 1mA$ $V_{IB} \leq 0.15V$	1.65~3.6	2.3~5.5			0.4	V
$I_I$	OE input leakage current	$V_I = V_{CCI}$ or GND, $T_A = 25^\circ\text{C}$	1.65~3.6	2.3~5.5	-1		1	$\mu A$
		$V_I = V_{CCI}$ or GND, $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$	1.65~3.6	2.3~5.5	-2		2	$\mu A$
$I_{OZ}$	A or B port output current in high impedance state	$OE = V_{IL}$ $T_A = 25^\circ\text{C}$	1.65~3.6	2.3~5.5	-1		1	$\mu A$
		$OE = V_{IL}$ $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$	1.65~3.6	2.3~5.5	-2		2	$\mu A$
$I_{CCA}$	VCCA supply current	$V_I = V_O = \text{Open}$ $I_O = 0$ $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$	1.65~3.6	2.3~5.5			1	$\mu A$
			3.6	0			1	$\mu A$
			0	5.5			-1	$\mu A$
$I_{CCB}$	VCCB supply current	$V_I = V_O = \text{Open}$ $I_O = 0$ $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$	1.65~3.6	2.3~5.5			8	$\mu A$
			3.6	0			-1	$\mu A$
			0	5.5			1	$\mu A$
$I_{CCB+I_{CCA}}$	Combined supply current	$V_I = V_O = \text{Open}$ $I_O = 0$	1.65~3.6	2.3~5.5			9	$\mu A$
$R_{PU}$	Resistor pull-up value	$T_A = 25^\circ\text{C}$	1.65~3.6	2.3~5.5	8	10	12	$k\Omega$
$R_{NPASS}$	The resistor of NMOSFET between A port and B port	$OE = V_{IH}$ $T_A = 25^\circ\text{C}$	1.8	3.3		28		$\Omega$

## Timing Requirements (NOTE1)

Output load:  $C_L = 15pF$ , push-pull driver, and  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .

PARAMETER		TEST CONDITION	MIN	MAX	UNIT
$V_{CCA} = 1.8V \pm 0.15V / 2.5V \pm 0.2V / V_{CCA} = 3.3V \pm 0.3V$					
Data Rate		$V_{CCB} = 2.5V \pm 0.2V$		21	Mbps
		$V_{CCB} = 3.3V \pm 0.3V$		24	
		$V_{CCB} = 5V \pm 0.5V$		24	
$t_w$	Pulse Duration	$V_{CCB} = 2.5V \pm 0.2V$	45		ns



PARAMETER	TEST CONDITION	MIN	MAX	UNIT
$V_{CCA}=1.8V\pm 0.15V / 2.5V\pm 0.2V / V_{CCA}=3.3V\pm 0.3V$				
	$V_{CCB}=3.3V\pm 0.3V$	40		
	$V_{CCB}=5V\pm 0.5V$	40		

NOTE1: The parameter's variation is guaranteed by design, not production tested.

### Switch Characteristics<sup>(NOTE2)</sup>

Output load:  $C_L=15pF$ ,  $T_A=25^\circ C$  for typical values (unless otherwise noted),  $V_{CCA}=1.8V$

PARAMETER	TEST CONDITION		$V_{CCB}=2.5V$		$V_{CCB}=3.3V$		$V_{CCB}=5V$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PHL}^{(NOTE3)}$	A-B	Push-pull		11		7.0		5.0	ns
		Open-drain	2.3	8.8	2.4	9.6	2.6	10	
$t_{PLH}^{(NOTE3)}$	A-B	Push-pull		7.5		6.7		5.7	ns
		Open-drain	45	260	36	208	27	198	
$t_{PHL}^{(NOTE3)}$	B-A	Push-pull		9.0		5.5		5.0	ns
		Open-drain	1.9	5.3	1.1	4.4	1.2	4	
$t_{PLH}^{(NOTE3)}$	B-A	Push-pull		7.4		5.8		4.1	ns
		Open-drain	45	175	36	140	27	102	
$t_{en}$ Enable time	OE-A or B			45		35		30	ns
$t_{dis}$ disable time	OE-A or B			200		200		200	ns
$t_{rA}$ Input rise time	A port rise time	Push-pull	3.2	9.5	2.3	9.3	2	7.6	ns
		Open-drain	38	165	30	132	22	95	
$t_{rB}$ Input rise time	B port rise time	Push-pull	4	10.8	2.7	9.1	2.7	7.6	ns
		Open-drain	34	145	23	106	10	58	
$t_{fA}$ Input fall time	A port fall time	Push-pull	2	5.9	1.9	6	1.7	13.3	ns
		Open-drain	4.4	6.9	4.3	6.4	4.2	6.1	
$t_{fB}$ Input fall time	B port fall time	Push-pull	2.9	13.8	2.8	16.2	2.8	16.2	ns
		Open-drain	6.9	13.8	7.5	16.2	7	16.2	
$t_{sk}$ Skew time	Channel to channel skew			0.7		0.7		0.7	ns

Output load:  $C_L=15\text{pF}$ ,  $T_A=25^\circ\text{C}$  for typical values (unless otherwise noted),  $V_{CCA}=2.5\text{V}$ 

PARAMETER	TEST CONDITION		$V_{CCB}=2.5\text{V}$		$V_{CCB}=3.3\text{V}$		$V_{CCB}=5\text{V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PHL}$ (NOTE3)	A-B	Push-pull		3.2		3.7		3.8	ns
		Open-drain	1.7	6.3	2	6	2.1	5.8	
$t_{PLH}$ (NOTE3)	A-B	Push-pull		3.5		4.1		4.4	ns
		Open-drain	45	250	36	206	27	190	
$t_{PHL}$ (NOTE3)	B-A	Push-pull		3		3.6		4.3	ns
		Open-drain	1.8	4.7	2.6	4.2	1.2	4	
$t_{PLH}$ (NOTE3)	B-A	Push-pull		2.5		1.6		1	ns
		Open-drain	44	170	37	140	27	102	
$t_{en}$ Enable time	OE-A or B					35		30	ns
$t_{dis}$ disable time	OE-A or B					200		200	ns
$t_{rA}$ Input rise time	A port rise time	Push-pull	2.8	7.4	2.6	6.6	1.8	5.6	ns
		Open-drain	38	150	28	121	24	89	
$t_{rB}$ Input rise time	B port rise time	Push-pull	3.2	8.3	2.9	7.2	2.4	6.1	ns
		Open-drain	34	151	24	112	12	64	
$t_{fA}$ Input fall time	A port fall time	Push-pull	1.9	5.7	1.9	5.5	1.8	5.3	ns
		Open-drain	4.4	6.9	4.3	6.4	4.2	5.8	
$t_{fB}$ Input fall time	B port fall time	Push-pull	2.2	7.8	2.4	6.7	2.6	6.6	ns
		Open-drain	5.1	8.8	5.4	9.4	5.4	10.4	
$t_{sk}$ Skew time	Channel to channel skew			0.7		0.7		0.7	ns

Output load:  $C_L=15\text{pF}$ ,  $T_A=25^\circ\text{C}$  for typical values (unless otherwise noted),  $V_{CCA}=3.3\text{V}$ 

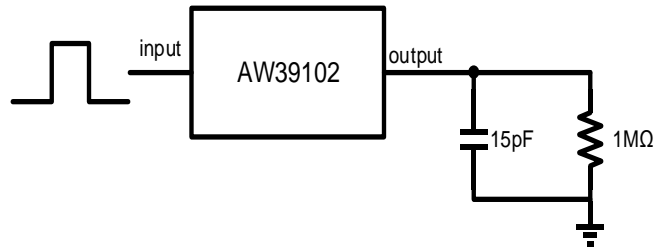
PARAMETER	TEST CONDITION		$V_{CCB}=3.3\text{V}$		$V_{CCB}=5\text{V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{PHL}$ (NOTE3)	A-B	Push-pull		2.4		3.1	ns
		Open-drain	1.3	4.2	1.4	4.6	
$t_{PLH}$ (NOTE3)	A-B	Push-pull		4.2		4.4	ns
		Open-drain	36	204	27	165	
$t_{PHL}$ (NOTE3)	B-A	Push-pull		2.5		3.3	ns
		Open-drain	1	124	1	97	
$t_{PLH}$ (NOTE3)	B-A	Push-pull		2.5		3.3	ns
		Open-drain	3	139	3	105	
$t_{en}$ Enable time	OE-A or B					30	ns
$t_{dis}$ disable time	OE-A or B					200	ns
$t_{rA}$ Input rise time	A port rise time	Push-pull	2.3	5.6	1.9	4.8	ns
		Open-drain	25	116	19	85	
$t_{rB}$ Input rise time	B port rise time	Push-pull	2.5	6.4	2.1	7.4	ns
		Open-drain	26	116	14	72	
$t_{fA}$ Input fall time	A port fall time	Push-pull	2	5.4	1.9	5	ns
		Open-drain	4.3	6.4	4.2	5.7	
$t_{fB}$ Input fall time	B port fall time	Push-pull	2.3	7.4	2.4	7.6	ns
		Open-drain	5	7.6	4.8	8.3	
$t_{sk}$ Skew time output	Channel to channel skew			0.7		0.7	ns

NOTE2: The parameters is guaranteed by design, not production tested.

NOTE3:  $t_{PHL}$  presents propagation delay from high to low, and  $t_{PLH}$  presents propagation delay from low to high.

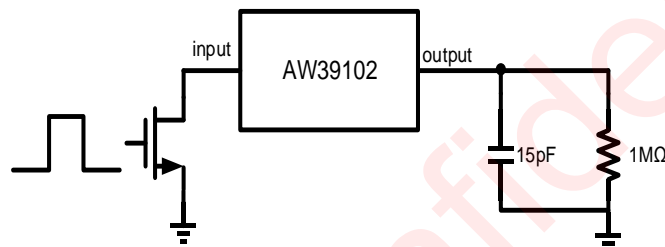
## TYPICAL CHARACTERISTICS

### Test Information



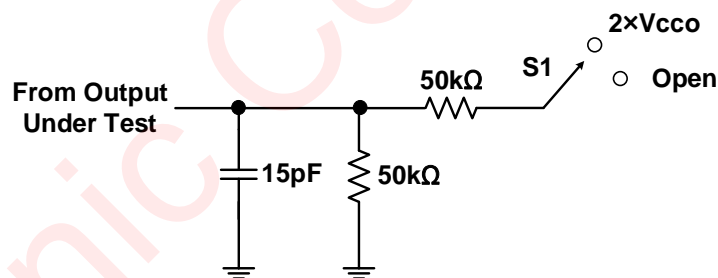
Test Circuit for Date Rate, Pulse Duration, Propagation Delay, Rise Time and Fall Time

Figure 5 Load Circuit of Push-Pull Driver



Test Circuit for Date Rate, Pulse Duration, Propagation Delay, Rise Time and Fall Time

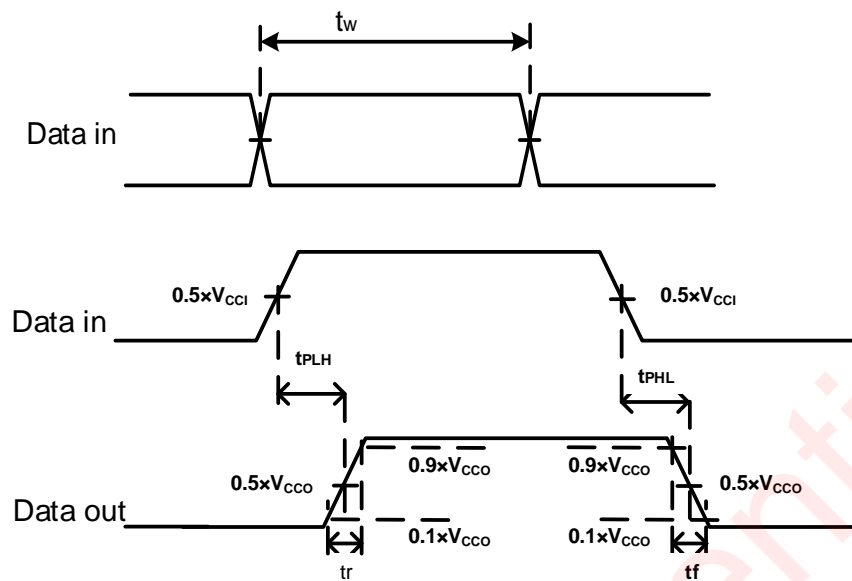
Figure 6 Load Circuit of Open-Drain Driver



TEST	S1
$t_{PZL}/t_{PLZ}$ ( $t_{dis}$ )	$2 \times V_{cco}$
$t_{PHZ}/t_{PZH}$ ( $t_{en}$ )	Open

1.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
2.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
3.  $V_{CCI}$  is the VCC associated with the input port.
4.  $V_{CCO}$  is the VCC associated with the output port.
5. The resistance and Capacitance values at output notes above are the total effective values.

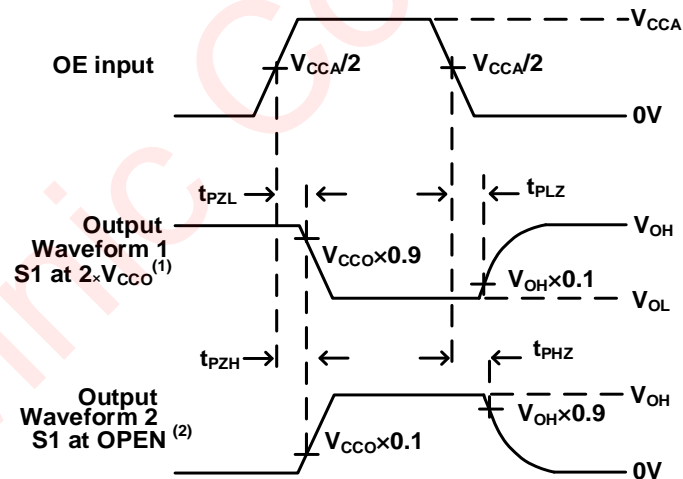
Figure 7 Load Circuit for Enable-Time and Disable-Time Measurement



The input pulses should have the following characteristics:

1.  $f_{IN} \leq 10\text{MHz}$ .
2.  $dv/dt \geq 1\text{V/ns}$ .

Figure 8 Timing Parameter Definition

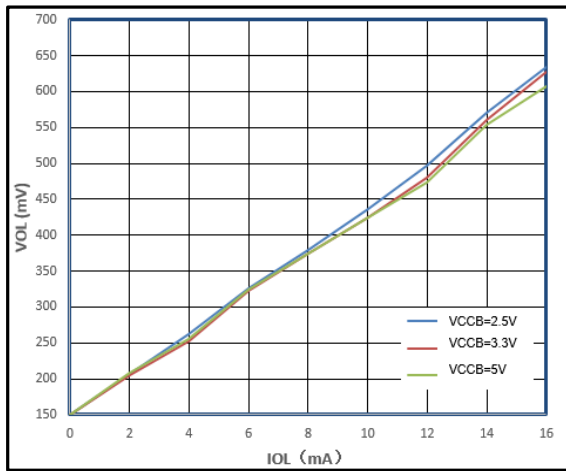


(1) The Waveform 1 is obtained under the condition that the input is low and S1 at  $2*V_{CCO}$ .

(2) The Waveform 2 is obtained under the condition that the input and S1 at OPEN.

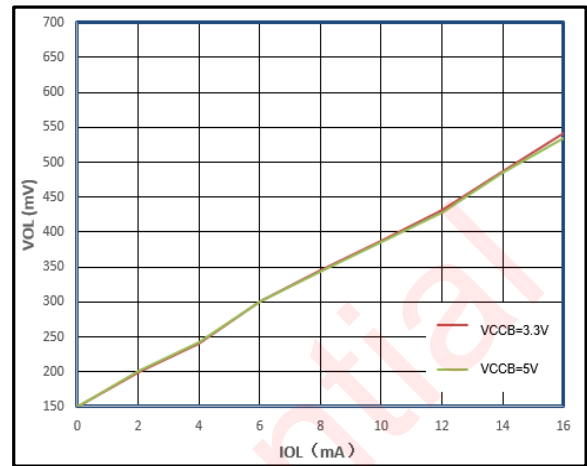
Figure 9 Enable and Disable Times

Typical Curve  $T_A=25^\circ\text{C}$



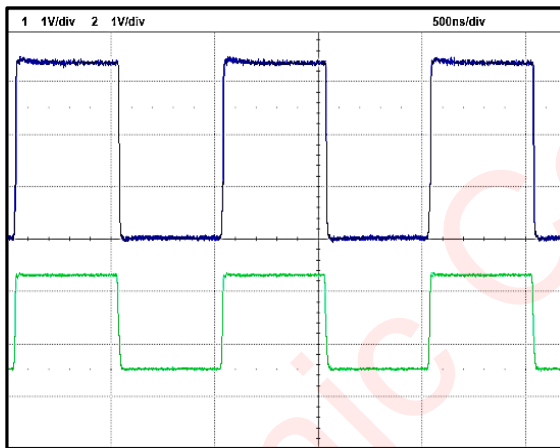
$V_{CCA}=1.8\text{V}$ ,  $OE=1$ ,  $V_{ILA}=0.15\text{V}$

Figure 10 Low-Level Output Voltage vs Low-Level Current



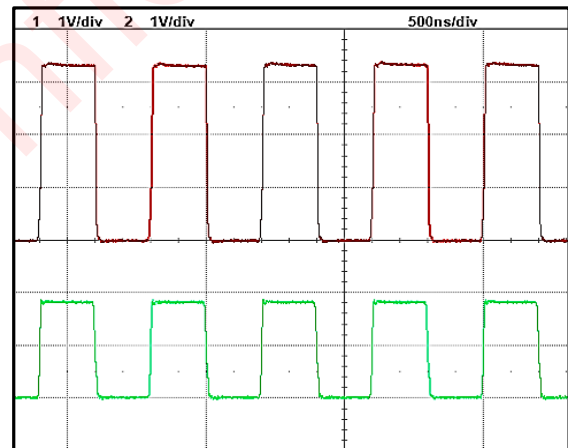
$V_{CCA}=3.3\text{V}$ ,  $OE=1$ ,  $V_{ILA}=0.15\text{V}$

Figure 11 Low-Level Output Voltage vs Low-Level Current



$V_{CCA}=1.8\text{V}$ ,  $V_{CCB}=3.3\text{V}$ ,  $OE=1$ , Push-Pull Driver  
Signal is translated from A port to B port

Figure 12 Level Translation of a 1MHz Signal



$V_{CCA}=1.8\text{V}$ ,  $V_{CCB}=3.3\text{V}$ ,  $OE=1$ , Push-Pull Driver  
Signal is translated from A port to B port

Figure 13 Level Translation of a 2.5MHz Signal

## DETAILED FUNCTIONAL DESCRIPTION

AW39102 is a 2-bit high-performance voltage-level translator without direction control signal, which is a non-inverting converter and can be used to convert digital signal with mixed-voltage systems. Port A can support I/O voltages from 1.65 V to 3.6 V, while Port B is able to support I/O voltage range from 2.3 V to 5.5 V. The chip uses a transmission gate architecture with an rising edge rate accelerator (one-shot), to increase overall data rate. Also, 10k $\Omega$  pull-up resistors are integrated in the chip, which ensures the chip not only supports push-pull applications but also can be used in open-drain applications directly.

### One-shot Accelerator

The One-Shot rising edge accelerator circuit speeds up the rising edge to help increasing the chip's data rate. Once the chip has detected the rising edge of the input signal from low to high, the one-shot circuit generates a pulse signal of approximately 25ns, which enables the internal pull-up PMOS transistor between power supply and output, thereby accelerating the output port from low to high. During this acceleration phase, the output resistance of the driver is reduced from 10k $\Omega$  to approximately 60 $\Omega$ . While detecting the output has been turned up, the one-shot pulse signal is finished and pull-up PMOS transistor is quickly turned off. This architecture reduces the average dynamic power consumption of the chip while allowing it to meet different drive requirements.

### Gate Bias

For the bidirectional voltage translator AW39102, a NMOS switch transistor is used between the input and output. When translating high level, the NMOS transistor is turned off, and the input and output terminals are isolated so that they do not impact each other. When the low level is translated, the NMOS switch transistor is fully turned on, so that the output terminal can be quickly pulled down to the low voltage level. Therefore, the gate bias voltage of the NMOS switch transistor is set to a fixed value about  $V_{CCA} + V_{TH}$ . It is also because of this architecture that  $V_{CCA} \leq V_{CCB}$  needs to be guaranteed in the applications.

### Enable Control

The AW39102's OE pin can disable the chip by setting OE to low voltage level, allowing all I/O to operate in the Hi-Z state. The disable time ( $t_{dis}$ ) represents the delay time from OE going low to the chip turns to Hi-Z state. In the Hi-Z state, the chip consumes ultra-low current. And the enable time ( $t_{en}$ ) indicates the delay from OE going high to the chip working in translation state. Meanwhile, OE is recommended to be tied to GND through a pull-down resistor to ensure the high-impedance state during power up or power down. The minimum value of the resistor is determined by the current-sourcing capability of the driver.

### Input Driver

The rising edge time of the signal ( $t_{rA}$ ,  $t_{rB}$ ) and propagation delay from low to high ( $t_{PLH}$ ) are determined by the rising edge rate of the input signal, the ONE-SHOT accelerator's pull-up capability, and the capacitive load of the port. The falling edge time of the signal ( $t_{fA}$ ,  $t_{fB}$ ) depends on the falling edge rate of the input signal, the output impedance of the external driver, and the capacitive load on the data line. Similarly,  $t_{PHL}$  and the maximum data rate also depend on the output impedance of the external driver. So, the test conditions for  $t_{rA}$ ,  $t_{rB}$ ,  $t_{fA}$ ,  $t_{fB}$ ,  $t_{PLH}$ ,  $t_{PHL}$  and maximum data rate in the data sheet are that the output impedance of the external driver is less than 50 $\Omega$ .

### Output Load

It is recommended that a PCB layout with short PCB layout length:

1. Avoid excessive capacitive load triggers ONE-SHOT circuit falsely;
2. It can ensure that the round trip delay of any reflection is less than a single ONE-SHOT duration;
3. Improve signal integrity.

Meanwhile, the pulse width of the ONE-SHOT circuit is approximately 25 ns, which determines the maximum output load capacitance that the chip can drive. For very heavy output capacitive loads, the one-shot accelerator will time-out before the output is fully pulled to high level, at which case the signal transmission will be distorted. So the ONE-SHOT duration design requires a trade-off between dynamic power consumption, capacitive load driving capability and maximum data rate. The signal  $t_w$  at the maximum translation rate should be greater than the maximum pulse width of the ONE-SHOT circuit, and the delay caused by the output capacitive load should be less than the maximum pulse width of the ONE-SHOT circuit.

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## APPLICATION INFORMATION

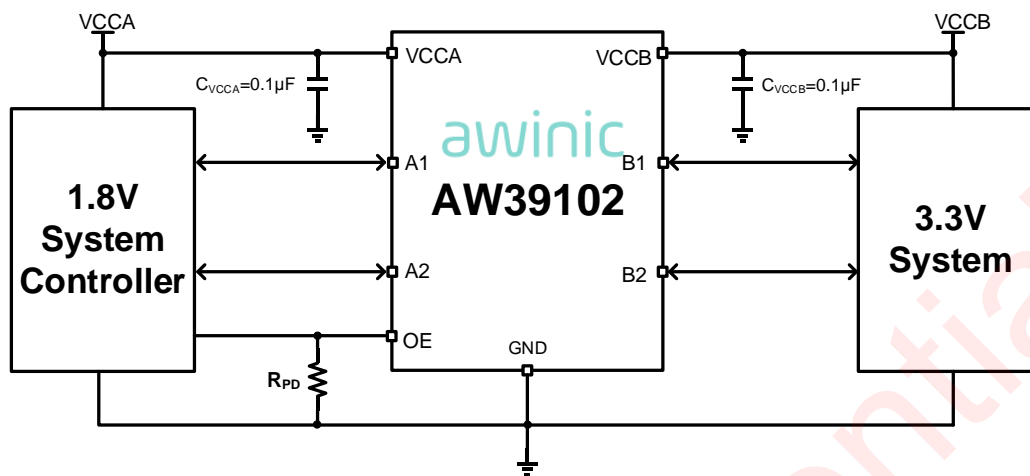


Figure 14 AW39102 Application Circuit

AW39102 is a 2-bit voltage-level translator without direction control signal, which is suitable for interfacing devices or systems operating at different interface voltages with one another. Port A can support I/O voltages from 1.65 V to 3.6 V, while Port B is able to support I/O voltage range from 2.3 V to 5.5 V. Also, 10kΩ pull-up resistors are integrated in the chip, which ensures the chip not only supports push-pull applications but also can be used in open-drain applications directly.

### VCC Capacitor Selection

The device is a 2-bit high-performance voltage-level translator that requires adequate power supply decoupling. Place a low equivalent-series-resistance (ESR) ceramic capacitor, recommend 0.1µF or larger than 0.1µF.

### R<sub>PD</sub> Selection

Drive OE pin HIGH to enable the device. If the voltage level of OE pin is low, the device works in High-impedance mode. OE pin is recommended to be tied to GND through a pull-down resistor to ensure the high-impedance state during power up or power down. OE pin is high impedance without internal pull down resistor, customer can choose the resistor value based on the source drive capability and current consumption.

## PCB LAYOUT CONSIDERATION

To make full use of the performance of AW39102, the guidelines below should be followed.

1.  $C_{VCCA}$  and  $C_{VCCB}$  should be placed on the top layer as close as possible to the VCCA and VCCB pin.
2. The trace of signals should be short enough to avoid any reflection when transmitted.

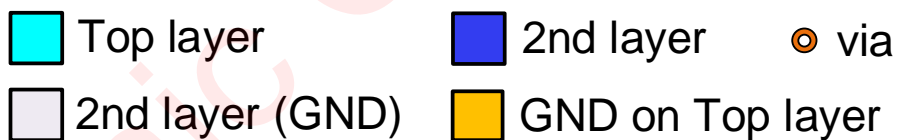
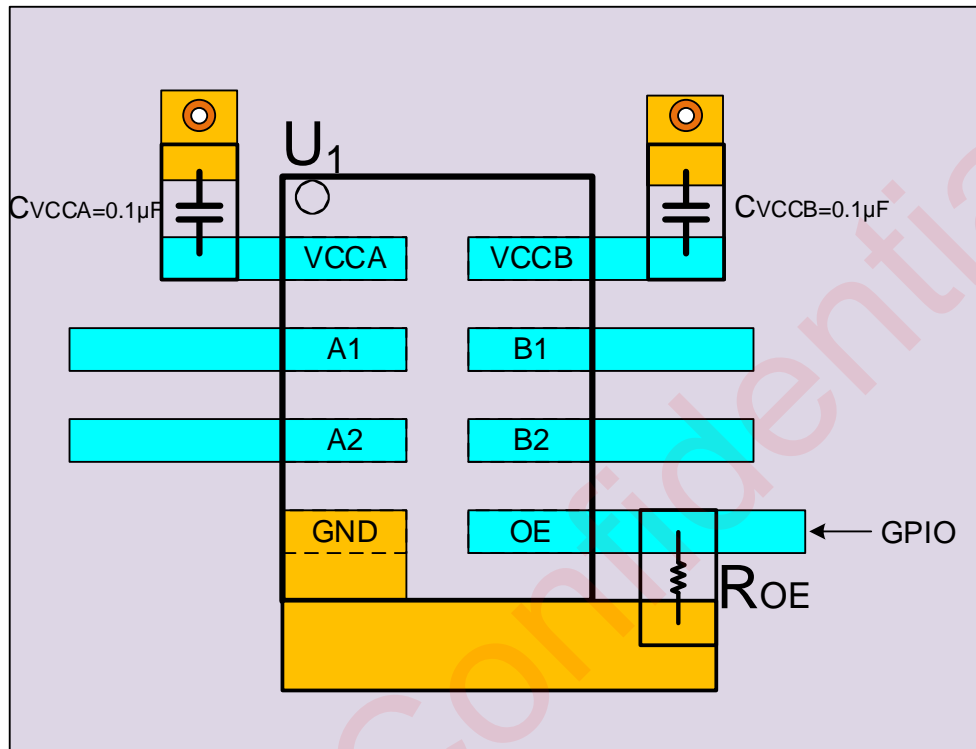
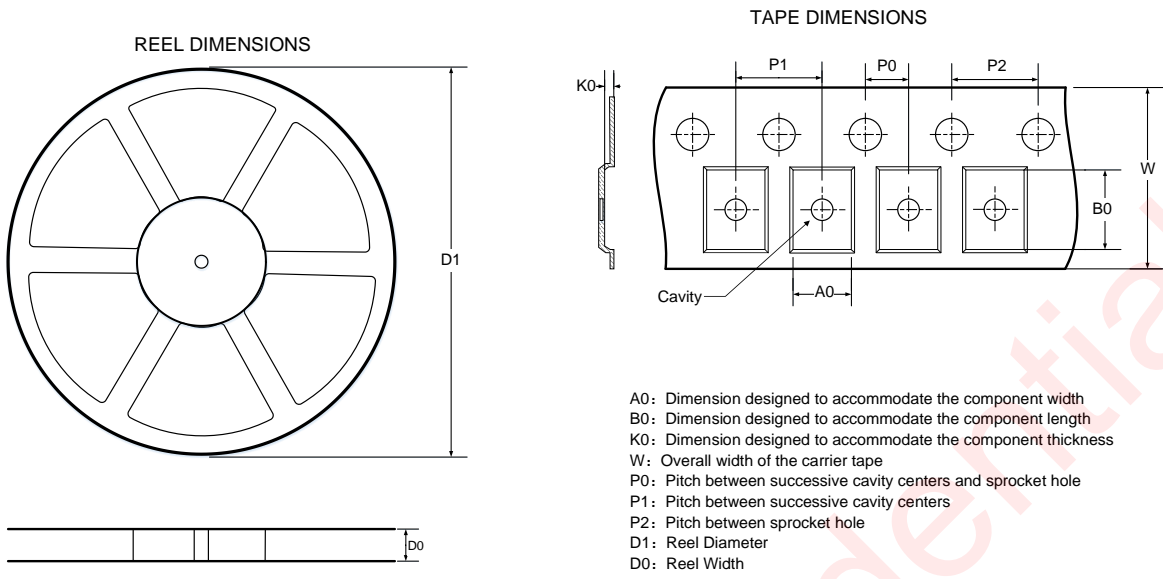
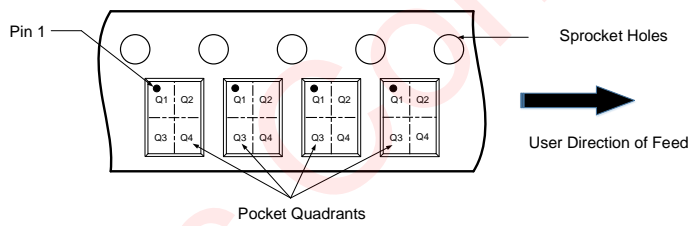


Figure 15 AW39102 Layout Example

### TAPE AND REEL INFORMATION



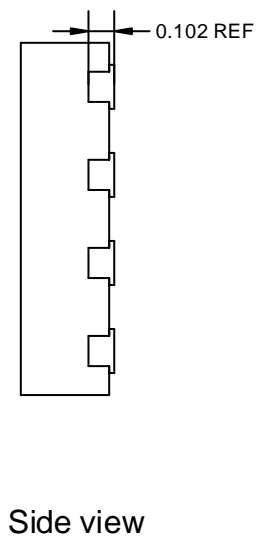
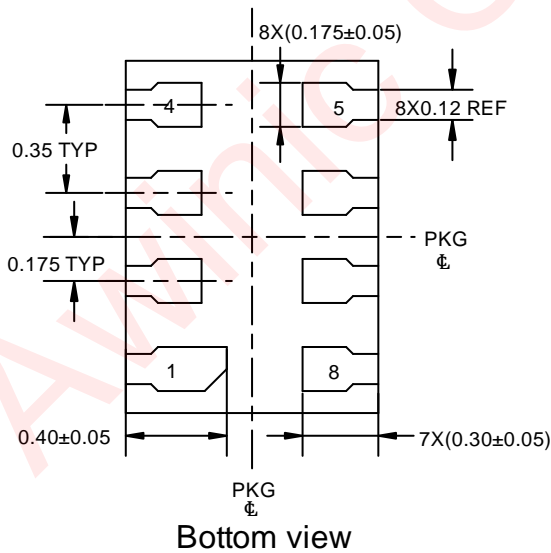
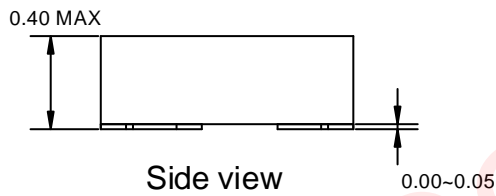
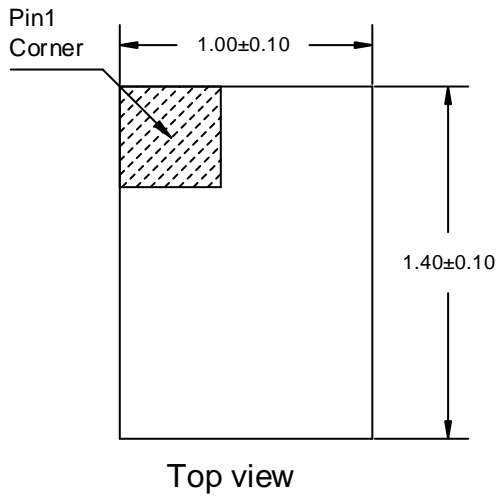
#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



All Dimensions are nominal

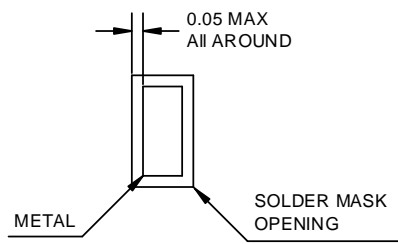
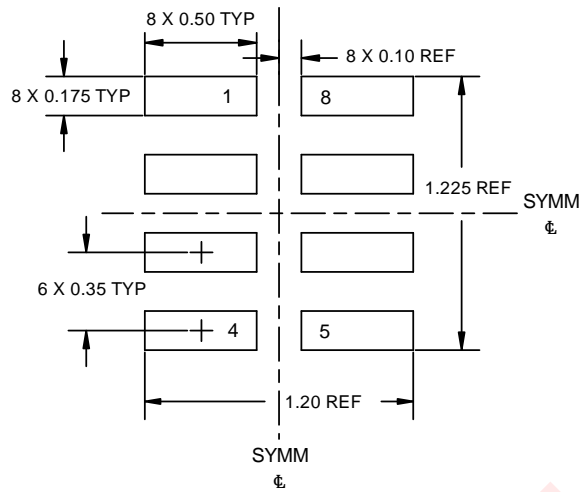
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
180	9.5	1.15	1.6	0.5	2	4	4	8	Q1

PACKAGE DESCRIPTION(POD)

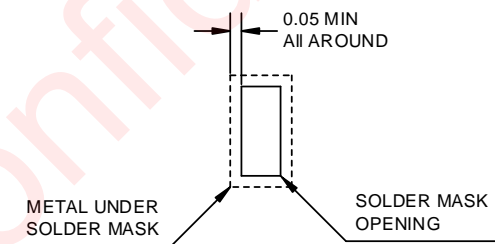


Unit: mm

LAND PATTERN DATA



NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

**REVISION HISTORY**

<b>Vision</b>	<b>Date</b>	<b>Change Record</b>
V1.0	Apr. 2019	Official Released
V1.1	May. 2019	Update waveform
V1.2	Dec. 2019	Update the Definition of $V_{IL}$ and $t_{dis}$

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