EMINENT

MN58406D

Integrated Proximity and Ambient Light Sensor w / Built-in LD

Product Specification

DOC. VERSION 0.2

EMINENT ELECTRONIC TECHNOLOGY

Aug 2018

Specification Revision History

Doc. Version	Revision Description	Date
0.1	Preliminary version	2018/07/27
0.2	Modify Physical Appearance&POD	2018/08/31

Overview

Description

The MN58406D integrates an ambient light (ALS) sensor, a proximity sensor (PS) and with both I^2C and Interrupt Pin outputs and with built-in LD. It is used in notebook PCs, smartphones, MIDs (mobile internet devices), PNDs (portable navigation devices), e-books, tablet PCs, flat-panel televisions, etc. for extending battery life and for better user visual experience. Ambient light sensor optimizes the screen brightness to extend battery and to increase lame life. Proximity sensor (PS) measures the IR reflection intensity which correlates to the distance of the object. Proximity sensor enables the device controller to turn off the LCD back-light and the touch-screen sensor when the device is held close to your ear, placed inside the pocket, purse, or bags. This function saves the battery power and avoids unintended touch-screen trigger. Proximity sensor can also work as a device wake-up sensor by sensing the user waving the hand in front of the device.

Features

- ALS and PS with built-in LD in a Single Chip
- Converters light intensity to digital data format
- Digital control and data output via I^2C (100 KHz and 400 KHz) interface
- Programmable analog gain and integration time for ALS and PS
- Integrated LD driver for Proximity detection
- Ambient IR cancellation during Proximity sensing
- Programmable interrupt function for ALS and PS with upper and lower thresholds
- Operating voltage ranges : 2.4V to 3.6V
- Active V_{DD} Pin Current :400uA
- Sleep Mode : 1uA typical current

Applications

- Smartphones
- Notebook computers
- Tablet PC, TV
- Consumer electronics and appliances

Physical Appearance

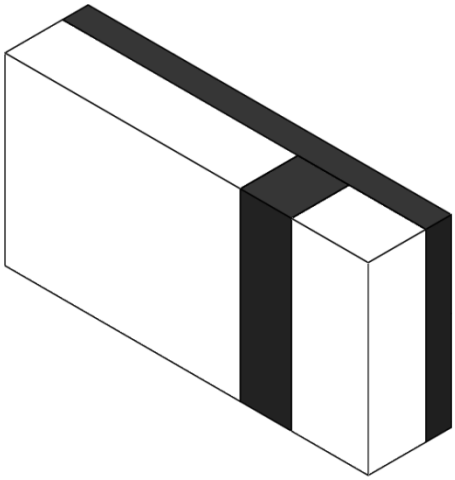


Figure 1.MN58406D Sensor Physical Appearance

Hardware Specifications

Block Diagram

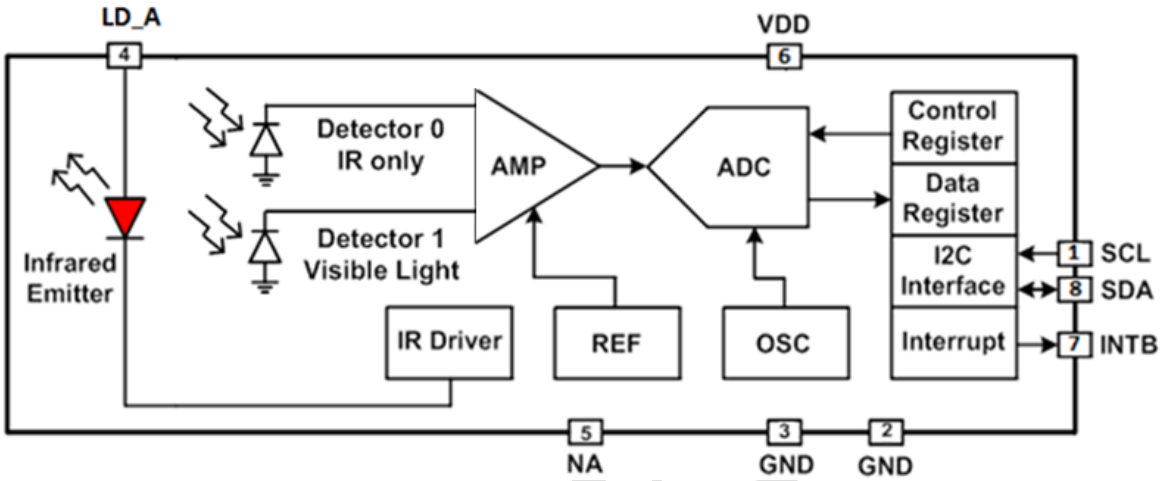


Figure 2.MN58406D Functional Block Diagram

Pin Out

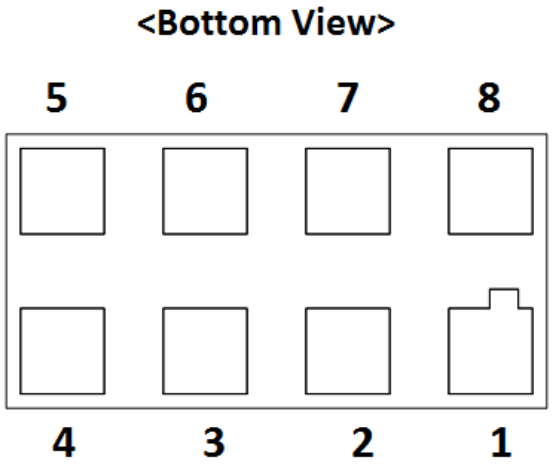


Figure 3.MN58406D DFN Pin Assignment

MN58406D Pin Descriptions

Pin No.	Name	Type	Description
1	SCL	Input	Serial Digital Input Clock
2	GND	Ground	Ground
3	GND	Ground	Ground
4	LD_A	Power	IR LD Anode
5	NA	Unused Pin	Floating
6	VDD	Power	Chip Core Power
7	INTB	Digital Out	Binary or Active Low (open drain)
8	SDA	I/O	Serial Digital I/O Data

Application Circuit

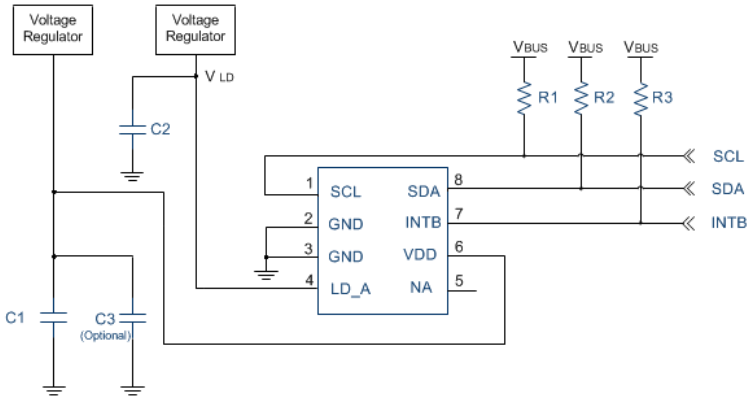


Figure 4(a). MN58406D Application Circuit using Separate Power Supplies

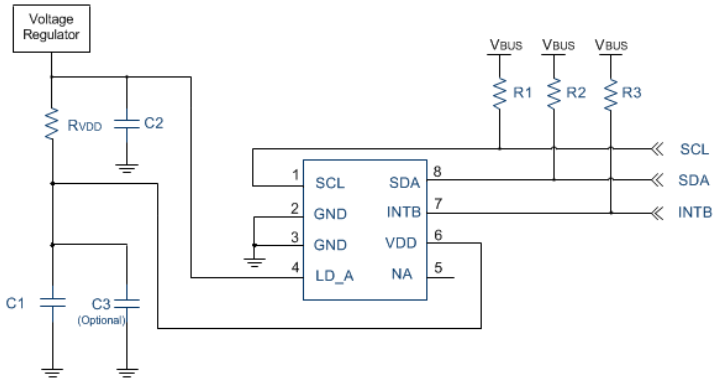


Figure 4(b). MN58406D Application Circuit using Single Power Supplies

Figure4. 58406D Application Circuit Diagram

MN58406D BOM List

Basic Application

Component	Function	Recommend Value	Quantity
C1	Bypass Capacitor	0.1uF	1
C2	Bypass Capacitor	2.2uF	1
C3	Bypass Capacitor	1uF (Optional)	1
R1, R2, R3	Pull-up Resistor	2.2KΩ ~ 10KΩ	3
R_{VDD}	Noise Filter Resistor	22Ω	1

Ordering MN58406D Chip Information

TBD

Absolute Maximum Ratings

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
V_{DD}	Supply Voltage	-0.3	--	4.2	V
V_O	Digital Voltage Range	-0.3	--	4.2	V
I_O	Digital Output Current	--	--	10	mA
T_S	Storage Temperature	-40	--	85	ºC

Note : All voltages are with respect to GND

Recommended Operating Conditions

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
V_{DD}	Supply Voltage	2.4	--	3.6	V
V_{BUS}	I^2C Voltage	1.7	--	3.6	V
V_{LD}	IR LD Voltage	2.4	--	4.5	V
T_A	Operation Temperature	-20	--	75	ºC

Electrical and Optical Characteristics

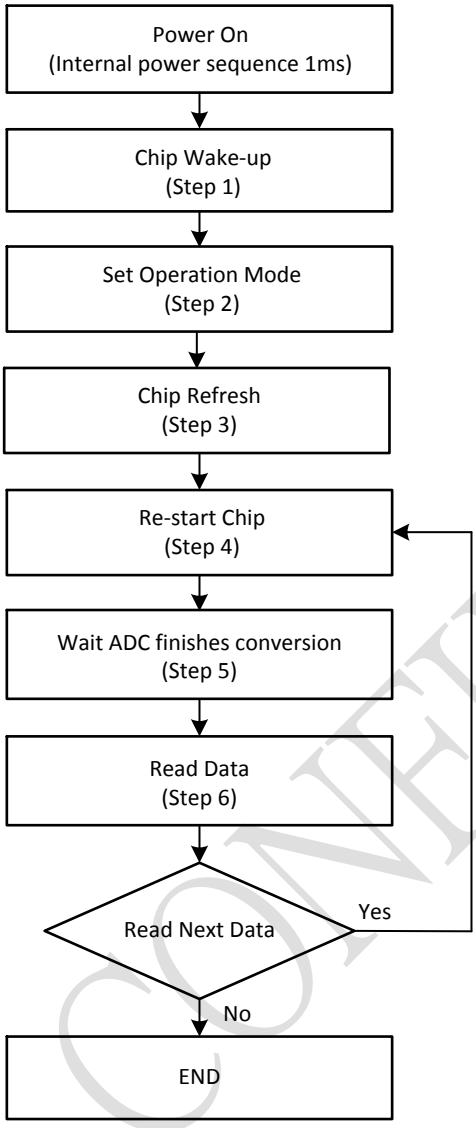
(Test Conditions : V_{DD} = 3.0V, +25°C)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
POWER ON RESET						
T_{RP}	Reset Timeout Period	V_{DD} = 2.4~3.6V	--	1	--	ms
POWER SUPPLY						
I_{DD}	Supply Current	Active	--	400	--	uA
		Sleep	--	1	--	uA
DIGITAL I/O CHARACTERISTICS						
V_{OL}	SDAOutput Low Voltage	5mA sink current	0	--	0.4	V
	INTBOutput Low Voltage	1mA sink current	0	--	0.4	
V_{IL}	I^2C Input Low Voltage	SCL, SDA	--	--	0.5	V
V_{IH}	I^2C Input High Voltage	SCL, SDA	1.4	--	--	V
Clock	Chip Clock		--	1.0	--	MHz
Ambient Light SENSOR						
A_{min}	Resolution		--	0.001	--	Lux/Count
A_{max}	Maximum Detection Range	*(Note1)*	--	100K	--	Lux
A_{ADC}	ALS output resolution		12	--	16	bits
PROXIMITY SENSOR						
I_{LD}	Peak LD Current	V_{LD} = 3.3V	--	10	--	mA
ESD TOLERANCE						
ESD HBM	Human Body Model		--	--	2000	V
ESD MM	Machine Model		--	--	200	V

Note1 : Measures using white LED light source and cover lens with 15% transmittance at 550 nm

Note2 : LD wavelength is 940nm

Basic Control Procedures



WriteByte(SlaveAddress, RegAddr, WriteData)

ReadByte1(SlaveAddress, RegAddr)

ReadByte2(SlaveAddress, ReadData)

```
// Step 1 : Chip Wake-up
    WriteByte(SlaveAddress, 0x11, 0x02)   // wake up

// Step 2 : Set Operation Mode
    WriteByte(SlaveAddress, 0x00, 0x01)   // for ALS mode
    WriteByte(SlaveAddress, 0x00, 0x02)   // for PS mode

// Step 3 : Chip Refresh
    WriteByte(SlaveAddress, 0xfd, 0x8e)
    WriteByte(SlaveAddress, 0xfb, 0x22)
    WriteByte(SlaveAddress, 0xfb, 0x20)
    WriteByte(SlaveAddress, 0xfd, 0x00)

// Step 4 : Re-start Chip
    WriteByte(SlaveAddress, 0x11, 0x00)   // chip reset
    WriteByte(SlaveAddress, 0x11, 0x02)   // chip start to run

// Step 5 : Wait ADC finishes conversion

// Step 6 : Read Data
    Read Reg0x13 ~ Reg0x16                // ALS data
    Read Reg0x1C ~ Reg0x1F                // PS data
```

Principles of Operation

The MN58406D provides control of PS, ALS and power management functionality through an internal state machine. After the Power on Reset (POR), the chip is in the sleep mode. When the chip enables the PS+ALS, Wait and active mode, the chip will continues through the PS, ALS and Wait states. When the chip enables the PS+ALS, single sensing and active mode, the chip will perform single PS and ALS measurement and then return to sleep mode.

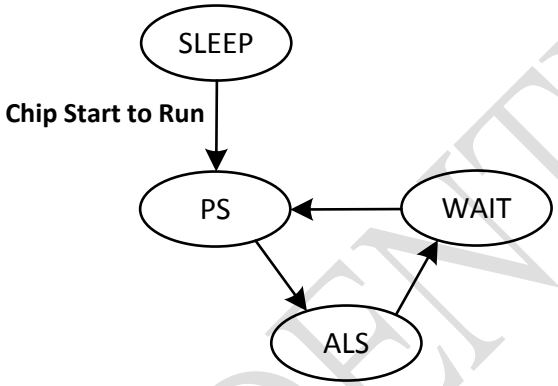


Figure 5(a).continuous sensing

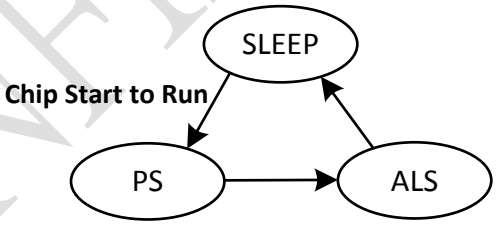


Figure 5(b).single sensing

Figure 5.Simplified State Diagram

I²C Waveform and Typical Characteristic

I²C Bus Timing Characteristics

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
SCL Clock frequency	f(SCL)	10	100	10	400	KHz
Bus free time between start and stop condition	t(BUF)	4.7	-	1.3	-	us
Hold time (repeated) start condition	t(HD:STA)	4.0	-	0.6	-	us
Set-up time for a repeated start condition	t(SU:STA)	4.7	-	0.6	-	us
Set-up time for Stop condition	t(SU:STO)	4.0	-	0.6	-	us
Data hold time	t(HD:DAT)	0	3000	0	900	ns
Data Set-up time	t(SU:DAT)	250	-	100	-	ns
I²C clock (SCK) low period	t(LOW)	4.7	-	1.3	-	us
I²C clock (SCK) high period	t(HIGH)	4.0	-	0.6	-	us
Detect clock/data low timeout	t(TIMEOUT)	25	35	-	-	ms
Clock/Data fall time	t(F)	-	1000	-	300	ns
Clock/Data rise time	t(R)	-	1000	-	300	ns

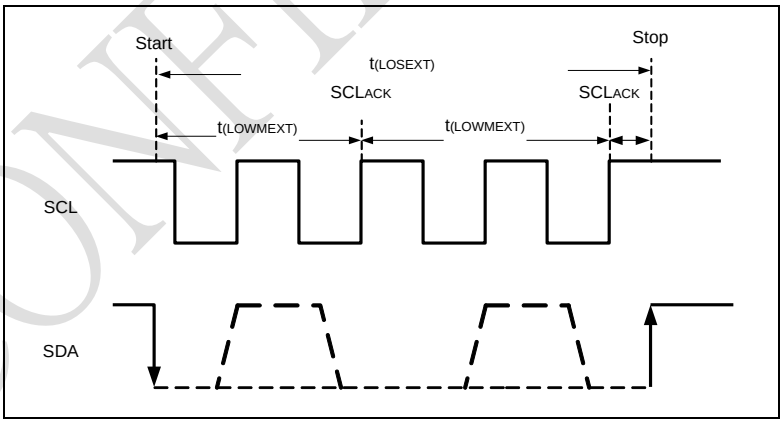


Figure 5. I²C Bus Timing Diagram (Magnified)

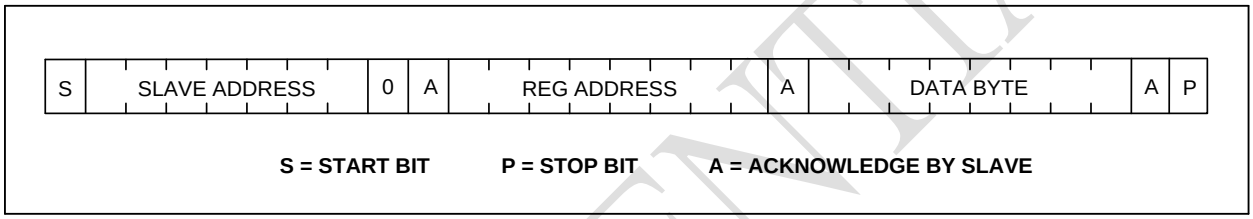
I²C Slave Address

Ordering Chip Information	Write to Slave	Read from Slave
MN58406D	1000001<u>0</u>	1000001<u>1</u>

* *This chip supports the general call and software reset of I²C bus. General call on the I2C bus after receiving slave address **0x00** followed by the second byte (command byte) **arbitrary value** and the third byte (data byte) **0x06** should perform a software reset.*

I²CRead/Write Data Format

Send (Single Write) data into register



Receive (Single Read) data from register

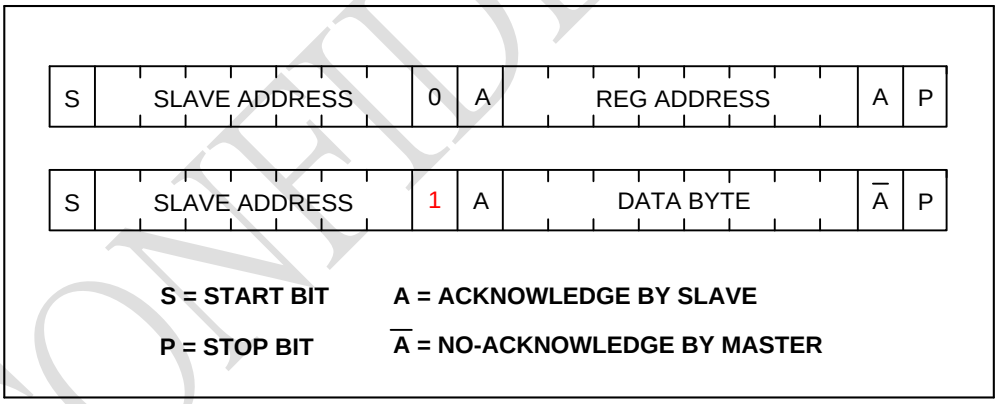


Figure 6. I²C Bus for "Send Byte" and "Receive Byte" Command Format

Principles of Operation

Register Table and Definitions

The register addresses are maintained inside the I^2C block, each having a 5-bit register address. Each address accommodates an 8-bit data register that can be either written or read via I^2C. The command registers program the sensor for various modes, setting and Interrupt threshold. The read-only registers contains output codes, gain value (gain setting selected by the sensor)

8-bit Address	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	R/W	WTIME[3:0]				*(Reserved)*		MODE[1:0]		0x00
0x01	R/W	*(Reserved)*		ALS_INTEG[3:0]				ALS_GAINS[1:0]		0x1F
0x02	R/W	*(Reserved)*					ALS_FILTER[2:0]			0x15
0x03	R/W	*(Reserved)*		PS_INTEG[3:0]				PS_GAINS[1:0]		0x1F
0x04	R/W	*(Reserved)*					PS_FILTER[2:0]			0x13
0x05	R/W	*(Reserved)*			PS_IR_MODE	*(Reserved)*		PS_IR_DRIVE[1:0]		0x23
0x06	R/W	*(Reserved)*		INT_CTRL[1:0]		PS_PERSIST[1:0]		PS_INTTY[1:0]		0x20
0x07	R/W	*(Reserved)*				ALS_PERSIST[1:0]		ALS_INTTY[1:0]		0x10
0x08	R/W	ALS_INT_L[7:0]								0x00
0x09	R/W	ALS_INT_L[15:8]								0x00
0x0A	R/W	ALS_INT_H[7:0]								0xFF
0x0B	R/W	ALS_INT_H[15:8]								0xFF
0x0C	R/W	PS_INT_L[7:0]								0x00
0x0D	R/W	PS_INT_L[15:8]								0x00
0x0E	R/W	PS_INT_H[7:0]								0xFF
0x0F	R/W	PS_INT_H[15:8]								0xFF
0x11	R/W	*(Unused)*						RESETN	SLEEP	0x03
0x12	R - R/W	*(Unused)*			ALS_CMP_H	ALS_CMP_L	ALS_INT_FLAG	ALS_CMP_RSTN	ALS_LOCK	0x02
0x13	R	ALS_CH0_DATA[7:0]								--
0x14	R	ALS_CH0_DATA[15:8]								--
0x15	R	ALS_CH1_DATA[7:0]								--
0x16	R	ALS_CH1_DATA[15:8]								--
0x1B	R - R/W	*(Unused)*			PS_CMP_H	PS_CMP_L	PS_INT_FLAG	PS_CMP_RSTN	PS_LOCK	0x02
0x1C	R	PALS_DATA[7:0]								--
0x1D	R	PALS_DATA[15:8]								--
0x1E	R	PS_DATA[7:0]								--
0x1F	R	PS_DATA[15:8]								--
0x20	R	REVNO[7:0]								--
0x22	R/W	PS_OFFSET[7:0]								0x00
0x23	R/W	PS_OFFSET[15:8]								0x00

Read and Write Registers Definition

Note: The value in { } is the default value

REGISTER 0x00

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WTIME[3:0]				*Reserved*		MODE[1:0]	
R/W {0000}				--		R/W {00}	

Bit 7 - Bit 4 (WTIME[3:0]) : Wait Time Selection (at clock frequency = 1MHz)

0000 : Wait timer disable

0001 : 2ms

0010 : 4ms

0011 : 8ms

0100 : 12ms

0101 : 20ms

0110 : 30ms

0111 : 40ms

1000 : 50ms

1001 : 75ms

1010 : 100ms

1011 : 150ms

1100 : 200ms

1101 : 300ms

1110 : 400ms

1111 : Single sensing

Note : *In single sensing, the chip will perform single PS or ALS measurement and then return to idle and reset mode. The single sensing mode is recommended for saving chip operation power.*

Bit 3- Bit 2 : *Reserved. Write as 00*

Bit 1 - Bit 0 (MODE[1:0]) : Operation Mode Selection

00 : IDLE mode

01 : ALS mode

10 : PS mode

11 : PS and ALS mode

REGISTER 0x01

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

Reserved	ALS_INTEG[3:0]	ALS_GAINS[1:0]
--	R/W {0111}	R/W {11}

Bit 7- Bit 6 : *Reserved. Write as 00*

Bit 5 - Bit 2 (ALS_INTEG[3:0]) : ALS Integration Time

ALS_INTEG[3:0]	ALS Integration Time
0000	--
0001	--
0010	8
0011	16
0100	32
0101	64
0110	128
0111	256
1000	512
1001	768
1010	1024
1011	2048
1100	4096
1101	6144
1110	8192
1111	10240

Bit 1 - Bit 0 (ALS_GAINS[1:0]) : ALS Gain Setting

00 : Not used

01 : Middle gain

10 : Not used

11 : Low gain

REGISTER 0x02

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved					ALS_FILTER[2:0]		
--					R/W {101}		

Bit 7- Bit 3 : *Reserved. Write as 00010*

Bit 2 - Bit 0 (ALS_FILTER[2:0]) : Filter Order Setting for ALS Mode

000 : 1-order filter setting

001 : 2-order filter setting

010 : 4-order filter setting

011 : 8-order filter setting

100 : 16-order filter setting

101 : 32-order filter setting

110 : 64-order filter setting

111 :128-order filter setting

REGISTER 0x03

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		PS_INTEG[3:0]				PS_GAINS[1:0]	
--		R/W {0111}				R/W {11}	

Bit 7- Bit 6 : *Reserved. Write as 00*

Bit 5 - Bit 1 (PS_INTEG[3:0]) : PS Integration Time

PS_INTEG[3:0]	PS Integration Time
0000	--
0001	8
0010	16
0011	24
0100	32
0101	48
0110	80
0111	144
1000	272
1001	384
1010	520
1011	784
1100	1040
1101	2064
1110	4112
1111	6160

Bit 1 - Bit 0 (PS_GAINS[1:0]) : PS Gain Setting

00 : Not used

01 : Middle gain

10 : Not used

11 : Low gain

REGISTER 0x04

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved					PS_FILTER[2:0]		
--					R/W {011}		

Bit 7- Bit 3 : *Reserved. Write as 00010*

Bit 2 - Bit 0 (PS_FILTER[2:0]) : Filter Order Setting for PS Mode

000 : 1-order filter setting

001 : 2-order filter setting

010 : 4-order filter setting

011 : 8-order filter setting

100 : 16-order filter setting

101 : 32-order filter setting

110 : 64-order filter setting

111 : 128-order filter setting

REGISTER 0x05

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved			PS_IR_MODE	*Reserved*		PS_IR_DRIVE[1:0]	
--			R/W {0}	--		R/W {11}	

Bit 7- Bit 5: *Reserved. Write as 001*

Bit 4 (PS_IR_MODE) : IR_LD Mode Selection for PS Mode

0 : current source mode

1: voltage source mode

Bit 3 - Bit 2 : *Reserved. Write as 00*

Bit 1 - Bit 0 (PS_IR_DRIVE [1:0]) : LD Drive Strength for Current Source Mode of PS Mode

00 : Reserved

01 : Reserved

10 : Reserved

11 : 10mA

REGISTER 0x06

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		INT_CTRL		PS_PERSIST[1:0]		PS_INTTY[1:0]	
--		R/W {10}		R/W {00}		R/W {00}	

Bit 7- Bit 6 : *Reserved. Write as 00*

Bit 5 – Bit 4 (INT_CTRL[1:0]) : Interrupt Control

00 : ALS_INT_FLAG or PS_INT_FLAG (logical OR)

01 : ALS_INT_FLAG

10 : PS_INT_FLAG

11 : ALS_INT_FLAG And PS_INT_FLAG

Bit 3 - Bit 2 (PS_PERSIST[1:0]) : Interrupt Persistence for PS Mode

00 : set interrupt flag if 1 frame conversion result exceeds the PS threshold value

01 : set interrupt flag if 4 frame conversion result exceeds the PS threshold value

10 : set interrupt flag if 8 frame conversion result exceeds the PS threshold value

11 : set interrupt flag if 16 frame conversion result exceeds the PS threshold value

Bit 1 - Bit 0 (PS_INTTY[1:0]) : Interrupt Mode Selection for PS Mode

00 : disable mode

The PS_INT_FLAG is cleared to logic 0

01 : binary mode

In binary mode, the PS interrupt-flag is equal to comparator output (PS_CMP_H).

10 : active-low mode

In active-low mode, if PS_INT_FLAG = 1, read-only registers REG0x1C~REG0x1F will be auto lock, and when the lock changes 1 to 0 (unlock), the PS interrupt-flag will be auto cleared to 0.

11 : frame finish notice

The chip sent the interrupt signal to host that remains low 30-clock cycle on INTB at each frame finish.

REGISTER 0x07

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved				ALS_PERSIST[1:0]		ALS_INTTY[1:0]	
--				R/W {00}		R/W {00}	

Bit 7- Bit 4 : *Reserved. Write as 0001*

Bit 3 - Bit 2 (ALS_PERSIST[1:0]) : Interrupt Persistence for ALS Mode

00 : set interrupt flag if 1 frame conversion result exceeds the ALS threshold value

01 : set interrupt flag if 4 frame conversion result exceeds the ALS threshold value

10 : set interrupt flag if 8 frame conversion result exceeds the ALS threshold value

11 : set interrupt flag if 16 frame conversion result exceeds the ALS threshold value

Bit 1 - Bit 0 (ALS_INTTY[1:0]) : Interrupt Mode Selection for ALS Mode

00 : disable mode

The ALS_INT_FLAG is cleared to logic 0

01 : binary mode

In binary mode, the ALS interrupt-flag is equal to comparator output (ALS_CMP_H).

10 : active-low mode

In active-low mode, if ALS_INT_FLAG = 1, read-only registers REG0x13~REG0x16 will be auto lock, and when the lock changes 1 to 0 (unlock), the PS interrupt-flag will be auto cleared to 0.

11 : frame finish notice

The chip sent the interrupt signal to host that remains low 30-clock cycle on INTB at each frame finish.

REGISTER 0x08

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ALS_INT_L[7:0]							
R/W {00000000}							

Bit 7 - Bit 0 (ALS_INT_L[7:0]) : Low 8 Bits (of 16 bits) Interrupt Low Threshold for ALS

REGISTER 0x09

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ALS_INT_L[15:8]							
R/W {00000000}							

Bit 7 - Bit 0 (ALS_INT_L[15:8]) : High 8 Bits (of 16 bits) Interrupt Low Threshold for ALS

REGISTER 0x0A

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ALS_INT_H[7:0]							
R/W {11111111}							

Bit 7 - Bit 0 (ALS_INT_H[7:0]) : Low 8 Bits (of 16 bits) Interrupt High Threshold for ALS

REGISTER 0x0B

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ALS_INT_H[15:8]							
R/W {11111111}							

Bit 7 - Bit 0 (ALS_INT_H[15:8]) : High 8 Bits (of 16 bits) Interrupt High Threshold for ALS

REGISTER 0x0C

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PS_INT_L[7:0]							
R/W {00000000}							

Bit 7 - Bit 0 (PS_INT_L[7:0]) : Low 8 Bits (of 16 bits) Interrupt Low Threshold for PS

REGISTER 0x0D

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PS_INT_L[15:8]							
R/W {00000000}							

Bit 7 - Bit 0 (PS_INT_L[15:8]) : High 8 Bits (of 16 bits) Interrupt Low Threshold for PS

REGISTER 0x0E

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PS_INT_H[7:0]							
R/W {11111111}							

Bit 7 - Bit 0 (PS_INT_H[7:0]) : Low 8 Bits (of 16 bits) Interrupt High Threshold for PS

REGISTER 0x0F

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PS_INT_H[15:8]							
R/W {11111111}							

Bit 7 - Bit 0 (PS_INT_H[15:8]) : High 8 Bits (of 16 bits) Interrupt High Threshold for PS

REGISTER 0x11

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Unused						RESETN	SLEEP
--						R/W {1}	R/W {1}

Bit 7 - Bit 2 : *Unused*

Bit 1 (RESETN) : Chip Reset Control

0 : the chip reset (exclusive of I^2C registers)

1 : the chip start to run

Bit 0 (SLEEP) : Chip Sleep Mode Setting

0 : active mode

1 : sleep mode

REGISTER 0x12

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Unused			ALS_CMP_H	ALS_CMP_L	ALS_INT_FLAG	ALS_CMP_RSTN	ALS_LOCK
--			R {--}	R {--}	R {--}	R/W {1}	R/W {0}

Bit 7 - Bit 5 : *Unused*

Bit 4 (ALS_CMP_H) : ALS Mode Comparator High Bit

When = 0, the selected channel output is below interrupt low threshold value

When = 1, the selected channel output is above interrupt high threshold value

Bit 3 (ALS_CMP_L) : ALS Mode Comparator Low Bit

When = 1, the selected channel output is below interrupt low threshold value

When = 0, the selected channel output is above interrupt high threshold value

Bit 2 (ALS_INT_FLAG) : ALS Interrupt Flag

When = 0, no ALS interrupt event has occurred since power on or last ALS interrupt-flag clear.

When = 1, an ALS interrupt event occurred.

Bit 1 (ALS_CMP_RSTN) : ALS Mode Comparator Reset Control

0 : the ALS_CMP_H and ALS_CMP_L are cleared to logic 0

1 : normal operation

Bit 0 (ALS_LOCK) : ALS Data Lock Setting

0 : ALS data unlock

1 : ALS data lock (read-only registers REG0x13~REG0x16, ALS_CMP_H and ALS_CMP_L data lock)

REGISTER 0x13

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH0_DATA[7:0]							
R {--}							

Bit 7 - Bit 0 (CH0_DATA[7:0]) : Low 8 Bits (of 16 bits) Channel 0 Output

In ALS mode, this is the low byte of the ambient IR channel.

REGISTER 0x14

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH0_DATA[15:8]							
R {-}							

Bit 7 - Bit 0 (CH0_DATA[15:8]) : High 8 Bits (of 16 bits) Channel 0 Output

In ALS mode, this is the high byte of the ambient IR channel.

REGISTER 0x15

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH1_DATA[7:0]							

R {--}

Bit 7 - Bit 0 (CH1_DATA[7:0]) : Low 8 Bits (of 16 bits) Channel 1 Output

In ALS mode, this is the low byte of the ambient channel.

REGISTER 0x16

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH1_DATA[15:8]							
R {--}							

Bit 7 - Bit 0 (CH1_DATA[15:8]) : High 8 Bits (of 16 bits) Channel 1 Output

In ALS mode, this is the high byte of the ambient channel.

REGISTER 0x1B

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Unused			PS_CMP_H	PS_CMP_L	PS_INT_FLAG	PS_CMP_RSTN	PS_LOCK
--			R {--}	R {--}	R {--}	R/W {1}	R/W {0}

Bit 7 - Bit 5 : *Unused*

Bit 4 (PS_CMP_H) : PS Mode Comparator High Bit

When = 0, the PS_DATA output is below interrupt low threshold value

When = 1, the PS_DATA output is above interrupt high threshold value

Bit 3 (PS_CMP_L) : PS Mode Comparator Low Bit

When = 1, the PS_DATA output is below interrupt low threshold value

When = 0, the PS_DATA output is above interrupt high threshold value

Bit 2 (PS_INT_FLAG) : PS Interrupt Flag

When = 0, no PS interrupt event has occurred since power on or last PS interrupt-flag clear.

When = 1, anPS interrupt event occurred.

Bit 1 (PS_CMP_RSTN) : PS Mode Comparator Reset Control

0 : the PS_CMP_H and PS_CMP_L are cleared to logic 0

1 : normal operation

Bit 0 (PS_LOCK) : PS Data Lock Setting

0 : PS data unlock

1 : PS data lock (read-only registers REG0x1C~REG0x1F, PS_CMP_H and PS_CMP_L data lock)

REGISTER 0x1C

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PALS_DATA[7:0]							
R {--}							

Bit 7 - Bit 0 (PALS_DATA[7:0]) : Low 8 Bits (of 16 bits) PALS_DATA Output

In PS mode, this is the low byte of the ambient IR channel.

REGISTER 0x1D

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PALS_DATA[15:8]							
R {-}							

Bit 7 - Bit 0 (PALS_DATA[15:8]) : High 8 Bits (of 16 bits) PALS_DATA Output

In PS mode, this is the high byte of the ambient IR channel.

REGISTER 0x1E

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PS_DATA[7:0]							
R {--}							

Bit 7 - Bit 0 (PS_DATA[7:0]) : Low 8 Bits (of 16 bits) PS_DATA Output

In PS mode, this is the low byte of the IR_LD reflection channel.

REGISTER 0x1F

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PS_DATA[15:8]							
R {--}							

Bit 7 - Bit 0 (PS_DATA[15:8]) : High 8 Bits (of 16 bits) PS Output

In PS mode, this is the high byte of the IR_LD reflection channel.

REGISTER 0x20

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
REVNO[7:0]							
R {10001000}							

Bit 7 - Bit 0 (REVNO[7:0]) : 8 Bits Revision Number

REGISTER 0x22

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PS_OFFSET[7:0]							
R/W {00000000}							

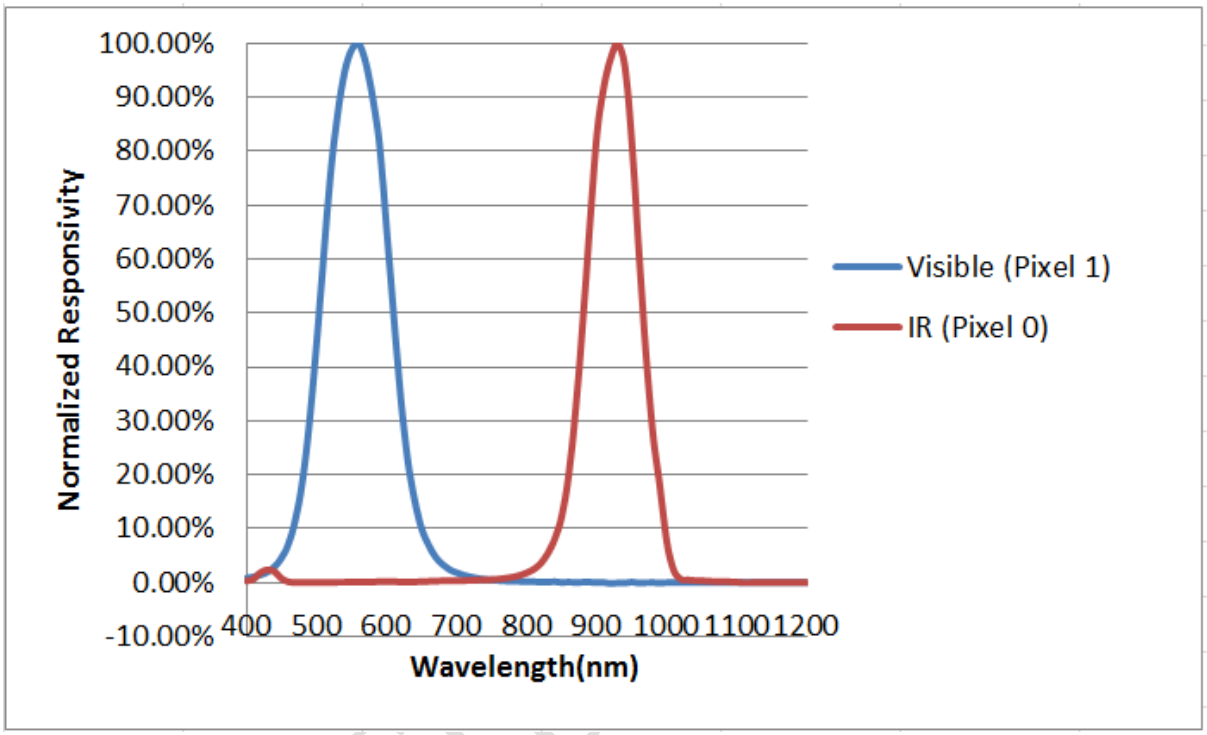
Bit 7 - Bit 0 (PS_OFFSET[7:0]) : Low 8 Bits (of 16 bits) offset compensation for PS_DATA

REGISTER 0x23

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PS_OFFSET[15:8]							
R/W {00000000}							

Bit 7 - Bit 0 (PS_OFFSET[15:8]) : High 8 Bits (of 16 bits) offset compensation for PS_DATA

Spectral Response



MN58406D Package Outline

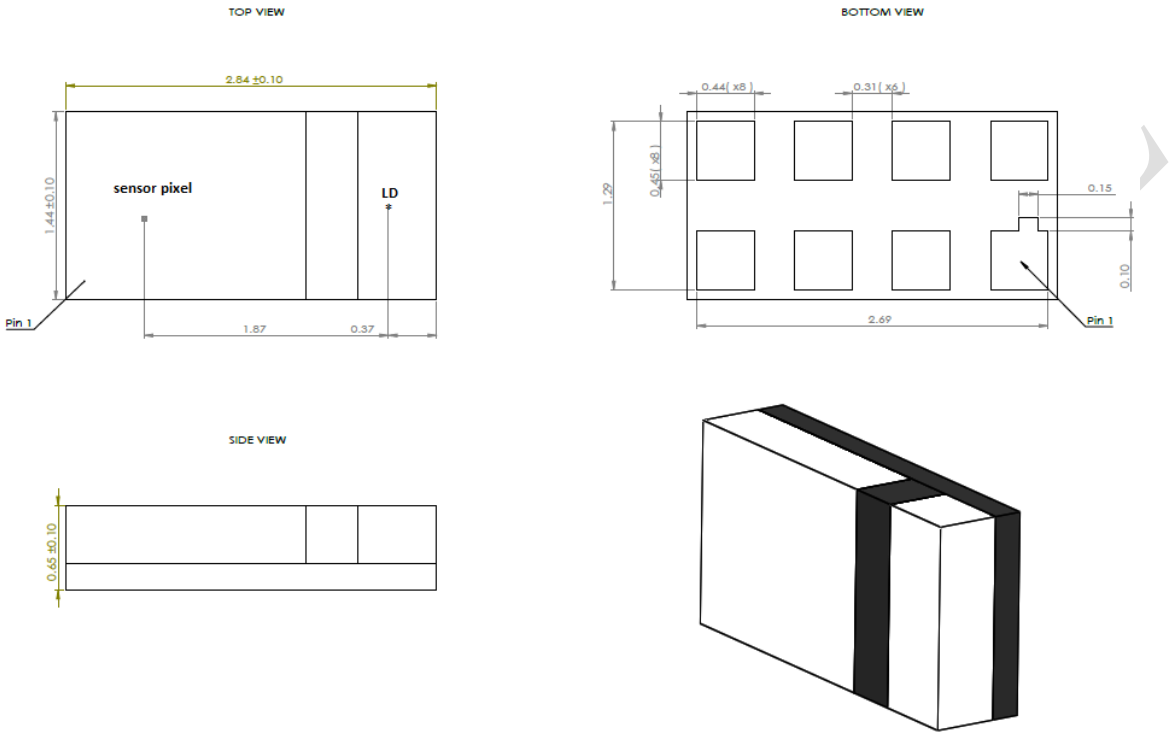


Figure 7-1.MN58406D Package of Dimension (Unit: mm)

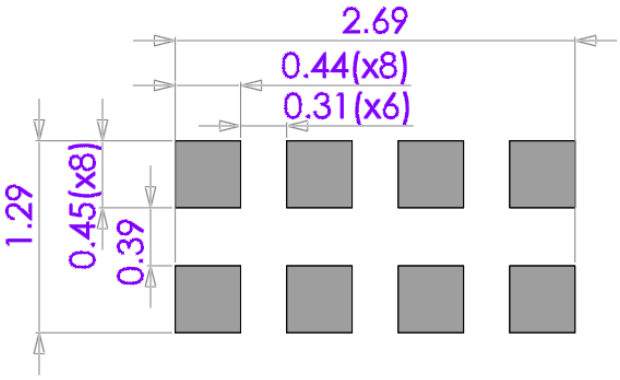


Figure 7-2.PCB layout for MN58406D (Unit: mm)

MN58406D Shipping Package Method

TBD

Figure 8.MN58406D Shipping Package Method (Unit: mm)

Shipping Box Label

TBD

Figure 9.MN58406D Shipping Package Label

Reliability and Reflow Profile

Pb-Free Process - Classification Temperatures (T_c)

Package Thickness	Volume mm³ <350	Volume mm³ 350 - 2000	Volume mm³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

Note 1: At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Tables above. The use of a higher Tp does not change the classification temperature (Tc).
Note 2: Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.
Note 3: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.
Note 4: Moisture sensitivity levels of components intended for use in a Pb-free assembly process **shall** be evaluated using the Pb-free classification temperatures and profiles defined in Tables above and below, whether or not Pb-free.
Note 5: SMD packages classified to a given moisture sensitivity level by using Procedures or Criteria defined within any previous version of J-STD-020, JESD22-A112 (rescinded), IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired.

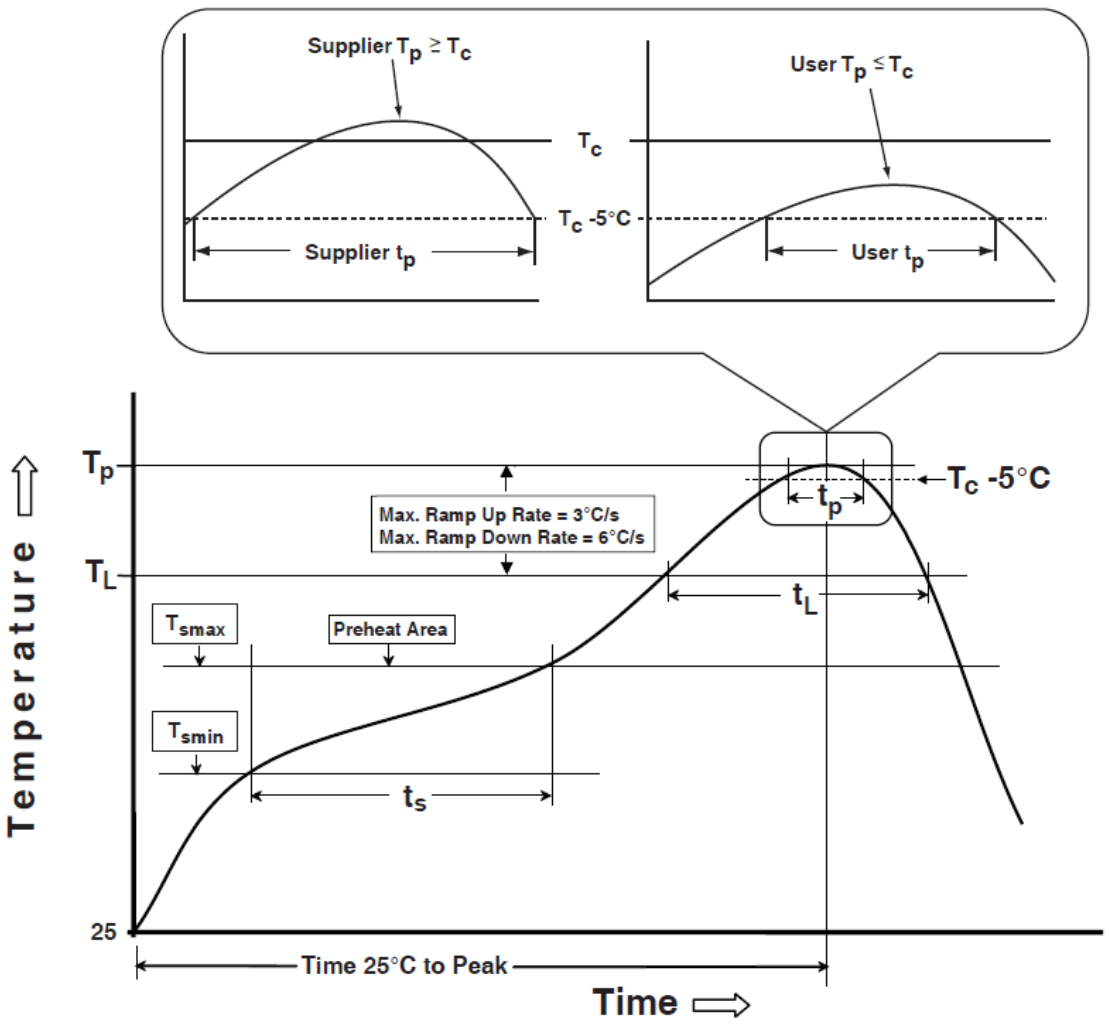
Moisture Sensitivity Levels

			SOAK REQUIREMENTS				
					ACCELERATED EQUIVALENT[1]		
	FLOOR LIFE		STANDARD		eV 0.40-0.48	eV 0.30-0.39	
LEVEL	TIME	CONDITION	TIME (hours)	CONDITION	TIME (hours)	TIME (hours)	CONDITION
1	Unlimited	≤30 °C/85% RH	168 +5/-0	85 °C/85% RH	NA	NA	NA
2	1 year	≤30 °C/60% RH	168 +5/-0	85 °C/60% RH	NA	NA	NA
2a	4 weeks	≤30 °C/60% RH	696[2] +5/-0	30 °C/60% RH	120 +1/-0	168 +1/-0	60 °C/60% RH
3	168 hours	≤30 °C/60% RH	192[2] +5/-0	30 °C/60% RH	40 +1/-0	52 +1/-0	60 °C/60% RH
4	72 hours	≤30 °C/60% RH	96[2] +2/-0	30 °C/60% RH	20 +0.5/-0	24 +0.5/-0	60 °C/60% RH
5	48 hours	≤30 °C/60% RH	72[2] +2/-0	30 °C/60% RH	15 +0.5/-0	20 +0.5/-0	60 °C/60% RH
5a	24 hours	≤30 °C/60% RH	48[2] +2/-0	30 °C/60% RH	10 +0.5/-0	13 +0.5/-0	60 °C/60% RH
6	Time on Label (TOL)	≤30 °C/60% RH	TOL	30 °C/60% RH	NA	NA	NA

Note 1: CAUTION - To use the "accelerated equivalent" soak conditions, correlation of damage response (including electrical, after soak and reflow), should be established with the "standard" soak conditions. Alternatively, if the known activation energy for moisture diffusion of the package materials is in the range of 0.40 - 0.48 eV or 0.30 - 0.39 eV, the "accelerated equivalent" may be used. Accelerated soak times may vary due to material properties (e.g., mold compound, encapsulant, etc.). JEDEC document JESD22-A120 provides a method for determining the diffusion coefficient.
Note 2: The standard soak time includes a default value of 24 hours for semiconductor manufacturer's exposure time (MET) between bake and bag and includes the maximum time allowed out of the bag at the distributor's facility.
If the actual MET is less than 24 hours the soak time may be reduced. For soak conditions of 30 °C/60% RH, the soak time is reduced by 1 hour for each hour the MET is less than 24 hours. For soak conditions of 60 °C/60% RH, the soak time is reduced by 1 hour for each 5 hours the MET is less than 24 hours.
If the actual MET is greater than 24 hours the soak time must be increased. If soak conditions are 30 °C/60% RH, the soak time is increased 1 hour for each hour that the actual MET exceeds 24 hours. If soak conditions are 60 °C/60% RH, the soak time is increased 1 hour for each 5 hours that the actual MET exceeds 24 hours.
Note 3: Supplier may extend the soak times at their own risk.

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Ramp-up rate (T_L to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (T_p)	For users T_p must not exceed the Classification temp in Table 4-1. For suppliers T_p must equal or exceed the Classification temp in Table 4-1.	For users T_p must not exceed the Classification temp in Table 4-2. For suppliers T_p must equal or exceed the Classification temp in Table 4-2.
Time (t_p)* within 5 °C of the specified classification temperature (T_c), see Figure 5-1.	20* seconds	30* seconds
Ramp-down rate (T_p to T_L)	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.		



单击下面可查看定价，库存，交付和生命周期等信息

>>Eminent(義明科技)